CHIP-CEIVER™ - Single Chip FM Transceiver
902 - 928 MHz

NT2903

FEATURES

- **Direct-Conversion, Zero-IF, Architecture**
- **Wide Bandwidth FM Transceiver**
- **Suitable for FM/FSK Modulation**
- **Dual, On-Chip PLL Synthesizers/VCOs**
- **3-wire serial interface**
- **System Noise Figure 4.7 dB (typ.)**[*]
- **2.7 - 3.3V Operation / Standby Mode**
- **No Tune "Tankless" Detector**
- **RF Output +1.5 dBm**
- **Low Cost, Thin-Quad Flat Package, (TQFP-48)**

APPLICATIONS

Analog/Digital "900 MHz" Cordless Phones
Telemetry/Data Radios
Wireless Local Area Networks (WLAN)
ISM Band (900 MHz) Wireless Products

GENERAL DESCRIPTION

The NT2903 CHIP-CEIVER™ is a complete, single chip, FM transceiver solution, which will operate in any 24 MHz band from 800-1000 MHz, including the Industrial Scientific Medical (ISM) band (902-928 MHz). Utilizing a unique direct-conversion, zero-intermediate frequency (zero-IF) receiver architecture, the NT2903 CHIP-CEIVER™ provides radio designers with a "simple" RF path design solution. The device is fabricated as a monolithic, BiCMOS, integrated circuit. The device's receiver section provides all of the required RF synthesis, filtering, gain control, AFC, and demodulation functions. The transmitter section contains a directly modulated VCO and RF power amplifier (PA). Internal, dual, high-performance phase locked loop (PLL) synthesizers/VCOs allow full-duplex Tx/Rx operation over the entire RF tuning range. Tuning, power management, and gain control functions are accomplished via a 3-wire serial interface.

[*] Refer to Applications section for additional details

PRODUCT DESCRIPTION

The BiCMOS construction of the NT2903 CHIP-CEIVER™ provides a high level of integration, with high performance operation and low power consumption. The CHIP-CEIVER™ operates over an industrial temperature range of -20°C to +65°C and over the supply voltage of +2.7 V to +3.3 V. The device is available in an industry standard plastic package as a thin-quad flat package (TQFP).

FUNCTIONAL DESCRIPTION

A functional block diagram of the NT2903 CHIP-CEIVER™ is shown in Fig.(1). The receive section of the device consists of several major function blocks, including a switchable RF input attenuator, quadrature mixer (down-conversion), differential to single-ended buffers, PLL synthesizer / voltage controlled oscillator (VCO), I/Q low-pass filters, variable gain amplifiers (VGA), DC offset correction circuitry, quadrature mixer (up-conversion), zero-crossing detector, Period-to-Digital converter (P/D), Linearization ROM, and a Digital-to-Analog converter (DAC). Additionally, the device contains a reference crystal oscillator / automatic frequency control (AFC) circuitry. The transmit section of the device consists of a PLL synthesizer / directly modulated voltage controlled oscillator (VCO), and a RF power amplifier (PA).
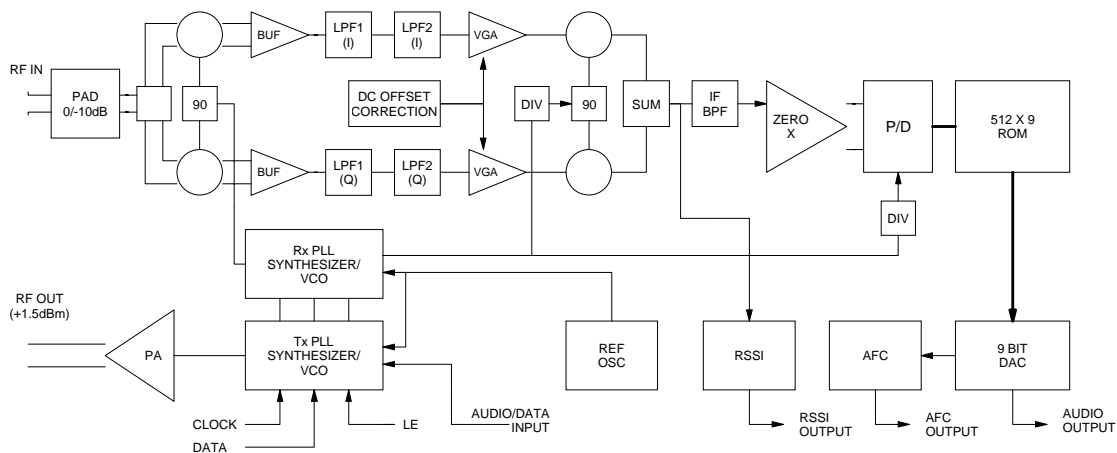

Figure (1), NT2903 CHIP-CEIVER™ - Functional Block Diagram

The receiver section of the NT2903 CHIP-CEIVER™ utilizes a quadrature mixer in a direct-conversion, zero-intermediate frequency (zero-IF) approach. After quadrature down-conversion and baseband filtering, a quadrature mixer up-converts the complex baseband signal to an intermediate frequency (IF) for digitization. Direct conversion, (zero-IF) has several advantages over super-heterodyne approaches. First, the problem of image is eliminated because the IF is zero. Second, the use of active, low pass, filters provide a high level of integration, while eliminating the need for external IF filters and IF transformers. The digital data from the P/D converter is fed to a "brick wall" filter, which limits excess receiver bandwidth, thereby improving receiver performance.

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FUNCTIONAL DESCRIPTION - Cont.

Receiver selectivity is accomplished using low pass filters (LPFs) in the I/Q complex baseband section. The device employs fully integrated, active filters for channel selectivity and receiver bandwidth control.

The transmitter section of the NT2902 CHIP-CEIVER™ is comprised of a modulator circuit, a PLL synthesizer / VCO, and a RF power amplifier (PA) capable of providing +1.5 dBm into a 50Ω load. A description of each of the major function blocks follows:

RF Input Attenuator Pad – A switchable 0/-10dB attenuator pad allows high signal level capability at the RF Input of the receiver. This pad is located prior to the quadrature mixer (down-conversion) and can be either manually controlled via the 3-wire interface, or automatically controlled via the AGC section of the device.

Quadrature Mixer (down-conversion) - The quadrature mixer is a critical part of the CHIP-CEIVER™ zero intermediate-frequency (zero-IF) design. The main advantage of the quadrature mixer is its ability to translate the RF frequency directly to a zero-IF, thereby eliminating the image frequency. Consequently, the image filter between the external LNA and the RF input to the CHIP-CEIVER™ can be eliminated in most designs. The design requirements for the duplexer and RF bandpass filter may also be relaxed. In addition, the quadrature mixer achieves a lower overall noise figure by virtue of image frequency elimination. The balanced mixers in the quadrature mixer are designed to closely track each other in both amplitude and phase response. Additionally, the quadrature LO signal is generated by direct division of the receiver LO, thereby eliminating external phase shifting networks. Furthermore, for improved noise immunity, all internal RF signal paths are fully differential, thereby providing common mode noise rejection. The gain of the mixer can be adjusted by attenuating the baseband output.

PLL Synthesizer (Receive) - The receive (Rx) on-chip PLL synthesizer with voltage controlled oscillator (VCO), is designed to provide a low phase noise, local oscillator (LO) drive for the quadrature, down-conversion RF mixer. The RxVCO operates in a balanced mode at 2x the Rx frequency (≈1.8 GHz). The ≈1.8 GHz VCO is immediately divided by 2 to ≈900 MHz, subsequently this signal is fed to a modulus prescaler (32/33) and then into the synthesizer which produces a 50 kHz signal. This feedback signal is compared at the phase detector with a reference signal (50 kHz), which is derived from the reference oscillator and reference divider. The ≈1.8 GHz divide by 2 also produces the quadrature LO drive (≈900 MHz) for the RF quadrature mixer. The Rx VCO center frequency is determined by an external tank circuit comprised of a printed, center-tapped, inductor. The tank circuit is connected to RVCO (41) and /RVCO (42) respectively. An external PLL loop filter network, connected to the RPLL pin (39), filters the VCO control voltage. This control voltage (K_{VCO} 52 MHz/V @ 1.8GHz) is used to tune the tank frequency of the VCO via an internal, common-anode, varactor pair. The receive frequency for the CHIP-CEIVER™ is programmed via a three (3) wire compatible, serial interface (Data, Clock, and Load Enable).

FUNCTIONAL DESCRIPTION - Cont.

Buffer Amplifiers – The buffer amplifiers provide differential to single-ended conversion of the baseband signal prior to the I/Q low-pass filters, which are referenced to an internally generated virtual ground.

LPF1 (I/Q) – This first stage of the I/Q baseband low pass filter (LPF) section consists of active, Sallen-key type filters. These filters provide a combination of low noise figure and gain along with a wide dynamic input range. The purpose of these filters is to provide preliminary rejection of the out-of-band interfereres. The reduction of out-of-band interferer levels, reduce the dynamic range requirements for the following filter stages in LPF2. The –3dB corner frequency of these LPFs are set via external RC values.

LPF2 (I/Q) – This second stage of the I/Q baseband low pass filter (LPF) section consists of active, transconductance (gm) type filters. Combined with LPF1, these filters provide the required channel selectivity by passing the entire desired frequency spectrum, while attenuating noise and adjacent channel interference (ACI), outside of the desired signal's bandwidth.

DC Offset Correction – A proprietary DC offset correction circuit is used in the NT2903 to control DC offset voltages which can degrade receiver performance. The correction circuit operates automatically in a continuous mode.

Quadrature Mixer (up-conversion) - The quadrature up-conversion mixer forms yet another important part of the overall CHIP-CEIVER™ design. This quadrature mixer translates the filtered baseband signal from one frequency to another i.e. the zero-IF, complex, baseband spectrum is translated by the quadrature up-conversion mixer to a frequency centered about the LO mixer frequency. The resultant up-converted IF signal is low enough in frequency to provide adequate SNR at the output of the period-to-digital converter (P/D), yet high enough to satisfy signal sampling criterion.

IF BPF - The intermediate frequency (IF), bandpass filter (BPF) after the quadrature up-conversion mixer passes the lowest frequency signal components and rejects the third harmonic component of the up-conversion mixer's local oscillator (LO). The IF bandpass filter is comprised of cascaded, active, transconductance filters with Butterworth response characteristics.

RSSI - The receive signal strength indication (RSSI) measurement circuitry incorporates a log amplifier and detector for the purpose of measuring the received RF carrier power level. The output is a DC voltage, which is linear over a 50dB dynamic range. The RSSI measurement range is from -116dBm to -66dBm with the RF input pad bypassed (0dB) and the quadrature mixer gain set to high. The RSSI conversion factor is -30mV/dB, with a voltage range of 1.8VDC.

FUNCTIONAL DESCRIPTION - Cont.

AFC – Automatic Frequency Control of the receive local oscillator (LO) frequency is used to improve receiver performance. Without AFC, frequency offsets cause a reduction in SINAD due to filter distortion. A reduction in SINAD of 4-5dB is typical at a frequency offset of ±20kHz. Additionally, due to the zero-IF architecture of the NT2903 AFC is used to reduce beat note levels.

The AFC correction voltage, which is generated internally in the NT2903, is available as a DC voltage at the AFC (46) output pin. This correction voltage is typically used to bias an external varactor, which is parallel to the input load capacitor of the reference oscillator circuit. The AFC correction voltage is derived by double integration of the demodulated FM signal. The AFC attack time is governed by two factors; an external capacitor connected to the AFCC (47) pin and a loop damping resistor and capacitor at the output pin of the AFC (46) output pin.

Comparator - A high speed BiCMOS comparator performs the basic function of a "Limiter" and is used to detect the intermediate frequency (IF) zero-crossing events. The "half-cycle" intervals of the IF are output from the comparator in the form of a pulse, which is subsequently measured by the Period-to-Digital (P/D) converter. Complimentary outputs from the comparator provide alternating "half-cycle" gating signals to the P/D converter.

Period-to-Digital (P/D) Converter - The quantizer used in the CHIP-CEIVER™ employs the NUMA Technologies' Period-to-Digital (P/D) converter as the digitizer. The basic principal of the P/D relies on it's ability to integrate and dump sequential half-cycle intervals of the IF signal with high resolution. The numerical output from the P/D is the form of 1/f or period of the intermediate frequency (IF) signal.

The clock signal for the P/D is derived from the RxVCO oscillator. A functional block diagram of the P/D clock generation is shown in Fig. (2).
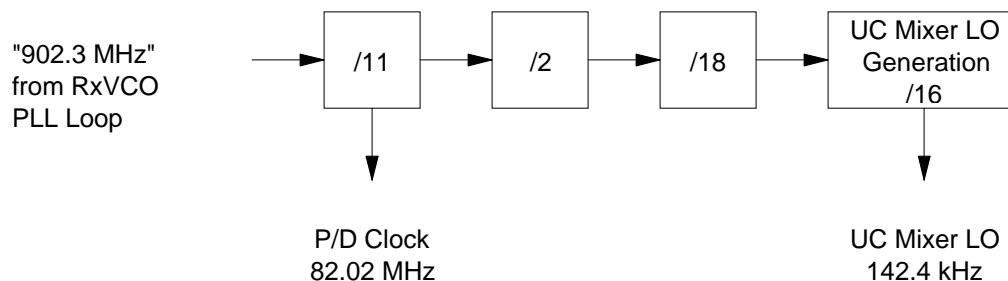

Figure (2), P/D Converter Clock Generation - Functional Block Diagram

FUNCTIONAL DESCRIPTION - Cont.

Linearization ROM – The information from the period-to-digital converter (P/D) is in the form of a period measurement (1/f) of each half cycle of the IF signal. Each data value from the P/D is used to address a pre-programmed value in the linearization ROM. In this manner, the linearization ROM is used as a look-up table which provides the required 1/p conversion to convert the period information of the P/D to frequency, in a linear fashion. The ROM maybe programmed with different numerical values, thereby providing different detector response characteristics, for use in either analog or digital modulation schemes.

D/A Converter - The Digital-to-Analog (DAC) converter along with the output from the P/D converter form a "tankless discriminator". A digital-to-analog converter (DAC) provides a special transfer function, which is required to linearize the digital data "period" value from the P/D converter. The resultant analog signal is the recovered audio (demodulated FM).

PLL Synthesizer (Transmit) - The transmit (Tx) on-chip PLL synthesizer with an on-chip, voltage controlled oscillator (VCO), contains a dual-modulus prescaler (32/33) and employs a digital phase locked loop architecture. The transmit VCO operates at ≈900 MHz. The transmit PLL accepts modulation audio to provide a frequency modulated (FM) RF carrier. Utilizing a direct modulation approach, the modulation voltage is directly applied to the PLL loop filter. The VCO center frequency is determined by an external tank circuit comprised of two inductors connected to the TVCO (15) and /TVCO (16). An external PLL loop filter network, connected to the TPLL pin (13), filters the VCO control voltage. This control voltage (K_{VCO} 26 MHz/V) is used to tune the tank frequency of the VCO via an internal, common-anode, varactor pair. The transmit frequency for the CHIP-CEIVER™ is programmed via a three (3) wire compatible, serial interface (Data, Clock, and Load Enable).

PA - The on-chip RF power amplifier is a differential gain stage. The power amplifier requires a combiner network as shown in the application circuit (Fig 3). The combiner network converts the amplifier's differential output (balanced 700Ω) to a single-ended one, capable of delivering +1.5 dBm into a 50Ω load.

Variable Receiver Gain - The gain of the receiver can be dynamically adjusted via the 3-wire interface to maintain signal linearity before the demodulator. This enables the achievement of high values of SINAD for an analog FM link. An Automatic Gain Control (AGC) function is also available on chip. The gain can be manually adjusted in 3 locations by the following:

1. A 10dB RF pad before the Quadrature mixer (PAD in figure 1)
2. Four step baseband attenuators in the RF quadrature I and Q mixer load circuits giving nominal voltage conversion gains of 18, 8, -2, -13dB for each channel.
3. Three step baseband Variable Gain Amplifiers after the baseband I and Q low pass filters giving voltage gains of 40, 30, 20 and 10 dB.

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PIN CONFIGURATION

Plastic Thin Quad Flat Package (TQFP-48 pin)
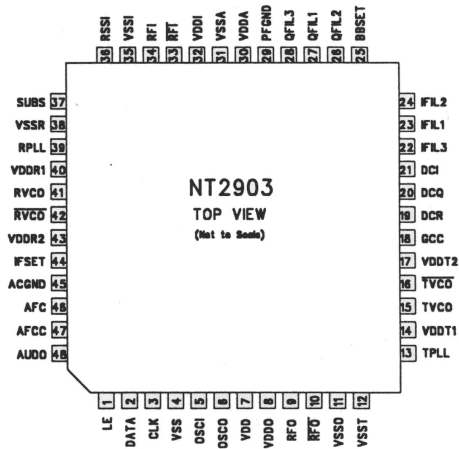
PIN DESCRIPTIONS

This section summarizes the pin descriptions of the NT2903 CHIP-CEIVER™ by pin name.

Pin Name	Pin Number	Description
LE	(1)	Load Enable: This CMOS compatible input when HIGH allows data to be shifted into the internal shift register.
DATA	(2)	Serial Data Input: This CMOS compatible input accepts data MSB first. Refer to page (13) for additional information on the programming format.
CLK	(3)	Serial Clock: This CMOS compatible input shifts serial data into the internal 20-bit serial shift register, upon the rising edge of the clock signal.
VSS	(4)	Digital ground: This is the ground pin for the internal CMOS digital circuitry, crystal oscillator, AFC, period-to-digital (P/D) converter, ROM, and Digital-to-Analog converter (DAC).
OSCI	(5)	Oscillator Input: This CMOS input is the reference frequency input for both the Tx and Rx PLLs. When used with an external reference oscillator, the signal level should be within the range of 200-400mV peak. Additionally, this input can be used with the OSCO pin to form a Colpitts crystal oscillator. Figure (3) of the application circuit illustrates the use of the internal oscillator.

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PIN DESCRIPTIONS - Cont.

OSCO	(6)	Oscillator Output: This CMOS compatible output is used in conjunction with OSCIN to form a Colpitts oscillator using an external, low cost, crystal (parallel-resonant).
VDD	(7)	Digital power supply: This is the power supply pin for the internal CMOS digital circuitry, crystal oscillator, AFC, period-to-digital (P/D) converter, and Digital-to-Analog converter (DAC). This pin should be de-coupled to ground, as close to the pin as possible, with a high quality .1μF ceramic capacitor.
VDDO	(8)	RF output power supply: This is the power supply pin for the internal power amplifier (PA) and transmit VCO prescaler.
RFO, \RFO	(9, 10)	RF Amplifier Outputs: These are the differential outputs of the power amplifier which require a combiner network as shown in the application circuit (Fig 3). The output impedance of the power amplifier (PA) is $\approx 700\Omega$ (differential). The combiner circuit, (Fig 3) allows the delivery of 1.5 dBm into a 50Ω load.
VSSO	(11)	RF output ground: This is the ground pin for the internal power amplifier (PA) and transmit TxVCO prescaler.
VSST	(12)	Transmit VCO ground: This is the ground pin for the internal transmit voltage controlled oscillator and transmit PLL charge pump. This pin should be connected to an RF ground plane using through-hole vias.
TPLL	(13)	Transmit Voltage Controlled Oscillator: This pin connects to an external PLL loop filter. This filtered tuning voltage provides the tuning voltage for the internal varactor tuning diodes. The PLL loop dynamics are controlled by the loop filter component values. Transmitter modulation is accomplished by directly applying the modulating signal (Audio/Data) to the PLL loop, via an external coupling network.

PIN DESCRIPTIONS - Cont.

VDDT1 (14,17) Transmit VCO power supply: These are the power supply
VDDT2 pins for the internal transmit voltage controlled oscillator
and transmit PLL charge pump. These pins should be de-
coupled to ground, as close to each pin as possible, with RF
quality 100pF and 1.0nF ceramic capacitors.

TVCO (15,16) Transmit VCO Tank: These single-end outputs drive the
/TVCO external, balanced, VCO resonant tank circuit. The tank
circuit generates the overall oscillation frequency for the
TxVCO. Careful layout is required to prevent RF leakage to
the RxVCO tank circuit and the associated receive input
circuitry.

GCC (18) Gain Control Capacitor: This pin connects to an external
100 nF capacitor connected to VSSA, which provides de-
coupling for the internal gain control circuitry.

DCR (19) DC Offset RSSI: This pin is connected to an external
330 nF capacitor connected to VSSA, which removes
residual DC offset from the RSSI measurement circuitry.

DCQ (20) DC Offset (Q): This pin is connected to an external 330 nF
capacitor connected to VSSA, which removes residual DC
offset from the baseband signal Q(t).

DCI (21) DC Offset (I): This pin is connected to an external 330 nF
capacitor connected to VSSA, which removes residual DC
offset from the baseband signal I(t).

IFIL1,2,3 (23, 24, 22) Baseband In-phase (I) Filter: These pins connect to an
external RC network which set the corner frequency of the
first I/Q baseband, Sallen-key, filter stage.

BBSET (25) Baseband Filter Set: This pin connects to an external resistor,
which sets the corner frequency of the transconductance (gm)
baseband (I/Q) filter stages.

QFIL1,2,3 (27, 26, 28) Baseband Quadrature (Q) Filter: These pins connect to an
external RC network which set the corner frequency of the
first I/Q baseband, Sallen-key, filter stage.

PIN DESCRIPTIONS - Cont.

PFGND (29) Pre-Filter Ground: This pin connects to an external 100 nF capacitor connected to VSSA, which provides de-coupling for the internal pre-filter buffer ground nodes.

VDDA (30) Baseband and IF Filter power supply: This is the power supply pin for the I/Q filters, amplifiers, RSSI, up-conversion mixer, and IF filter. This pin should be de-coupled to ground, as close to the pin as possible, with a high quality .1μF and 1nF ceramic capacitors.

VSSA (31) Baseband and IF Filter ground: This is the ground pin for the I/Q filters, amplifiers, RSSI, up-conversion mixer, and IF filter.

VDDI (32) RF Input power supply: This is the power supply pin for the internal RF Quadrature mixer. This pin should be de-coupled to ground, as close to the pin as possible, with RF quality 100pF and 1.0nF ceramic capacitors.

\RFI
RFI (33, 34) RF Input (balanced 100Ω): This is the small signal RF differential inputs to the NT2903. An RF differential input signal is generated by an external phase splitter circuit and matching circuit, as shown in the applications circuit in (Fig 3). These inputs must be AC coupled to prevent damage to the input bias circuitry.

VSSI (35) RF Input ground: This is the ground pin for the internal RF Quadrature mixer. This pin should be connected to an RF ground plane using through-hole vias.

RSSI (36) Receive Signal Strength Indicator: This output pin provides a current output, into an external shunt resistor and capacitor (48kΩ//10nF) connected to VSS, to develop a filtered voltage level, proportional to the receive RF signal strength. The output is linear over a 50 dB range with an output swing of 0.2 to 2.0 Vdc. The active range of the RSSI is from low signal strength, i.e. –116dBm to –66dBm (GC$_{HIGH}$).

PIN DESCRIPTIONS - Cont.

SUBS*	(37)	Substrate: This pin is connected to the silicon substrate and should be connected to a "clean" ground plane.
		*This pin shall become a modulation input for utilization of the separate modulation varactor in future versions if required.
VSSR	(38)	Receive VCO ground: This is the ground pin for the internal receive voltage controlled oscillator and receive PLL charge pump. This pin should be connected to an RF ground plane using through-hole vias.
RPLL	(39)	Receive Voltage Controlled Oscillator: This pin connects to an external PLL loop filter. This filtered tuning voltage provides the tuning voltage for the internal varactor tuning diodes. The PLL loop dynamics are controlled by the loop filter component values.
VDDR1 **VDDR2**	(40,43)	Receive VCO power supply: These are the power supply pins for the internal receive voltage controlled oscillator and receive PLL charge pump. These pins should be de-coupled to ground, as close to each pin as possible, with RF quality 100pF and 1.0nF ceramic capacitors.
RVCO **/RVCO**	(41,42)	Receive VCO Tank: These single-end outputs drive the external, balanced, RxVCO resonant tank circuit. The tank circuit generates the overall oscillation frequency for the RxVCO. The RxVCO tank frequency is 2X the desired Rx LO frequency, since the on-chip quadrature generation circuitry divides this LO signal by 2. The CHIP-CEIVER™ is a direct conversion, zero-IF receiver, therefore the quadrature LO frequency is the same as the receive frequency, (i.e. no IF offsets). Careful layout is required to prevent RF leakage to the TxVCO tank circuit and associated transmit circuitry.
IFSET	(44)	IF Filter: This pin connects to an external resistor, which sets the corner frequencies of the IF transconductance (gm) filter stages.
ACGND	(45)	AC Ground: This pin connects to an external 100 nF capacitor connected to VSSA, which provides de-coupling for the internal baseband and IF filter ground nodes.

PIN DESCRIPTIONS - Cont.

AFC   (46)   Automatic Frequency Control: This output pin connects to an external filter, which provides the DC control voltage for the automatic frequency control (AFC) circuitry. The component values of the filter establish the AFC loop delay or "attack time".

AFCC   (47)   Automatic Frequency Control Capacitor: This pin connects to external de-coupling capacitors (150 nF), which provide filtering for an internal reference voltage.

AUDO   (48)   Audio Output: In the Analog mode, this output pin provides the recovered, demodulated audio signal. The audio signal level is 200 mVrms. (typ). In the Digital mode, this CMOS compatible output provides serial data from the internal data slicer.

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Tx/Rx PLL PROGRAMMING and SERIAL INTERFACE

The Tx/Rx VCO divide ratios are controlled by a standard 3-wire bus comprised of Clock, Load Enable, and Data inputs. The programming word contains 20 bits, the first two bits select the programming of the receive VCO frequency, the transmit VCO frequency, the reference frequency or the device operational modes. The remaining bits contain the data to be programmed.
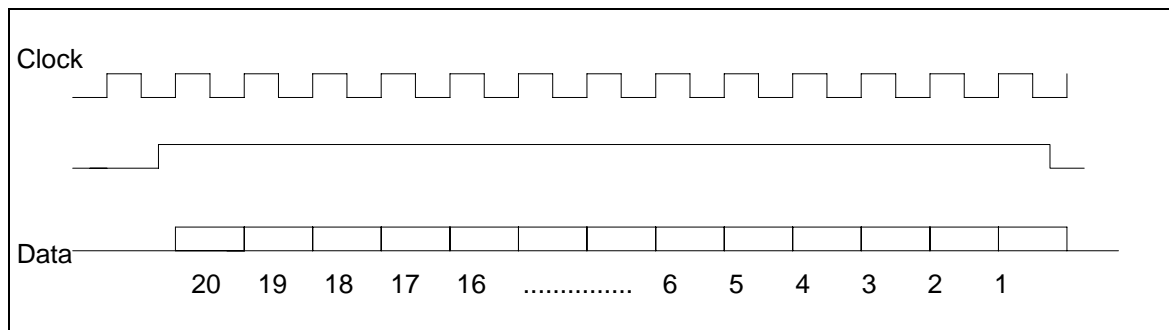
The above diagram shows the programming format.

Data is clocked into the internal shift registers on the positive edge of the CLOCK (3) pin, while Load Enable (1) pin is held HIGH. Data is loaded from the shift registers into the data registers on the negative edge of the Load Enable (LE). This load is NOT synchronized with the programmable divider, i.e. the load is controlled directly by the negative falling edge of the Load Enable.

Data Register Contents

Reference Frequency Select

Bit 1 (last bit loaded)		Load control bit 1 = (0)
Bit 2		Load control bit 2 = (0)
Bit 3	Ref(1) LSB	Reference divide register (count 1 to 1024)
Bit 4	Ref(2)	Reference divide register (count 1 to 1024)
Bit 5	Ref(3)	Reference divide register (count 1 to 1024)
Bit 6	Ref(4)	Reference divide register (count 1 to 1024)
Bit 7	Ref(5)	Reference divide register (count 1 to 1024)
Bit 8	Ref(6)	Reference divide register (count 1 to 1024)
Bit 9	Ref(7)	Reference divide register (count 1 to 1024)
Bit 10	Ref(8)	Reference divide register (count 1 to 1024)
Bit 11	Ref(9)	Reference divide register (count 1 to 1024)
Bit 12	Ref(10) MSB	Reference divide register (count 1 to 1024)

Internal Reference Frequency = (Reference Oscillator Frequency) / Ref(10:1)

PLL Data Register Contents Cont.

Receive VCO Frequency Select

Bit 1 (last bit loaded)	Load control bit 1 = (1)			
Bit 2	Load control bit 2 = (0)			
Bit 3 LSB VCO frequency	A	Ra(1)	A register
Bit 4 VCO frequency	A	Ra(2)	A register
Bit 5 VCO frequency	A	Ra(3)	A register
Bit 6 VCO frequency	A	Ra(4)	A register
Bit 7 MSB VCO frequency	A	Ra(5)	A register
Bit 8 LSB VCO frequency	M*	Rm(1)	M register
Bit 9 VCO frequency	M	Rm(2)	M register
Bit 10 VCO frequency	M	Rm(3)	M register
Bit 11 VCO frequency	M	Rm(4)	M register
Bit 12 VCO frequency	M	Rm(5)	M register
Bit 13 VCO frequency	M	Rm(6)	M register
Bit 14 VCO frequency	M	Rm(7)	M register
Bit 15 VCO frequency	M	Rm(8)	M register
Bit 16 VCO frequency	M	Rm(9)	M register
Bit 17 MSB VCO frequency	M	Rm(10)	M register

Bit 18   Rx VCO Trim bit 1

Bit 19   Rx VCO Trim bit 2

Bit 20   Rx VCO Trim bit 3

*Future version to provide an additional M counter bit.

RxVCO Frequency = Internal Reference Frequency x $(32 \times M(10{:}1) + A(5{:}1))$

Rx VCO Trim Bits			
3	2	1	Trim Number
0	0	0	0 – Minimum C
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7 – Maximum C

PLL Data Register Contents - Cont.

Transmit VCO Frequency Select

Bit 1 (last bit loaded)	Load control bit 1 = (0)			
Bit 2	Load control bit 2 = (1)			
Bit 3 LSB VCO frequency	A	Ta(1)	A register
Bit 4 VCO frequency	A	Ta(2)	A register
Bit 5 VCO frequency	A	Ta(3)	A register
Bit 6 VCO frequency	A	Ta(4)	A register
Bit 7 MSB VCO frequency	A	Ta(5)	A register
Bit 8 LSB VCO frequency	M	Tm(1)	M register
Bit 9 VCO frequency	M	Tm(2)	M register
Bit 10 VCO frequency	M	Tm(3)	M register
Bit 11 VCO frequency	M	Tm(4)	M register
Bit 12 VCO frequency	M	Tm(5)	M register
Bit 13 VCO frequency	M	Tm(6)	M register
Bit 14 VCO frequency	M	Tm(7)	M register
Bit 15 VCO frequency	M	Tm(8)	M register
Bit 16 VCO frequency	M	Tm(9)	M register
Bit 17 MSB VCO frequency	M	Tm(10)	M register

Future version to provide an additional M counter bit.

Bit 18   Tx VCO Trim bit 1
Bit 19   Tx VCO Trim bit 2
Bit 20   Tx VCO Trim bit 3

TxVCO Frequency = Internal Reference Frequency x $(32 \times M(10{:}1) + A(5{:}1))$

Tx VCO Trim Bits			
3	**2**	**1**	**Trim Number**
0	0	0	0 – Minimum C
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7 – Maximum C

PLL Data Register Contents - Cont.

Mode and Test Mode select

Bit 1   Load Control Bit 1   (Last bit loaded)
Bit 2   Load Control Bit 2
For Mode and Test Mode select (BIT 2 = 1, Bit 1 = 1,)

Bit 3	Auto Gain Control	0 = Off	1 = On
Bit 4	Receive Section	0 = Off	1 = On
Bit 5	Transmit Section	0 = Off	1 = On
Bit 6	Receive Charge Pump Current	0 = 0.2mA	1 = 1.0mA
Bit 7	Transmit Charge Pump Current	0 = 0.2mA	1 = 1.0mA
Bit 8	Rx Charge Pump Polarity	0 = Normal	1 = Invert
Bit 9	Tx Charge Pump Polarity	0 = Normal	1 = Invert
Bit 10	Mixer Gain Control	(Bit 1)	
Bit 11	Mixer Gain Control	(Bit 2)	
Bit 12	Baseband Gain & RF Pad Cntrl	(Bit 1)	
Bit 13	Baseband Gain & RF Pad Cntrl	(Bit 2)	
Bit 14	Baseband Gain & RF Pad Cntrl	(Bit 3)	
Bit 15	AFC Polarity	0 = Normal	1 = Invert
Bit 16	AFC Enable	0 = Disable	1 = Enable
Bit 17	Audio/Data Output Select	0 = Analog	1 = Digital
Bit 18	Test Mode	(Bit 1)	
Bit 19	Test Mode	(Bit 2)	
Bit 20	Test Mode	(Bit 3)	

<u>TEST MODE</u>

Test Bits				Test Mode
3	2	1	I.D	
0	0	0		Normal Mode
0	0	1	TeA	Divider outputs at AUDO (digital) - Rx on Rxsynth out; Tx on Tx synth out; Rx + Tx on Ref synth out
0	1	0	TeB	6 poles of IF filter bypassed
0	1	1	TeC	Demodulator test – Input at IF filter input via AFCC (47) pin, AFC disabled
1	0	0	TeD	I Baseband output routed to AUDO (analog)
1	0	1	TeE	Q Baseband output routed to AUDO (analog)
1	1	0	TeF	2nd Mixer output routed to AUDO (analogue)
1	1	1	TeG	IF filter test – input at IF filter input via AFCC, filter output routed to AUDO (analog); AFC disabled

PLL Data Register Contents - Cont.

Gain Control – (Automatic / Manual)

Gain switches to maximum following Load Enable (1) HIGH. The receive signal level is evaluated at intervals of 0.5ms and depending upon its signal level, the receiver gain is either unchanged, stepped up, or stepped down by one gain control increment, according to the table below. For example, if the channel is changed and the received signal is very strong then the change from maximum to minimum gain would take 7 x 0.5ms = 3.5ms.

Auto Mode (Bit 3 = 1)

Nominal RF Signal Level		Voltage Gain dB				
		RF section		Baseband section		
Increasing	Decreasing	RF pad	RF Mixer	1st Block	2nd Block	3rd Block
	< -86dBm	0	15	10	10	10
> -80dBm	< -76dBm	0	15	0	10	10
> -70dBm	< -66dBm	0	5	0	10	10
> -60dBm	< -56dBm	0	5	0	0	10
> -50dBm	< -46dBm	0	-5	0	0	10
> -40dBm	< -36dBm	0	-5	0	0	0
> -30dBm	< -26dBm	-10	-5	0	0	0
> -20dBm		-10	-20	0	0	0

Manual Mode (Bit 3 = 0)

Mixer Gain Control		Baseband Gain & RF Pad Control			Voltage Gain dB				
					RF section		Baseband section		
2	1	3	2	1	RF pad	RF Mixer	1st Block	2nd Block	3rd Block
0	0	X	X	X		-20			
0	1	X	X	X		-5			
1	0	X	X	X		5			
1	1	X	X	X		15			
X	X	0	0	0	-10		0	0	0
X	X	0	0	1	0		0	0	0
X	X	0	1	0	0		0	0	10
X	X	0	1	1	0		0	10	10
X	X	1	0	0	0		10	10	10
X	X	1	0	1	-10		10	10	10
X	X	1	1	0	-10		10	10	0
X	X	1	1	1	-10		10	0	0

ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
OVERALL DEVICE:					
Power Supply Voltage	Vdd	2.7	3	3.3	V
Operating Temperature	Topr	-20		65	C
Frequency of Operation	Fin	902		928	MHz
SYSTEM LEVEL SPECIFICATIONS: (See applications circuit (Fig. 3) for additional details)					
Input Sensitivity (12db SINAD)		-114	-115		dBm
Noise Figure **	NF		4.7	6.3	dB
Input IP3	IIP3	-7.9	-6.9		dBm
Adj. Channel Rej.* (20dB SINAD)	ACI	55	65	70	dB
Out of Band Rejection		70			dB
Tx Carrier Rejection		65			dB
Receiver Bandwidth (-3dB)		110	120	130	kHz
RSSI (-116 to -66)**	RSSI	0.2		2	Vdc
RSSI Conversion Factor (Log)		-25	-30	-35	mV/dB
Channel Spacing			150		kHz
Channel Step Size		50			kHz
L.O. Spurious Output			-60	-57	dBc
Tx Output Power (At Antenna Input)	Po	-3	-0.5	1	dBm
Tx-Rx Frequency Bands		902.3-905.0 & 925.05-927.75			MHz
DEVICE LEVEL SPECIFICATIONS:					
Noise Figure **	NF		8.5	9.2	dB
Input IP3	IIP3	3.1	4		dBm
Input 1dB compression point	ICP	-25	-24		dBm
Desensitisation (5dB SINAD)		-16	-15		dBm
I/Q Phase Imbalance (overall)			1	3	Deg.
I/Q Amplitude Imbalance (overall)			0.5	1	dB
Standby Current	Istb		50		A
Rx Current Consumption (w/RF VCO)	Idd(Rx)		25		mA
Total Current Consumption (Rx+Tx)	Idd(Total)		40	44	mA
RECEIVER SECTION: (Device)					
PLL (Rx)					
Phase Noise (10kHz Offset)		-85	-90		dBc/Hz
Spurious Products (Unwanted)		-60			dBc
Step Size		50			kHz
Reference Frequency (External)		5		20	MHz
RF Quadrature Mixer					
Gain (Hi/Lo) ***	Gv	24/14	25/15	26/16	dB
Noise Figure	NF		7.7	8.5	dB
Input IP3	IIP3	6.1	6		dBm
Output 1dB compression point	OCP		-21		dBm
Amplitude Imbalance				0.5	dB
Phase Imbalance				1	Deg

* 300kHz Channel Spacing ** RF Gain Control (High) *** Includes External Input Balun, (See Application Circuit, Figure (3))

ELECTRICAL SPECIFICATIONS – Cont.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Buffer Amplifier					
Gain	Gv	4.8	5	5.2	dB
Gain	Gp	8.5	8.7	9	dB
Noise Figure	NF		3.3	3.8	dB
Input IP3	IIP3	10.5	10.3		dBm
Output 1dB compression point	OCP		-17		dBm
LPF1 Filter (Sallen-Key)					
Gain	Gv, Gp	11.8	12	12.2	dB
Noise Figure	NF		4.9	5.4	dB
Output 1dB compression point	OCP		-13		dBm
Corner Frequency (-3dB)			60		kHz
Filter Poles			2		
LPF2 Filter (Transconductance)					
Gain	Gv, Gp	5	6	7	dB
Noise Figure	NF	20	21	22	dB
Output 1dB compression point	OCP		-19		dBm
Corner Frequency (-3dB)			70		kHz
Filter Poles			6		
Variable Gain Amplifier / DC Offset					
Gain Range	Gv, Gp		40		dB
Noise Figure	NF		11.8	12.3	dB
Quadrature Mixer (Up-conversion)					
Gain	Gv, Gp	-1.5	0	1.5	dB
Noise Figure	NF	19	20	21	dBm
Amplitude Imbalance			0.1	0.2	dB
Phase Imbalance				0.2	Deg
IF Bandpass Filter (BPF)					
Gain	Gv, Gp	-1	0	1	
Noise Figure	NF		36	37	dB
Lower Corner Frequency (-3dB)		75	80	85	kHz
Upper Corner Frequency (-3dB)		200	220	240	kHz
Poles			10		
Audio Output*					
Output Level (Std.Test Conditions)		170	200	230	mVrms
SINAD (-85dBm RF Level)			40		dB
SNR (-85dBm RF Level, +/-25kHz)			56		dB
Output Impedance (AUDOUT, Pin 13)		2		10	kohms
Bandwidth (-3dB)		0.3		48	kHz
Beat Note Level			-75		dBc
Automatic Frequency Control (AFC)					
Correction Range (+/-)			20		kHz
Frequency Tolerance		100	200	300	Hz

* Maximum run length (digital mode) 1mS.
High frequency audio response to be 72kHz in future version.

ELECTRICAL SPECIFICATIONS – Cont.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
TRANSMIT SECTION: (Device)					
PLL (Tx)					
Phase Noise (10kHz Offset)		-85	-90		dBc/Hz
Phase Noise (100kHz Offset)		-105	-108		dBc/Hz
Phase Noise (1.0MHz Offset)		-125	-128		dBc/Hz
Phase Noise (22.75MHz Offset)		-150	-155		dBc/Hz
Spurious Products (Unwanted)		-60			dBc
Step Size		50			kHz
Reference Frequency (External)		5		20	MHz
Power Amplifier (PA)**					
Power Output		0	1.5	3	dBm
Harmonic Level (2nd)			-54.2		dBc
Harmonic Level (3rd)			-44.2		dBc
Harmonic Level (4th)			-70.9		dBc
Transmit Audio Response					
Input Level (Standard Test Conditions)			200		mVrms
Bandwidth (-3dB)*		0.1		48	kHz

* Maximum run length (digital mode) 1mS.

   High frequency audio response to be 72kHz in future version.

** Includes External Output Balun, (See Applications Circuit, Figure (3))

BOARD LAYOUT

Designing ultra-high frequency (UHF) RF circuits requires careful attention to detail and layout. Careful attention to layout should be observed to minimize stray inductance and capacitance effects. This attention to detail will preserve RF sensitivity of the NT2903 CHIP−CEIVER™. At high frequencies, microstrip or strip-line transmission line techniques must be employed. Using "state-of-the-art" CAD techniques for PCB layout, standard FR-4 fiberglass PCB material (1.6-mm thickness) may be employed. For maximum performance, however, RF quality substrate material should be used.

SUPPLY DECOUPLING

Positive supply connections for the NT2903 are nominally 2.7V to 3.3V. All supply pins must be bypassed to an RF, Analog, or Digital ground plane depending upon the type of supply pin. For RF supply pins, a 100 pF ceramic capacitor in parallel with a 1.0 nF ceramic capacitor, both RF quality, should provide adequate decoupling. For analog and digital supply pins, 0.01-0.1μF RF quality capacitors should be used. The bypass capacitors should be placed as close to all power supply pins as possible. An effort should be made to minimize the trace length between the capacitor leads and the respective NT2903 power supply and common pins.

GROUNDING

The circuit designer should attempt to locate the NT2903 CHIP-CEIVER™, associated analog input circuitry and interconnections as far as possible from logic circuitry. A solid RF analog ground should be placed around the LNA and associated RF filter circuitry, while a solid digital ground should be placed around the reference oscillator. Analog signals should be routed as far as possible from digital signals and should cross them at right angles. Ground connections for the NT2903. Connect all ground pins together to a low impedance ground plane, as close to the device as possible. Observe proper RF grounding and shielding techniques. The NT2903 CHIP-CEIVER™ should be used with separate analog and digital ground planes. The digital and analog ground planes should be "summed" at one point, typically at the power supply filter capacitor.

OPERATING PRECAUTIONS

NUMA Technologies' plastic molded BiCMOS LSI devices are designed and manufactured for trouble-free operation when used under normal operating conditions. Our products are subjected to stringent electrostatic, mechanical strength, and environmental tests for assured reliability. When working with our products the user should observe the following precautions:

(1) Use the product in the range of the rated operating voltage, operating temperature, operating input/output voltage and input/output current. If the product is used outside these operating parameters, the user may experience high failure rates.

(2) Do not expose the product to excessive mechanical vibration, repetitive shock, or rapid or cyclic temperature changes. These factors can cause the bond wires in the plastic package to break.

(3) Although all terminals have electrostatic protection, damage may still occur if very high electrostatic potentials are applied. Use of a conductive container or aluminum foil for packaging and transportation is recommended. (Untreated plastic containers are NOT recommended.) Use grounded soldering tools and test equipment.

(4) The NT-2902 employs Electrostatic Discharge (ESD) protection. CMOS inputs shall be rated to 2Kv human body model / 1Kv charge contact model. Bipolar RF inputs shall be protected to the greatest extent possible and consistent with industry standards, while meeting RF performance parameters.

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APPLICATION INFORMATION -- "900 MHz" Analog Cordless Telephone

A circuit diagram for a high performance, cordless telephone transceiver is shown in Figure (3). This circuit is applicable to cordless phones compliant for use in the USA operating in the 902-928 MHz ISM band. The circuit will operate with a supply voltage of 2.7V to 3.3V. The "adjustment free" discriminator of the CHIP-CEIVER™, along with the elimination of IF filters, provides a cost effective solution to cordless telephone applications.

Tuning and power management functions for the NT2903 (U2) are accessed via an industry standard 3-wire compatible serial interface. The "printed" VCO inductors (L4, L5, L7, and L8) allow the transceiver to be tuned over the range of 902 to 928 MHz. An RF duplexer comprised of two dielectric resonant filters (FL1 and FL2) and a SAW filter (FL3) provide all of the required RF filtering. A low cost microprocessor with an analog-to-digital converter (A/D) input, can be used to measure the RSSI pin (36) of U2, which is proportional to the receive signal strength.
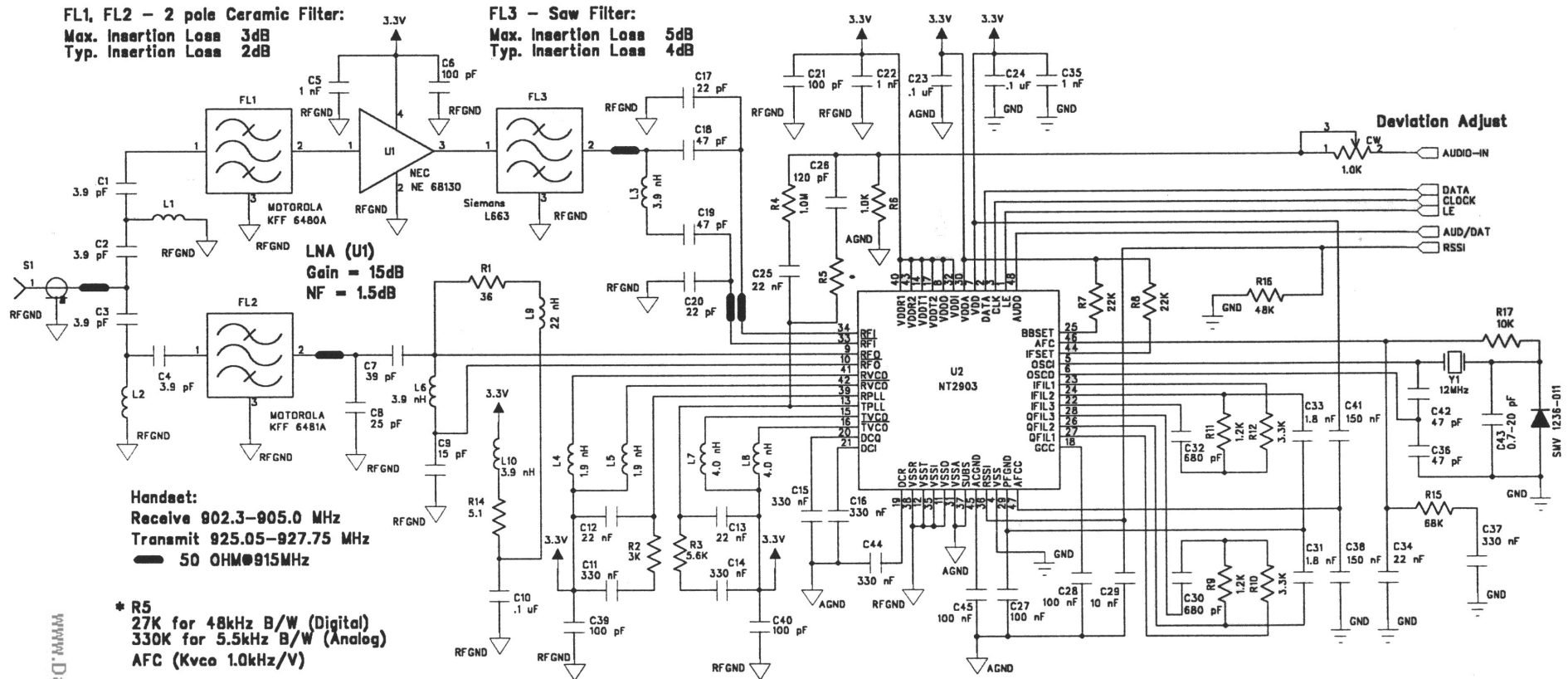
Figure (3), "900 MHz", High Performance, Cordless Telephone

RECEIVER TEST SPECIFICATIONS:

Standard Receiver Test Conditions:

Unless otherwise specified, the standard receiver test conditions are:
TA = 25°C
Fmod = 1kHz
RF input carrier deviation = 25kHz peak
Detected audio is C message weighted
Interfering carrier deviation = 25kHz
$F_{MOD\ INT} = 400Hz$
TxVCO On, locked, and modulated

Sensitivity & Noise Figure:

Given the worst case variation in the external blocks used in the receiver design, as shown in Fig. (3), the recovered audio SINAD shall be ≥12 dB @ RF input level of -114dBm. Typically, the 12dB SINAD is achieved at RF input level of -115dBm.

Output Audio Level:

The nominal audio output level with ±25kHz FM deviation shall be ≥ 200 mVrms.

Dynamic Range:

The Rx section of the NT2903 must maintain all aspects of specified operation from the lower RF input limit up to 0 dBm. (experience no significant change in the overall performance) There shall be no disruption in the Prescaler or the VCO operation (both Tx and Rx). Additionally, the device shall withstand input power levels of up to +5dBm at the NT2903 RF inputs (/RFI, RFI), without damage.

The system SINAD and SNR resulting from an RF level being applied at 20dB above the minimum RF input level (required to produce 12dB SINAD) shall be maintained up to the maximum specified RF input level of 0 dBm. Also, the specified recovered audio output level at the audio output pin, AUDO (48) shall be maintained.

Intermodulation:

Given the worst case variations in the external circuit blocks, the input IP3 shall not be lower than -14 dBm. (this occurs using the typical Ceramic & SAW filter losses).

The test (standard two tone test)conditions for this test are two equal level carriers placed on the 1st & 2nd adjacent channels to the desired test channel. For intermodulation test the 1st adjacent carrier is unmodulated but the 2nd adjacent is modulated with 400Hz tone & 25kHz deviation.

Spurious Response:

a) *Spurious Responses due to I/P signals > ± 500kHz of the Channel Center Freq.:*
Spurious responses due to prescaler generated products which are modulated onto the LO should allow an interfering input signal to be at least 70 dB higher than the minimum RF carrier input level required to produce 25 dB SINAD. The resulting in-band spurious signal may be allowed to degrade the SINAD from 25 to 20dB.

Receiver spurious response is also measured for various possible interfering frequencies and should allow an interfering input signal(e.g. 1/2 Tx LO+/-IF, 2 TxLO-RXLO +/-IF etc.) to be at least 70 dB higher than the minimum RF carrier input level required to produce 25 dB SINAD. The resulting in-band spurious signal may be allowed to degrade the SINAD from 25 to 20dB.

b) *Spurious Responses due to I/P signals +/- 325 to 500 kHz of the Channel Center Freq.:*
The receiver should allow an interfering input signal to be at least 60 dB higher than the minimum RF carrier input level required to produce 25 dB SINAD. The resulting in-band spurious signal may be allowed to degrade the SINAD from 25 to 20dB.

c) *Adjacent Channel:*
For the adjacent channel rejection measurement interfering carrier is applied at Fc ± one channel spacing. The receiver should allow an interfering adjacent channel input signal to be at least 55 dB higher than the minimum RF carrier input level required to produce 25 dB SINAD. The resulting adjacent channel signal may be allowed to degrade the SINAD from 25 to 20dB.

d) *Common Channel Suppression:*
Common channel suppression is used to express the ability of the receiver to discriminate against a modulated signal of the same frequency. The receiver common channel suppression should be greater than -12dB for analog modulated signals. The resulting co-channel signal may be allowed to degrade the SINAD from 25 to 20dB.

Output match for the external SAW filter:

The NT2903 shall present an input of match of 10dB or better over the pass band for the SAW filter output. The NT2903 receiver performance should not degrade due to an out-of-band impedance presented by the SAW filter at the RF inputs /RFI(33), RFI(34).

Port Isolation:

The Rx LO leakage at the RF input port shall be <-50dBm.

Rx Spurious Emissions:

The maximum level of any Rx spurious output shall be <-70dBm at the antenna.

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Transmitter Test Specifications:

Spurious Outputs: The maximum spurious output levels at the antenna for the transmitter operating on both handset and base frequencies are shown below in Fig.(4) and Fig. (5)
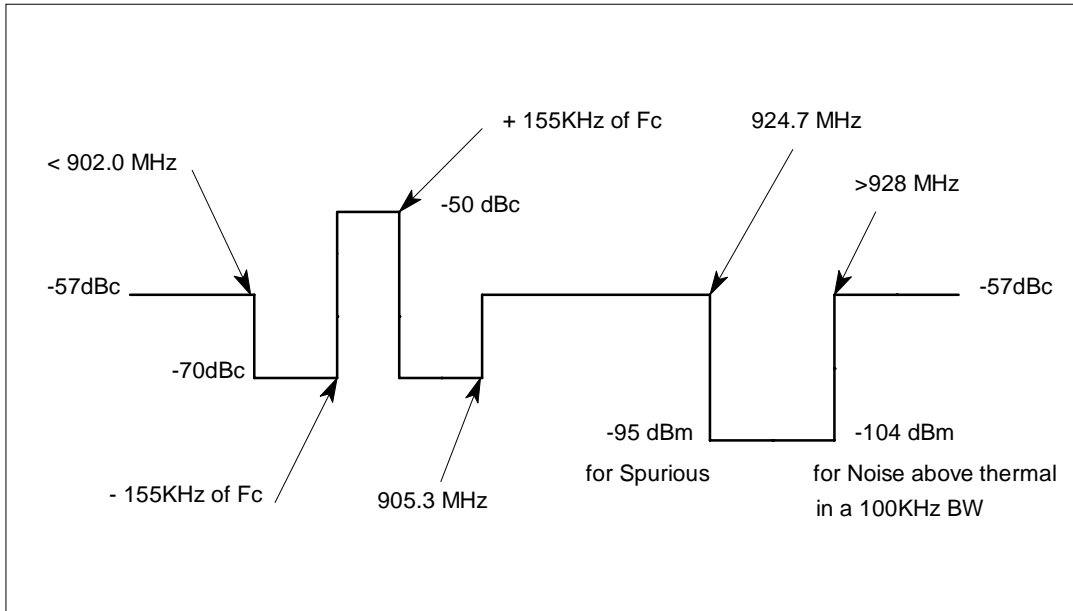

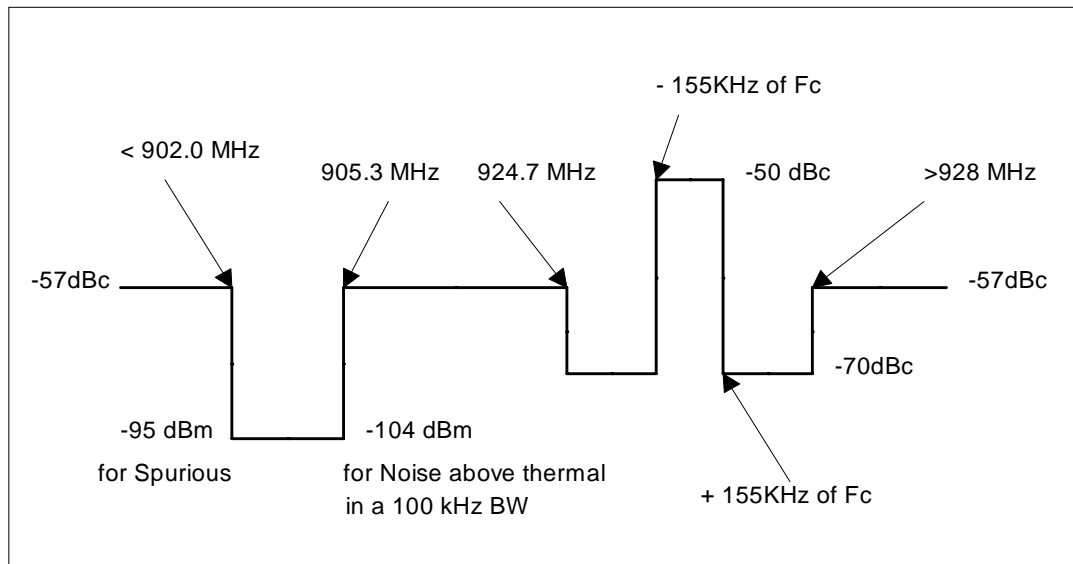Figure (4) - Base Transmitter Spurious Limits

Figure (5) - Handset Spurious Output Limits

Any spurious signals produced by the device shall met FCC spurious emissions specifications, as specified under part 15, section 15.209 of the FCC rules, with reasonable margin.

Tx & Rx VCOs:

Tx & Rx VCO's shall tune over a frequency range of 902-928 MHz and over the temperature range of –10 to 60°C. The amplitude variation over the total tuning range should be less than 1dB.(± 0.5dB) The maximum change in the VCO frequency in the locked state due to different loads (short/open) or when antenna is touched or brought near a metal object at the antenna input shall be ±2.5 kHz.

Tx Amplifier:

Power level at the output of the amplifier shall be +1.5dBm with a variation in power level < ±1.5 dB. (This includes the variations in amplitude from the VCO as well)

Load Pull:

The Tx amplifier should be stable (in-band) over VSWR of 10:1, the transmitter frequency change under the similar circumstances should not be more than ± 2.5kHz.

Transmitter Test:

The transmitter modulation response and SINAD shall not change while the Rx receive levels vary from 0 to -116dBm. The transmitter performance shall also remain unaffected over the specified temperature range of –10 to 60°C, TxVCO loop voltage, and when different loads are presented at the antenna.

Device Test Specifications (NT2903)

De-sensitization:

Receiver de-sensitization shall be tested by applying an interferer, ±500kHz from the receive carrier frequency, at the input of the device along with a desired signal. The desired signal shall be applied such that a reference SINAD of 25dB is achieved. Furthermore, an interferer shall be applied at a power level of –15dBm. The resultant SINAD shall not be less than 20dB, in the presence of the specified interferer.

IIP3 Measurement:

The Input IP3 for the *device* (NT2903) shall be tested by applying two (2) interfering signals at the input of the device along with a desired signal. The desired signal level at the input to the device shall be set at –77dBm. Given the desired signal level, the measured SINAD shall not exceed a reduction of 5dB from the reference SINAD of ≥25dB, in the presence of the specified interferers. The interferers shall have the following characteristics:

        T1   -25dBm, Fc+300kHz, Modulation = Off
        T2   -25dBm, Fc+600kHz, Modulation = 400Hz, ±25kHz Deviation

Frequency Tables:

This section outlines the frequencies and corresponding channel numbers used by the handset and base unit of both 900 MHz analog and digital phones.

Handset:

Channel	Transmit	Receive	Rx LO
1	925.05	902.3	1804.6
2	925.35	902.6	1805.2
3	925.65	902.9	1805.8
4	925.95	903.2	1806.4
5	926.25	903.5	1807.0
6	926.55	903.8	1807.6
7	926.85	904.1	1808.2
8	927.15	904.4	1808.8
9	927.45	904.7	1809.4
10	927.75	905.0	1810.0

Base:

Channel	Transmit	Receive	Rx LO
1	902.3	925.05	1850.1
2	902.6	925.35	1850.7
3	902.9	925.65	1851.3
4	903.2	925.95	1851.9
5	903.5	926.25	1852.5
6	903.8	926.55	1853.1
7	904.1	926.85	1853.7
8	904.4	927.15	1854.3
9	904.7	927.45	1854.9
10	905.0	927.75	1855.5