MP7641

8-Channel Voltage Output 10 MHz Input Bandwidth 8-Bit Multiplying DACs with Serial Digital Port

FEATURES

- 8 Independent 2-Quadrant Multiplying 8-Bit DACs
- Dual Positive (+10 V and +5 V) Supplies or Dual (±5 V) Supplies Capability
- High Speed:
  - 12.5 MHz Digital Clock Rate
  - V_{REF} to V_{OUT} Settling Time: 150ns to 8–bit (typ)
  - Voltage Reference Input Bandwidth: 10 MHz
- Low Power: 150mW
- Low AC Voltage Reference Feedthrough
- Excellent Channel-to-Channel Isolation
- DNL = ±0.8 LSB, INL = ±1 LSB (typ)
- DACs Matched to ±0.5% (typ)
- Chip Select Available: MP7651
- Low Harmonic Distortion: 0.25% typical with V_{REF} = 1 V p-p @ 1 MHz
- $V_{REF}/2$ Output Preset Level
- Latch-Up Free
- ESD Protection: 2000 V Minimum

APPLICATIONS

- Direct High-Frequency Automatic Gain Control
- Video AGC & CCD Level AGC
- Convergence Adjustment for High-Resolution Monitors (Workstations)

GENERAL DESCRIPTION

The MP7641 is ideal for direct gain control of video, composite video, CCD and other high frequency analog signals. The device includes 8-channels of high speed, high bandwidth, two quadrant multiplying, 8-bit accurate digital-to-analog converter. It includes an output drive buffer per channel capable of driving a ±1mA (typ) to a load. DNL of better than ±0.8 LSB is achieved with a channel-to-channel matching of better than 0.5% (typ). Stability, matching, and precision of the DACs are achieved by using EXAR's thin film technology. Also, excellent channel-to-channel isolation is achieved with EXAR's BiCMOS process which cannot be achieved using a typical CMOS technology.

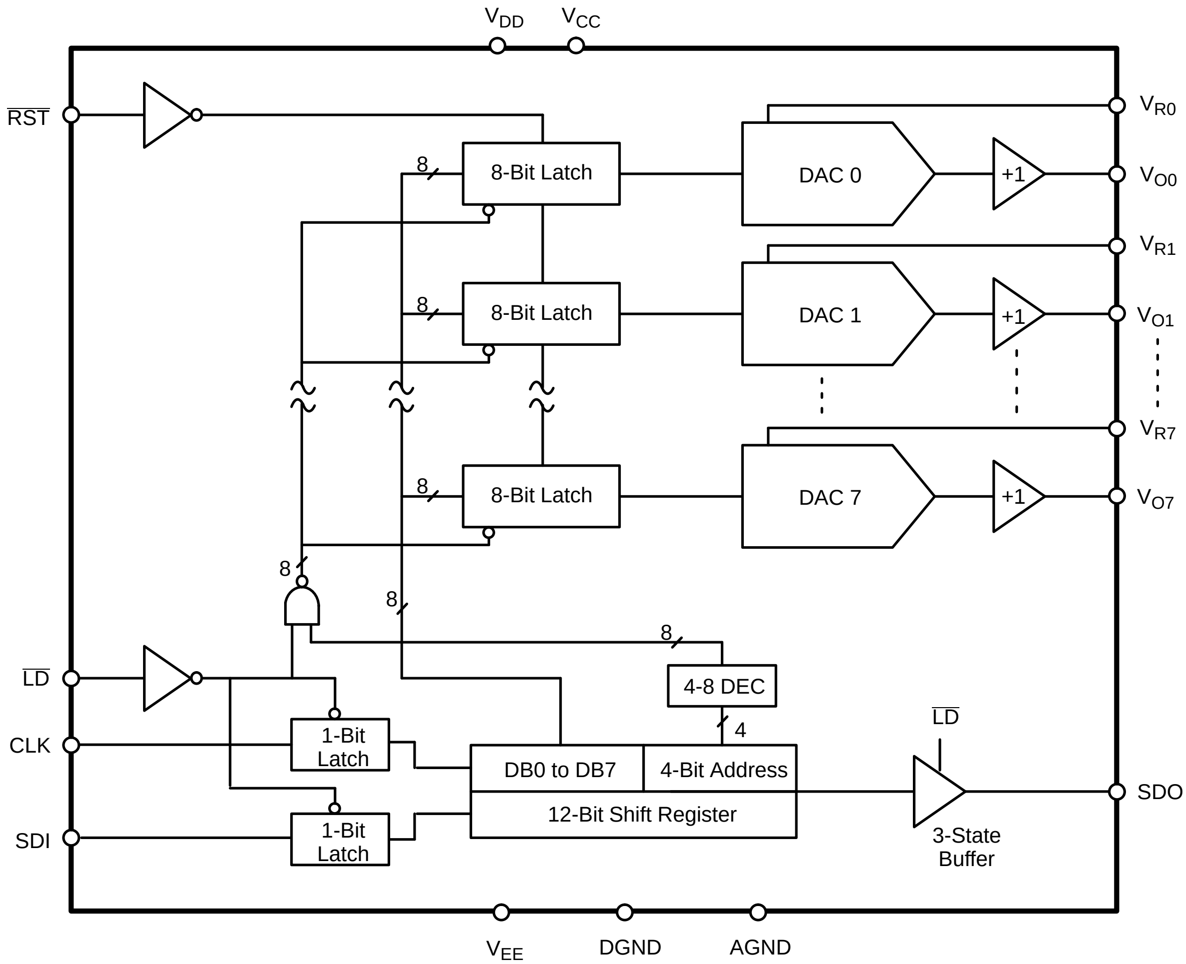
An open loop architecture (patent pending) provides wide small signal bandwidth from V_{REF} to output up to 10 MHz (typ), fast output settling time, and V_{REF} feedthrough isolation of –65dB or better. In addition, low distortion in the order of 0.25% with a 1 V p-p, 1 MHz signal is achieved.

The combination of a constant input Z and the ability to vary AGND within ±300 mV allows flexibility for optimum system design.

The MP7641 has a serial data 3-wire standard µ-processor logic interface to reduce pin count, package size, and board wire (space).

The MP7641 is fabricated on a junction isolated, high speed BiCMOS (BiCMOS IV™) process with thin film resistors. This process enables precision high speed analog/digital (mixed-mode) circuits to be fabricated on the same chip.

SIMPLIFIED BLOCK DIAGRAM©

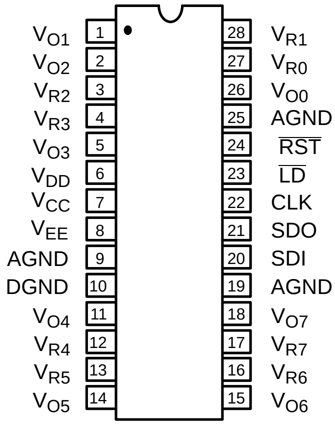


ORDERING INFORMATION

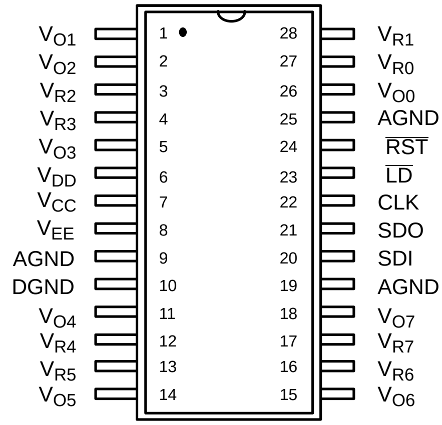
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
SOIC	–40 to +85°C	MP7641AS	±1	±0.8	±1.5
Plastic Dip	–40 to +85°C	MP7641AN	±1	±0.8	±1.5

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP (0.300")
NN28



28 Pin SOIC (EIAJ, 0.335")
R28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	V_{O1}	DAC 1 Output
2	V_{O2}	DAC 2 Output
3	V_{R2}	DAC 2 Reference Input
4	V_{R3}	DAC 3 Reference Input
5	V_{O3}	DAC 3 Output
6	V_{DD}	Digital Positive Supply
7	V_{CC}	Analog Positive Supply
8	V_{EE}	Analog Negative Supply
9	AGND	Analog Ground
10	DGND	Digital Ground
11	V_{O4}	DAC 4 Output
12	V_{R4}	DAC 4 Reference Input
13	V_{R5}	DAC 5 Reference Input
14	V_{O5}	DAC 5 Output
15	V_{O6}	DAC 6 Output

PIN NO.	NAME	DESCRIPTION
16	V_{R6}	DAC 6 Reference Input
17	V_{R7}	DAC 7 Reference Input
18	V_{O7}	DAC 7 Output
19	AGND	Analog Ground
20	SDI	Serial Data/Address Input
21	SDO	Serial Data Output
22	CLK	Shift Register Clock
23	$\overline{LD}$	Load Signal; Load Data to Selected DACs
24	$\overline{RST}$	Reset Signal; Reset all DACs to $V_{REF}/2$
25	AGND	Analog Ground
26	V_{O0}	DAC 0 Output
27	V_{R0}	DAC 0 Reference Input
28	V_{R1}	DAC 1 Reference Input

ELECTRICAL CHARACTERISTICS TABLE FOR DUAL SUPPLIES

Unless Otherwise Noted: V_{DD} = 5 V, V_{CC} = +5 V, V_{EE} = –5 V, V_{REF} = 3 V and –3 V, T = 25°C, Output Load = Open, AGND=DGND=0 V

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DC CHARACTERISTICS								
Resolution (All Grades)	N	8			8		Bits	
Differential Non-Linearity	DNL			±0.8		±1	LSB	
Integral Non-Linearity	INL			±1		±1	LSB	
Monotonicity			Guaranteed		Guaranteed			
Gain Error	GE			±1.5		±1.5	% FSR	FSR = Full Scale Range[1]
Zero Scale Offset	Z_{OFS}		±20	±75		±75	mV	
Output Drive Capability	I_O		±1				mA	
REFERENCE INPUTS								
Impedance of V_{REF}	REF	6	12	18	6	18	kΩ	
Voltage Range	V_R	V_{EE} +1.5		V_{CC} –1.8		V	V_{REF}	Max Swing is AGND ±3 V
DYNAMIC CHARACTERISTICS[2]								R_L = 5 k, C_L = 20 pF
Input to Output Bandwidth			10				MHz	V_R = 1.6 V p–p, R_L = 5kΩ to V_{EE}
Input to Output Settling Time[5]			150				ns	V_R = 1.6 V p–p, R_L = 5kΩ to V_{EE}
Small Signal Voltage Reference Input to Output Bandwidth	ft_r		10				MHz	V_{OUT}=50mV p-p above code 16
Small Signal Voltage Reference Input to Output Bandwidth	ft_r	5	8				MHz	V_{OUT}=50mV p-p for all codes
Voltage Settling from V_{REF} to V_{DAC} Out	t_{sr}		275	300		325	ns	V_R=0 to V_R = 3V Step[6] to 1 LSB
Voltage Settling from Digital Code to V_{DAC} Out	t_{sd}		275	300		325	ns	ZS to FS to 1 LSB
V_{REF} Feedthrough	F_{DT}		–65				dB	Codes=0 @ 1 MHz
Group Delay	GD		20				ns	
Harmonic Distortion	T_{HD}		0.5				%	V_{REF}=1MHz Sine 3V p-p
Channel-to-Channel Crosstalk	C_T		–75				dB	@ 1 MHz, single channel
Digital Feedthrough	Q			1			nVS	CLK to V_{OUT}
Power Supply Rejection Ratio	PSRR			0.02			%/%	ΔV=±5%
POWER CONSUMPTION								
Positive Supply Current	I_{CC}		15	25		30	mA	V_{REF} = 0 V
Negative Supply Current	I_{EE}		15	25		30	mA	V_{REF} = 0 V
Power Dissipation	P_{DISS}		150	250		300	mW	V_{REF} = 0 V, Codes = all 1
DIGITAL INPUT CHACTERISTICS								
Logic High[3]	V_{IH}	2.4			2.4		V	
Logic Low[3]	V_{IL}			0.8		0.8	V	
Input Current	I_L			±10		±10	µA	
Input Capacitance[2]	C_L			8		8	pF	

ELECTRICAL CHARACTERISTICS TABLE

Description	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Conditions
DIGITAL TIMING SPECIFICATIONS[2, 4]								
Input Clock Pulse Width	t_{CH}, t_{CL}	40			50		ns	
Data Setup Time	t_{DS}	10			10		ns	
Data Hold Time	t_{DH}	15			15		ns	
CLK to SDO Propagation Delay	t_{PD}			40		50	ns	
DAC Register Load Pulse Width	t_{LD}	100			100		ns	
Reset Pulse Width	t_{RST}	50			60		ns	
Clock Edge to Load Rising Edge	t_{CKLD1}	100			100		ns	
Clock Edge to Load Falling Edge	t_{CKLD2}	0			0		ns	
Load Falling Edge to SDO 3-state Enable	t_{HZ1}	50			60		ns	
Load Rising Edge to SDO 3-state Disable	t_{HZ2}	35			50		ns	
Load Falling Edge to CLK Disable	t_{LDCK1}	25			40		ns	
Load Rising Edge to CLK Enable	t_{LDCK2}	35			50		ns	
LD Set-up Time with Respect to CLK	t_{LDSU}	15			20		ns	

NOTES

1 Full Scale Range (FSR) is 3V.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 *See Figures 2 and 3*.
5 For reference input pulse: $t_R = t_F \geq 100$ ns.

Specifications are subject to change without notice

ELECTRICAL CHARACTERISTICS TABLE FOR DUAL POSITIVE SUPPLIES

Unless Otherwise Noted: V_{DD} = 5 V, V_{CC} = 10 V, V_{EE} = 0 V, V_{REF} = 3 V and –3 V, T = 25°C, Output Load = Open, AGND = (V_{CC} + V_{EE})/2 = 5 V, DGND = 0 V

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DC CHARACTERISTICS								
Resolution (All Grades)	N	8			8		Bits	
Differential Non-Linearity	DNL			±0.8		±1	LSB	
Integral Non-Linearity	INL			±1		±1	LSB	
Monotonicity			Guaranteed		Guaranteed			
Gain Error	GE			±1.5		±1.5	% FSR	FSR = Full Scale Range[1]
Zero Scale Offset	Z_{OFS}		±20	±75		±75	mV	
Output Drive Capability	I_O		±1				mA	
REFERENCE INPUTS								
Impedance of V_{REF}	REF	6	12	18	6	18	kΩ	
Voltage Range	V_R	V_{EE} +1.5		V_{CC} –1.8		V	V_{REF}	Max Swing is AGND ±3 V
DYNAMIC CHARACTERISTICS[2]								R_L = 5 k, C_L = 20 pF
Input to Output Bandwidth			10				MHz	V_R = 1.6 V p–p, R_L = 5kΩ to V_{EE}
Input to Output Settling Time[5]			150				ns	V_R = 1.6 V p–p, R_L = 5kΩ to V_{EE}
Small Signal Voltage Reference Input to Output Bandwidth	ft_r		10				MHz	V_{OUT}=50mV p-p above code 16
Small Signal Voltage Reference Input to Output Bandwidth	ft_r	5	8				MHz	V_{OUT}=50mV p-p for all codes
Voltage Settling from V_{REF} to V_{DAC} Out	t_{sr}		275	300		325	ns	V_R=0 to V_R = 3V Step[6] to 1 LSB
Voltage Settling from Digital Code to V_{DAC} Out	t_{sd}		275	300		325	ns	ZS to FS to 1 LSB
V_{REF} Feedthrough	F_{DT}		–65				dB	Codes=0 @ 1 MHz
Group Delay	GD		20				ns	
Harmonic Distortion	T_{HD}		0.5				%	V_{REF}=1MHz Sine 3V p-p
Channel-to-Channel Crosstalk	C_T		–75				dB	@ 1 MHz, single channel
Digital Feedthrough	Q			1			nVS	CLK to V_{OUT}
Power Supply Rejection Ratio	PSRR			0.02			%/%	ΔV=±5%
POWER CONSUMPTION								
Positive Supply Current	I_{CC}		15	25		30	mA	V_{REF} = 0 V
Negative Supply Current	I_{EE}		15	25		30	mA	V_{REF} = 0 V
Power Dissipation	P_{DISS}		150	250		300	mW	V_{REF} = 0 V, Codes = all 1
DIGITAL INPUT CHACTERISTICS								
Logic High[3]	V_{IH}	2.4			2.4		V	
Logic Low[3]	V_{IL}			0.8		0.8	V	
Input Current	I_L			±10		±10	µA	
Input Capacitance[2]	C_L			8		8	pF	

ELECTRICAL CHARACTERISTICS TABLE

Description	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Conditions
DIGITAL TIMING SPECIFICATIONS[2, 4]								
Input Clock Pulse Width	t_{CH}, t_{CL}	40			50		ns	
Data Setup Time	t_{DS}	10			10		ns	
Data Hold Time	t_{DH}	15			15		ns	
CLK to SDO Propagation Delay	t_{PD}			40		50	ns	
DAC Register Load Pulse Width	t_{LD}	100			100		ns	
Reset Pulse Width	t_{RST}	50			60		ns	
Clock Edge to Load Rising Edge	t_{CKLD1}	100			100		ns	
Clock Edge to Load Falling Edge	t_{CKLD2}	0			0		ns	
Load Falling Edge to SDO 3-state Enable	t_{HZ1}	50			60		ns	
Load Rising Edge to SDO 3-state Disable	t_{HZ2}	35			50		ns	
Load Falling Edge to CLK Disable	t_{LDCK1}	25			40		ns	
Load Rising Edge to CLK Enable	t_{LDCK2}	35			50		ns	
LD Set-up Time with Respect to CLK	t_{LDSU}	15			20		ns	

NOTES

1 Full Scale Range (FSR) is 3V.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 *See Figures 2 and 3*.
5 For reference input pulse: $t_R = t_F \geq 100$ ns.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)[1,2]

V_{CC} to AGND . . . . +6.5 V
V_{EE} to AGND . . . . –6.5 V
V_{CC} to DGND . . . . +13.0 V
V_{EE} to DGND . . . . –6.5 V
V_{Ri} to AGND . . . . V_{CC} to V_{EE}
V_{Oi} to AGND . . . . V_{CC} to V_{EE}
Digital Input & Output Voltage to DGND –0.5 to V_{DD} +0.5 V

Operating Temperature Range
Extended Industrial . . . . –40°C to +85°C
Maximum Junction Temperature . . . . . –65°C to 150°C
Storage Temperature . . . . 150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Package Power Dissipation Rating @ 75°C
PDIP, SOIC 1000mW
Derates above 75°C . . . . 6mW/°C

NOTES:

1 Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

APPLICATIONS INFORMATION

Refer to Section 8 for Applications Information

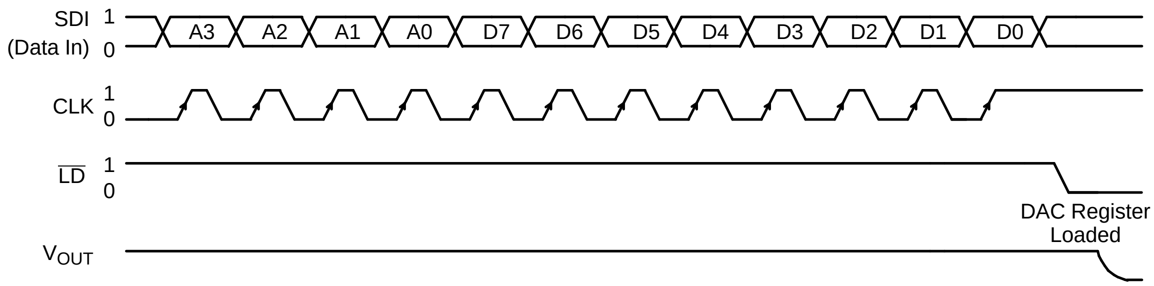


Figure 1. Serial Data Timing and Loading

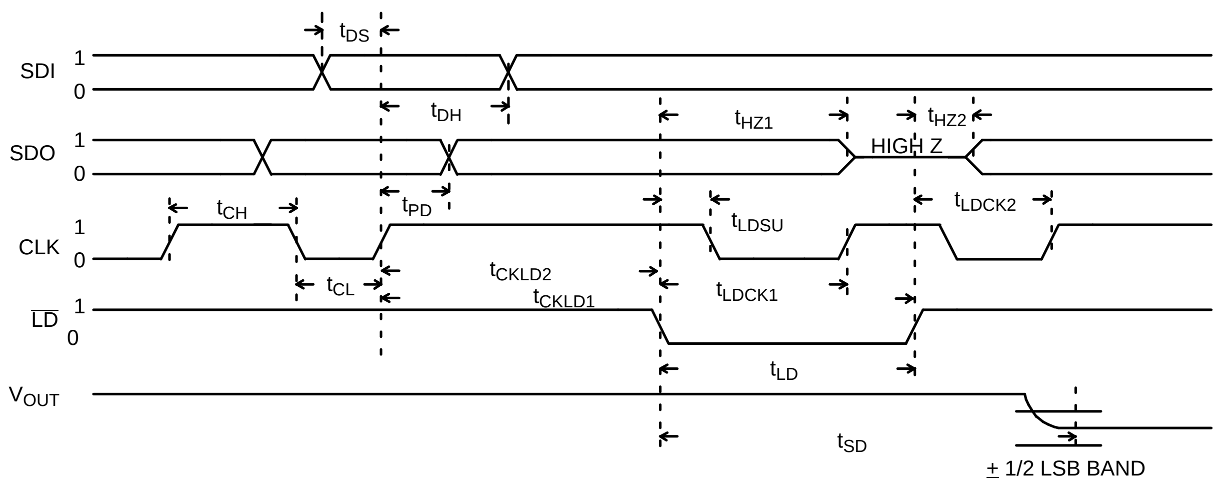


Figure 2. Detail Serial Data Input Timing ($\overline{RST}$ = "1")

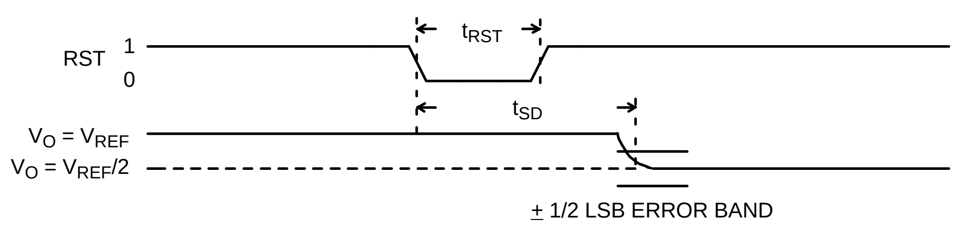


Figure 3. RESET Operation

THEORY OF OPERATION

The MP7641 is equipped with a serial data 3-wire standard µ-processor logic interface to reduce pin count, package size, and board wire (space). This interface consists of $\overline{LD}$ which controls the transfer of data to the selected DAC channel, SDI (serial data/address input), CLK (shift register clock) and SDO (serial data output). When the $\overline{LD}$ signal is high, CLK signal loads the digital input bits (SDI) into the 12-bit shift register (4 bits address A3 to A0, then 8 bits data D7 to D0). The $\overline{LD}$ signal going low loads this data into the selected DAC. The $\overline{LD}$ signal going low also disables the serial data input (SDI), output (SDO 3-stated) and the CLK input. This design tremendously reduces digital noise, and glitch transients into the DACs due to free running CLK and SDI. Also, 3-stating the SDO output with $\overline{LD}$ signal would allow read back of pre-stored digital data of the selected package using one SDO wire for all DAC ICs on the board. Note also that the reset signal ($\overline{RST}$) resets all analog outputs to 1/2 of V_{REF}, regardless of any digital inputs. Note that the input V_{Ri} is referenced to AGND.

Function	A3	A2	A1	A0	$\overline{LD}$	CLK	$\overline{RST}$	SDI	SDO
Shift Data In and Out	X	X	X	X	1	0→1 Repeat	1	Data Input Valid	Data Output Valid
Stop Shifting Data In and Out	X	X	X	X	0	X	1	X	Hi-Z
Load DACs									
	0	0	0	0	No Operation				
DAC 0	0	0	0	1	1→0	X	1	X	Hi-Z
DAC 1	0	0	1	0	1→0	X	1	X	Hi-Z
DAC 2	0	0	1	1	1→0	X	1	X	Hi-Z
DAC 3	0	1	0	0	1→0	X	1	X	Hi-Z
DAC 4	0	1	0	1	1→0	X	1	X	Hi-Z
DAC 5	0	1	1	0	1→0	X	1	X	Hi-Z
DAC 6	0	1	1	1	1→0	X	1	X	Hi-Z
DAC 7	1	0	0	0	1→0	X	1	X	Hi-Z
⋮	⋮	⋮	⋮	⋮	No Operation	X	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	X	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	X	⋮	⋮	⋮
⋮	1	1	1	0	No Operation	X	1	X	Hi-Z
⋮	1	1	1	1	No Operation	X	1	X	Hi-Z
Reset all DACs to $V_{REF/2}$	X	X	X	X	X	X	0	X	X

Table 1. Digital Function Truth Table
Serial In/Serial Out

DB7 MSB	DB6	DB5	DB4	DB3	DB2	DB1	DB0 LSB	DAC Output Voltage $V_{Oi} = AGND + (V_{Ri} - AGND)\left(\frac{D}{256}\right)$
0	0	0	0	0	0	0	0	AGND
0	0	0	0	0	0	0	1	$(V_{Ri} - AGND)\left(\frac{1}{256}\right) + AGND$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	$(V_{Ri} - AGND)\left(\frac{254}{256}\right) + AGND$
1	1	1	1	1	1	1	1	$(V_{Ri} - AGND)\left(\frac{255}{256}\right) + AGND$

Table 2. DAC Transfer Function
Analog Output vs. Digital Code

OPERATION WITH DUAL POSITIVE POWER SUPPLIES

For the dual positive supplies operation, V_{CC} = +10 V, V_{DD} = 5 V, V_{EE} = 0 V and analog output zero level is to be referenced to (V_{CC} + V_{EE}) /2 by setting the AGND pin to 5 V.

MICROPROCESSOR INTERFACE

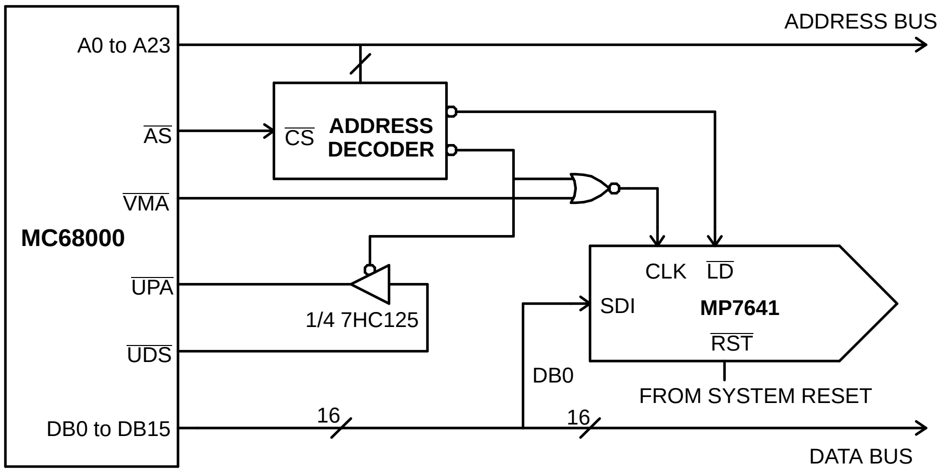
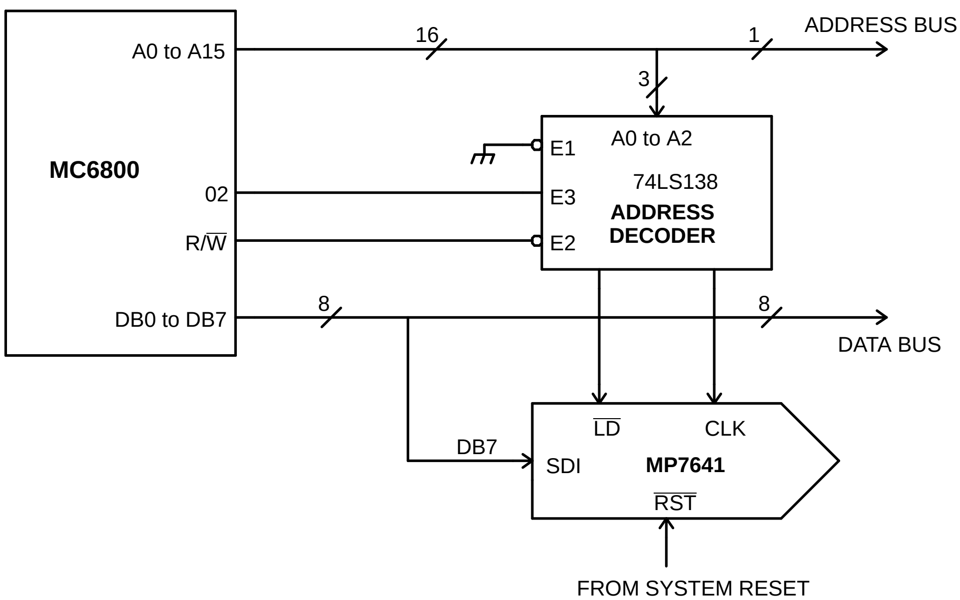


Figure 4. MC68000 Interface (Simplified Diagram)



NOTES:
1. Execute consecutive memory write instructions while manipulating the data between WRITEs so that each WRITE presents the next bit
2. The serial data loading is triggered by the CLK pulse which is asserted by a decoded memory WRITE location 2000, R/W, and 02. A WRITE to address 4000 transfers data from the input shift register to the DAC register.

Figure 5. MC6800 Interface (Simplified Diagram)

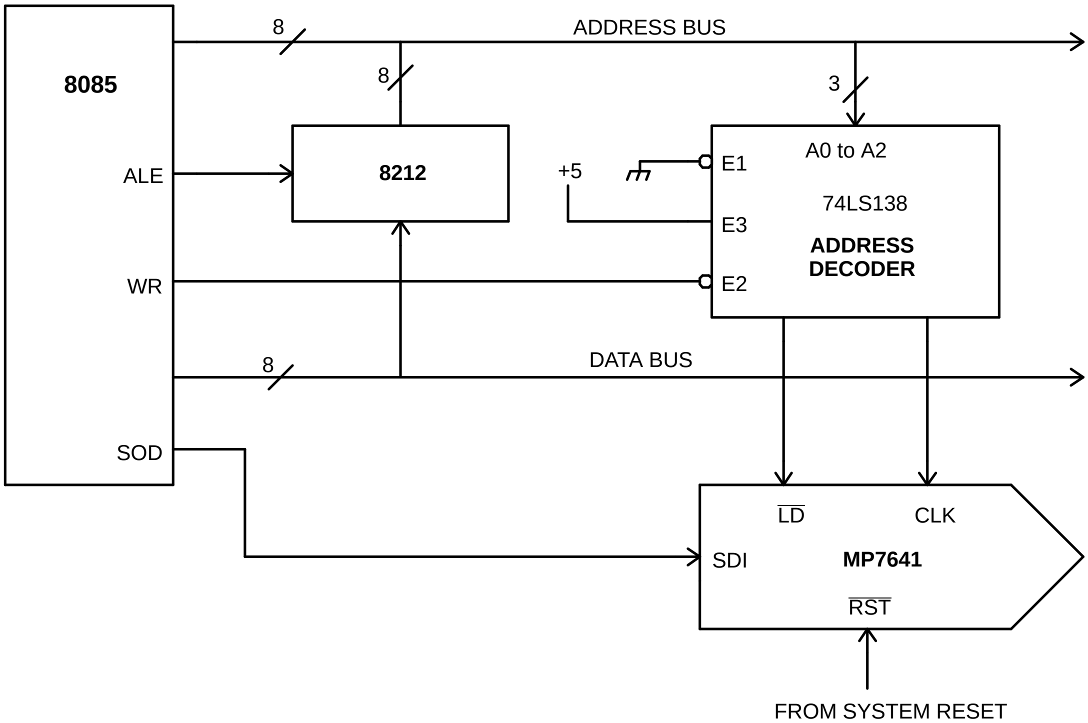


Figure 6. 8085 Interface (Simplified Diagram)

NOTES:
1. Clock generated by $\overline{WR}$ and decoding address 8000
2. Data is clocked into the DAC shift register by executing memory write instructions. the clock input is generated by decoding address 8000 and $\overline{WR}$. Data is then loaded into the DAC register with a memory write instruction to address 4000.
3. Serial data must be present in the right justified format in registers H & L of the microprocessor.

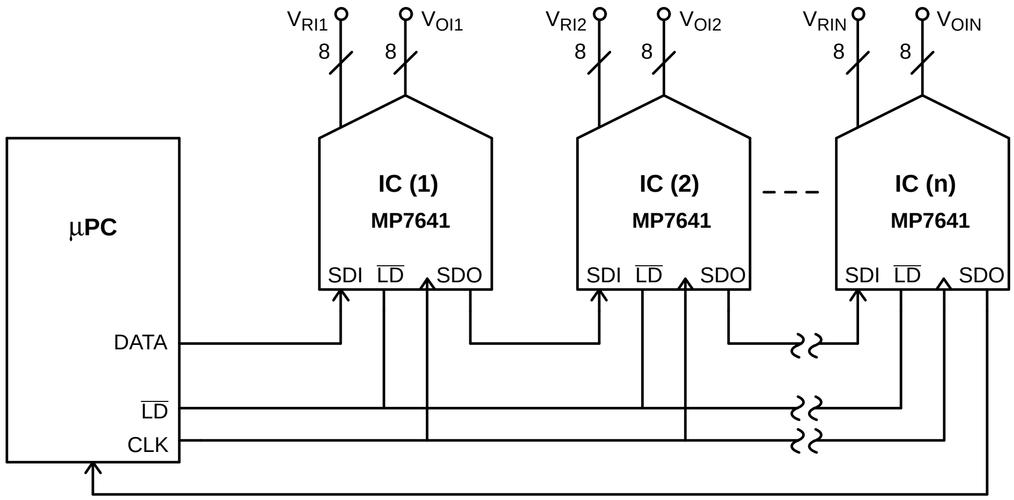


Figure 7. Simplified Diagram Configuration A

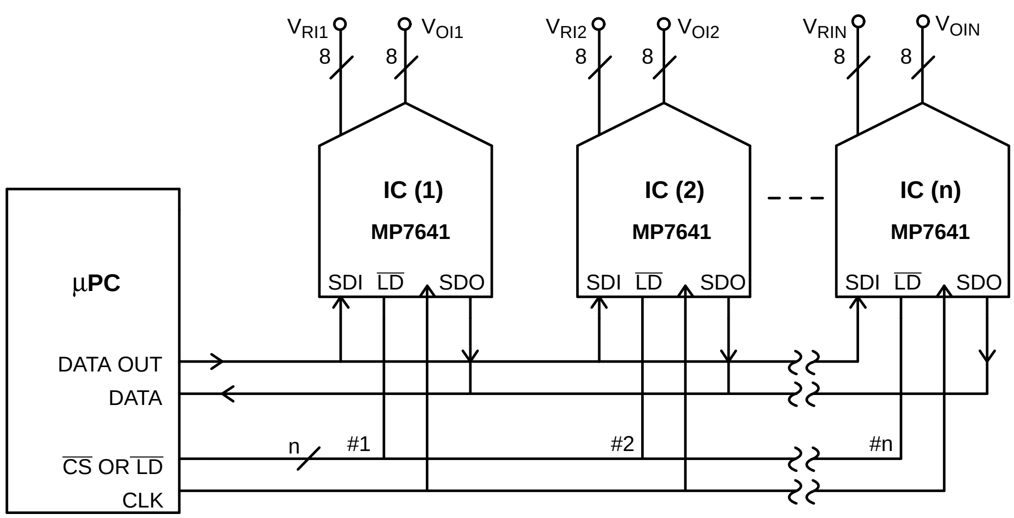


Figure 8. Simplified Diagram Configuration B

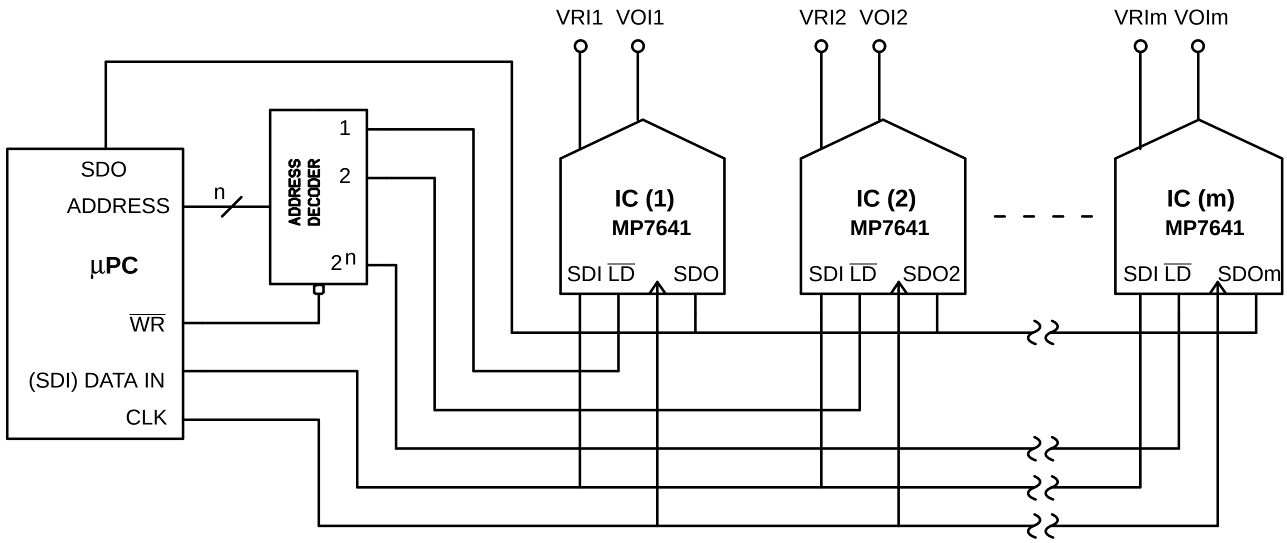
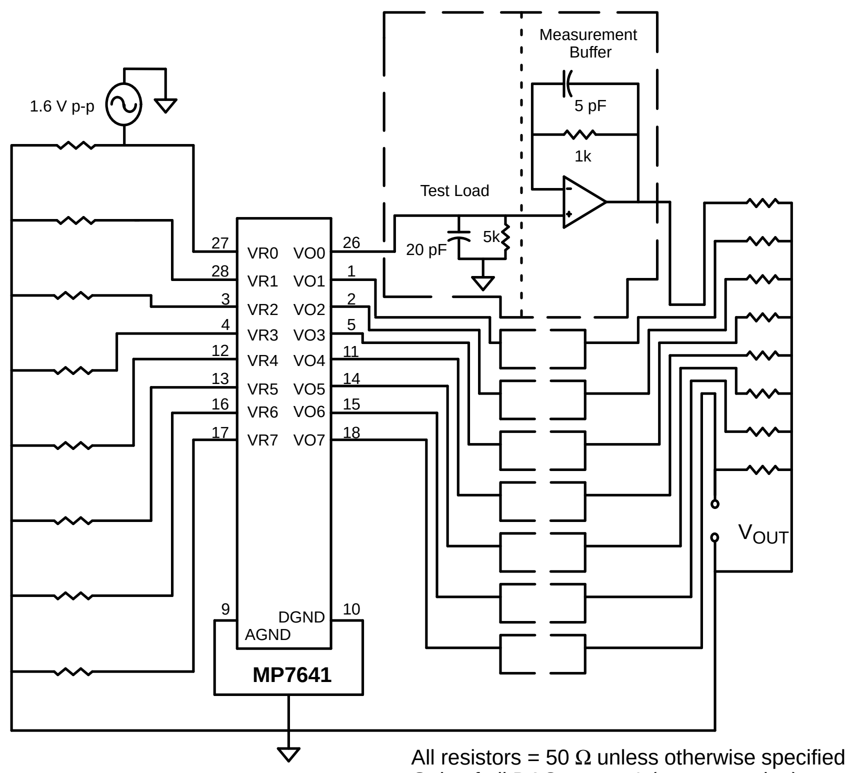


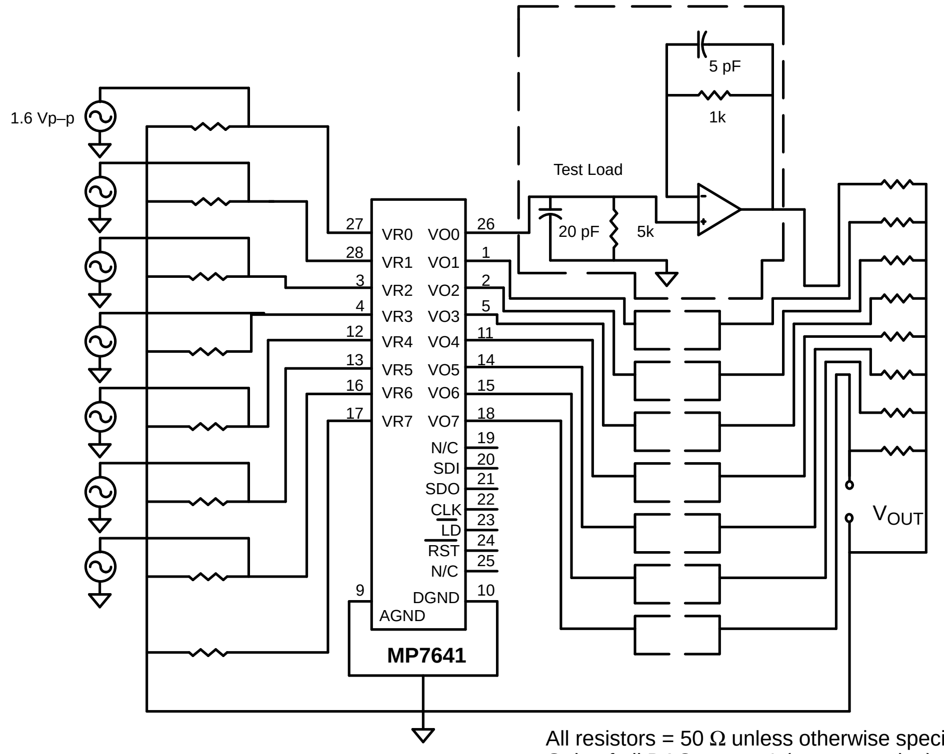
Figure 9. Simplified Diagram Configuration C

MP7641 EVALUATION BOARD



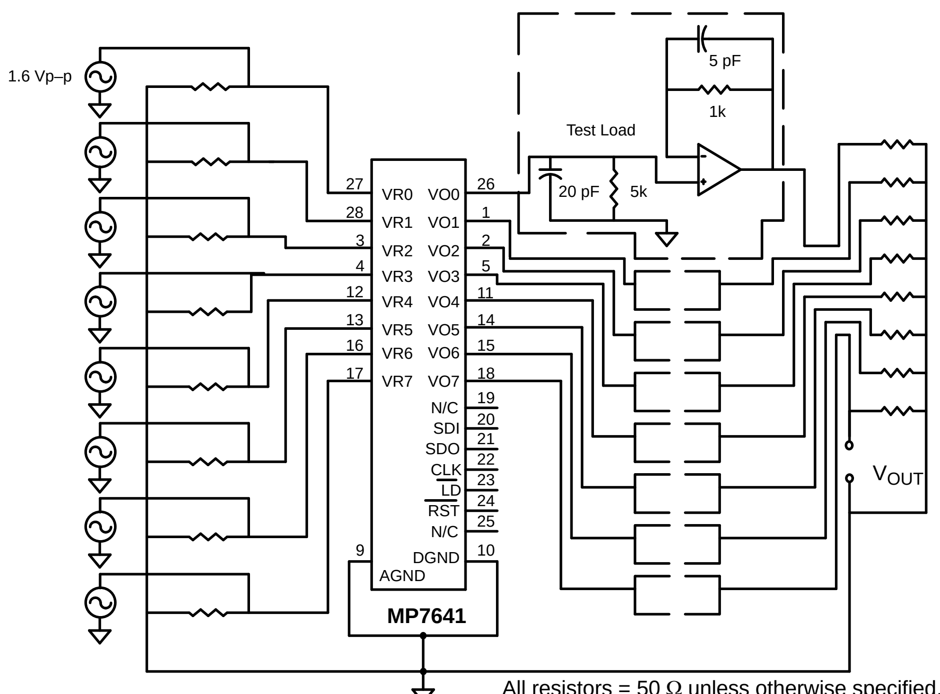
All resistors = 50 Ω unless otherwise specified
Gain of all DACs set to 1 (no attenuation)
NOTE: See Graphs 1 through 8

Figure 10. Single Channel Crosstalk



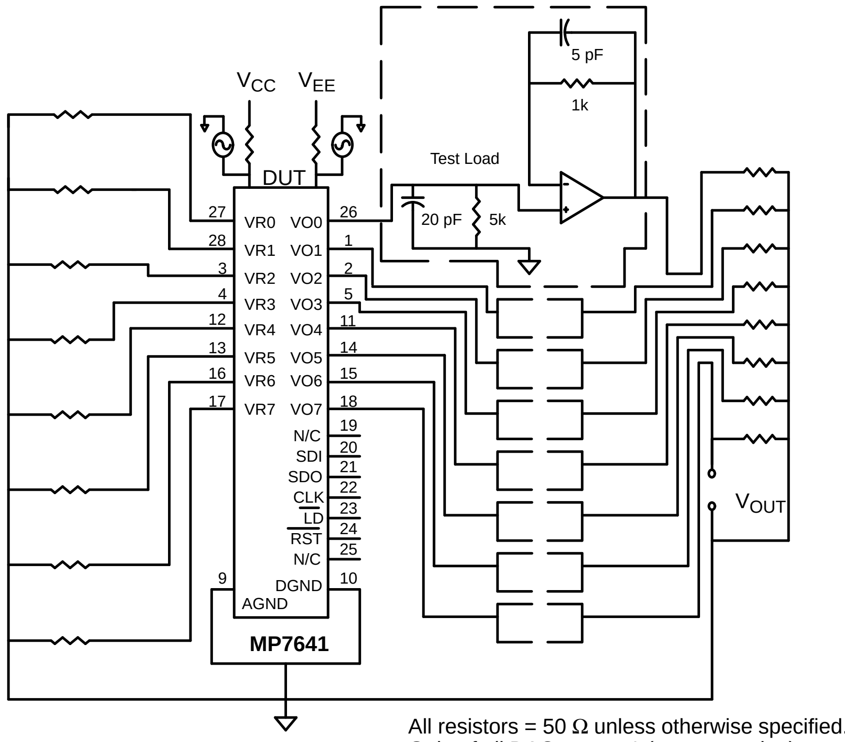
All resistors = 50 Ω unless otherwise specified.
Gain of all DACs set to 1 (no attenuation).
NOTE: See *Graph 20B*.

Figure 11. All Hostile Crosstalk



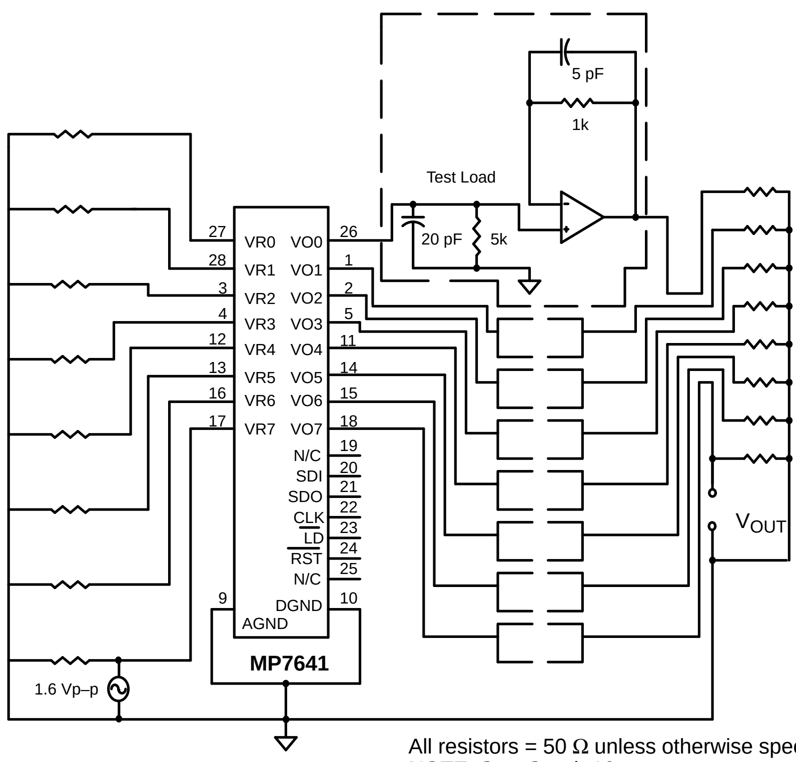
All resistors = 50 Ω unless otherwise specified.
Gain of all DACs set to 1 (no attenuation) except monitored DAC set to 0 (full attenuation).
NOTE: See *Graph 20A.*

Figure 12. All Hostile Crosstalk & Feedthrough



All resistors = 50 Ω unless otherwise specified.
Gain of all DACs set to 1 (no attenuation).
NOTE: See *Figure 12.*

Figure 13. PSRR

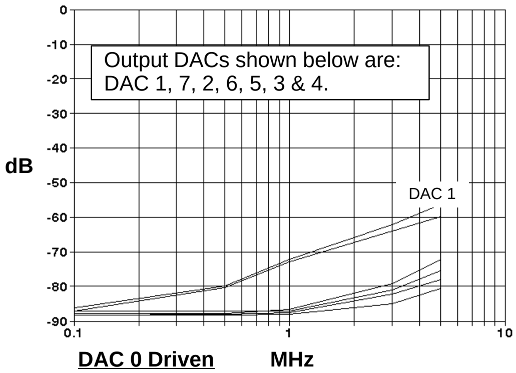


All resistors = 50 Ω unless otherwise specified.
NOTE: See *Graph 16.*

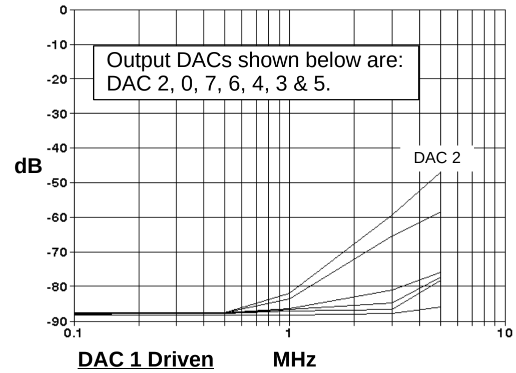
Figure 14. Frequency Response / THD Response

PERFORMANCE CHARACTERISTICS

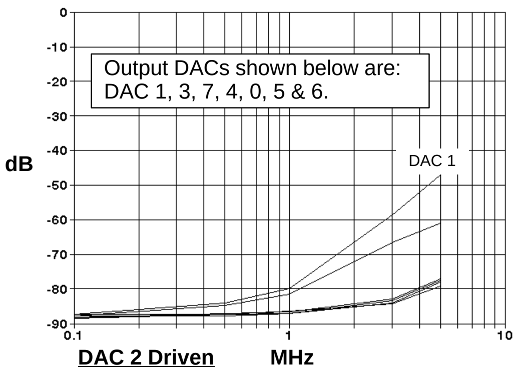
Channel-to-Channel Crosstalk (Gain vs. Frequency; All DACs set to full scale; V_{REF}=1.6 Vp-p)



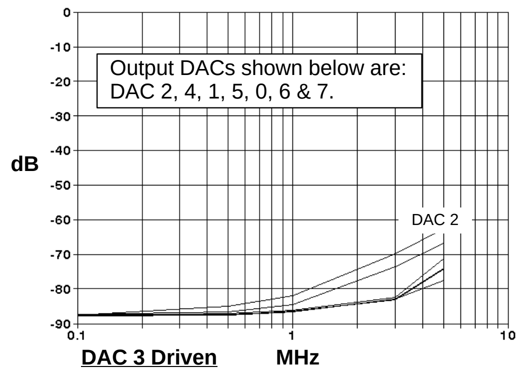
Graph 1.



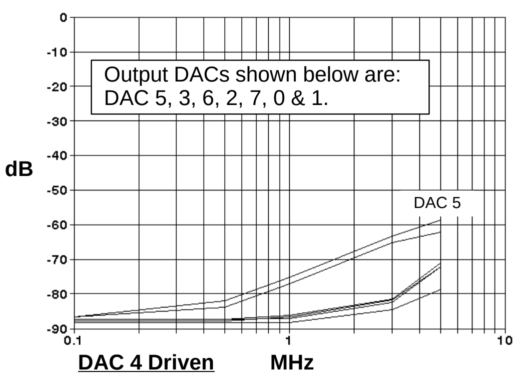
Graph 2.



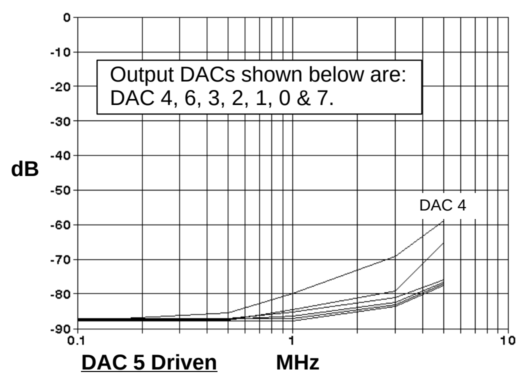
Graph 3.



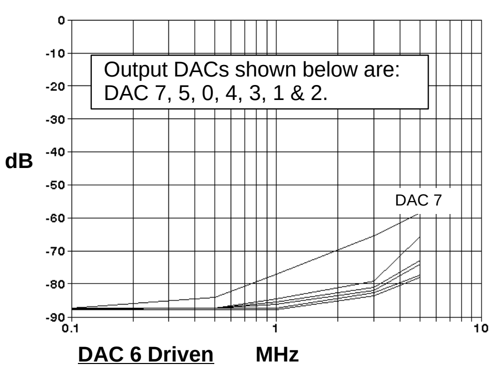
Graph 4.



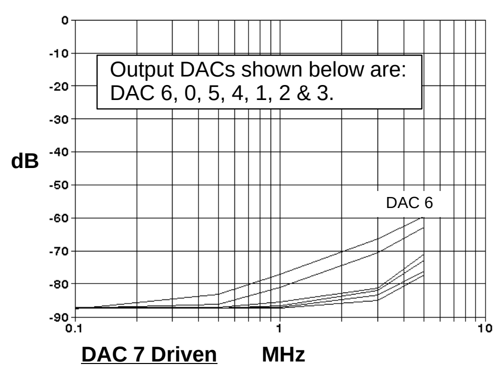
Graph 5.



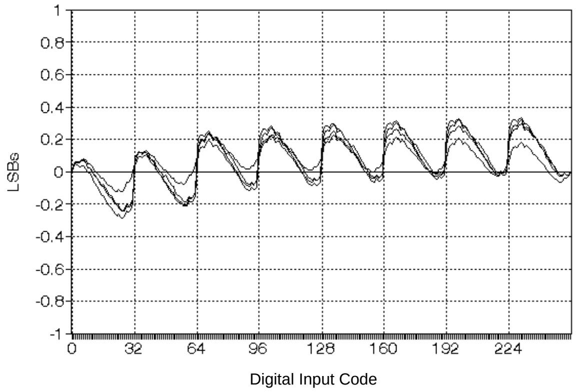
Graph 6.



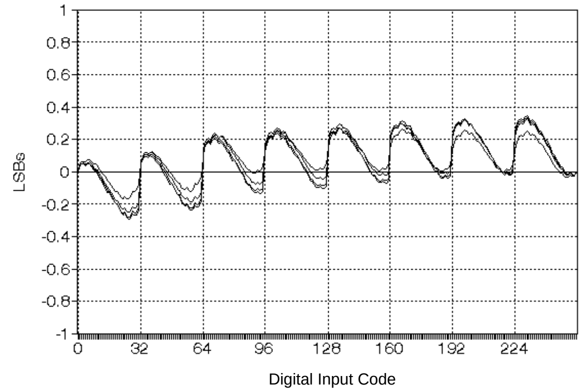
Graph 7.



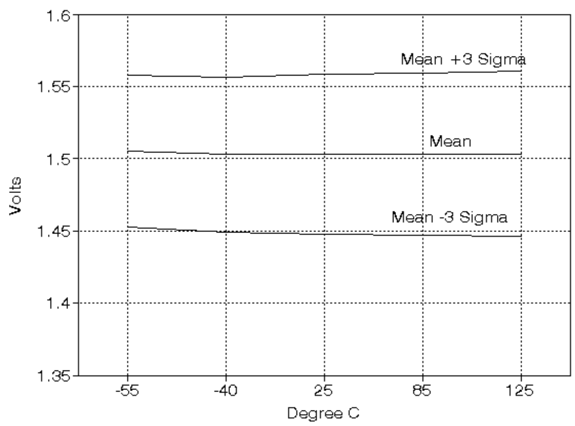
Graph 8.



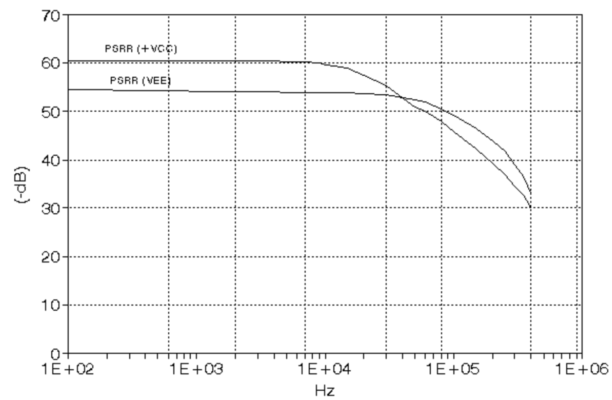
Graph 9. Linearity Error vs. Digital Input Code DACs 0 to 3



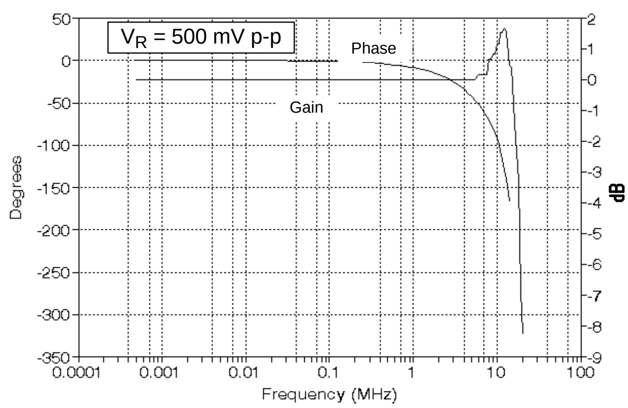
Graph 10. Linearity Error vs. Digital Input Code DACs 4 to 7



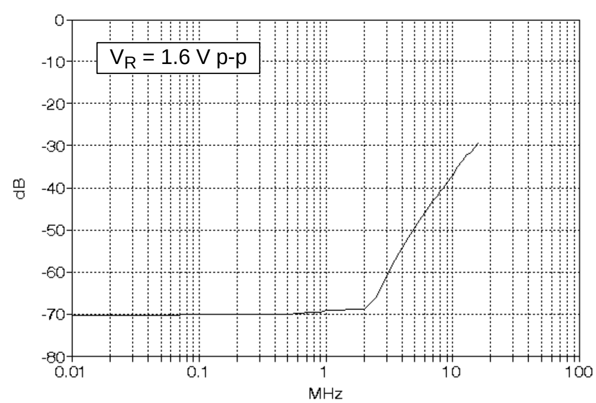
Graph 11. Reset Voltage vs. Temperature



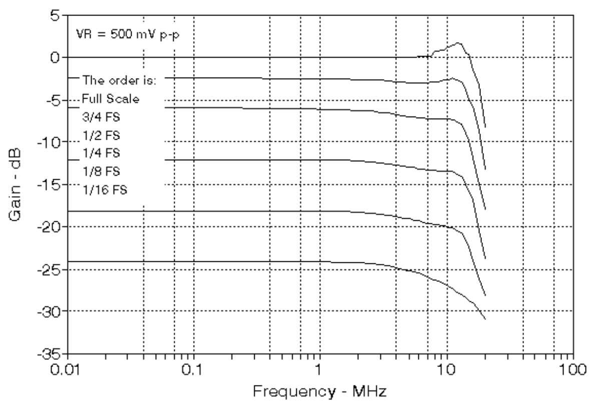
Graph 12. PSRR vs. Frequency



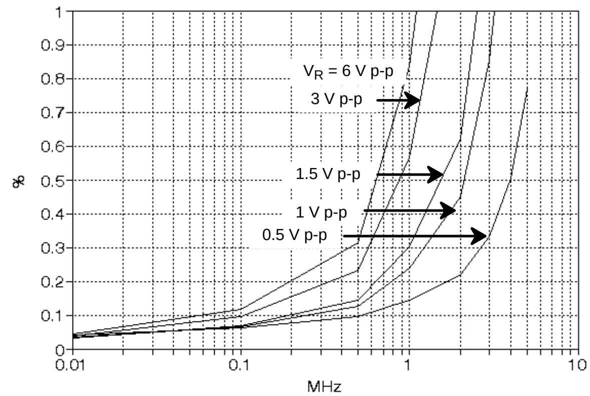
Graph 13. Gain & Phase vs. Frequency



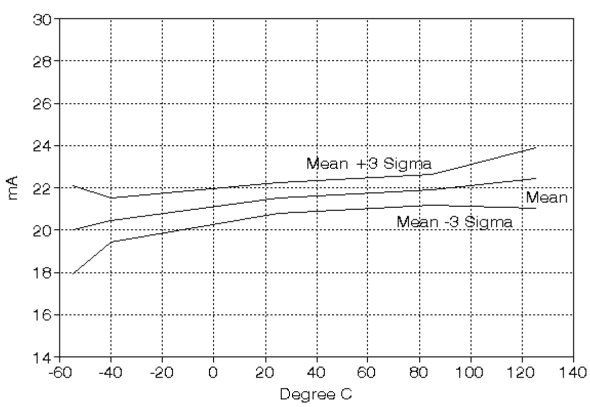
Graph 14. Feedthrough vs. Frequency



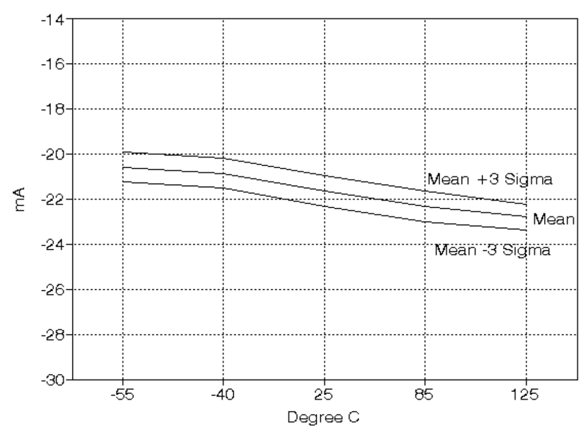
Graph 15. Gain (V_O/V_R) vs. Frequency Open Loop/Unloaded Output*



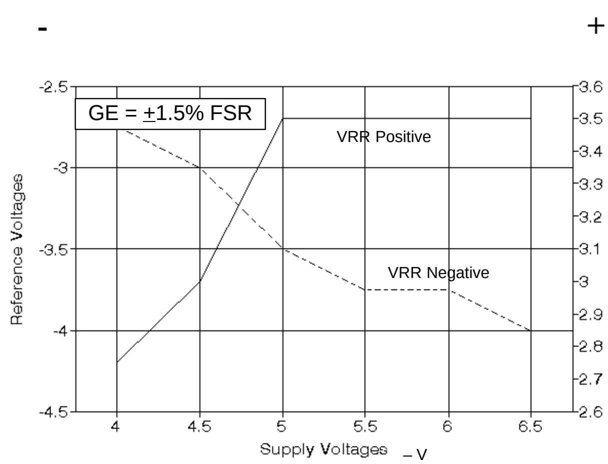
Graph 16. THD vs. Frequency



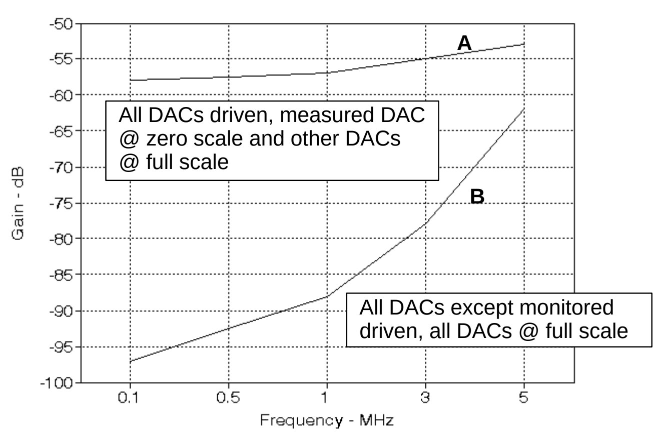
Graph 17. I_{CC} vs. Temperature



Graph 18. I_{EE} vs. Temperature



Graph 19. Reference Input Voltage Range vs. Supply Voltages



Graph 20. All Channel Crosstalk vs. Frequency

* A 2K or 5K resistor across output and V_{EE} will remove peaking (see Graph 26).

$\overline{LD}$ (5 V/DIV)

V_R = 3 V
Digital Code = 255→0→255

V_O (2 V/DIV)

2µs/DIV

Graph 21. Digital Settling

V_R (2 V/DIV)

Digital Code = All Ones

V_O (2 V/DIV)

2µs/DIV

Graph 22. Pulse Response ($t_R = t_F$ = 100 ns for V_R)

V_R (2 V/DIV)

V_O (2 V/DIV)

2µs/DIV

Graph 23. 128 kHz Sawtooth Waveform Response

$\overline{LD}$ (5 V/DIV)

V_O (10mV/DIV)

2µs/DIV

Graph 24. Clock and SDI Feedthrough

$\overline{LD}$ (5 V/DIV)

V_O (10mV/DIV)

2µs/DIV

Graph 25. Clock/SDI Feedthrough

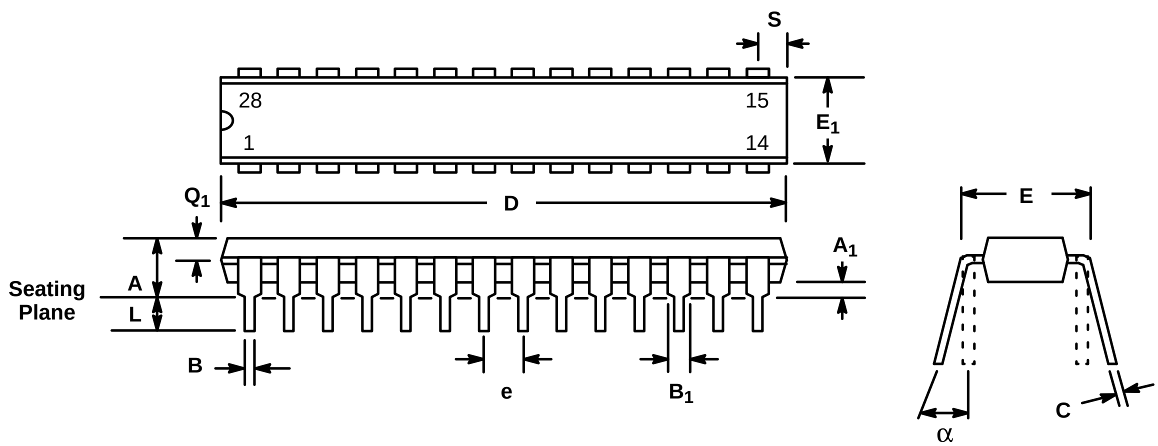
Gain (5 dB/DIV)

Group Delay (20 ns/DIV)

MHz

Graph 26. Typical Gain and Group Delay vs. Frequency (with 5K resistor across output to V_{EE})

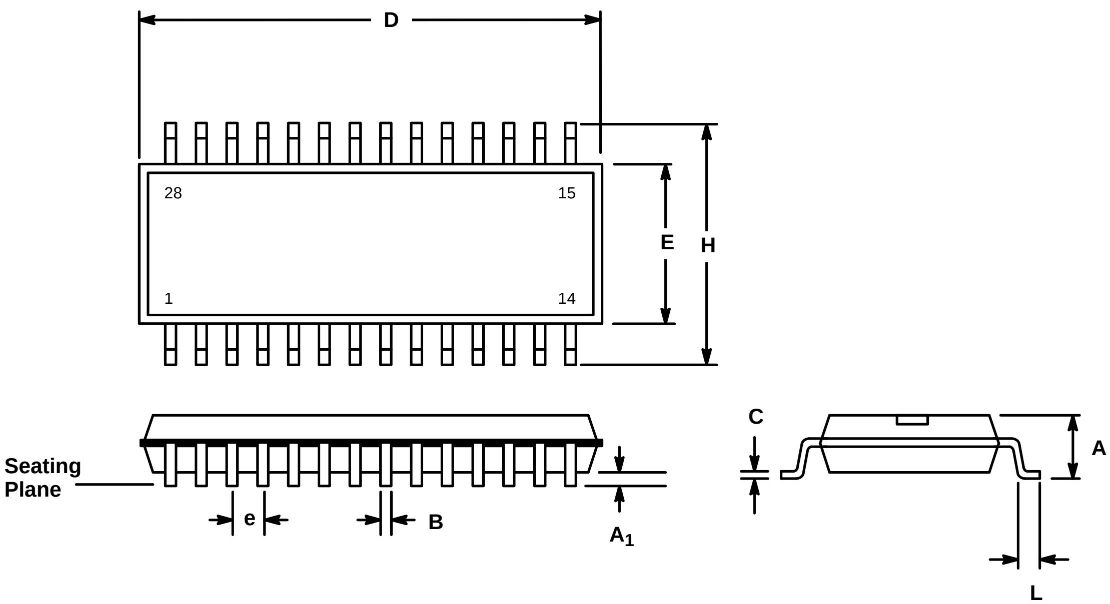
28 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
NN28



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.130	0.230	3.30	5.84
A_1	0.015	—	0.381	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.340	1.485	34.04	37.72
E	0.290	0.325	7.37	8.26
E_1	0.240	0.310	6.10	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.020	0.100	0.508	2.54

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

28 LEAD SMALL OUTLINE
(335 MIL EIAJ SOIC)
R28



SYMBOL	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.60	2.80	0.102	0.110
A_1	0.2 (typ.)		0.008 (typ.)	
B	0.3	0.5	0.012	0.020
C	0.10	0.20	0.004	0.008
D	17.6	18.0	0.693	0.709
E	8.3	8.5	0.327	0.335
e	1.27 (typ.)		0.050 (typ.)	
H	11.5	12.1	0.453	0.477
L	0.8	1.2	0.031	0.047

Notes

Notes

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