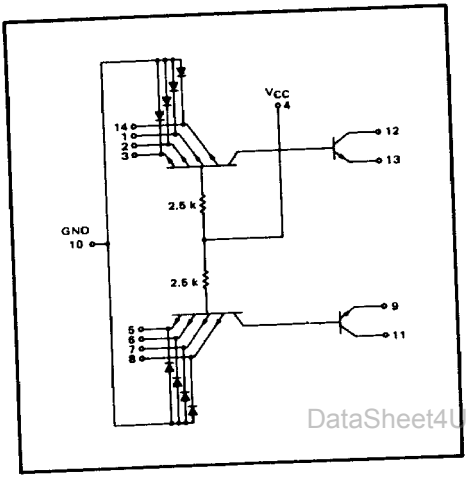
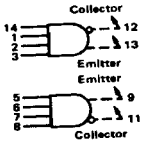
DUAL 4-INPUT EXPANDER FOR "AND-OR-INVERT" GATES

MC2106 • MC2156
MC2006 • MC2056



This device consists of two independent 4-input AND gates. The outputs of each gate are made available as ORing nodes. Using the MC2102 series and the MC2106 series with any one of the basic expandable gates, up to 10 AND gates can be ORed together.



Total Power Dissipation = 14 mW typ/Pkg.

Propagation Delay Times:

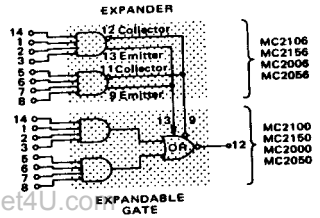
Δt_{pd} = +1.0 ns typ
When added to the expandable AND-OR-INVERT gates.

$\Delta t_{pd}/pF$ = +0.7 ns/pF typ
Caused by additional capacitance at expansion points.

TYPE NO.	INPUT LOADING FACTOR	(I_F)	TEMPERATURE RANGE
MC2106 MC2156	1	−2.0 mA	−55°C to +125°C
MC2006 MC2056	1	−2.5 mA	0°C to +75°C

Full output loading factor of the expandable gate is maintained.

APPLICATION: EXPANDABLE 2-WIDE 4-INPUT, "AND-OR-INVERT" GATE WITH A DUAL 4-INPUT EXPANDER CONNECTED.

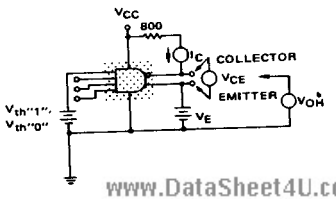


POSITIVE LOGIC

$$12 = \overline{(14 \cdot 1 \cdot 2 \cdot 3) + (5 \cdot 6 \cdot 7 \cdot 8)} + \overline{(5 \cdot 6 \cdot 7 \cdot 8) + (14 \cdot 1 \cdot 2 \cdot 3)}$$

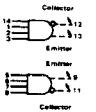
EXPANDABLE GATE — EXPANDER

V_{CE}, V_{OH} TEST CIRCUIT



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander. The other expander is tested in a similar manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.



	@ Test Temperature	TEST CONDITIONS mA I_C	I_{in}	Volts V_R	V_{E1}	V_{B2}	V_{E2}	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CR}	V_{CRH}	V_{CC}	V_{CCH}
MC2106, MC2156	−55°C	6.0	1.0	4.5	1.00	0.90	0.8	2.0	0.9	5.5	*	-	5.0	-
	+25°C	6.0	1.0	4.5	0.85	0.75	0.8	1.7	1.1	5.5	*	**	5.0	8.0
	+125°C	6.0	1.0	4.5	0.65	0.55	0.8	1.4	0.9	5.5	*	-	5.0	-
MC2006, MC2056	0°C	6.0	1.0	4.5	0.90	0.80	0.8	1.9	1.0	5.5	*	-	5.0	-
	+25°C	6.0	1.0	4.5	0.85	0.75	0.8	1.8	1.1	5.5	*	**	5.0	7.0
	+75°C	6.0	1.0	4.5	0.75	0.65	0.8	1.7	1.0	5.5	*	-	5.0	-

Characteristic	Symbol	Pin Under Test	MC2106, MC2156 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC2006, MC2056 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_C	I_{in}	V_R	V_{E1}	V_{B2}	V_{E2}	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CR}	V_{CRH}	V_{CC}	V_{CCH}	Gnd†
Input																												
Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	2,3,14	-	-	-	-	-	-	-	-	4	-	1,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1	-	-	-	-	-	-	-	-	4	-	2,3,10,14
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1	13	-	-	-	-	-	12	-	4	-	10
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	1	-	13	-	-	-	-	-	12	-	4	-	10
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	1	-	-	-	-	-	-	-	-	-	4	-	2,3,10,14
Output																												
Output Voltage	V_{OH} ①	12	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	Vdc	-	-	-	-	-	13	-	-	1	-	12	-	4	-	10
	V_{OL} ①	12	-	0.65	-	0.65	-	0.65	-	0.65	-	0.65	-	0.65	Vdc	12	-	-	13	-	-	-	1	-	-	-	4	-	10
Leakage Current	$I_{O\,LK}$	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	13	-	-	12	-	-	4	-	1,2,3,10,14
Power Requirements (Total Device)																												
Maximum Power Supply Current	②	4	-	-	-	7.0	-	-	-	-	-	7.5	-	-	mAdc	-	-	-	-	-	9,13	-	-	-	-	11,12	-	4	1,2,3,10,14
Power Supply Drain	P_{DH}	4	-	3.0	-	3.0	-	3.0	-	3.6	-	3.6	-	3.6	mAdc	-	-	-	-	-	9,13	-	-	-	-	-	4	-	10‡
	P_{DL}	4	-	4.25	-	4.25	-	4.25	-	5.25	-	5.25	-	5.25	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,10,14

* Indicated pins tied to V_{CC} thru 800 ohms ± 1.0% resistor.

** Indicated pins tied to V_{CCH} thru 800 ohms ± 1.0% resistor.

† Ground inputs to gate not under test during ALL tests, unless otherwise noted.

‡ The inputs of both gates must be ungrounded.

① V_{CE} is referenced to the emitter voltage (Pin 13). The other gate is referenced to (Pin 9).

② Pin 9 ties to Pin 13. Pin 12 ties to Pin 11.

Table 3-4 DSP56001A Identification by Signal Name (Continued)

Signal Name	132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.	Signal Name	132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.
$\overline{WT}$	45	L13	nc	103	
X/$\overline{Y}$	48	N13	nc	107	
XTAL	126	A6	nc	110	
nc	3		nc	116	
nc	4		nc	117	
nc	7		nc	122	
nc	17		nc	125	
nc	18		nc	132	
nc	21				

Power and ground pins have special considerations for noise immunity. See the section **Design Considerations**.

Table 3-5 DSP56001A Power Supply Pins

132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.	Power Supply	Circuit Supplied
63	L8	V_{CCN}	Address Bus Buffers
64			
55	L6	GNDN	
56	L9		
73			
74			