FAIRCHILD

A Schlumberger Company

F3861
Peripheral Input/Output

Microprocessor Product

Description

The Fairchild F3861 Peripheral Input/Output (PIO) device provides two 8-bit I/O ports, external interrupt, and a programmable timer. An 8-bit wide bidirectional data bus transfers I/O data bytes between the F3870 Central Processing Unit (CPU) and the PIO.

The PIO is used in systems that require the I/O capability and interrupt functions of the F3851 PSU but do not need the read-only memory (ROM) storage of the PSU. The PIO is pin-compatible with the PSU.

The F3861 PIO has five versions available, each with its own set of preassigned I/O port addresses and interrupt vectors.

The F3861 is manufactured using isoplanar N-channel, silicon-gate technology; therefore, power dissipation is very low (less than 250 mW).

- 16 Bidirectional, Individualy Controlled I/O Lines Organized as Two 8-bit Ports
- Programmable Timer--Preset, Start, Stop, and Read-Back Ability; Selectable Timer Count Rates
- Full Interrupt Level--Daisy-Chain Expandable, Independent Interrupt Address Vectors for Timer and External Interrupt
- Pulse Width Measurement Capability
- TTL and LSTTL Compatible
- +5 V and +12 V Power Supplies
- 2-MHz Operation
- Low Power Dissipation, Typically Less Than 250 mW

Connection Diagram

Signal Functions

3
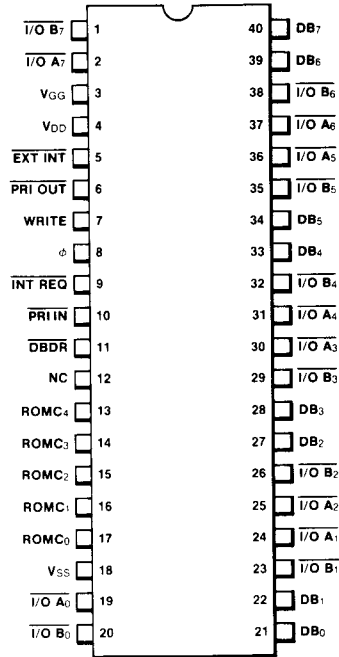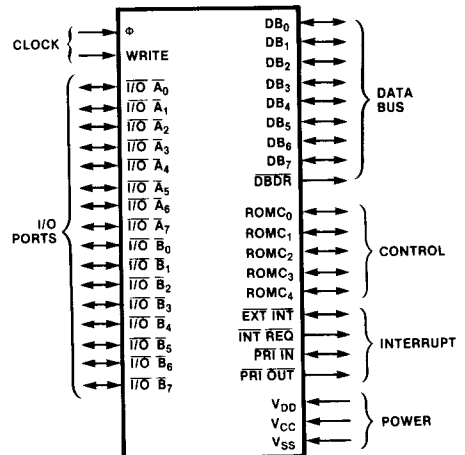
Device Organization

The peripheral input/output device includes I/O logic, timer logic, interrupt logic, data bus logic and control logic, as illustrated in figure 1.

The interrupt logic responds to an interrupt request signal originating from internal timer logic or an external device. Based on priority considerations, the interrupt request is passed on to the F3850 CPU. The programmable timer uses a polynomial shift register in conjunction with interrupt logic to generate real-time intervals.

The 8-bit data bus in the PIO is the main path for transfer of information between the F3850 CPU and other devices in the F8 microprocessor system. The device contains four preassigned I/O port addresses: the two lowest are assigned to the two I/O ports (A and B) and are used to tranfer data to and from external devices. The other two I/O addresses are assigned to two internal registers of the PIO that control interrupt logic and are treated as I/O ports.

Signal Descriptions

The F3861 input and output signals are described in table 1.

System Clock Timing

All timing within the F3861 PIO is controlled by the Φ and WRITE signals, which are input from the F3850 CPU. Refer to the F3850 data sheet for a description of these clock signals. The WRITE clock refreshes and updates PIO registers, which are dynamic. The Φ clock also drives the programmable timer.

I/O Ports

The PIO has two bidirectional 8-bit I/O ports used to transmit data between itself and external devices. In binary notation, the address for port A is XXXXXX00 and for port B is XXXXXX01, where the X binary digits are the unique I/O port select code for the PIO (see table 2). For example, if the port select code is 000001, port A may be called port 4 and port B may be called port 5. (The PIO port select code is never designated as all 0s, since ports 0 and 1 are reserved for the F3850 CPU.) In addition, the interrupt control Port (ICP) is addressed as port XXXXXX10 and the binary timer is addressed as port XXXXXX11, which become ports 6 and 7, respectively, for the port select code example given above.
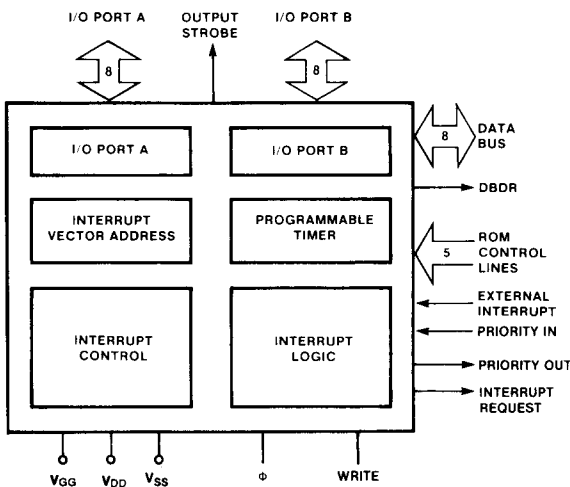
Figure 1 F3861 Block Diagram

Table 2 F3861 Port Addresses

ADDRESS	ASSIGNED TO
XXXX XX00	I/O Port A
XXXX XX01	I/O Port B
XXXX XX10	Interrupt Control Register
XXXX XX11	Programmable Timer

The port and interrupt address vector assignments are given in table 3.

Table 3 F3861 Port and Address Assignments (HEX)

Version	Port Addresses	Interrupt Address Vector	
		Timer	External
F3861A	4-7	0600	068C
F3861B	8-B	0340	03C0
F3861C	20-23	0320	03A0
F3861D	24-27	0360	03E0
F3861E	4-7	0020	00A0

Table 1 F3861 Signal Descriptions

Mnemonic	Pin No.	Name	Description
Clock			
Φ	8	Clock	The two clock input signals originate at the F3850 CPU.
WRITE	7		
I/O Ports			
I/O A_0 –	19, 24,	I/O Ports A	Bidirectional ports through which the PIO communicates with
I/O A_7	25, 30		logic external to the microprocessor system.
	31, 36		
	37, 2		
I/O B_0 –	20, 23,	I/O Ports B	
I/O B_7	226, 29,		
	31, 35,		
	38, 1		
Control			
$ROMC_0$	17, 16,	Read Only	Input signals that originate at the F3850 CPU and control
$ROMC_4$	15, 14,	Memory	internal functions of the PIO.
	13	Control	
Data Bus			
DB_0 –	21, 22,	Data Bus	Bidirectional three-state lines that link the PIO to all other
DB_7	27, 28,		devices within the microprocessor system.
	33, 34,		
	39, 40		
DBDR	11	Data Bus Drive	A low output, open drain signal that indicates the data bus currently contains data flowing from the PIO.
Interrupt			
EXT INT	5	External Interrupt	A high-to-low transition on this input signal is interpreted as an interrupt request from an external device.
INT REQ	9	Interrupt Request	This output signal is the INT REQ input to the F3850 CPU; it must be output low to interrupt the CPU, which occurs only if PRI IN is low and PIO interrupt control logic is requesting an interrupt.
PRI IN	10	Priority In	Unless this input signal is low, the PIO does not set the INT REQ signal low in response to an interrupt.
PRI OUT	6	Priority Out	This output signal becomes the PRI IN signal to the next device in the interrupt-priority daisy chain; it is output high unless the PRI IN signal is entering the PIO low and the PIO is not requesting an interrupt.
Power			
V_{DD}	4	Power Supply	5 V ($\pm$ 5%)
V_{GG}	3	Power Supply	+ 12 V ($\pm$ 5%)
V_{SS}	18	Ground	System ground—O V; V_{DD} and V_{GG} are referenced to V_{SS}.

Port Pin Description

An output instruction (OUT or OUTS) causes the contents of the CPU accumulator (ACC) to be latched into the addressed port. An input instruction (IN or INS) transfers the contents of the port to the ACC (port 6 is an exception that is described later). The I/O pins on the PIO are logically inverted; the schematic of an I/O pin and available output drive options are shown in figure 2. Each output pin has an output latch that holds the data last output to that pin. The I/O ports of the PIO are configured in the standard pull-up option.

Figure 2 I/O Pin Diagram with Output Buffer Options
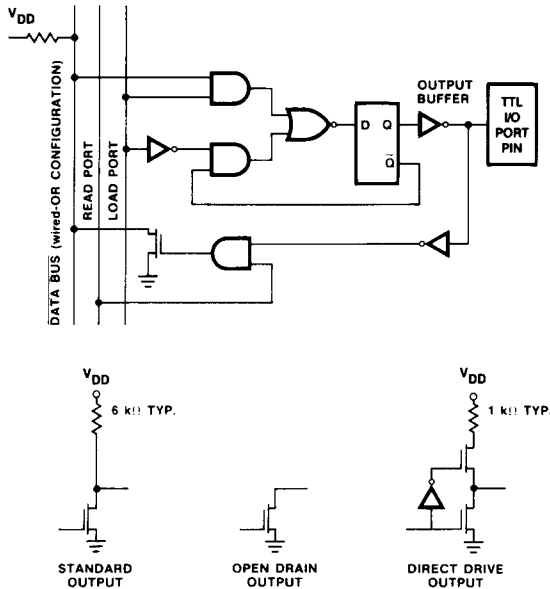
Each I/O port pin is a wire-AND structure between an internal output data latch and the external signal. The latch is loaded from the data bus. The output latches are not initialized by the system reset sequence.

When outputting data through an I/O port, the pin can be connected directly to a TTL gate input; data is input to the pin from a TTL device output. Since the I/O pin and the TTL device output are wire-ANDed, it is possible for the state of one to affect the transfer of data out from the I/O pin or in from the TTL device output. In most cases, therefore, I/O port bits should be set for a high level (logic 0) before data input to prevent incoming logic zeros from being masked by logic ones present at the port from previous outputs. However, the ability to mask bits of a port to logic 1 is useful during some input functions.

Programmable Timer

The 8-bit shift register, addressable as an I/O port, functions as a polynomial timer. This timer is loaded with a value of delay; it counts down this value of delay and, after the programmed interval, generates an interrupt through the interrupt logic of the PIO.

The OUT or OUTS instruction is used to load the interval value into the programmable timer; the port number is H'07', H'0B', H'23', or H'27', as appropriate. The timer times out after a time interval given by the product

$$\text{(period of } \Phi \text{ clock)} \times \text{(timer counts)} \times 31$$

The timer continues to run after a time-out; subsequent time-outs occur at intervals of 7905 Φ clock periods. The timer does not run if it is loaded with the value H'FF'.

Interrupt Logic

The interrupt logic block is programmed by output instructions to the interrupt control port (port H'06', H'0A', H'22', or H'26', as appropriate). Only the least significant two bits are used; their interpretation is as follows.

Contents of ICP	Interpretation
B'XXXXXX00'	Disable all interrupts
B'XXXXXX01'	Enable external interrupt, disable timer interrupt
B'XXXXXX10'	Disable all interrupts
B'XXXXXX11'	Disable external interrupt, enable timer interrupt

Note: The X designation represents "don't care" binary digits.

Figure 3 PIO Data Bus Timing
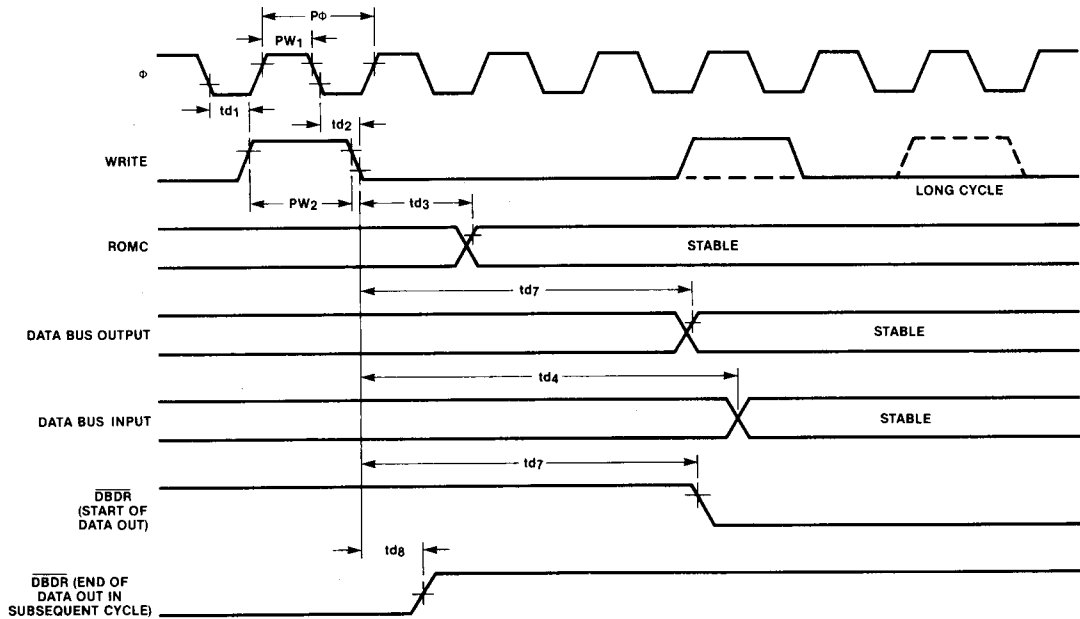
3

Instruction Execution

The PIO responds to signals that are output by the F3850 CPU in the course of implementing instruction cycles. Figure 3 illustrates timing during PIO data output to the data bus. This timing applies whenever a PIO is the data source. The PIO places data on the data bus, even in the worst case, in time for the setup required by any F3850 CPU destination. The PIO receives a byte input from the data bus when commanded by an output instruction to load one of its two I/O ports or internal registers. Data bus timing requirements for input to the PIO are also shown in figure 3; signal characteristics are given in the "Timing Characteristics" section. The data bus drive (DBDR) signal is low while data output by the PIO is stable on the data bus. Thus, a DBDR low signal indicates that the data bus currently contains data flowing from a PIO. For systems with more than one program storage unit (PSU) or PIO, the DBDR output signals may be wire-ORed and the result used as a bus data flow direction indicator. The DBDR signal may remain low until timing interval td of the next instruction cycle following the one in which DBDR was set low.

The PIO device executes the OUT instruction in the same manner as the OUTS instruction; the same is true for the IN and INS instructions. The difference between the long- and short-form instructions is only in the source of the I/O address.

The F8 input/output instructions place the I/O port address on the data bus during one instruction cycle and then use the data bus in the following instruction cycle to do the actual I/O data movement. The read only memory control (ROMC) lines coming from the F3850 CPU signal the PIO that an I/O data movement is occurring during the current instruction cycle. Therefore, the PIO needs to recognize whether the contents of the data bus during the instruction cycle just prior matched any of its four assigned I/O addresses, wherever the ROMC lines indicate an I/O transfer. The address select logic constantly monitors the data bus for a match to any of the four addresses and holds the information of a match through the following cycle.

Input instructions that select a port cause the contents of the selected port to be placed on the data bus during the input cycle. Only the two I/O ports (lowest two addresses)

respond to input instructions. Output instructions that select a port transfer the contents of the data bus to that port. Outputs of the latches change at the end of the I/O transfer cycle.

Interrupt Handling

A typical F8 system interrupt interconnection is shown in figure 4. Each PSU and PIO has a PRI IN and PRI OUT line so that they can be daisy-chained together in any order to form a priority level of interrupts. When a PIO receives an interrupt (either timer or external), it pulls its PRI OUT output signal high, signaling all lower priority peipherals that it has a higher priority interrupt request pending on the CPU. Also, when the PIO device PRI IN input signal is pulled high by a higher priority peripheral, signaling the PIO that there is a still higher priority interrupt request, it passes that signal along by pulling its PRI OUT signal high. When the CPU processes an interrupt request, it commands the interrupting device to place its interrupt vector address on the data bus. Only the device with a PRI IN signal low and an interrupt request pending responds. Should there be another lower priority device with a pending request, it does not respond at that time because its PRI IN input signal is high.

If there are both a timer interrupt request and an external interrupt request when the CPU starts to process the requests, the timer interrupt is handled first.

Within each local interrupt control circuit is a 16-bit interrupt address vector. This vector is the address to which the program counter is set after an interrupt is acknowledged and is therefore the address of the first executable instruction of the interrupt routine.

The interrupt address is unique to the version of the PIO device selected by the user. Fifteen bits are fixed: bits 0 through 6 and bits 8 through 15. Bit 7 (2^7) is dependent on the type of interrupt. This bit is a 0 for internal timer-generated interrupts and a 1 for external interrupts. When the interrupt logic sends an interrupt request signal and the CPU is enabled to service it, the normal state sequence of the CPU is interrupted at the end of an instruction. The CPU signals the interrupt circuits through the five ROMC lines. The requesting local interrupt circuit sends a 16-bit interrupt address vector (from the interrupt address generator) onto the data bus in two consecutive bytes. The address is made available to the program counter through the address demultiplexer circuits. It is simultaneously made available to all other devices connected to the data bus and is the address of the next instruction to be executed. The program counter of each memory device is set with this new address while the stack register is loaded with the previous contents of the program counter. The information in the program counter is lost. Thus, the next instruction to be executed is determined by the value of the interrupt address vector.

The interrupt control bit (ICB) of the CPU (loaded in the W register) allows interrupts to be recognized. Clearing the ICB prevents acknowledgement of interrupts. The ICB is cleared during power-on, during external reset, and after an interrupt is acknowledged. The interrupt status of the PSU, PIO, or memory interface (MI) device is not affected by execution of the disable interrupt (DI) instruction from the CPU. At the conclusion of most instructions, the fetch logic checks the state of the interrupt request line. If an interrupt, occurs the next instruction fetch cycle is suspended and the system is forced into an interrupt sequence.

Figure 4 F8 System Interrupt Interconnection
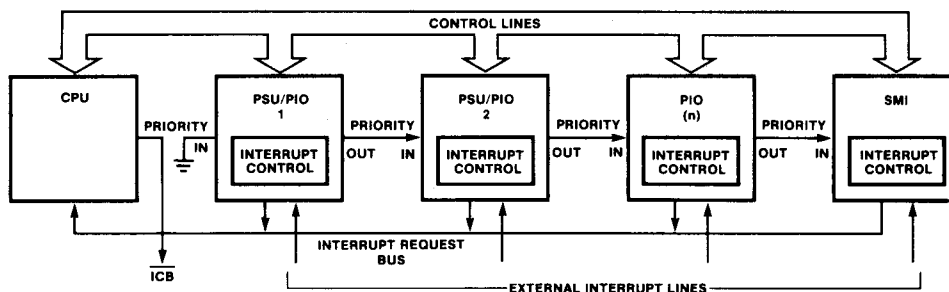
Interrupt Sequence

Figure 5 details the interrupt sequence that occurs, whether the interrupt request is from an external source through the $\overline{EXT}$ $\overline{INT}$ pin or from the PIO device internal timer. Events are labeled A through G.

Event A
An interrupt request must satisfy a set-up time requirement. If not satisfied, the $\overline{INT}$ $\overline{REQ}$ signal delays going low until the next negative edge of the WRITE clock.

Event B
Event B represents the instruction being executed when the interrupt occurs. The last cycle of B is normally the instruction fetch for the next cycle. However, if B is not a privileged instruction and the CPU interrupt control bit is set, the last cycle becomes a freeze cycle raher than a fetch. At the end of the freeze cycle the interrupt request latches are inhibited from altering the interrupt daisy chain so that sufficient time is allowed for the daisy chain to settle.

If B is a privileged instruction, the instruction fetch is not replaced by a freeze cycle; instead, the fetch is performed and the next instruction is executed. Although unlikely to be encountered, a series of privileged instructions would be executed sequentially. One more instruction (a protected instruction) is executed after the last privileged instruction. The last cycle of the protected instruction then performs the freeze.

In figure 5, the dashed lines on the $\overline{EXT}$ $\overline{INT}$ (EI) timing illustrate the last opportunity for the $\overline{EXT}$ $\overline{INT}$ signal to cause the last cycle of a nonprotected instruction to become a freeze cycle. The freeze cycle is a short cycle (four Φ clock periods) in all cases except where B is the decrement scratchpad instruction, in which case the freeze cycle is a long cycle (six Φ clock periods).

The $\overline{INT}$ $\overline{REQ}$ signal goes low on the next negative edge of the WRITE signal if both the $\overline{PRI}$ $\overline{IN}$ signal is low and the appropriate interrupt enable bit of the ICP is set.

Event C
This is a no-operation (NO-OP) long cycle, allowing time for the $\overline{PRI}$ $\overline{IN}$/$\overline{PRI}$ $\overline{OUT}$ chain to settle. At a 2-Mhz Φ clock rate, a total of seven PIO, PSU, or MI devices can be daisy-chained without the need for look-ahead logic.

Event D
In PSU circuits, the program counter (PO) is pushed to the stack register (P) to save the return address. The interrupting PIO places the lower eight bits of the interrupt vector address onto the data bus. This is always a long cycle.

Event E
In this long cycle, the PIO places the upper eight bits of the interrupt vector address onto the data bus.

3

Figure 5   Interrupt Sequence
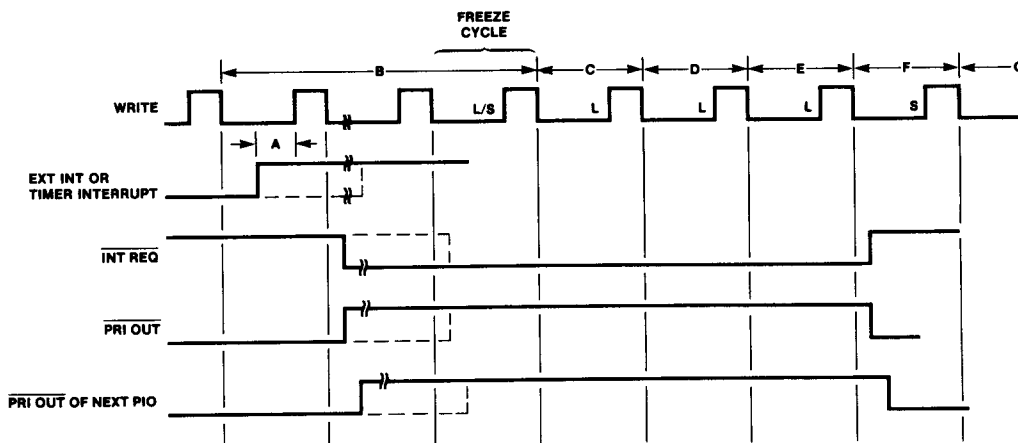
Event F
In this short cycle, the PIO interrupting interrupt request latch is cleared. Also, the CPU interrupt control bit is cleared, thus disabling interrupts until an EI instruction is performed. Additionally, during Event F, the PRI IN/PRI OUT daisy-chain freeze is removed, since the interrupt vector address has been passed to the CPU. Another action is the fetch of the instruction from the interrupt address.

Event G
This event starts executing the first instruction of the interrupt service routine.

Summary of Interrupt Sequence
For the PIO, the interrupt response time is defined as the time elapsed between the occurrence of the EXT INT signal going active (or the timer transition to H'N') and the beginning of execution of the first instruction of the interrupt service routine. The interrupt response time is a variable dependent on what the microprocessor is doing when the interrupt request occurs.

As shown in figure 5, the minimum interrupt response time is three long cycles plus two short cycles plus one write clock pulse width plus a set-up time of an EXT INT signal prior to the leading edge of the write pulse, a total of 27 φ clock periods plus the set-up time. At 2 MHz, this is 14.25 μs. Although the maximum could theoretically be infinite, a practical maximum is 35 μs (based on the interrupt request occurring near the beginning of a PI and LR K, P sequence).

ROMC States

Table 4 shows the function performed by the PIO device for each ROMC command. Each function is performed entirely within one machine cycle (one cycle of the WRITE clock). All other ROMC states are decoded as NO-OP.

Table 4 PIO Functions Versus ROMC States

ROMC State Binary	Hex	PIO Functions
01111	0F	If this circuit is interrupting and is highest in the priority chain, move lower half of interrupt vector into the data bus.
10000	10	Place interrupt circuitry in an inhibit state that prevents altering the interrupt priority chain.
10011	13	If the contents of the data bus in the prior cycle was an address of I/O ports on this device, move the current contents of the data bus into the appropriate port (I/O A, I/O B, timer or control).
11011	1B	If the contents of the data bus in the prior cycle was an address of I/O ports on this device, move the contents of the appropriate I/O port onto the data bus (I/O A or I/O B).

Timing Characteristics

Timing signals are illustrated in figures 3, 6, and 7; the signal timing characteristics are presented in table 5.
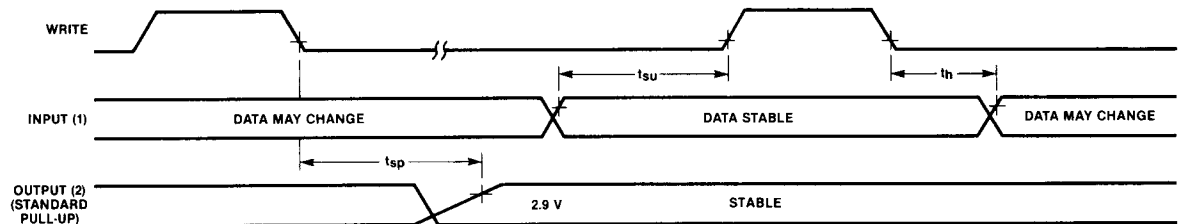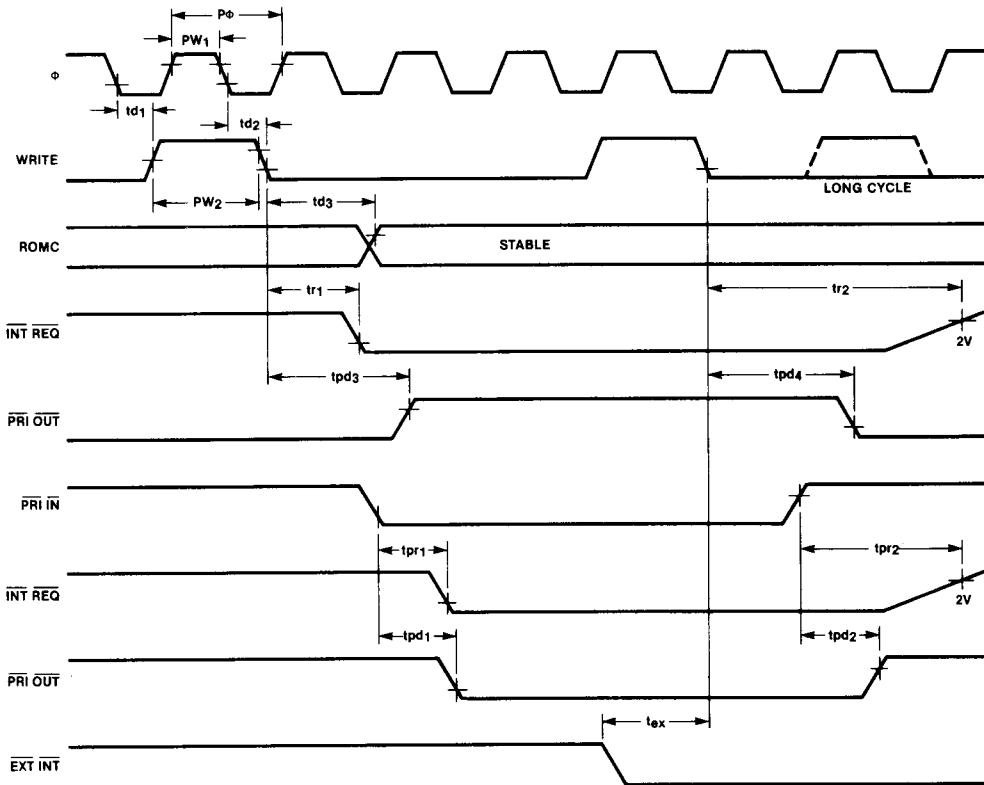
Figure 6 F3861 Input/Output Timing

Figure 7 F3861 Interrupt Logic Timing

Note: Timing measurements are made at valid logic level to valid logic level of the signals references, unless otherwise noted.

Table 5 F3861 Timing Characteristics

The ac characteristics are $V_{SS} = 0V$, $V_{CC} = +5V(\pm 5\%)$,
$T_A = 0$ C to $+70°C$.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
PΦ	Φ Period	0.5		10	5µs	
PW_1	Φ Pulse Width	180		PΦ − 180	ns	t_r, t_f = ns typ.
td_1	Φ to WRITE + Delay	60		250	ns	C_L = 100 pF
td_2	Φ to WRITE − Delay	60		225	ns	C_L = 100 pF
td_4	WRITE to DB Input Delay			2PΦ + 1.0	µs	
PW_2	WRITE Pulse Width	PΦ − 100		PΦ	ns	t_r, t_f = 50 ns typ.
PW_S	WRITE Period; Short		4PΦ			
PW_L	WRITE Period; Long		6PΦ			
td_3	WRITE to ROMC Delay			550	ns	
	WRITE to DB Output Delay					
td_7	WRITE to $\overline{DBDR}$ - Delay	2PΦ + 100 − td_2	2PΦ + 200	2PΦ + 850 − td_2	ns	C_L = 100 pF
td_8	WRITE to $\overline{DBDR}$ + Delay		200		ns	Open Drain
tr_1	WRITE to $\overline{INT}$ $\overline{REQ}$ − Delay			430	ns	C_L = 100 pF(1)
tr_2	WRITE to $\overline{INT}$ $\overline{REQ}$ + Delay			430	ns	C_L = 100 pF (3)
tpr_1	PRI IN to $\overline{INT}$ $\overline{REQ}$ − Delay			240	ns	C_L = 100 pF (2)
tpr_2	PRI IN to $\overline{INT}$ $\overline{REQ}$ + Delay			240	ns	C_L = 100 pF
tpd_1	PRI IN to $\overline{PRI}$ $\overline{OUT}$ − Delay					
tpd_2	PRI IN to $\overline{PRI}$ $\overline{OUT}$ + Delay			365	ns	C_L = 50 pF
tpd_3	WRITE to $\overline{PRI}$ $\overline{OUT}$ + Delay			700	ns	C_L = 50 pF
tpd_4	WRITE to $\overline{PRI}$ $\overline{OUT}$ − Delay			640	ns	C_L = 50 pF
*t_{sp}	WRITE to Output Stable			2.5	µs	C_L = 50 pF Standard Pull-up
*t_{su}	I/O Setup Time	1.3			µs	
*t_h	I/O Hold Time	0			ns	
*t_{ex}	$\overline{EXT}$ $\overline{INT}$ Setup Time	400			ns	

Notes:
1. Assume Priority In was enabled ($\overline{PRI}$ $\overline{IN}$ = 0) in the previous F8 cycle before the interrupt is detected in the PIO.
2. The PSU has an interrupt pending before priority in is enabled.
3. Assume the pin is tied to the $\overline{INT}$ $\overline{REQ}$ input of the F3850 CPU.
4. The starred ★ parameters in the table represent those most frequently of importance when interfacing to an F8 system. Other parameters are typically those that are relevant between F8 chips and are not normally of concern to the user.
5. Input and output capacitance is 3 to 5 pF typical on all pins except V_{DD}, V_{GG}, and V_{SS}.

DC Characteristics

The dc characteristics of the F3861 PIO are supplied in table 6.

Table 6 F3861 PIO DC Characteristics

Symbol	Parameter	Signal	Min	Max	Units	Test Conditions
V_{IH}	Input High Voltage	Data Bus (DBO-DB7)	3.5	V_{DD}	V	
V_{IL}	Input Low Voltage		V_{SS}	0.8	V	
V_{OH}	Output High Voltage		3.9	V_{DD}	V	$I_{OH} = -100\ \mu A$
V_{OL}	Output Low Voltage		V_{SS}	0.4	V	$I_{OL} = 1.6$ mA
I_{IH}	Input High Current			1	μA	$V_{IN} = 6V$, 3-State mode
I_{OL}	Input Low Current			-1	μA	$V_{IN} = V_{SS}$, 3-State mode
V_{IH}	Input High Voltage	Clock Lines	4.0	V_{DD}	V	
V_{IL}	Input Low Voltage	(Φ,WRITE)	V_{SS}	0.8	V	
I_L	Leakage Current			1	μA	$V_{IN} = 6V$
V_{IH}	Input High Voltage	Priority In and Control	3.5	V_{DD}	V	
V_{IL}	Input Low Voltage	Lines (PRI IN, ROMCO-	V_{SS}	0.8	V	
I_L	Leakage Current	ROMC4)		1	μA	$V_{IN} = 6V$
V_{OH}	Output High Voltage	Priority Out (PRI OUT)	3.9	V_{DD}	V	$I_{OH} = -100\ \mu A$
V_{OL}	Output Low Voltage		V_{SS}	0.4	V	$I_{OL} = 100\ \mu A$
V_{OH}	Output High Voltage	Interrupt Request			V	Open Drain Output (1)
V_{OL}	Output Low Voltage	(INT REQ)	V_{SS}	0.4	V	$I_{OL} = 1$ mA
I_L	Leakage Current			1	μA	$V_{IN} = 6V$
V_{OH}	Output High Voltage	Data Bus Drive				External Pull-up
V_{OL}	Output Low Voltage	(DBDR)	V_{SS}	0.4	V	$I_{OL} = 2$ mA
I_L	Leakage Current			1	μA	$V_{IN} = 6V$
V_{IH}	Input High Voltage	External Interrupt	3.5		V	
V_{IL}	Input Low Voltage	(EXT INT)		1.2	V	
V_{IC}	Input Clamp Voltage			15	V	$I_{IH} = 185\ \mu A$
I_{IH}	Input High Current			10	μ	$V_{IN} = V_{DD}$
I_{IL}	Input Low Voltage			-225	μA	$V_{IN} = 2V$
I_{IL}	Input Low Current		-150	-500	μA	$V_{IN} = V_{SS}$
V_{OH}	Output High Voltage	I/O Port	3.9	V_{DD}	V	$I_{OH} = -30\ \mu A$
V_{OH}	Output High Voltage	(Standard Pull-Up)	2.9	V_{DD}	V	$I_{OH} = -100\ \mu A$
V_{OL}	Output Low Voltage		V_{SS}	0.4	V	$I_{OL} = 2$mA
V_{IH}	Input High Voltage		2.9	V_{DD}	V	Internal Pull-up to V_{DD} (3)
V_{IL}	Input Low Voltage		V_{SS}	0.8	V	
I_{IL}	Leakage Current, DC/PC			-1.6	mA	$V_{IN} = 0.4$ V
I_{IL}	Leakage Current, DC/PL/DM			-2.0	mA	$V_{IN} = 0.4$ V
I_L	Input Low Current			-1.6	mA	$V_{IN}\ V_{SS}$ (4) (7)

Notes:
1. Pull-up resistor to V_{DD} on CPU.
2. Positive current is defined as conventional current flowing into the pin referenced.
3. Hysteresis input circuit provides additional 0.3 V noise immunity while internal/external pull-up provides TTL compatibility.
4. Measured an K a high-level I/O port OUT port.
5. $V_{SS} = °V$, $V_{DD} = \pm 5V \pm 5\%$, $V_{GG} = +12V \pm 5\%$, $T_A = 0°C$ to $70°C$
6. Output device off.
7. -2.0 mA for extended temperature range.

The supply currents are given in table 7.

Table 7 Supply Currents

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{DD}	V_{DD} Current		30	70	mA	F = 2 MHz, Outputs Unloaded
I_{GG}	V_{GG} Current		10	18	mA	f = 2 MHZ, Outputs Unloaded

Absolute Maximum Ratings

These are stress ratings only, and functional operation at these ratings, or under any conditions above those indicated in this data sheet, is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect device reliability, and exposure to stresses greater than those listed may cause permanent damage to the device.

V_{GG}	+ 15 V, − 0.3 V
V_{DD}	+ 17 V, − 0.3 V
External Interrupt Input	− 600 µA, + 225 µA
All Other Inputs and Outputs	+ 7 V, − 0.3 V
Storage Temperature	− 55°C, + 150° C
Operating Temperature	0°C, + 70°C

Note
All voltages are with respect to V_{SS}.

Recommended Operating Ranges

Part Number	Supply Voltage (V_{DD})			V_{GG}			V_{SS}
	Min	Typ	Max	Min	Typ	Max	
F3861	+ 4.75 V	+ 5 V	+ 5.25 V	+ 11.4 V	+ 12 V	+ 12.6 V	0 V

Ordering Information

Part Number	Package	Temperature Range
F3861	Ceramic	C
F3861 DM	Ceramic	M
*F3861 PC	Plastic	C

C = Commericial Temperature Range 0° to + 70°C
L = Limited Temperature Range − 40°C to + 85°C
M = Military Temperature Range − 55°C to + 125°C
* Version A, B, C, D, and E are stocked items.