# Cyclone III FPGA Family



ES-01020-2.0 Errata Sheet

## Introduction

This errata sheet provides updated information on Cyclone® III devices. This document addresses known device issues and includes methods to work around the issues.

Table 1 shows the specific issues and which Cyclone III devices each issue affects.

*Table 1. Cyclone III FPGA Family Issue*

| Issue | Affected Devices | Solution |
|---|---|---|
| MSEL pins may be sensed at a different setting than was intended if connected to $V_{CCIO}$ for logic high and $V_{CCIO}$ sags below 0.75 V after power on reset and before configuration starts. | All Cyclone III devices | For a solution, refer to "MSEL Pin Connection". |
| Momentary current surge from the $V_{CCINT}$ supply after configuration. | EP3C25 ES Revision B and C<br>EP3C120 ES Revision A | Fixed in EP3C25 Revision D, EP3C120 ES Revision B and EP3C120 Revision C |
| Issue with static current in I/O banks powered at 3.3-V $V_{CCIO}$. The affected devices might draw more current than expected. | EP3C25 ES Revision B and C<br><br>EP3C120 ES Revision A and B | Fixed in EP3C25 Revision D and EP3C120 Revision C |

## MSEL Pin Connection

Altera has identified an issue with Cyclone III MSEL pins connected to $V_{CCIO}$ for logic high. If $V_{CCIO}$ sags below 0.75 V after power on reset and before configuration starts, the MSEL pins may be sensed at a different setting than was intended. The device might then require a power cycle to recover. This issue does not occur when the device is in user mode or when configuration has started.

### Solution

Connect MSEL pins to $V_{CCA}$ for a logic high. If $V_{CCA}$ sags below the device's POR trip point then the POR circuit will reset the device.

If you have already connected the MSEL pins to $V_{CCIO}$ on your board, make sure that $V_{CCIO}$ rises monotonically to its recommended operating condition voltage level and stays within the voltage min and max. A monotonic rise will prevent the issue from occurring.

## Configuration Transition Current Issue



Cyclone III EP3C25 ES Revision B and C and EP3C120 ES Revision A devices might exhibit a momentary current surge from the $V_{CCINT}$ supply after configuration. If your system's $V_{CCINT}$ supply does not provide this current, the Cyclone III device might not transition into user mode as intended. This issue will be fixed in all production devices. While the size of the current surge is dependent on your design and on Quartus II placement and routing, the following currents are maximums for each device.

*Table 2. Transition Current*

| Device | Peak Current from $V_{CCINT}$ Supply During Transition |
|---|---|
| EP3C25 | 600mA |
| EP3C120 | 3A |

If you use JTAG for initialization, the duration of the current surge is a maximum of 74 `TCK` clock periods. If you use the `CLKUSR` pin for initialization, the duration of the current surge is a maximum of 74 `CLKUSR` clock periods. Otherwise, the duration of the current surge is a maximum of 15µs. The fastest rise time within the surge is 150ns.

### Workaround

To ensure $V_{CCINT}$ voltage level stability during the transition from configuration mode to user mode, the system needs to supply the peak transition current. Table 3 lists the maximum $V_{CCINT}$ supply impedance allowed to meet the current surge while maintaining voltage level stability. Additionally, Table 3 lists typical capacitors, along with a voltage regulator, that can produce a $V_{CCINT}$ supply impedance that is at or lower than the maximum.

*Table 3. $V_{CCINT}$ Supply Impedance and Typical Capacitors (Part 1 of 2)*

| Device | Maximum $V_{CCINT}$ Supply Impedance *(1)*, *(2)* | Typical VCCINT Capacitor *(3)* |
|---|---|---|
| EP3C25 | 0.25 Ω | 100 µF low ESR tantalum and 10 µF ceramic |

| Table 3. $V_{CCINT}$ Supply Impedance and Typical Capacitors (Part 2 of 2) | | |
|---|---|---|
| **Device** | **Maximum $V_{CCINT}$ Supply Impedance** *(1)*, *(2)* | **Typical VCCINT Capacitor** *(3)* |
| EP3C120 | 0.05 Ω | 470 µF low ESR tantalum and 100 µF ceramic |

***Notes to Table 3:***
(1) Impedances as listed result in a $V_{CCINT}$ drop of no more than 150mV.
(2) Impedance is over the range of DC to 2.4MHz.
(3) Minimum capacitors at one each per Cyclone III device to meet the transition current surge. Normal user mode operation likely requires additional bulk and decoupling capacitors.

Typically a robust $V_{CCINT}$ power system designed to handle Cyclone III user mode operation meets the above impedances. For example, the $V_{CCINT}$ power systems on the Cyclone III FPGA Starter Kit board (3C25) and the Cyclone III FPGA Development Kit board (3C120) are below the maximum impedances.

## 3.3-V I/O Power Static Current Issue

Altera has identified an issue with static current in I/O banks powered at 3.3-V $V_{CCIO}$ on Cyclone III EP3C25 Revision B and C and EP3C120 Revision A and B engineering sample devices. The affected devices might draw more current than expected as stated in Table 4. You should take the additional I/O current into consideration when designing the $V_{CCIO}$ power system on your board. This issue does not affect I/O banks powered at 3.15V $V_{CCIO}$ or below.

| Table 4. Additional I/O Current Note (1) | |
|---|---|
| **Device** | **Maximum Increase of ICCIO Per I/O Bank Powered at 3.3-V VCCIO** |
| EP3C25 | 8 mA |
| EP3C120 | 15mA |

***Note to Table 4:***
(1) This current increase per 3.3-V I/O bank is in addition to the existing power estimations shown in the PowerPlay Early Power Estimator or Quartus II PowerPlay Power Analyzer tools.

This issue will be fixed in production silicon for the EP3C25 Revision D and EP3C120 Revision C and their later revisions.

## Revision History

The following is the revision history for this errata:

## Version 1.0

Initial release.

## Version 2.0

The following changes were made to the *Cyclone III FPGA Family Errata Sheet* version 2.0:

- Added "Configuration Transition Current Issue" on page 2.
- Added "3.3-V I/O Power Static Current Issue" on page 3.

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