

Precision 8-Ch/Dual 4-Ch Low Voltage Analog Multiplexers

FEATURES

- Pin-For-Pin compatibility with DG408/409
- 2.7- to 12-V Single Supply or ± 3 - to ± 6 -V Dual Supply Operation
- Lower On-Resistance: $r_{DS(on)}$ - 17 Ω Typ.
- Fast Switching: t_{ON} - 38 ns, t_{OFF} - 18 ns
- Break-Before-Make Guaranteed
- Low Leakage: $I_{S(off)}$ - 0.2 nA Max.
- Low Charge Injection: 1 pC
- TTL, CMOS, LV Logic (3 V) Compatible
- -82 dB Off-Isolation at 1 MHz
- 2000-V ESD Protection (HBM)

BENEFITS

- High Accuracy
- Single and Dual Power Rail Capacity
- Wide Operating Voltage Range
- Simple Logic Interface

APPLICATIONS

- Data Acquisition Systems
- Battery Operated Equipment
- Portable Test Equipment
- Sample and Hold Circuits
- Communication Systems
- SDSL, DSLAM
- Audio and Video Signal Routing

DESCRIPTION

The DG408L/409L are low voltage pin-for-pin compatible companion devices to the industry standard DG408/409 with improved performance.

Using BiCMOS wafer fabrication technology allows the DG408L/409L to operate on single and dual supplies. Single supply voltage ranges from 3- to 12-V while dual supply operation is recommended with ± 3 to ± 6 V.

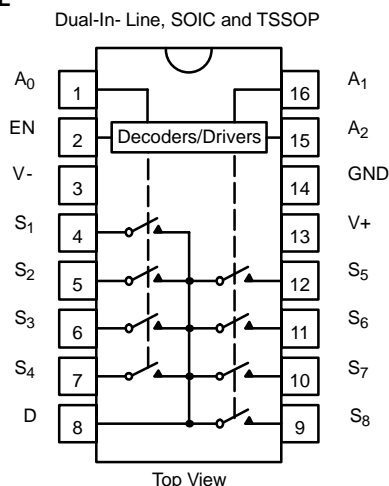
The DG408L is an 8-channel single-ended analog multiplexer

designed to connect one of eight inputs to a common output as determined by a 3-bit binary address (A_0, A_1, A_2). The DG409L is a dual 4-channel differential analog multiplexer designed to connect one of four differential inputs to a common dual output as determined by its 2-bit binary address (A_0, A_1). Break-before-make switching action to protect against momentary crosstalk between adjacent channels.

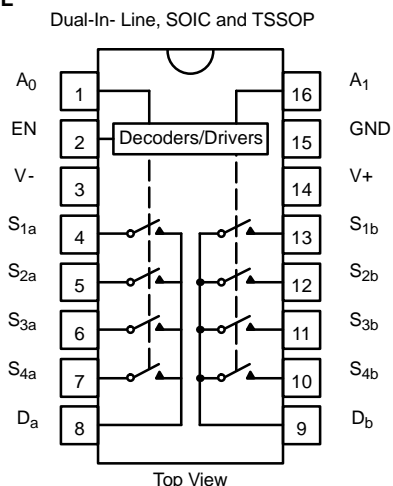
The DG408L/409L provides lower on-resistance, faster switching time, lower leakage, less power consumption and higher off-isolation than the DG408/409.

FUNCTIONAL BLOCK DIAGRAMS AND PIN CONFIGURATIONS

DG408L



DG409L





TRUTH TABLES AND ORDERING INFORMATION

TRUTH TABLE — DG408L				
A ₂	A ₁	A ₀	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE — DG409L			
A ₁	A ₀	EN	On Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" = $V_{AL} \leq 0.8 V$
 Logic "1" = $V_{AH} \geq 2.4 V$
 X = Don't Care

For low and high voltage levels for V_{AX} and V_{EN} consult "Digital Control" parameters for specific $V+$ operation.

ORDERING INFORMATION — DG408L		
Temp Range	Package	Part Number
-40 to 85°C	16-Pin SOIC	DG408LDY
	16-Pin TSSOP	DG408LDQ
-55 to 125°C	16-Pin CerDIP	DG408LAK
		DG408LAK/883
	LCC-20*	DG408LAZ/883

*Block Diagram and Pin Configuration not shown.

ORDERING INFORMATION — DG409L		
Temp Range	Package	Part Number
-40 to 85°C	16-Pin SOIC	DG409LDY
	16-Pin TSSOP	DG409LDQ
-55 to 125°C	16-Pin CerDIP	DG409LAK
		DG409LAK/883
	LCC-20*	DG409LAZ/883

*Block Diagram and Pin Configuration not shown.

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-

V+ 14 V

GND 7 V

Digital Inputs^a, V_S, V_D (V-) -0.3 V to (V+) +0.3 V

Current (Any Terminal) 30 mA

Peak Current, S or D
 (Pulsed at 1 ms, 10% Duty Cycle Max) 100 mA

Storage Temperature: (A Suffix) -65 to 150°C
 (D Suffix) -65 to 125°C

Power Dissipation (Package)^b

16-Pin Plastic TSSOP^c 650 mW

16-Pin Narrow SOIC^c 600 mW

16-Pin CerDIP^d 900 mW

LCC-20^e 750 mW

Notes

- Signals on S_X, D_X, A_X, or EN exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads soldered or welded to PC board.
- Derate 7.6 mW/°C above 75°C.
- Derate 12 mW/°C above 75°C.
- Derate 10 mW/°C above 75°C.



SPECIFICATIONS (SINGLE SUPPLY 12 V)									
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}, \pm 10\%, V_- = 0\text{ V}$ $V_{EN} = 0.8\text{ V or } 2.4\text{ V}^f$	Temp ^b	Typ ^d	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min ^c	Max ^c	Min ^c	Max ^c	
Analog Switch									
Analog Signal Range ^e	V_{ANALOG}		Full		0	12	0	12	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_D = 10.8\text{ V}, V_D = 2\text{ V or } 9\text{ V}, I_S = 10\text{ mA}$ Sequence Each Switch On	Room Full	17		29 38		29 35	Ω
$r_{DS(on)}$ Matching Between Channels ^g	Δr_{DS}	$V_D = 10.8\text{ V}, V_D = 2\text{ V or } 9\text{ V}, I_S = 10\text{ mA}$	Room	1		3		3	
On-Resistance Flatness ^l	$r_{FLAT(on)}$		Room	3		7		7	
Switch Off Leakage Current	$I_{S(off)}$	$V_{EN} = 0\text{ V}, V_D = 11\text{ V or } 1\text{ V}$ $V_S = 1\text{ V or } 11\text{ V}$	Room Full		-1 -15	1 15	-1 -10	1 10	nA
	$I_{D(off)}$		Room Full		-1 -15	1 15	-1 -10	1 10	
Channel On Leakage Current	$I_{D(on)}$	$V_S = V_D = 1\text{ V or } 11\text{ V}$	Room Full		-1 -15	1 15	-1 -10	1 10	
Digital Control									
Logic High Input Voltage	V_{INH}		Full		2.4		2.4		V
Logic Low Input Voltage	V_{INL}		Full			0.8		0.8	
Input Current	I_{IN}	$V_{AX} = V_{EN} = 2.4\text{ V or } 0.8\text{ V}$	Full		-1.5	1.5	-1	1	μA
Dynamic Characteristics									
Transition Time	t_{TRANS}	$V_{S1} = 8\text{ V}, V_{S8} = 0\text{ V}, (DG408L)$ $V_{S1b} = 8\text{ V}, V_{S4b} = 0\text{ V}, (DG409L)$ See Figure 2	Room Full	30		60 68		60 65	ns
Break-Before-Make Time	t_{OPEN}	$V_{S(all)} = V_{DA} = 5\text{ V}$, See Figure 4	Room Full	11	1		1		
Enable Turn-On Time	$t_{ON(EN)}$	$V_{AX} = 0\text{ V}, V_{S1} = 5\text{ V} (DG408L)$ $V_{AX} = 0\text{ V}, V_{S1b} = 5\text{ V} (DG409L)$ See Figure 3	Room Full	38		55 60		55 60	
Enable Turn-Off Time	$t_{OFF(EN)}$		Room Full	18		25 35		25 30	
Charge Injection ^e	Q	$C_L = 1\text{ nF}, V_{GEN} = 0\text{ V}, R_{GEN} = 0\text{ Ω}$	Room	1		5		5	pC
Off Isolation ^{e, h}	OIRR	$f = 100\text{ kHz}, R_L = 1\text{ kΩ}$	Room	-70					dB
Crosstalk ^e	X_{TALK}		Room	-82					
Source Off Capacitance ^e	$C_{S(off)}$	$f = 1\text{ MHz}, V_S = 0\text{ V}, V_{EN} = 0\text{ V}$	Room	7					pF
Drain Off Capacitance ^e	$C_{D(off)}$	$f = 1\text{ MHz}, V_D = 2.4\text{ V}, V_{EN} = 0\text{ V}$	Room	20					
Drain On Capacitance ^e	$C_{D(on)}$	$f = 1\text{ MHz}, V_D = 0\text{ V}, V_{EN} = 2.4\text{ V}$ (DG409L only)	Room	31					
Power Supplies									
Power Supply Range	V+				3	12	3	12	V
Power Supply Current	I+	$V_{EN} = V_A = 0\text{ V or } 5\text{ V}$	Room	0.2		0.7		0.7	mA

SPECIFICATIONS (DUAL SUPPLY V+ = 5 V, V- = 5 V)									
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, V- = -5 V ± 10%, V- = 0 V VEN = 0.6 V or 2.4 V ^f	Temp ^b	Typ ^d	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min ^c	Max ^c	Min ^c	Max ^c	
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}		Full		-5	5	-5	5	V
Drain-Source On-Resistance	r _{DS(on)}	V _D = ± 3.5 V, I _S = 10 mA Sequence Each Switch On	Room Full	20		40 50		40 50	Ω
Switch Off Leakage Current ^a	I _{S(off)}	V+ = 5.5 V, V- = 5.5 V VEN = 0 V, VD = ± 4.5 V, VS = ∓ 4.5 V	Room Full		-1 -15	1 15	-1 -10	1 10	nA
	I _{D(off)}		Room Full		-1 -15	1 15	-1 -10	1 10	
Channel On Leakage Current ^a	I _{D(on)}	V+ = 5.5 V, V- = 5.5 V VEN = 2.4 V, VD = ± 4.5 V, VS = ∓ 4.5 V	Room Full		-1 -15	1 15	-1 -10	1 10	
Digital Control									
Logic High Input Voltage	V _{INH}		Full		2.4		2.4		V
Logic Low Input Voltage	V _{INL}		Full			0.6		0.6	
Input Current ^a	I _{IN}	V _{AX} = V _{EN} = 2.4 V or 0.6 V	Full		-1.5	1.5	-1	1	μA
Dynamic Characteristics									
Transition Time ^e	t _{TRANS}	V _{S1} = 3.5 V, V _{S8} = -3.5 V, (DG408L) V _{S1b} = 3.5 V, V _{S4b} = -3.5 V, (DG409L) See Figure 2	Room Full	30		60 78		60 65	ns
Break-Before-Make Time ^e	t _{OPEN}	V _{S(all)} = V _{DA} = 3.5 V, See Figure 4	Room Full	8	1		1		
Enable Turn-On Time ^e	t _{ON(EN)}	V _{AX} = 0 V, V _{S1} = 3.5 V (DG408L) V _{AX} = 0 V, V _{S1b} = 3.5 V (DG409L) See Figure 3	Room Full	25		55 68		55 60	
Enable Turn-Off Time ^e	t _{OFF(EN)}		Room Full	20		40 50		40 45	
Source Off Capacitance ^e	C _{S(off)}	f = 1 MHz, V _S = 0 V, V _{EN} = 0 V	Room	6					pF
Drain Off Capacitance ^e	C _{D(off)}	f = 1 MHz, V _D = 0 V, V _{EN} = 0 V	Room	15					
Drain On Capacitance ^e	C _{D(on)}	f = 1 MHz, V _D = 0 V, V _{EN} = 2.4 V	Room	29					



SPECIFICATIONS (SINGLE SUPPLY 5 V)									
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 5\text{ V}, \pm 10\%, V_- = 0\text{ V}$ $V_{EN} = 0.6\text{ V or } 2.4\text{ V}^f$	Temp ^b	Typ ^d	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min ^c	Max ^c	Min ^c	Max ^c	
Analog Switch									
Analog Signal Range ^e	V_{ANALOG}		Full		0	5	0	5	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_+ = 4.5\text{ V}, V_D \text{ or } V_S = 1\text{ V or } 3.5\text{ V}, I_D = 5\text{ mA}$	Room Full	35		49 62		40 62	Ω
$r_{DS(on)}$ Matching Between Channels ^g	Δr_{DS}	$V_+ = 4.5\text{ V}, V_D = 1\text{ V or } 3.5\text{ V}, I_S = 5\text{ mA}$	Room	1.5		3		3	
On-Resistance Flatness ^l	$r_{FLAT(on)}$		Room			4		4	
Switch Off Leakage Current ^a	$I_{S(off)}$	$V_+ = 5.5\text{ V}, V_S = 1\text{ V or } 4\text{ V}$ $V_D = 4\text{ V or } 1\text{ V}$	Room Full		-1 -15	1 15	-1 -10	1 10	nA
	$I_{D(off)}$		Room Full		-1 -15	1 15	-1 -10	1 10	
Channel On Leakage Current ^a	$I_{D(on)}$	$V_+ = 5.5\text{ V}, V_D = V_S = 1\text{ V or } 4\text{ V}$ Sequence Each Switch On	Room Full		-1 -15	1 15	-1 -10	1 10	
Digital Control									
Logic High Input Voltage	V_{INH}	$V_+ = 5\text{ V}$	Full		2.4		2.4		V
Logic Low Input Voltage	V_{INL}		Full			0.6		0.6	
Input Current ^a	I_{IN}	$V_{AX} = V_{EN} = 2.4\text{ V or } 0.6\text{ V}$	Full		-1.5	1.5	-1	1	μA
Dynamic Characteristics									
Transition Time ^e	t_{TRANS}	$V_{S1} = 3.5\text{ V}, V_{S8} = 0\text{ V}, (\text{DG408L})$ $V_{S1b} = 3.5\text{ V}, V_{S4b} = 0\text{ V}, (\text{DG409L})$ See Figure 2	Room Full	44		125 138		125 135	ns
Break-Before-Make Time ^e	t_{OPEN}	$V_{S(all)} = V_{DA} = 3.5\text{ V}$, See Figure 4	Room Full	17	1		1		
Enable Turn-On Time ^e	$t_{ON(EN)}$	$V_{AX} = 0\text{ V}, V_{S1} = 3.5\text{ V} (\text{DG408L})$ $V_{AX} = 0\text{ V}, V_{S1b} = 3.5\text{ V} (\text{DG409L})$ See Figure 3	Room Full	43		60 70		60 65	
Enable Turn-Off Time ^e	$t_{OFF(EN)}$		Room Full	26		45 60		45 50	
Charge Injection ^e	Q	$C_L = 1\text{ nF}, R_{GEN} = 0\ \Omega, V_{GEN} = 0\text{ V}$	Room	1		5		5	pC
Off Isolation ^{e, h}	OIRR	$R_L = 1\text{ k}\Omega, f = 100\text{ kHz}$	Room	-70					dB
Crosstalk ^e	X_{TALK}		Room	-80					
Source Off Capacitance ^e	$C_{S(off)}$	$f = 1\text{ MHz}, V_S = 0\text{ V}, V_{EN} = 0\text{ V}$	Room	8					pF
Drain Off Capacitance ^e	$C_{D(off)}$	$f = 1\text{ MHz}, V_D = 0\text{ V}, V_{EN} = 0\text{ V}$	Room	21					
Drain On Capacitance ^e	$C_{D(on)}$	$f = 1\text{ MHz}, V_D = 0\text{ V}, V_{EN} = 2.4\text{ V}$ (DG409L only)	Room	32					



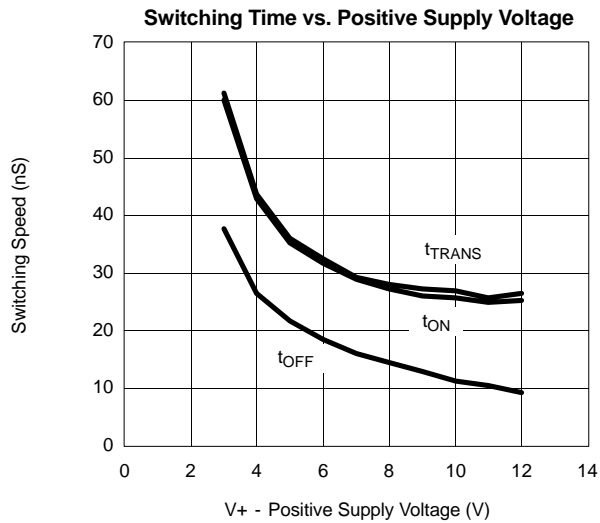
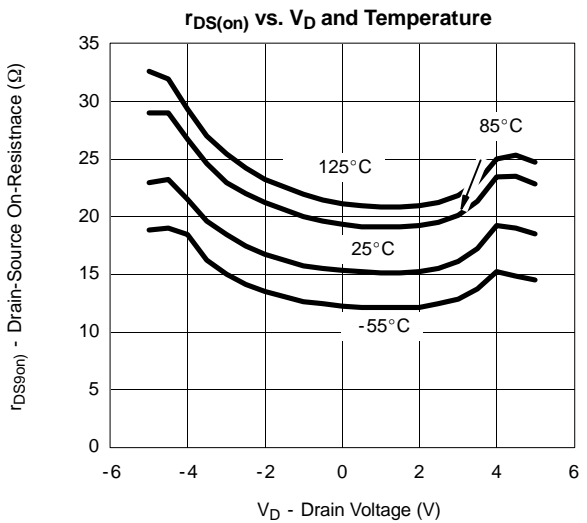
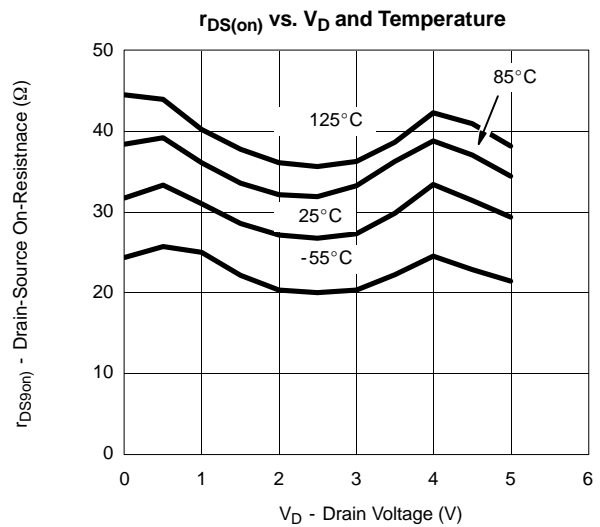
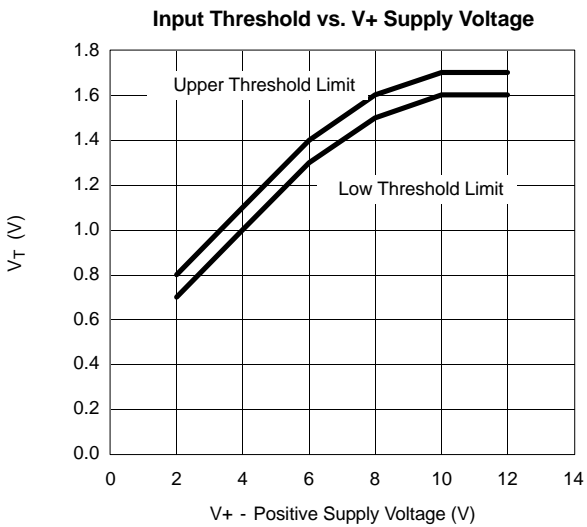
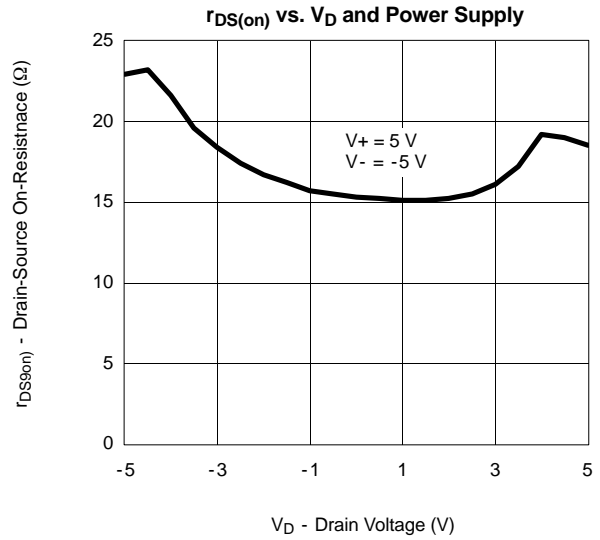
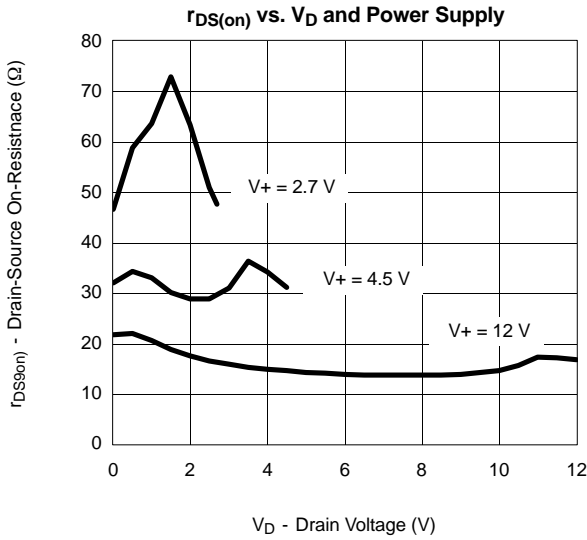
SPECIFICATIONS (SINGLE SUPPLY 3 V)									
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 3\text{ V}, \pm 10\%, V_- = 0\text{ V}$ $V_{EN} = 0.4\text{ V or } 2.0\text{ V}^f$	Temp ^b	Typ ^d	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min ^c	Max ^c	Min ^c	Max ^c	
Analog Switch									
Analog Signal Range ^e	V_{ANALOG}		Full		0	3	0	3	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_+ = 2.7\text{ V}, V_D = 0.5\text{ or } 2.2\text{ V}, I_S = 5\text{ mA}$	Room Full	60		80 105		80 100	Ω
Switch Off Leakage Current ^a	$I_{S(off)}$	$V_+ = 3.3\text{ V}, V_S = 2\text{ or } 1\text{ V}, V_D = 1\text{ or } 2\text{ V}$	Room Full		-1 -15	1 15	-1 -10	1 10	nA
	$I_{D(off)}$		Room Full		-1 -15	1 15	-1 -10	1 10	
Channel On Leakage Current ^a	$I_{D(on)}$	$V_+ = 3.3\text{ V}, V_D = V_S = 1\text{ or } 2\text{ V}$ Sequence Each Switch On	Room Full		-1 -15	1 15	-1 -10	1 10	
Digital Control									
Logic High Input Voltage	V_{INH}		Full		2		2		V
Logic Low Input Voltage	V_{INL}		Full			0.4		0.4	
Input Current ^a	I_{IN}	$V_{AX} = V_{EN} = 2.4\text{ V or } 0.4\text{ V}$	Full		-1.5	1.5	-1	1	μA
Dynamic Characteristics									
Transition Time	t_{TRANS}	$V_{S1} = 1.5\text{ V}, V_{S8} = 0\text{ V}, (\text{DG408L})$ $V_{S1b} = 1.5\text{ V}, V_{S4b} = 0\text{ V}, (\text{DG409L})$ See Figure 2	Room Full	75		150 175		150 175	ns
Break-Before-Make Time	t_{OPEN}	$V_{S(all)} = V_{DA} = 1.5\text{ V}$, See Figure 4	Room Full	32	1		1		
Enable Turn-On Time	$t_{ON(EN)}$	$V_{AX} = 0\text{ V}, V_{S1} = 1.5\text{ V} (\text{DG408L})$ $V_{AX} = 0\text{ V}, V_{S1b} = 1.5\text{ V} (\text{DG409L})$ See Figure 3	Room Full	70		95 115		95 105	
Enable Turn-Off Time	$t_{OFF(EN)}$		Room Full	55		100 115		100 105	
Charge Injection ^e	Q	$C_L = 1\text{ nF}, R_{GEN} = 0\ \Omega, V_{GEN} = 0\text{ V}$	Room	0.4		5		5	pC
Off Isolation ^{e, h}	OIRR	$f = 100\text{ kHz}, R_L = 1\text{ k}\Omega$	Room	-70					dB
Crosstalk ^e	X_{TALK}		Room	-79					
Source Off Capacitance ^e	$C_{S(off)}$	$f = 1\text{ MHz}, V_S = 0\text{ V}, V_{EN} = 0\text{ V}$	Room	8					pF
Drain Off Capacitance ^e	$C_{D(off)}$	$f = 1\text{ MHz}, V_D = 0\text{ V}, V_{EN} = 0\text{ V}$	Room	19					
Drain On Capacitance ^e	$C_{D(on)}$	$f = 1\text{ MHz}, V_D = 0\text{ V}, V_{EN} = 2\text{ V}$ (DG409L only)	Room	33					

Notes

- Leakage parameters are guaranteed by worst case test condition and not subject to production test.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.
- $\Delta r_{DS(on)} = r_{DS(on)} \text{ Max} - r_{DS(on)} \text{ Min}$.
- Worst case isolation occurs on Channel 4 do to proximity to the drain pin.
- $r_{DS(on)}$ flatness is measured as the difference between the minimum and maximum measured values across a defined Analog signal.



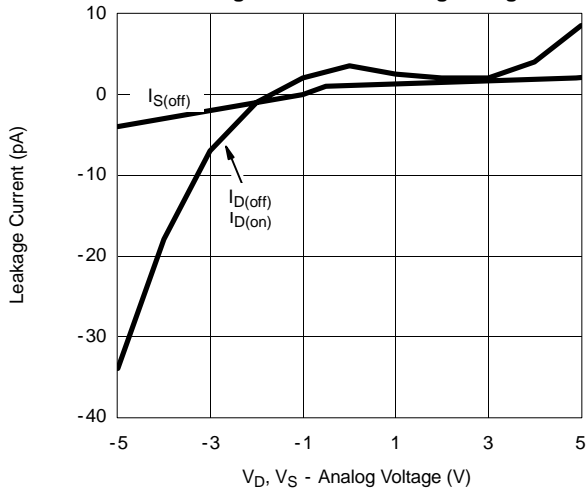
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



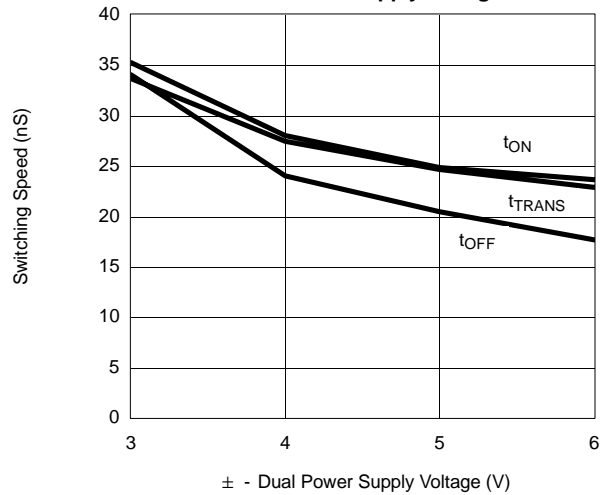


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

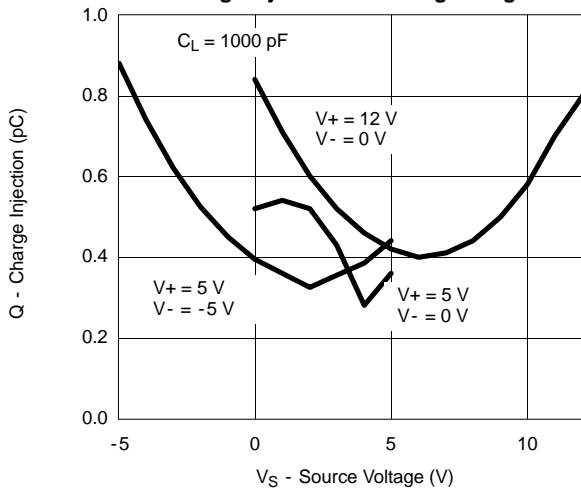
Leakage Current vs. Analog Voltage



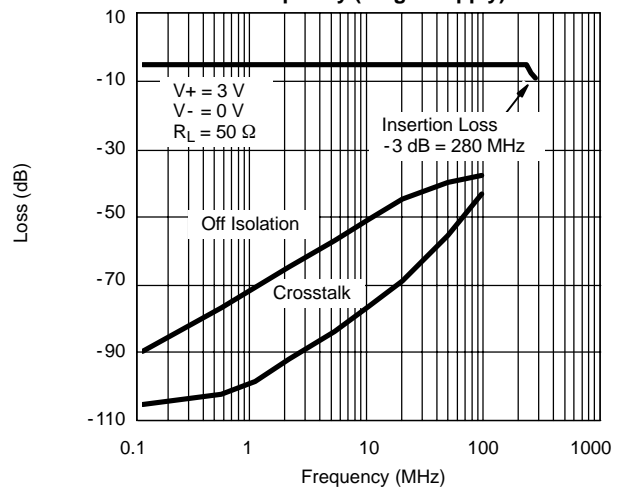
Switching Time vs. Dual Power Supply Voltage



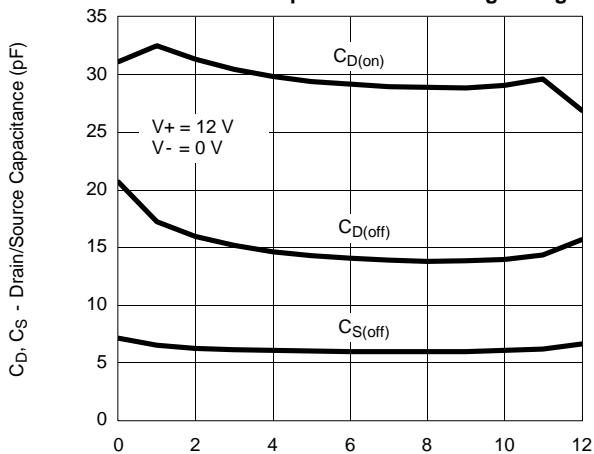
Charge Injection vs. Analog Voltage



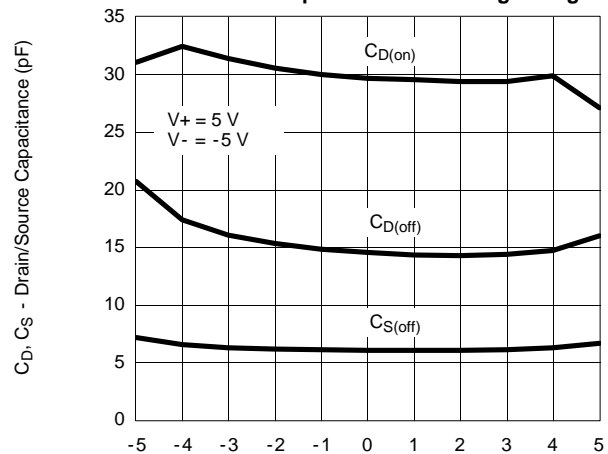
Insertion Loss, Off Isolation and Crosstalk vs. Frequency (Single Supply)



Drain/Source Capacitance vs. Analog Voltage



Drain/Source Capacitance vs. Analog Voltage



SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

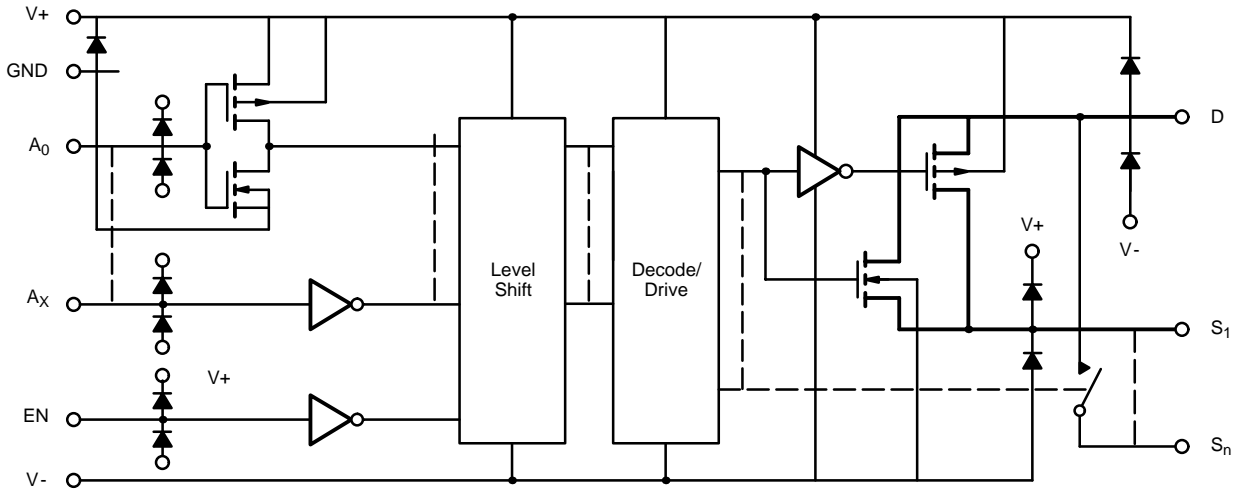


FIGURE 1.

TEST CIRCUITS

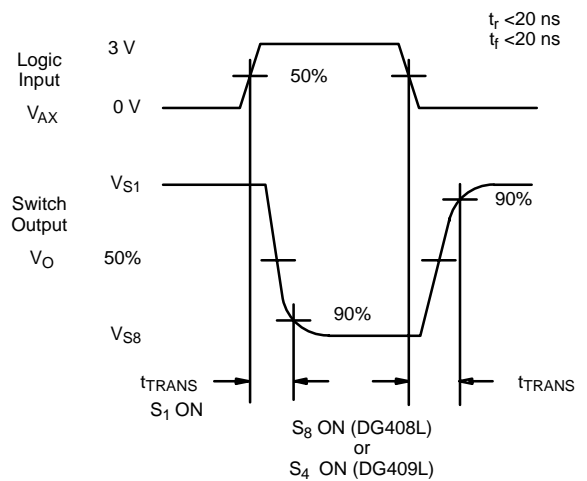
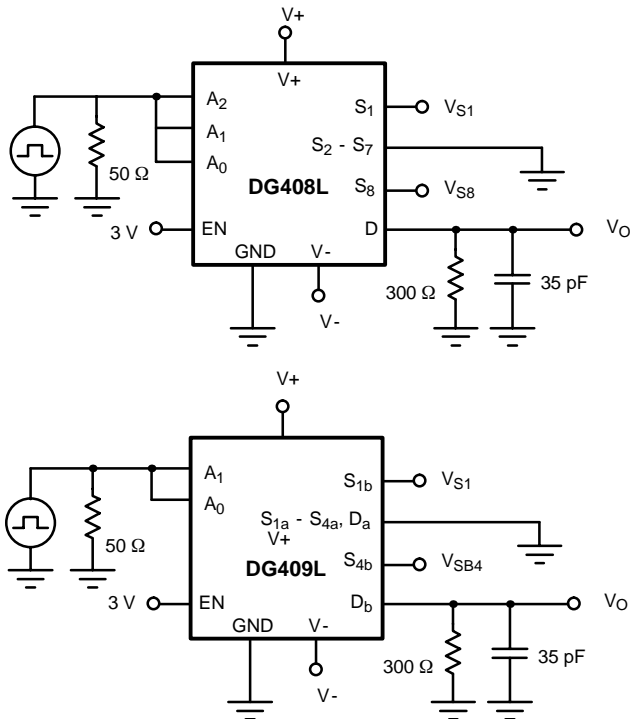


FIGURE 2. Transition Time

TEST CIRCUITS

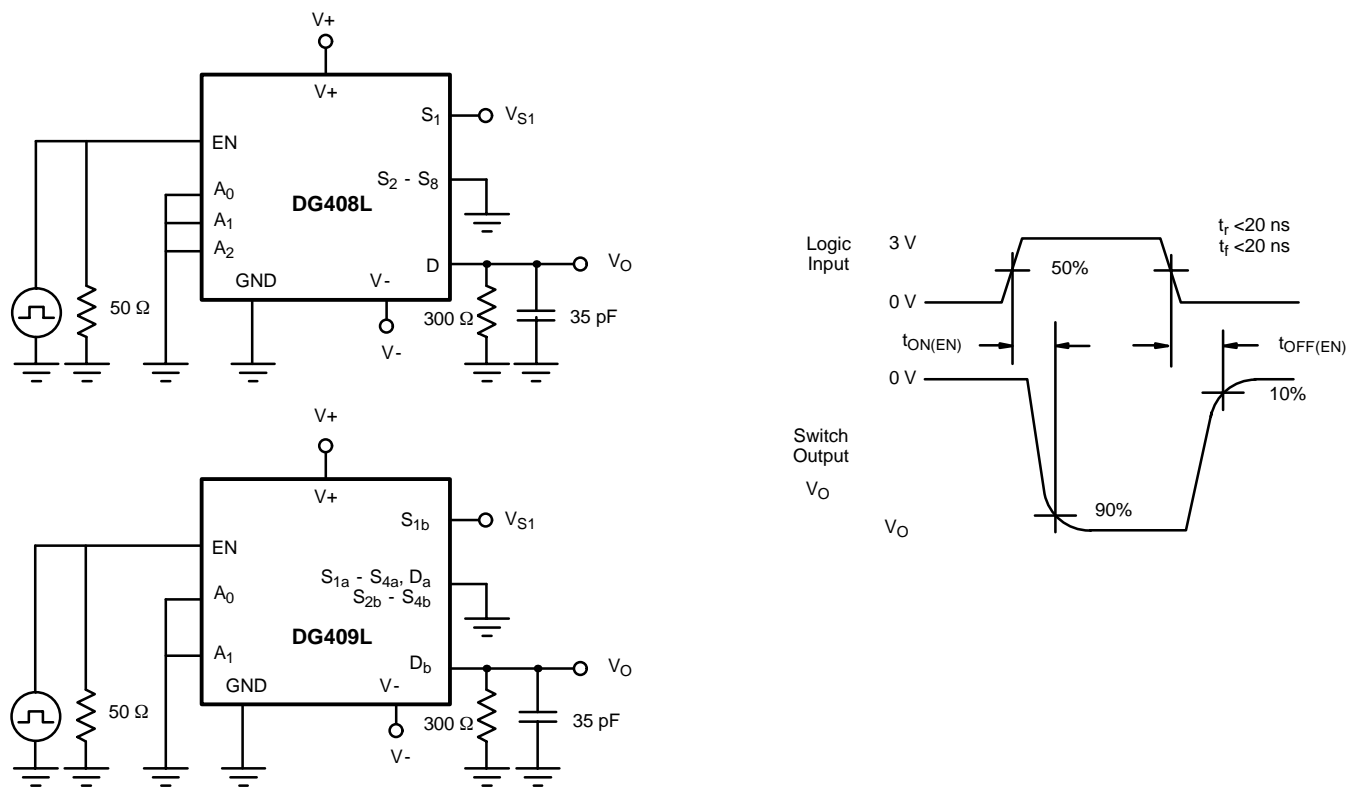


FIGURE 3. Enable Switching Time

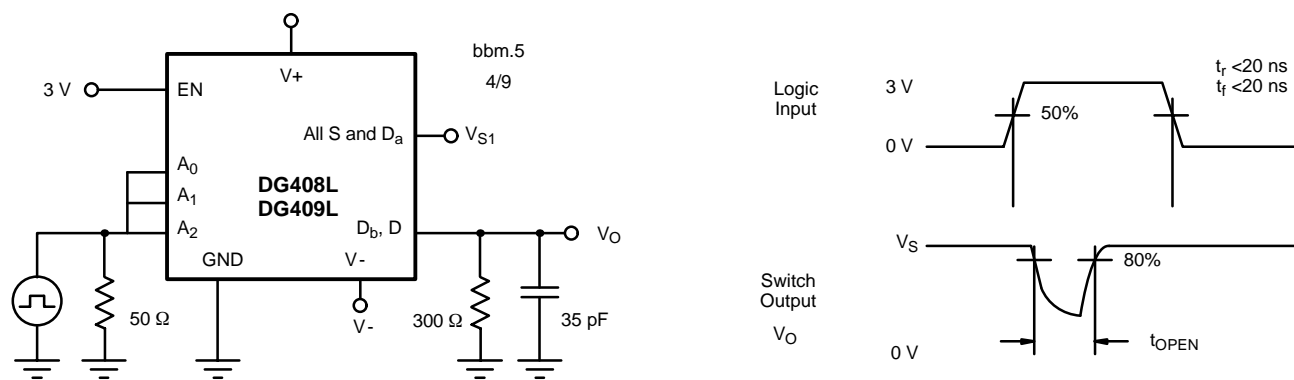


FIGURE 4. Break-Before-Make Interval

TEST CIRCUITS

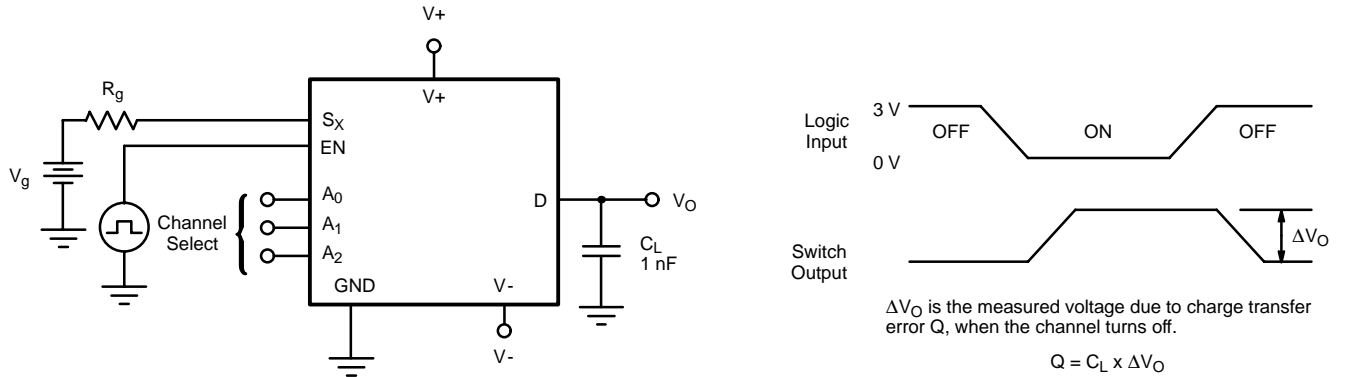


FIGURE 5. Charge Injection

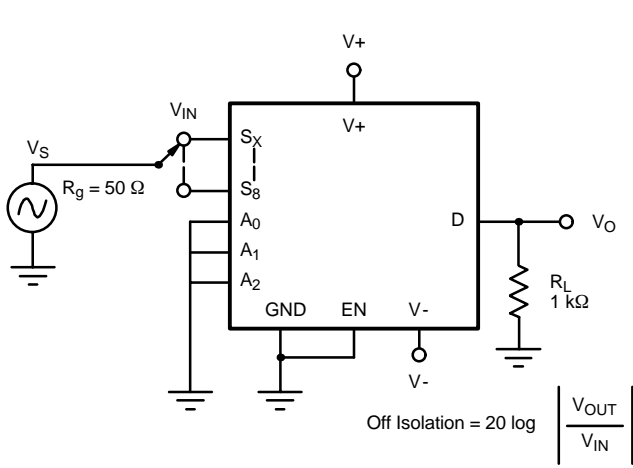


FIGURE 6. Off Isolation

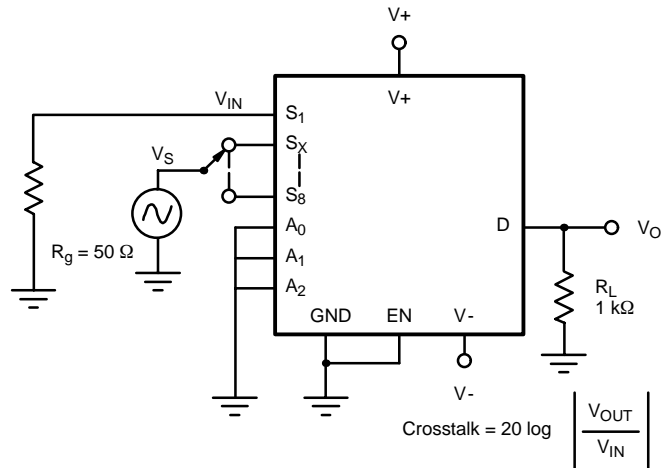


FIGURE 7. Crosstalk

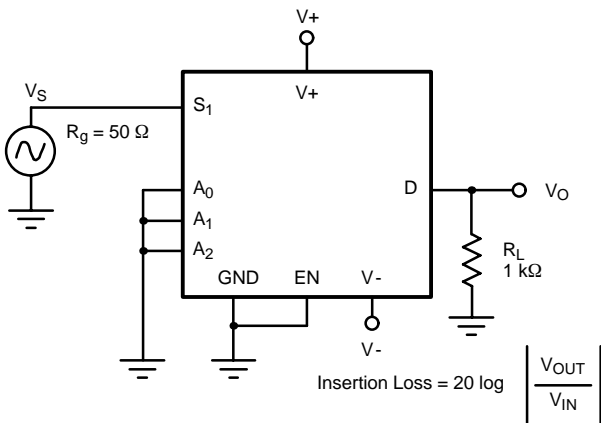


FIGURE 8. Insertion Loss

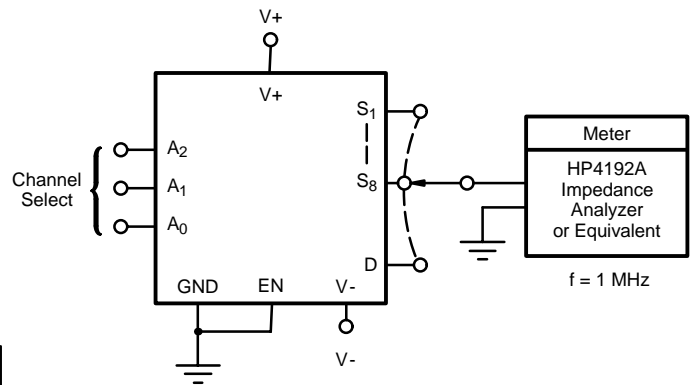


FIGURE 9. Source Drain Capacitance