Quad Channel, 16-Bit, Serial Input, 4-20mA & Voltage Output DAC, Dynamic Power Control, HART Connectivity

Preliminary Technical Data

AD5755-1

FEATURES

16/12-Bit Resolution and Monotonicity
Dynamic Power Control for Thermal Management
Voltage or Current Output on the Same Pin
IOUT Range: 0mA-20mA, 4mA–20mA or 0mA–24mA
±0.05% Total Unadjusted Error (TUE) Max
VOUT Range: 0-5V, 0-10V, ±5V, ±10V,±6V,±12V
±0.05% Total Unadjusted Error (TUE) Max
User programmable Offset and Gain
On Chip Diagnostics
On-Chip Reference (±5 ppm/°C)
–40°C to +105°C Temperature Range

APPLICATIONS

Process Control
Actuator Control
PLC's
HART Network Connectivity

PRODUCT HIGHLIGHTS

Dynamic Power Control for Thermal management

16bit performance

Multi-channel

HART Compliant

GENERAL DESCRIPTION

The AD5755-1 is a quad, voltage and current output DAC, which operates with a power supply range from -26v to +33v. On chip dynamic power control minimizes package power dissipation in current mode. This is achieved by regulating the voltage on the output driver from between 7V-30V.

Each channel has a corresponding CHART pin so that HART signals can be coupled onto the AD5755-1's current output.

The part uses a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and that is compatible with standard SPI®, QSPI™, MICROWIRE™, DSP and microcontroller interface standards. The interface also features optional CRC-8 packet error checking as well as a watchdog timer that monitors activity on the interface.

Table 1. Complementary Devices

Part No.	Description
ADR445	5V, Ultralow Noise, LDO XFET Voltage Reference with Current Sink and Source
ADP1871	Synchronous Buck Controller with Constant On-Time, Valley Current Mode, and Power Save Mode

FUNCTIONAL BLOCK DIAGRAM

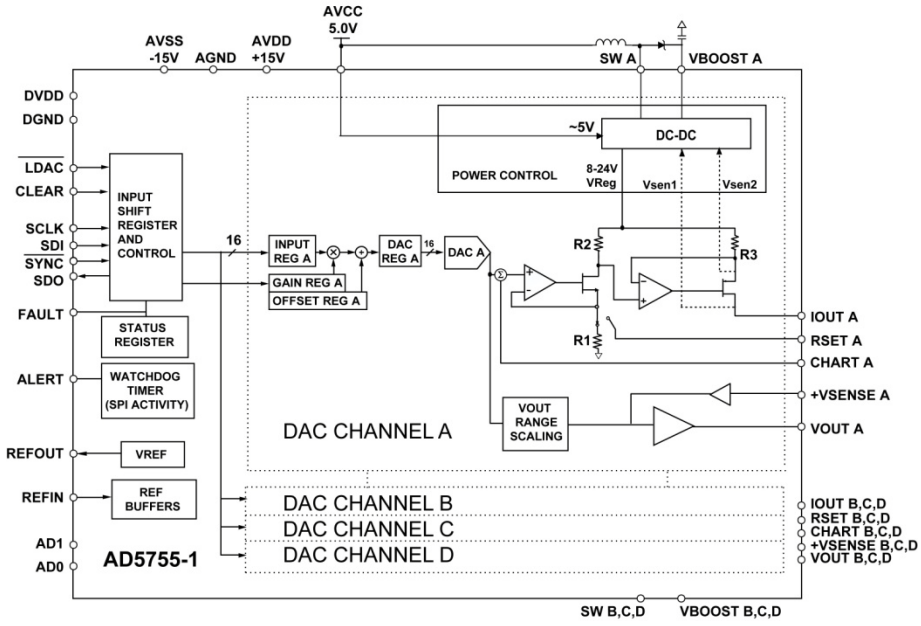

Figure 1.

Rev. PrD

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SPECIFICATIONS

AVDD = 15V, AVSS = -15V/0V, $V_{BOOSTA,B,C,D}$ = +10.8 V to +33 V, DVDD = AVCC = 2.7 V to 5.5 V, DCDC disabled, AGND = DGND = $GNDSW_{A,B,C,D}$ = 0 V, REFIN= +5, V_{OUT} : R_L = 1kΩ, C_L = 220pF, I_{OUT} : R_L = 300Ω, all specifications T_{MIN} to T_{MAX} unless otherwise noted.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE OUTPUT					
Output Voltage Ranges	0		5	V	
	0		10	V	AVDD needs to have min **TBDv** headroom on output.
	- 5		+ 5	V	
	-10		+ 10	V	AVDD/AVSS need to have min **TBDv** headroom on output.
	0		6	V	
	0		12	V	AVDD needs to have min **TBDv** headroom on output.
	-6		+6	V	
	-12		+2	V	AVDD/AVSS need to have min **TBDv** headroom on output.
ACCURACY					
Resolution	16			Bits	
Total Unadjusted Error (TUE)					
	−0.04		+0.04	% FSR	
	−0.02	TBD	+0.02	% FSR	T_A = 25°C
TUE TC[2]		±3		ppm FSR/°C typ	
Relative Accuracy (INL)	−0.006		+0.006	% FSR	
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Bipolar Zero Error	−TBD		+TBD	%FSR	
	−0.008	TBD	+0.008	%FSR	T_A = 25°C
Bipolar Zero TC[2]		±3		ppm FSR/°C	
Zero-Scale Error	−TBD		+TBD	%FSR	
	−0.016	TBD	+0.016	%FSR	T_A = 25°C
Zero-Scale TC[2]		±3		ppm FSR/°C	
Gain Error	−TBD		+TBD	% FSR	
	−TBD	TBD	+TBD	% FSR	T_A = 25°C
Gain TC[2]	−TBD	TBD	+TBD	ppm FSR/°C	
Full-Scale Error	−TBD		+TBD	% FSR	T_A = 25°C
	−TBD	TBD	+TBD	% FSR	T_A = 25°C
Full-Scale TC[2]	−TBD	TBD	+TBD	ppm FSR/°C	
OUTPUT CHARACTERISTICS[2]					
Headroom		1	TBD	V	
Output Voltage Drift vs. Time		±TBD		ppm FSR	Drift after 500 hours, T_J = 150°C (this is included in the TUE specifications)
		±TBD		ppm FSR	Drift after 1000 hours, T_J = 150°C (this is included in the TUE specifications)
Short-Circuit Current		15/8		mA	Programmable by user, defaults to 15ma Typ level.
Load	1			kΩ	For specified performance
Capacitive Load Stability					
R_L = ∞			20	nF	
R_L = 2 kΩ			TBD	nF	
R_L = ∞			2	µF	External compensation capacitor of min TBD pF connected.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DC Output Impedance		0.3		Ω	
DC PSRR		TBD		µV/V	
			TBD	µV/V	
CURRENT OUTPUT					
Output Current Ranges	0		24	mA	
	0		20	mA	
	4		20	mA	
Resolution	16			Bits	
ACCURACY (External R_{set})					
Total Unadjusted Error (TUE)					
	−0.05		+0.05	% FSR	
	−0.02	TBD	+0.02	% FSR	T_A = 25°C
TUE TC[2]	−TBD	±TBD	+TBD	ppm	
Relative Accuracy (INL)	−0.006		+0.006	% FSR	
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Offset Error	−0.035		+0.035	% FSR	
	−TBD	TBD	+TBD	% FSR	T_A = 25°C
Offset Error Drift[2]		±TBD		ppm FSR/°C	
Gain Error	−0.02		+0.02	% FSR	
	−TBD	TBD	+TBD	% FSR	T_A = 25°C
Gain TC[2]	−TBD		+TBD	ppm FSR/°C	
Full-Scale Error	−0.05		+0.05	% FSR	
	−TBD	TBD	+TBD	% FSR	T_A = 25°C
Full-Scale TC[2]	−TBD		+TBD	ppm FSR/°C	
ACCURACY (Internal R_{set})					
Total Unadjusted Error (TUE)					
	−0.12		+0.12	% FSR	
	−0.02	TBD	+0.02	% FSR	T_A = 25°C
TUE TC[2]	−TBD	±TBD	+TBD	ppm	
Relative Accuracy (INL)	−0.006		+0.006	% FSR	
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Offset Error	−0.04		+0.04	% FSR	
	−TBD	TBD	+TBD	% FSR	T_A = 25°C
Offset Error Drift[2]		±TBD		ppm FSR/°C	
Gain Error	−0.08		+0.08	% FSR	
	−TBD	TBD	+TBD	% FSR	T_A = 25°C
Gain TC[2]	−TBD		+TBD	ppm FSR/°C	
Full-Scale Error	−0.12		+0.12	% FSR	
	−TBD	TBD	+TBD	% FSR	T_A = 25°C
Full-Scale TC[2]	−TBD		+TBD	ppm FSR/°C	
OUTPUT CHARACTERISTICS[2]					
Current Loop Compliance Voltage		TBD	AVDD - 2.5	V max	
Output Current Drift vs. Time		±TBD		ppm FSR	Drift after 500 hours, T_J = 150°C (this is included in the TUE specifications)
		±TBD		ppm FSR	Drift after 1000 hours, T_J = 150°C (this is included in the TUE specifications)

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
Resistive Load		See Comment		Ω max	Chosen such that compliance is not exceeded. Plus see graph on load vs AVcc and DCDC switching freq.
Inductive Load		See Comment		H max	Will need appropriate cap at higher inductance values. See Page X of Datasheet.
DC PSRR		TBD		µA/V	
			TBD	µA/V	
Output Impedance		50		MΩ	
REFERENCE INPUT/OUTPUT					
Reference Input[2]					
Reference Input Voltage	4.95	5	5.05	V nom	For specified performance
DC Input Impedance	5	TBD		MΩ min	
Reference Output					
Output Voltage	4.998	5	5.002	V	T_A = 25°C
Reference TC[2,3]	-10	±5	10	ppm/°C	
Output Noise (0.1 Hz to 10 Hz)[2]		TBD		µV p-p typ	
Noise Spectral Density[2]		TBD		nV/√Hz typ	At 10 kHz
Output Voltage Drift vs. Time[2]		±TBD		ppm	Drift after 500 hours, T_J = 150°C
		±TBD		ppm	Drift after 1000 hours, T_J = 150°C
Capacitive Load[2]			TBD	nF	
Load Current		5		mA	
Short Circuit Current		7		mA	
Line Regulation[2]		10		ppm/V	
Load Regulation[2]		TBD		ppm/mA	
Thermal Hysteresis[2]		TBD		ppm	
DC-DC					
SWITCH					
SWITCH On Resistance		0.5		ohm	
SWITCH Leakage Current		TBD		uA	VIN=TBD, IOUT=TBD, RLOAD=TBD
Peak Current Limit		0.8		A	
OSCILLATOR					
Oscillator Frequency	TBD	TBD	TBD	KHz	
Maximum Duty Cycle		TBD		%	
DIGITAL INPUTS[2]					JEDEC compliant
V_{IH}, Input High Voltage	2			V	
V_{IL}, Input Low Voltage			0.8	V	
Input Current	−1		+1	µA	Per pin
Pin Capacitance		10		pF	Per pin
DIGITAL OUTPUTS[2]					
SDO, ALERT					
V_{OL}, Output Low Voltage			0.4	V	sinking 200 µA
V_{OH}, Output High Voltage	DVDD −0.5			V	sourcing 200 µA
High Impedance Leakage Current	−1		+1	µA	
High Impedance Output Capacitance		5		pF	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{FAULT}$					
V_{OL}, Output Low Voltage			0.4	V	10kΩ pull-up resistor to DVDD
V_{OL}, Output Low Voltage		0.6		V	At 2.5 mA
V_{OH}, Output High Voltage	3.6			V	10kΩ pull-up resistor to DVDD
POWER REQUIREMENTS					
AV_{DD}	12		33	V	
AV_{SS}	−26.4		−10.8	V	Bipolar Supply Mode (In uni-polar supply mode tie AVss to AGND)
DVDD, AVCC					
Input Voltage	2.7		5.5	V	
AI_{DD}			TBD	mA	Output unloaded
AI_{SS}			TBD	mA	Bipolar Supply Mode only, outputs unloaded
DI_{CC}			TBD	mA	V_{IH} = DVDD, V_{IL} = GND
AIcc			TBD	mA	DCDC 's not enabled
Power Dissipation		TBD		mW	AV_{DD} = 33V, AV_{SS} = 0V, outputs unloaded
		TBD		mW	AV_{DD} = 33V, AV_{SS} = -26.4 V, outputs unloaded
		TBD		mW	AV_{DD} = 15V, AV_{SS} = -15 V, outputs unloaded

[1]Temperature range: −40°C to +105°C; typical at +25°C.
[2] Guaranteed by design and characterization; not production tested.
[3] The on-chip reference is production trimmed and tested at 25°C and 85°C. It is characterized from −40°C to +105°C.

AC PERFORMANCE CHARACTERISTICS

AVDD = 15V, AVSS = -15V/0V, $V_{BOOSTA,B,C,D}$ = +10.8 V to +33 V, DVDD = AVCC = 2.7 V to 5.5 V, DCDC disabled, AGND = DGND = $GNDSW_{A,B,C,D}$ = 0 V, REFIN= +5, V_{OUT} : R_L = 1kΩ, C_L = 220pF, I_{OUT} : R_L = 300Ω, all specifications T_{MIN} to T_{MAX} unless otherwise noted.

Table 3.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Voltage Output					
Output Voltage Settling Time		TBD	TBD	µs typ	10 V step to ±0.03% FSR
		TBD	TBD	µs typ	100mv step to 1 LSB (16-Bit LSB)
Slew Rate		1		V/µs	
Power-On Glitch Energy		10		nV-sec	
Digital-to-Analog Glitch Energy		10		nV-sec	
Glitch Impulse Peak Amplitude		20		mV	
Digital Feedthrough		1		nV-sec	
DAC to DAC Crosstalk		TBD		nV-sec	
Output Noise (0.1 Hz to 10 Hz Bandwidth)		0.1		LSB p-p	(16-Bit LSB)
Output Noise (100 kHz Bandwidth)			TBD	µV rms	
Output Noise Spectral Density		TBD		nV/√Hz	Measured at 10 kHz
AC PSRR		TBD		dB	100mV 150KHz Sinewave superimposed on power supply voltage
AC PSRR		TBD		dB	200mV 50/60Hz Sinewave superimposed on power supply voltage
Current Output					
Output Current Settling Time		TBD	TBD	µs typ	To 0.1% FSR
		-		ms typ	See Figure 7 and Figure 8
Output Noise (0.1 Hz to 10 Hz Bandwidth)		0.1		LSB p-p	(16-Bit LSB)
Output Noise (100 kHz Bandwidth)			80	µV rms	
Output Noise Spectral Density		TBD		nV/√Hz	Measured at 10 kHz
Slew Rate		TBD		uA/µs	
		TBD		µs	To 0.1% FSR. See Figure 7 and Figure 8 for plots with a channels DC-DC enabled.

[1] Guaranteed by characterization, not production tested.

TIMING CHARACTERISTICS

AVDD = 15V, AVSS = -15V/0V, $V_{BOOSTA,B,C,D}$ = +10.8 V to +33 V, DVDD = AVCC = 2.7 V to 5.5 V, DCDC disabled, AGND = DGND = $GNDSW_{A,B,C,D}$ = 0 V, REFIN= +5, V_{OUT} : R_L = 1kΩ, C_L = 220pF, I_{OUT} : R_L = 300Ω, all specifications T_{MIN} to T_{MAX} unless otherwise noted.

Table 4.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	13	ns min	24/32nd SCLK falling edge to $\overline{SYNC}$ rising edge
t_6	198	ns min	$\overline{SYNC}$ high time
t_7	5	ns min	Data setup time
t_8	5	ns min	Data hold time
t_9	20	µs min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (all DACs updated or any channel has digital slew rate control enabled)
	5	µs min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (single DAC updated)
t_{10}	10	ns min	$\overline{LDAC}$ pulse width low
t_{11}	500	ns max	$\overline{LDAC}$ falling edge to DAC output response time
t_{12}	See AC Performance Characteristics	µs max	DAC output settling time
t_{13}	10	ns min	CLEAR high time
t_{14}	TBD	µs max	CLEAR activation time
t_{15}	25	ns max	SCLK rising edge to SDO valid ($C_{L\ SDO}$ = 35 pF)
t_{16}	20	µs min	$\overline{SYNC}$ rising edge to DAC output response time (LDAC = 0) (all DACs updated)
	5	µs min	$\overline{SYNC}$ rising edge to DAC output response time (LDAC = 0) (single DAC updated)
t_{17}	500	ns min	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ rising edge
t_{18}	700	ns min	RESET pulsewidth
t_{19}	20	µs min	$\overline{SYNC}$ high to next $\overline{SYNC}$ low (Ramp enabled)
	5	µs min	$\overline{SYNC}$ high to next $\overline{SYNC}$ low (Ramp disabled)

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DVDD) and timed from a voltage level of 1.2 V.
[3] See Figure 2 , Figure 3 , Figure 4 and Figure 5

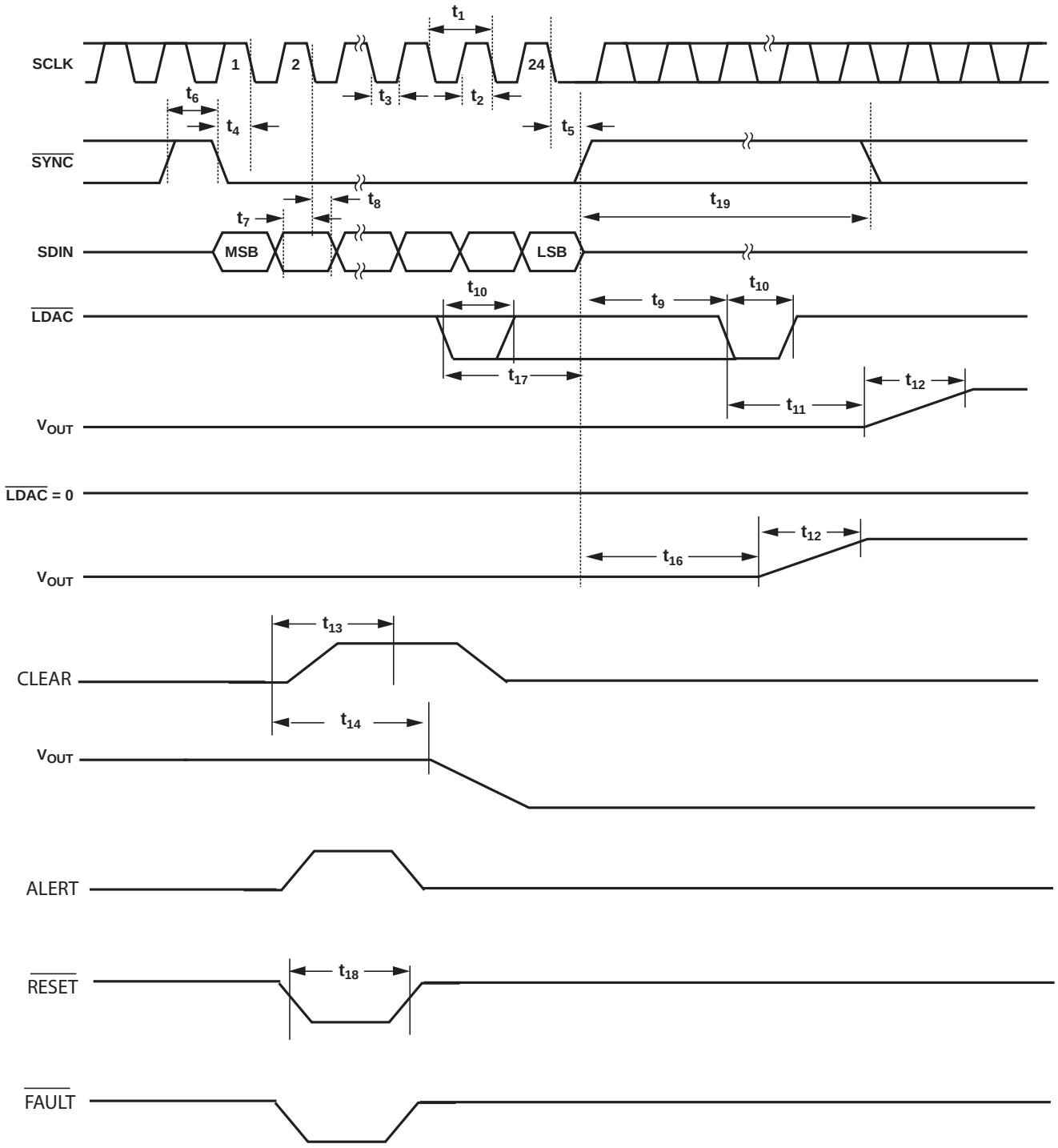


Figure 2. Serial Interface Timing Diagram

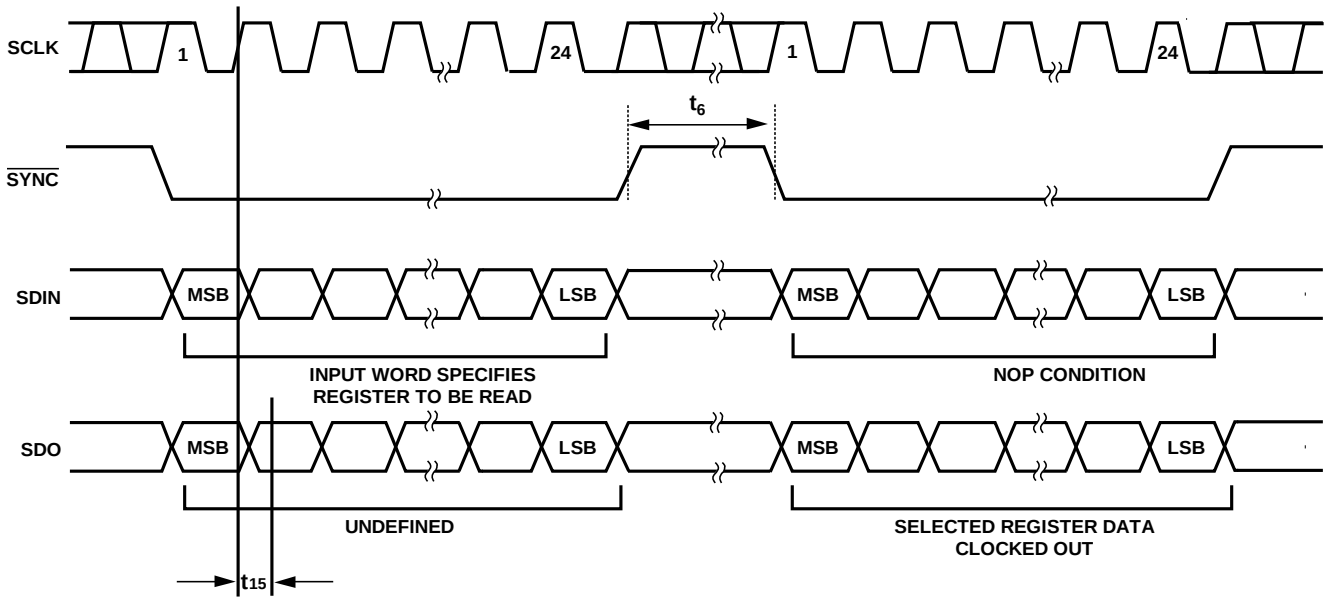


Figure 3. Readback Timing Diagram

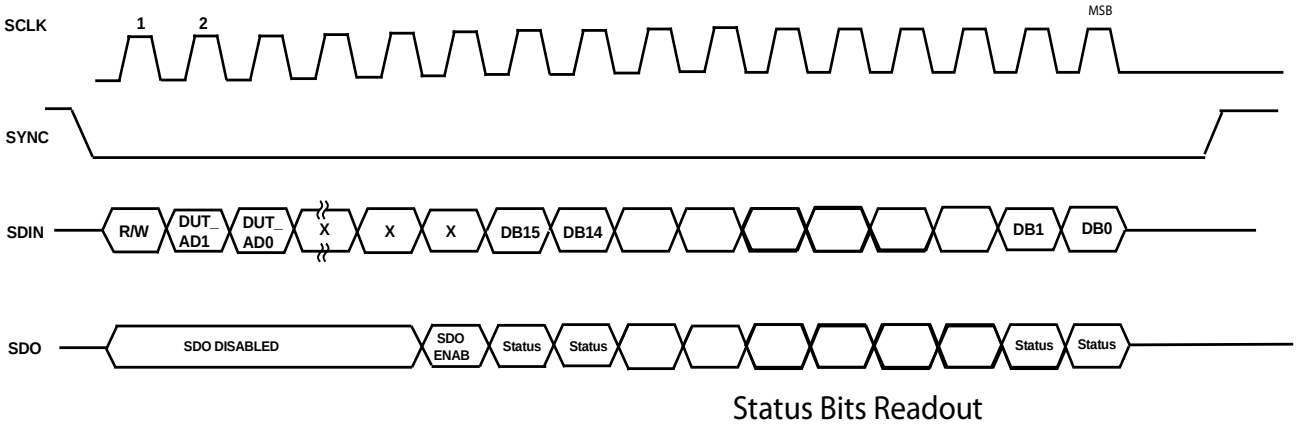


Figure 4. Status Readback during write

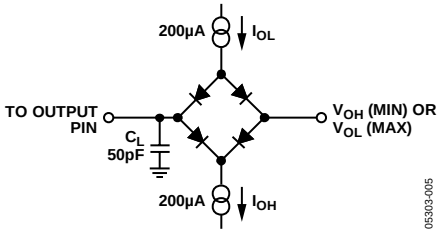


Figure 5. Load Circuit for SDO Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 5.

Parameter	Rating
AV_{DD} to AGND, DGND	−0.3 V to +33 V
AV_{SS} to AGND, DGND	+0.3 V to −28 V
AV_{DD} to AV_{SS}	−0.3 V to +60 V
AV_{cc} to AGND	−0.3 V to +7 V
DVDD to DGND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to DVDD + 0.3 V or +7 V (whichever is less)
Digital Outputs to DGND	−0.3 V to DVDD + 0.3 V
REFIN/REFOUT to AGND	−0.3 V to AVDD + 0.3 V or +7 V (whichever is less)
VOUTA, VOUTB, VOUTC, VOUTD to AGND	AV_{SS} to AV_{DD}
$+V_{SENSEA,B,C,D}$ to AGND	AV_{SS} to AD_{DD}
$COMP_{LVA,B,C,D}$ to AGND	0.3 V to +5 V
I_{OUT} A,B,C,D to AGND	−0.3 V to AV_{DD}
$R_{SETA,B,C,D}$ to AGND	−0.3 V to AVDD + 0.3 V or +7 V (whichever is less)
$SW_{A,B,C,D}$ / $V_{BOOSTA,B,C,D}$ to AGND	−0.3 to +33 V
$COMP_{DCDC\_A,B,C,D}$/ $CHART_{A,B,C,D}$ to AGND	−0.3 V to +5 V
AGND, $GNDSW_{A,B,C,D}$ to DGND	−0.3 V to +0.3 V
Operating Temperature Range (T_A)	
Industrial[1]	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	125°C
64-Lead LFCSP	
θ_{JA} Thermal Impedance[2]	20°C/W
Power Dissipation	$(T_J max - T_A)/\theta_{JA}$
Lead Temperature	JEDEC Industry Standard
Soldering	J-STD-020

[1] Power dissipated on chip must be derated to keep the junction temperature below 125°C
[2] Based on a JEDEC 4 layer test board

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

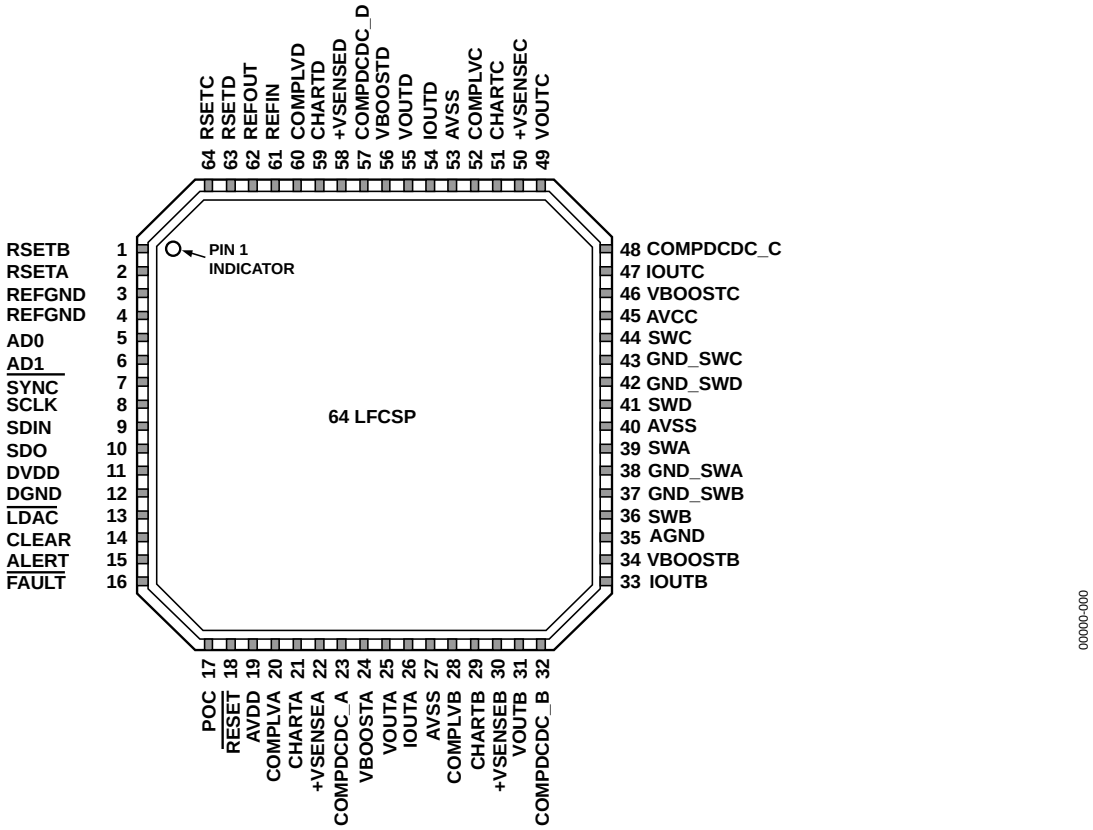


Figure 6. 64 LFCSP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	R_{SET_B}	An external, precision, low drift 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_B} temperature drift performance. See the Features section.
2	R_{SET_A}	An external, precision, low drift 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_A} temperature drift performance. See the Features section.
3	REFGND	Ground Reference Point for Internal Reference.
4	REFGND	Ground Reference Point for Internal Reference.
5	ADO	Address decode for the DUT on the board.
6	AD1	Address decode for the DUT on the board.
7	$\overline{SYNC}$	Active Low Input. This is the frame synchronization signal for the serial interface. While $\overline{SYNC}$ is low, data is transferred in on the falling edge of SCLK.
8	SCLK	Serial Clock Input. Data is clocked into the shift register on the rising edge of SCLK. This operates at clock speeds of up to 30 MHz.
9	SDIN	Serial Data Input. Data must be valid on the falling edge of SCLK.
10	SDO	Serial Data Output. Used to clock data from the serial register in readback mode. See Figure 3 and Figure 4.
11	DV_{DD}	Digital Supply Pin. Voltage ranges from 2.7 V to 5.5 V.
12	DGND	Digital Ground Pin.
13	$\overline{LDAC}$	Load DAC. Active Low Input. This is used to update the DAC registers and consequently the analog outputs. When tied permanently low the addressed DAC register is updated on the rising edge of $\overline{SYNC}$. If $\overline{LDAC}$ is held high during the write cycle the DAC input register is updated but the output update only takes place at the falling edge of $\overline{LDAC}$. See Figure 2. Using this mode all analog outputs can be updated simultaneously. The $\overline{LDAC}$ pin must not be left unconnected.
14	CLEAR	Active High, Edge Sensitive Input. Asserting this pin sets the Output Current/Voltage to the pre-programmed CLEAR CODE. Only channels enabled to be cleared will be cleared. See features section for

Pin No.	Mnemonic	Description
		more information. When CLEAR is active, the DAC register cannot be written to.
15	ALERT	Active High Output. This pin is asserted when there has been no SPI activity on the interface pins for a predetermined time. See features section for more information.
16	$\overline{\text{FAULT}}$	Active Low Output. This pin is asserted low when an open circuit in current mode is detected or a short circuit in voltage mode is detected or a PEC error is detected or an over temperature is detected (see Features section). Open Drain Output.
17	POC	Power- On Condition. This pin determines the Power on Condition. If POC='0', the device is powered up with the voltage and current channels in Tri-State mode. If POC='1', the device is powered up with a 30k Ω pull down resistor to GND on the voltage output channel, and the current channels in Tri-State mode.
18	$\overline{\text{RESET}}$	Hardware Reset. Active Low Input.
19	AV_{DD}	Positive Analog Supply Pin. Voltage ranges from 10.8 V to 33 V.
20	$COMP_{LV\_A}$	Optional compensation capacitor connection for V_{OUT_A}'s output buffer. Connecting a 220 pF capacitor between this pin and the V_{OUT_A} pin allows the voltage output to drive up to 1 µF. It should be noted that the addition of this capacitor reduces the bandwidth of the output amplifier, increasing the settling time.
21	CHARTA	Hart Input Connection for DAC Channel A
22	$+V_{SENSE\_A}$	Sense connection for the positive voltage output load connection for V_{OUT_A}. This pin must stay within ±3.0 V of V_{OUT_A} for correct operation.
23	$COMP_{DCDC\_A}$	DC-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of channel A's DC-DC converter.
24	V_{BOOST_A}	Supply for channel A's current output stage (See Figure 15). To use the DC-DC feature of the device, connect as shown in Figure 21.
25	V_{OUT_A}	Buffered Analog Output Voltage for DAC Channel A.
26	I_{OUT_A}	Current Output Pin for DAC Channel A.
27	AV_{SS}	Negative Analog Supply Pin. Voltage ranges from -10.8 V to -26.4 V. This pin can be connected to 0 V if the output voltage range is unipolar,.
28	$COMP_{LV\_B}$	Optional compensation capacitor connection for V_{OUT_B}'s output buffer. Connecting a 220 pF capacitor between this pin and the V_{OUT_B} pin allows the voltage output to drive up to1 µF. It should be noted that the addition of this capacitor reduces the bandwidth of the output amplifier, increasing the settling time.
29	CHARTB	Hart Input Connection for DAC Channel B
30	$+V_{SENSE\_B}$	Sense connection for the positive voltage output load connection for V_{OUT_B}. This pin must stay within ±3.0 V of V_{OUT_B} for correct operation.
31	V_{OUT_B}	Buffered Analog Output Voltage for DAC Channel B.
32	$COMP_{DCDC\_B}$	DC-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of channel B's DC-DC converter.
33	I_{OUT_B}	Current Output Pin for DAC Channel B.
34	V_{BOOST_B}	Supply for channel B's current output stage (See Figure 15). To use the DC-DC feature of the device, connect as shown in Figure 21.
35	AGND	Ground Reference Point for Analog Circuitry. This must be connected to 0 V.
36	$SW_{\_B}$	Switching output for Channel B's DC-DC circuitry. To use the DC-DC feature of the device, connect as shown in Figure 21.
37	$GNDSW_{\_B}$	Ground connection for DC-DC switching circuit. This pin should always be connected to GND.
38	$GNDSW_{\_A}$	Ground connection for DC-DC switching circuit. This pin should always be connected to GND.
39	$SW_{\_A}$	Switching output for Channel A's DC-DC circuitry. To use the DC-DC feature of the device, connect as shown in Figure 21.
40	AV_{SS}	Negative Analog Supply Pin. Voltage ranges from -10.8 V to -26.4 V.
41	$SW_{\_D}$	Switching output for Channel D's DC-DC circuitry. To use the DC-DC feature of the device, connect as shown in Figure 21.
42	$GNDSW_{\_D}$	Ground connections for DC-DC switching circuit. This pin should always be connected to GND.
43	$GNDSW_{\_C}$	Ground connections for DC-DC switching circuit. This pin should always be connected to GND.
44	$SW_{\_C}$	Switching output for Channel C's DC-DC circuitry. To use the DC-DC feature of the device, connect as shown in Figure 21.
45	AV_{CC}	Supply for DC-DC circuitry.
46	V_{BOOST_C}	Supply for channel C's current output stage (See Figure 15). To use the DC-DC feature of the device, connect as shown in Figure 21.

Pin No.	Mnemonic	Description
47	I_{OUT_C}	Current Output Pin for DAC Channel C.
48	$COMP_{DCDC\_C}$	DC-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of channel C's DC-DC converter.
49	V_{OUT_C}	Buffered Analog Output Voltage for DAC Channel C.
50	$+V_{SENSE\_C}$	Sense connection for the positive voltage output load connection for V_{OUT_C}. This pin must stay within ±3.0 V of V_{OUT_C} for correct operation.
51	CHARTC	Hart Input Connection for DAC Channel C
52	$COMP_{LV\_C}$	Optional compensation capacitor connection for V_{OUT_C}'s output buffer. Connecting a 220 pF capacitor between this pin and the V_{OUT_C} pin allows the voltage output to drive up to 1 µF. It should be noted that the addition of this capacitor reduces the bandwidth of the output amplifier, increasing the settling time.
53	AV_{SS}	Negative Analog Supply Pin.
54	I_{OUT_D}	Current Output Pin for DAC Channel D.
55	V_{OUT_D}	Buffered Analog Output Voltage for DAC Channel D.
56	V_{BOOST_D}	Supply for channel D's current output stage (See Figure 15). To use the DC-DC feature of the device, connect as shown in Figure 21.
57	$COMP_{DCDC\_D}$	DC-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of channel D's DC-DC converter.
58	$+V_{SENSE\_D}$	Sense connection for the positive voltage output load connection for V_{OUT_D}. This pin must stay within ±3.0 V of V_{OUT_D} for correct operation.
59	CHARTD	Hart Input Connection for DAC Channel D
60	$COMP_{LV\_D}$	Optional compensation capacitor connection for V_{OUT_D}'s output buffer. Connecting a 220 pF capacitor between this pin and the V_{OUT_D} pin allows the voltage output to drive up to 1 µF. It should be noted that the addition of this capacitor reduces the bandwidth of the output amplifier, increasing the settling time.
61	REFIN	External Reference Voltage Input.
62	REFOUT	Internal Reference Voltage Output.
63	R_{SET_D}	An external, precision, low drift 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_D} temperature drift performance. See the Features section.
64	R_{SET_C}	An external, precision, low drift 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_C} temperature drift performance. See the Features section.
	Exposed PADDLE	CONNECTED TO AVss

TYPICAL PERFORMANCE CHARACTERISTICS

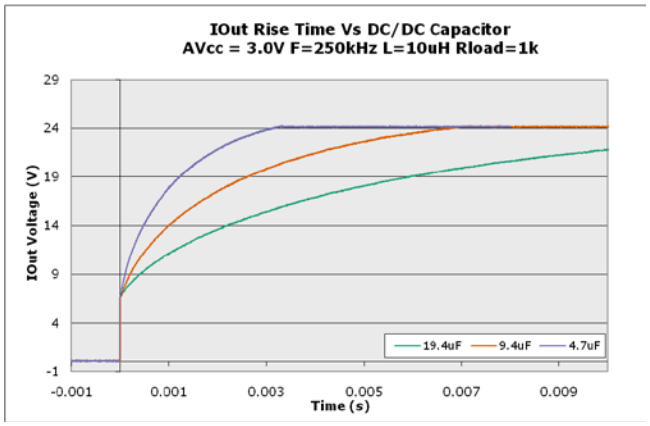


Figure 7. Iout settling 0-24mA though 1kΩ load, AV_{cc}=3.0V, L_{DCDC}=10uH, DCDC frequency=250kHz, C_{DCDC} varied. (See Figure 21)

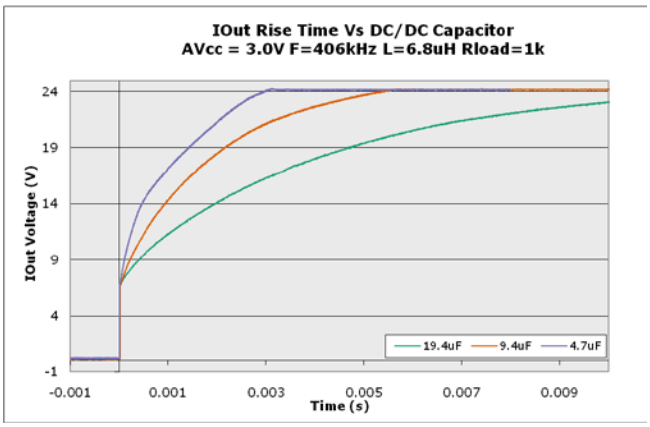


Figure 8. Iout settling 0-24mA though 1kΩ load, AV_{cc}=3.0V, L_{DCDC}=10uH, DCDC frequency=406kHz, C_{DCDC} varied. (See Figure 21)

TBD

Figure 9

TBD

Figure 10.

TBD

Figure 11.

TBD

Figure 12

THEORY OF OPERATION

The AD5755-1 is a quad, precision digital to current loop and voltage output converter designed to meet the requirements of industrial process control applications. It provides a high precision, fully integrated, low cost single-chip solution for generating current loop and unipolar/bipolar voltage outputs. The current ranges available are; 0 to 20mA, 0 to 24mA and 4 to 20mA, the voltage ranges available are; 0 to 5V, ±5V, 0 to 10V and ±10V, the current and voltage outputs are available on separate pins and only one is active at any one time. The desired output configuration is user selectable via the DAC Control Register.

On chip dynamic power control minimizes package power dissipation in current mode.

DAC ARCHITECTURE

The DAC core architecture of the AD5755-1 consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 13. The 4 MSBs of the 16/12-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects 1 of 15 matched resistors to either ground or the reference buffer output. The remaining 12/8 bits of the data-word drive switches S0 to S11 /S7 of a 12/8-bit voltage mode R-2R ladder network.

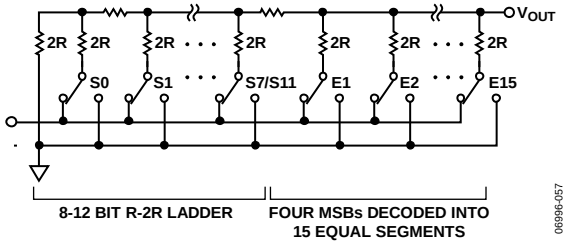


Figure 13. DAC Ladder Structure

The voltage output from the DAC core is either converted to a current (see Figure 15) which is then mirrored to the supply rail so that the application simply sees a current source output with respect to ground or it is buffered and scaled to output a software selectable unipolar or bipolar voltage range (See diagram, Figure 14). The current and voltage are output on separate pins and cannot be output simultaneously. A channels current and voltage output pins may be tied together.

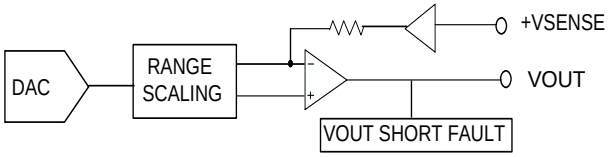


Figure 14. Voltage Output

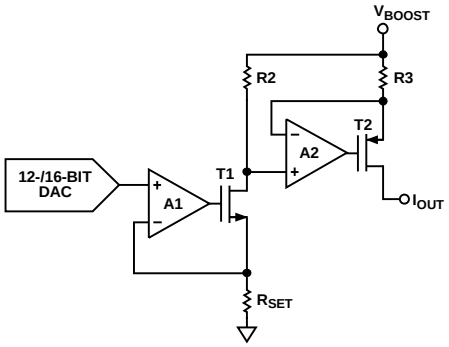


Figure 15. Voltage to Current conversion circuitry

Voltage Output Amplifier

The voltage output amplifier is capable of generating both unipolar and bipolar output voltages. It is capable of driving a load of 1 kΩ in parallel with 2000 pF to AGND. The source and sink capabilities of the output amplifier can be seen in Figure TBD. The slew rate is 1 V/µs with a full-scale settling time of 10 µs.(10V step).

Driving Large Capacitive Loads

The voltage output amplifier is capable of driving capacative loads of up to 1uF with the addition of a non-polarised compensation capacitors on each channel. Care should be taken to choose an appropriate value of compensation capacitor. This capacitor, while allowing the AD5755-1 to drive higher cap loads and reduce overshoot, will increase the settling time of the part and therefore effect the bandwidth of the system. Without the compensation capacitor, up to 20nF capacitive loads can be driven. See pin list for information on connecting compensation capacitors.

Reference Buffers

The AD5755-1 can operate with either an external or internal reference. The reference input has an input range of 4 V to 5 V, 5 V for specified performance. This input voltage is then buffered before it is applied to the DAC.

POWER ON STATE OF AD5755-1

On initial power-up of the AD5755-1 the power-on-reset circuit powers up in a state that is dependent on the POC (Power on Control) pin.

If POC = 0 both the Vout/Iout channels will power up in Tri-state mode.

If POC= 1 the Vout channel will Power up with 30k pull down to Ground, and the IOUT channel will power up to tri-state.

Even though the output ranges are not enabled, the default output range is 0-5V, and the Clear Code Register is loaded with all zeros. This means if the user CLEARS the part after power-up the output will be actively driven to zero volts. (If the channel has been enabled for clear)

SERIAL INTERFACE

The AD5755-1 is controlled over a versatile 3-wire serial interface that operates at clock rates of up to 30 MHz and is compatible with SPI®, QSPI™, MICROWIRE™, and DSP standards. Data coding is always straight binary.

Input Shift Register

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of a serial clock input, SCLK. Data is clocked in on the falling edge of SCLK.

There are two ways in which the DAC outputs can be updated as outlined below.

Individual DAC Updating

In this mode, $\overline{\text{LDAC}}$ is held low while data is being clocked into the DAC Data Register. The addressed DAC output is updated on the rising edge of $\overline{\text{SYNC}}$.

Simultaneous Updating of All DACs

In this mode, $\overline{\text{LDAC}}$ is held high while data is being clocked into the DAC Data Register. Only the first write to each channels data register will be valid after $\overline{\text{LDAC}}$ is brought high. Any subsequent writes while $\overline{\text{LDAC}}$ is still held high will be ignored. All the DAC outputs are updated by taking $\overline{\text{LDAC}}$ low any time after $\overline{\text{SYNC}}$ has been taken high.

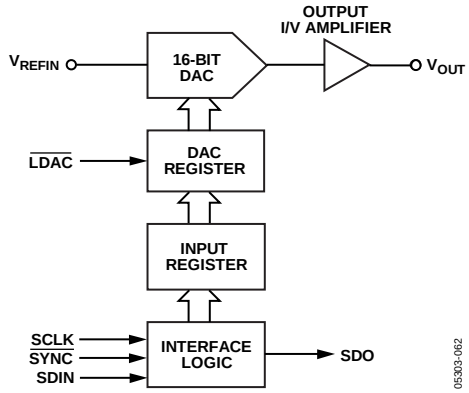


Figure 16. Simplified Serial Interface of Input Loading Circuitryfor One DAC Channel

TRANSFER FUNCTION

Table 10 shows the input code to ideal output voltage relationship for the AD5755-1 or straight binary data coding - ±10v output range shown.

Table 7. Ideal Output Voltage to Input Code Relationship

Digital Input				**Analog Output**
Straight Binary Data Coding				
MSB			**LSB**	**V_{OUT}**
1111	1111	1111	1111	$+2\ V_{REF} \times (32767/32768)$
1111	1111	1111	1110	$+2\ V_{REF} \times (32766/32768)$
1000	0000	0000	0000	0 V
0000	0000	0000	0001	$-2\ V_{REF} \times (32766/32768)$
0000	0000	0000	0000	$-2\ V_{REF} \times (32767/32768)$

REGISTERS

Table 8 below shows an overview of the Registers for the AD5755-1.

Table 8. Data and Control Registers for AD5755-1

DATA REGISTERS	**Description**
DAC Data Register (X4)	Used to write a DAC code to each DAC channel. AD5755-1 Data bits (D15 to D0), There are four DAC Data Registers, one per DAC Channel.
Gain Register (X4)	Used to program gain trim on per channel basis. AD5755-1 Data bits (D15 to D0), There are four Gain Registers, one per DAC channel.
Offset Register (X4)	Used to program offset tro, on per channel basis. AD5755-1 Data bits (D15 to D0), There are four Offset Registers, one per DAC channel.
Clear Code Register (X4)	Used to program Clear Code on per channel basis. AD5755-1 Data bits (D15 to D0), There are four Clear Code Registers, one per DAC channel.
CONTROL REGISTERS	
Main Control Register	Used to Configure the part for main operation. Sets functions such as status readback during write, enable output on all channels simultaneously, power on all DC-DC blocks simultaneously, enables and sets conditions of watchdog timer. See Features Section for more details.
Software Register	Has two functions. Used to perform a reset. Is also used as part of the watchdog timer feature to verify correct data communication operation.
Slew Rate Control Register (X4)	Use to program the slew rate of the output. There are four Slew Rate Control Registers, one per channel.
DAC Control Register (X4)	These registers are used to control the following… 1) Set the output range, e.g. 4-20ma, 0-10v etc.. 2) Set whether Internal/External sense Resistor used 3) Enable/Disable channel for CLEAR.. 4) Enable/Disable Over-range. 5) Enable/Disable output on a per channel basis.. 6) Power on DC-DC on a per channel basis. There are four DAC Control Registers, one per DAC channel.
DC-DC Control Register	Use to set the DC-DC Control parameters. Can control DC-DC max voltage, phase and frequency.
READBACK	
Status Register	

PROGRAMMING SEQUENCE TO WRITE/ENABLE THE OUTPUT CORRECTLY

To correctly write to and set up the part from a power on condition the sequence below should be followed. It is recommended to perform a hardware or software reset after initial power on.

Firstly, the DC-DC supply block needs to be configured. The user should set the DC-DC switching frequency, max output voltage allowed and the phase that the 4 DC-DC channels clock at. Secondly the DAC Control Register should be configured on a per channel basis. The output range is selected, and the DC-DC block is enabled (DC-DC). Other control bits may be configured at this point, however, the output enable bit (OUTEN) and the INT_ENABLE bit should not be set. Next, the user writes the required code to the DAC Data Register. This will implement a full DAC calibration internally. Finally the user writes to the DAC Control Register again to enable the output (set the OUTEN bit). A flow chart of this sequence is shown below.

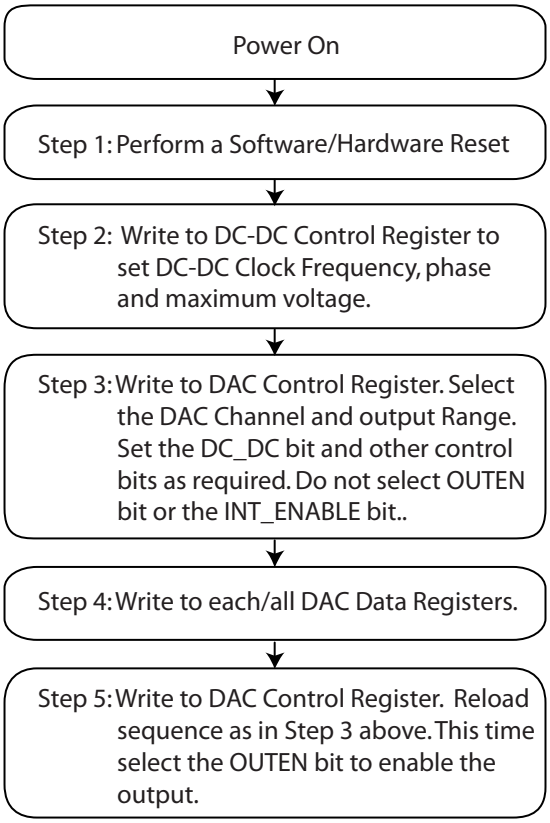


Figure 17. Programming Sequence for Enabling the Output Correctly

CHANGING AND REPROGRAMMING THE RANGE

When changing between ranges the same sequence as above should be used. It is recommended to set the range to its zero point (can be mid-scale or zeroscale) prior to disabling the output. As the DC-DC switching frequency, max voltage and phase have already been selected, there is no need to reprogram this. A flow chart of this sequence is shown below.

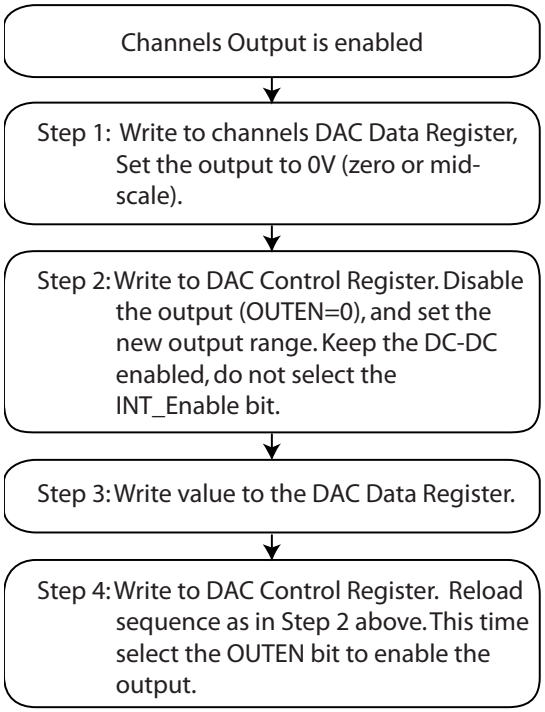


Figure 18. Steps for Changing the Output Range

DATA REGISTERS

The input register is 24 bits wide. When writing to a data register the following format must be used:

Table 9. AD5755-1 Writing to a Data Register

D23	D22	D21	D20	D19	D18	D17	D16	D15 to D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	DREG2	DREG1	DREG0	DAC_AD1	DAC_AD0	

Table 10. AD5755-1 Input Register Decode

Register	Function			
R/$\overline{W}$	Indicates a read from or a write to the addressed register.			
DUT_AD1, DUT_AD0	Used in association with External Pins AD1, AD0 to determine which AD5755-1 device is being addressed by the system controller.			
	DUT_AD1	**DUT_AD0**		**Function**
	0	0		Addresses Part with Pins AD1=0, AD0=0
	0	1		Addresses Part with Pins AD1=0, AD0=1
	1	0		Addresses Part with Pins AD1=1, AD0=0
	1	1		Addresses Part with Pins AD1=1, AD0=1
DREG2, DREG1, DREG0	Selects whether a data register or a control register is written to. If a control register is selected, a further decode of CREG bits is required to select the particular control register, as detailed below.			
	DREG2	**DREG1**	**DREG0**	**Function**
	0	0	0	Write to DAC Data Register (Individual Channel Write)
	0	1	0	Write to Gain Register
	0	1	1	Write to Gain Register (ALL DACS)
	1	0	0	Write to Offset Register
	1	0	1	Write to Offset Register (ALL DACS)
	1	1	0	Write to Clear Code Register
	1	1	1	Write to a Control Register
DAC_AD1, DAC_AD0	These bits are used to decode the DAC channel			
	DAC_AD1	**DAC_AD0**	**DAC Channel/ Register Address**	
	0	0	DAC A	
	0	1	DAC B	
	1	0	DAC C	
	1	1	DAC D	
	X	X	These are don't cares if they are not relevant to the operation being performed.	

DAC DATA REGISTER

Table 11. Programming the AD5755-1 DAC Data Registers

When writing to the AD5755-1 DAC Data Registers D15-D0 are used for DAC DATA bits. See Table x for input register decode.

MSB LSB

D23	D22	D21	D20	D19	D18	D17	D16	D15 to D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	DREG2	DREG1	DREG0	DAC_AD1	DAC_AD0	DATA

GAIN REGISTER

The Gain Register stores the Gain Code (M) which is used in the DAC transfer function to calculated the overall DAC input code (see formula below). The Gain Register is addressed by setting DREG bits to '0,1,0'. The DAC address bits select which DAC channel the gain write is addressed to. It is possible to write the same gain code to all 4 DAC channels at the same time by setting the DREG bits to 011. The AD5755-1 Gain Register is a 16/12 bit register (bits G15.. G0/G3) and allows the user to adjust the gain of each channel in steps of 1 LSB as shown in the Table below. The Gain Register coding is straight binary. In theory the gain can be tuned across the full range of the output. In practice, the maximum recommended gain trim is about 50% of programmed range in order to maintain accuracy.

Table 12. Programming the AD5755-1 Gain Register

R/$\overline{W}$	DUT_ AD1	DUT_ AD0	DREG2	DREG1	DREG0	DAC_ AD1	DAC_ AD0	**D15-D0**
0	DEVICE ADDRESS		010			DAC Channel Address		G15 to G0

Table 13. AD5755-1 Gain Register

Gain Adjustment	**G15**	**G14**	**G13**	**G12 to G4**	**G3**	**G2**	**G1**	**G0**
+65535 LSBs	1	1	1	1	1	1	1	1
+65534 LSBs	1	1	1	1	1	1	0	0
	-	-	-	-	-	-	-	-
1 LSBs	0	0	0	0	0	0	0	1
0 LSBs	0	0	0	0	0	0	0	0

OFFSET REGISTER

The Offset Register is addressed by setting the DREG BITS to DREG2 =1 DREG1=0, DREG0=0. The DAC address bits select with which DAC channel the offset write is addressed to. It is possible to write the same offset code to all 4 DAC channels at the same time by setting the DREG bits to 101. The AD5755-1 offset code is 16/12 bit (bits OF15.. OF0/OF3) and allows the user to adjust the offset of each channel by –32768/8192 LSBs to +32767/8191 LSBs in steps of 1 LSB as shown in the Table below.. The Offset Register coding is straight binary. The default code in the Offset Register is 0x8000/0x800. This will result in zero offset programmed to the output.

Table 14. Programming the AD5755-1 Offset Register

R/$\overline{W}$	DUT_ AD1	DUT_ AD0	DREG2	DREG1	DREG0	DAC_ AD1	DAC_ AD0	D15 to D0
0	DEVICE ADDRESS		100			DAC Channel Address		OF15 to OF0

Table 15. AD5755-1 Offset Register options

Offset Adjustment	**OF15**	**OF14**	**OF13**	**OF12 to OF4**	**OF3**	**OF2**	**OF1**	**OF0**
+32768 LSBs	1	1	1	1	1	1	1	1
+32767 LSBs	1	1	1	1	1	1	0	0
	-	-	-	-	-	-	-	-
No Adjustment (default)	1	0	0	0	0	0	0	0
	-	-	-	-	-	-	-	-
–32767 LSBs	0	0	0	0	0	0	0	0
–32768 LSBs	0	0	0	0	0	0	0	0

CLEAR CODE REGISTER

There is a per channel Clear Code Register. The Clear Code Register is 16 bits wide and is addressed by setting the DREG bits to'1,1,0'. It is also possible, via software, to enable/disable on a per channel basis which channels will be cleared when the CLEAR pin is activated. The default clear code is all 0's. See Features section for more information.

Table 16. Programming AD5755-1 Clear Code Register

D23	D22	D21	D20	D19	D18	D17	D16	D15 to D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	DREG2	DREG1	DREG0	DAC_AD1	DAC_AD0	CLEAR CODE
0	DEVICE ADDRESS		110			DAC Channel Address		DATA

CONTROL REGISTERS

When writing to a data register the following format must be used:

Table 17. Writing to a control register

MSB LSB

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12to D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	1	1	1	DAC_AD1	DAC_AD0	CREG2	CREG1	CREG0	

See Table 10 for configuration on bits D23 to D16. The control registers are addressed by setting the DREG bits to DREG2 = 1, DREG1 = 1, DREG0=1 and then setting the CREG2, CREG1 and CREG0 bits to the appropriate decode address for that register as per **Table 18** below. These CREG bits select between the various control registers.

Table 18. Register Access Decode

CREG2, (D15)	CREG1, (D14)	CREG0, (D13)	
0	0	0	Slew Rate Control Register (one per channel)
0	0	1	Main Control Register
0	1	0	DAC Control Register (one per channel)
0	1	1	DC-DC Control Register
1	0	0	Software Register (one per channel)

MAIN CONTROL REGISTER

CREG2, CREG1, CREG0 are set to '0,0,1' to select the Main Control Register. The Main Control Register options are shown below.

Table 19. Programming the Main Control Register

MSB **LSB**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3 to D0
0	0	1	POC	STATREAD	EWD	WD1	WD0	X	ShtCctLim	OUTEN ALL	DC-DC ALL	X

Table 20. Main Control Register Functions.

Option	Description
STATREAD	Enable status readback during a write. See Features section. STATREAD =1, Enable STATREAD =0, Disable
POC	The POC bit decides the state of the VOUT channel during normal operation. It's default value is 0. POC Bit = 0. The output will go to the value set by the POC pin when the current out channel is enabled. POC Bit = 1. The output will go to the opposite value of the POC pin if the channels I_{out} is enabled.
OUTEN ALL	Enables the output on all 4 DAC simultaneously. Do not use the OUTEN ALL bit when using the OUTEN bit in the DAC Control Registers.
DC_DCALL	When set, Powers up the DC-DC on all 4 channels Simultaneously. To Power down the DC-DCs all channels outputs must first be disabled. Do not use the DC_DCALL bit when using the DC_DC bit in the DAC Control Registers.
ShtCctLim	Programmable Short Circuit Limit on V_{out} pin in the event of a short circuit condition. 0=15ma 1=8ma
EWD	Enable Watchdog Timer. See features section for more information. EWD=1, Enable Watchdog EWD=0, Disable Watchdog
WD1, WD0	Timeout Select Bits. Used to select timeout period for watchdog timer. WD1 | WD0 | 0 | 0 | 5ms 0 | 1 | 10ms 1 | 0 | 100ms 1 | 1 | 200ms

DAC CONTROL REGISTER

The DAC Control Register is used to configure each DAC Channel. The DAC Control Register is selected by setting bits CREG2, CREG1, CREG0 to 0,1,0.

Table 21. Programming DAC Control Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	X	X	X	X	INT_ENABLE	CLR_EN	OUTEN	RSET	DC-DC	OVRNG	R2	R1	R0

Table 22. DAC Control Register Functions

Option	Description
RSET	Selects internal or external current sense resistor for selected DAC channel RSET = 0 Selects external Resistor RSET = 1 Selects Internal Resistor
R2,R1,R0	Selects output range enabled.

R2	R1	R0	Output Range Selected
0	0	0	0 to 5V Voltage Range
0	0	1	0 to 10V Voltage Range
0	1	0	±5V Voltage Range
0	1	1	±10V Voltage Range
1	0	0	4 to 20 mA Current Range
1	0	1	0 to 20 mA Current Range
1	1	0	0 to 24 mA Current Range

OVRNG	Enables 20% overrange on Vout Channel only. No current overrange available. OVRNG=1, Enabled OVRNG=0, Disabled
INT_ENABLE	Powers up the DC-DC, DAC and internal amplifiers for the selected channel. Does not enable the output. Can only be done on a per channel basis.
CLR_EN	Per channel Clear Enable bit. Selects if this channel will clear when the CLEAR pin is activated. CLR_EN=1, channel will clear when part is cleared. CLR_EN=0, channel will not clear when part is cleared.
OUTEN	Enables/Disables the selected output channel OUTEN=1, Enables channel OUTEN=0, Disable channel
DC_DC	Powers the DC-DC on selected channel. DC_DC = 1, Power up DC_DC DC_DC = 0, Power down DC_DC This allows per channel DC_DC power up/down. To power down the DCDC, OUTEN and INT_ENABLE bits must also be set to 0. All DC-DCs can also be powered up simultaneously using DCDC_All bit in the Main Control Register.

SOFTWARE REGISTER

The Software Register has three functions. It allows the user to perform a software reset to the part. It can be used to set bit D11 in the Status Register. Lastly it is also used as part of the watchdog feature to ensure that the SPI interface connections are working properly. To ensure all the datapath lines are working properly (i.e. SDI/SCLK/SYNC), the user must write 0x195 to the Software Register within the timeout period. If this command is not received within the timeout period, the ALERT pin will signal a fault condition. Note. This is only required when the Watchdog Timer function is enabled.

Table 23. Programming the Software Register

To program a software reset you need to write 1,0,0 to CREG2, CREG1, CREG0.

MSB **LSB**

D15	D14	D13	D12	D11 to D0
1	0	0	User Program Bit	RESET CODE/SPI CODE

Table 24. Software Register Functions

User Program Bit	This bit is mapped to bit D11 of the Status Register. When this bit is set to 1 bit D11 of the Status Register is set to 1. Likewise when D12 is set to 0 bit D11 of the Status Register is also set to zero. This feature can be used to ensure the SPI pins are working correctly by writing known bit to this register and reading back corresponding bit from the Status Register.	
RESET CODE/SPI CODE	**Option**	**Description**
	RESET CODE	Writing 0x555 to D11-D0 performs a reset.
	SPI CODE	If Watchdog Timer feature enabled, 0x195 must be written to the Software Register (D11-D0) within every timeout period to ensure valid data communication path.

DC-DC CONTROL REGISTER

The DC-DC Control Register allows the user control over the DC-DC Switching Frequency, and of the phase of when the per channel switching starts. The maximum allowable DC-DC output frequency is also programmable.

Table 25. Programming the DC-DC Control Register

MSB						LSB
D15	**D14**	**D13**	**D12 to D7**	**D5 to D4**	**D3 to D2**	**D1 to D0**
0	1	1	X	DC-DC Phase	DC-DC Freq	DC-DC MaxV

Table 26. DC-DC Control Register Options

Option	**Description**
DC-DCMaxV	Maximum allowed output Voltage of the DC-DC 00 = 25V ±1V 01 = 27.3 ±1V 10 = 28.6 ±1V 11 = 30 ±1V
DC-DC Freq	User Programmable DC-DC Switching Frequency: 00 = 250 Khz 01 = 406 Khz 10 = 649 Khz 11 = 812 Khz
DC-DC Phase	User Programmable DC-DC Phase (Between Channels) 00 = All DC-DCs clock on same edge 01 = ChanA, ChanB clock on same edge, ChanC & ChanD clock on opposite edge 10 = ChanA, ChanC clock on same edge, ChanB & ChanD on opposite edge 11 = ChanA,ChanB,ChanC, ChanD clock 90' out of phase from each other

SLEW RATE CONTROL REGISTER

This register is used to program the slew rate control for the selected DAC Channel. The CREG bits are set to '0,0,0' to select the Slew Rate Control Register. SR_CLOCK and SR_STEP allow the user to control the rate of the output SLEW. This feature is available on both the current and voltage outputs. With the slew rate control feature disabled the output value will change at a rate limited by the output drive circuitry and the attached load. **SE** enables output slew rate control. It can be both programmed and enabled/disabled on a per channel basis. For more information see the features section.

Table 27. Programming the Slew Rate Control Register

D15	D14	D13	D12	D11-D7	D6 to D3	D2 to D0
0	0	0	SE	X	SR_CLOCK	SR_STEP

READBACK OPERATION

Readback mode is invoked by setting the R/$\overline{W}$ bit = 1 in the serial input register write. With R/$\overline{W}$ = 1, bits DUT_AD1, DUT_AD0, in association with bits RD4, RD3, RD2, RD1, RD0 (See Table 29), select the register to be read. The remaining data bits in the write sequence are don't care. During the next SPI transfer, the data appearing on the SDO output contains the data from the previously addressed register. The readback diagram in Figure 3 shows the readback sequence.

Table 28. Input Shift Register Contents for a read operation

D23	D22	D21	D20	D19	D18	D17	D16	D15 to D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	RD4	RD3	RD2	RD1	RD0	X

Table 29. Read Address Decoding

RD4	RD3	RD2	RD1	RD0	Function
0	0	0	0	0	Read DACA Data Register
0	0	0	0	1	Read DACB Data Register
0	0	0	1	0	Read DACC Data Register
0	0	0	1	1	Read DACD Data Register
0	0	1	0	0	Read Control Register DAC A
0	0	1	0	1	Read Control Register DAC B
0	0	1	1	0	Read Control Register DAC C
0	0	1	1	1	Read Control Register DAC D
0	1	0	0	0	Read Gain Register A
0	1	0	0	1	Read Gain Register B
0	1	0	1	0	Read Gain Register C
0	1	0	1	1	Read Gain Register D
0	1	1	0	0	Read Offset Register A
0	1	1	0	1	Read Offset Register B
0	1	1	1	0	Read Offset Register C
0	1	1	1	1	Read Offset Register D
1	0	0	0	0	Clear Code Register DAC A
1	0	0	0	1	Clear Code Register DAC B
1	0	0	1	0	Clear Code Register DAC C
1	0	0	1	1	Clear Code Register DAC D
1	0	1	0	0	Slew Rate Control Register DAC A
1	0	1	0	1	Slew Rate Control Register DAC B
1	0	1	1	0	Slew Rate Control Register DAC C
1	0	1	1	1	Slew Rate Control Register DAC D
1	1	0	0	0	Read Status Register
1	1	0	0	1	Read Main Control Register
1	1	0	1	0	Read DC-DC Control Register

Read Back Example

To read back the Gain Register of Device #1 Channel A on the AD5755-1, the following sequence should be implemented:

1. Write 0xA80000 to the AD5755-1 input register. This configures the AD5755-1 device address #1 for read mode with the Gain Register of channel A selected.. Note that all the data bits, D15 to D0, are don't care.
2. Follow this with any read/write command. During this command, the data from the selected Gain Register is clocked out on the SDO line.

STATUS REGISTER

The Status Register is a read only register. This register contains any fault information as a well as a RAMP ACTIVE bit and a User Toggle Bit. By setting the STATREAD bit in the Main Control Register, the Status Register contents can be readback on the SDO pin during every write sequence.

Table 30. Decoding the Status Register

MSB **LSB**

D15 to D12	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	DC-DCD	DC-DCC	DC-DCB	DC-DCA	User Toggle Bit	PEC ERROR	RAMP ACTIVE	OVER TEMP	SHORT CCT VD	SHORT CCT VC	SHORT CCT VB	SHORT CCT VA	OPEN CCT ID	OPEN CCT IC	OPEN CCT IB	OPEN CCT IA

Table 31. Status Register Options

Option	Description
OPEN CCT IA	This bit will be set if a fault is detected on DACA I_{OUT} pin.
OPEN CCT IB	This bit will be set if a fault is detected on DACB I_{OUT} pin.
OPEN CCT IC	This bit will be set if a fault is detected on DACC I_{OUT} pin.
OPEN CCT ID	This bit will be set if a fault is detected on DACD I_{OUT} pin.
SHORT CCT VA	This bit will be set if a fault is detected on DACA V_{OUT} pin.
SHORT CCT VB	This bit will be set if a fault is detected on DACB V_{OUT} pin.
SHORT CCT VC	This bit will be set if a fault is detected on DACC V_{OUT} pin.
SHORT CCT VD	This bit will be set if a fault is detected on DACD V_{OUT} pin.
RAMP ACTIVE	This bit will be set while any one of the output channels are slewing (slew rate control enabled on at least one channel)
OVER TEMP	This bit will be set if the AD5755-1 core temperature exceeds approx. 150°C.
PEC ERROR	Denotes a PEC Error on the SPI Interface Transmit.
DC-DC A	DC-DC Failure on Channel A. This fault indicates that the DCDC is not operating, for example if the boost inductor is not connected.
DC-DCB	DC-DC Failure on Channel B. This fault indicates that the DCDC is not operating, for example if the boost inductor is not connected.
DC-DCC	DC-DC Failure on Channel C. This fault indicates that the DCDC is not operating, for example if the boost inductor is not connected.
DC-DCD	DC-DC Failure on Channel D. This fault indicates that the DCDC is not operating, for example if the boost inductor is not connected.
User Toggle Bit	User Writable bit that the user can set and readback while doing a Status Register read. This can be used to verify data communications if needed.

FEATURES

OUTPUT FAULT

The AD5755-1 is equipped with a $\overline{\text{FAULT}}$ pin, this is an active low open-drain output allowing several AD5755-1 devices to be connected together to one pull-up resistor for global fault detection. The $\overline{\text{FAULT}}$ pin is forced active by any one of the following fault scenarios;

1) The Voltage at I_{OUT} attempts to rise above the compliance range, due to an open-loop circuit or insufficient power supply voltage. The internal circuitry that develops the fault output avoids using a comparator with "window limits" since this would require an actual output error before the $\overline{\text{FAULT}}$ output becomes active. Instead, the signal is generated when the internal amplifier in the output stage has less than approximately one volt of remaining drive capability. Thus the $\overline{\text{FAULT}}$ output activates slightly before the compliance limit is reached. Since the comparison is made within the feedback loop of the output amplifier, the output accuracy is maintained by its open-loop gain and an output error does not occur before the $\overline{\text{FAULT}}$ output becomes active.
2) A short is detected on the voltage output pin. Short circuit current limited to 15ma or 8ma, this is programmable by the user.
3) An interface error is detected due to a PEC failure. See Packet Error Checking section.
4) If the core temperature of the AD5755-1 exceeds approx. 150°C.

The OPEN CCT and OVER TEMP bits of the Status Register are used in conjunction with the $\overline{\text{FAULT}}$ output to inform the user which one of the fault conditions caused the $\overline{\text{FAULT}}$ output to be activated.

VOLTAGE OUTPUT SHORT CIRCUIT PROTECTION

Under normal operation the voltage output will sink/source up to 10mA and maintain specified operation. The maximum current that the voltage output will deliver is 15mA, this is the short circuit current. This short circuit current is programmable by the user and can be set to 15mA or 8mA. If a short circuit is detected the $\overline{\text{FAULT}}$ will go low and the relevant SHORT CCT bit in the Status register will be set.

DIGITAL OFFSET AND GAIN CONTROL

Each DAC channel has a gain (M) and offset (C) register, which allow trimming out of the gain and offset errors of the entire signal chain. Data from the DAC Data Register is operated on by a digital multiplier and adder controlled by the contents of the M and C registers. The calibrated DAC data is then stored in the DAC2 register.

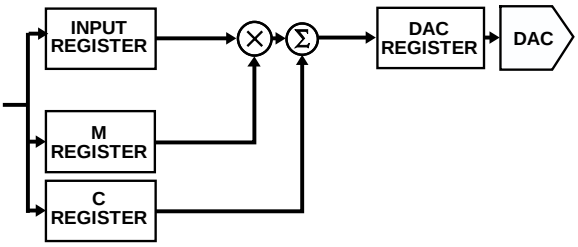


Figure 19. Digital Offset and Gain control

Although this diagram indicates a multiplier and adder for each channel, there is only one multiplier and one adder in the device, and they are shared among all 4 channels. This has implications for the update speed when several channels are updated at once.

Each time data is written to the M or C register the output is not automatically updated. Rather, the next write to the DAC channel will use these M&C values to perform a new calibration and automatically update the channel.

Data output from the DAC2 register is routed to the final DAC register by a multiplexer. Both the Gain Register and the Offset Register have 16 bits of resolution. The correct method to calibrate the gain/offset is firstly to calibrate out the gain and then calibrate the offset.

The value (in decimal) that is written to the DAC register can be calculated by:

$$Code_{DAC\ Register} = D \times \frac{(M+1)}{2^{16}} + C - 2^{15}$$

where:
D is the code loaded to the DAC channels input register.

M is the code in Gain Register – default code = $2^{16} - 1$

C is the code in Offset Register – default code = 2^{15}

STATUS READBACK DURING WRITE

The AD5755-1 has the ability to read back the Status Register contents during every write sequence. This feature is enabled via the STATREAD bit in the Main Control Register. This allows the user to continuously monitor the Status Register and act quickly in the case of a fault.

When Status Readback During Write is enabled the contents of the 16bit Status register (See Table 31) is outputted on the SDO pin as indicated in Figure 4.

The AD5755-1 will power up with this feature disabled. When this is enabled the normal readback feature is not available, except of the status register. To readback any other register set STATREAD low first before following the readback sequence. STATREAD may be set high again after the register read.

ASYNCHRONOUS CLEAR

CLEAR is an active high edge sensitive input that allows the output to be cleared to a pre programmed 16 bit code. This code is user programmable via a per-channel 16 bit Clear Code Register.

In order for a channel to clear, that channel must be enabled to be cleared via the CLR_EN bit in the channels DAC Control Register. If the channel is not enabled to be cleared then the output will remain in its current state independent of the CLEAR pin level.

When the CLEAR signal is returned low, the relevant outputs remains cleared until a new value is programmed.

PACKET ERROR CHECKING

To verify that data has been received correctly in noisy environments, the AD5755-1 offers the option of packet error checking based on an 8-bit (CRC-8) cyclic redundancy check. The device controlling the AD5755-1 should generate an 8-frame check sequence using the polynomial

$$C(x) = x_8 + x_2 + x_1 + 1$$

This is added to the end of the data word, and 32 bits are sent to the AD5755-1 before taking $\overline{\text{SYNC}}$ high. If the AD5755-1 sees a 32-bit frame, it will perform the error check when $\overline{\text{SYNC}}$ goes high. If the check is valid, then the data will be written to the selected register. If the error check fails, the $\overline{\text{FAULT}}$ pin will go low and the PEC ERROR bit in the Status Register will be set. After reading the Status Register, $\overline{\text{FAULT}}$ will return high (assuming there are no other faults) and the PEC ERROR bit will be cleared automatically.

The PEC can be used for both transmit and receive of data packets. If Status Readback During Write is enabled, the 'PEC' values returned during the Status Readback During Write should be ignored. All other PEC values will be valid though and the user can still use the normal readback operation to monitor Status Register activity.with PEC.

WATCHDOG TIMER

If enabled, an on chip watchdog timer will generate an alert signal if 0x195 has not been written to the Software Register within the programmed timeout period. This feature is useful to ensure communication has not been lost between the MCU and the AD5755-1 and that these datapath lines are working properly (i.e. SDI/SCLK/SYNC). If 0x195 is not received by the Software Register within the timeout period, the ALERT pin will signal a fault condition. The ALERT signal is active high and can be connected directly to the CLEAR pin to enable a CLEAR in the event that data communications are lost from the MCU.

The watchdog timer is enabled and the timeout period (50,100,150 or 200ms) set in the control register (See Table 19).

OUTPUT ALERT

The AD5755-1 is equipped with a ALERT pin, this is An active high CMOS output. The AD5755-1 has an internal watchdog timer. If enabled, it will monitor SPI communications. If 0x195 is not received by the Software Register within the timeout period, the ALERT pin will go active.

INTERNAL REFERENCE

The AD5755-1 contains an integrated +5V voltage reference with initial accuracy of ±2mV max and a temperature drift coefficient of ±5 ppm max. The reference voltage is buffered and externally available for use elsewhere within the system.

EXTERNAL CURRENT SETTING RESISTOR

Referring toFigure 15, R1 is an internal sense resistor as part of the voltage to current conversion circuitry. The stability of the output current value over temperature is dependent on the stability of the value of R1. As a method of improving the stability of the output current over temperature an external 15kΩ low drift resistor can be connected to the R_{SET} pin of the AD5755-1 to be used instead of the internal resistor R1. The external resistor is selected via the DAC Control register. See Table 21.

HART

The AD5755-1 has 4 CHART pins, one corresponding to each output channels. A HART signal can be coupled into these pins. The HART signal will appear on the corresponding current output, if the output is enables. Table 32 below shows the recommended input voltages for the HART signal at the CHART pin. If these voltages are used the current output should meet the HART amplitude specifications. Figure 20 is the recommended circuit for attenuating and coupling in the HART signal.

Table 32. CHART input voltage to HART output current

	CHART input voltage	Current output (HART)
Internal Rset	150mVp-p	1mAp-p
External Rset	170mVp-p	1mAp-p

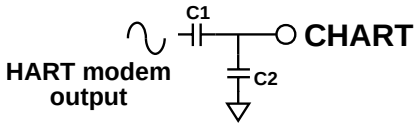


Figure 20. Coupling HART signal

A minimum capacitance of C1+C2 will be required to ensure that the 1.2kHz and 2.2kHz "HART frequencies" are not significantly attenuated at the output. This will be in the order of 10's of nF's.

Digitally controlling the slew rate of the output is necessary to meet the analog rate of change requirements for HART.

SLEW RATE CONTROL

The Slew Rate Control feature of the AD5755-1 allows the user to control the rate at which the output value changes. This feature is available on both the current and voltage outputs. With the slew rate control feature disabled the output value will change at a rate limited by the output drive circuitry and the attached load. If the user wishes to reduce the slew rate this can be achieved by enabling the slew rate control feature. With the feature enabled via the SREN bit of the Slew Rate Control Register, (See Table 27) the output, instead of slewing directly between two values, will step digitally at a rate defined by two parameters accessible via the Slew Rate Control Register as shown in Table 27. The parameters are SR_CLOCK and SR_STEP. SR_CLOCK defines the rate at which the digital slew will be updated, e.g. if the selected update rate is 8KHz the output will update every 125µs, in conjunction with this the SR_STEP defines by how much the output value will change at each update. Together both parameters define the rate of change of the output value. Table 33 and Table 34 outline the range of values for both the SR_CLOCK and SR_STEP parameters.

Table 33. Slew Rate Update Clock Options

SR_CLOCK	Update Clock Frequency (Hz)*
0000	64K
0001	32K
0010	16K
0011	8k
0100	4k
0101	2k
0110	1k
0111	500
1000	250
1001	125
1010	64
1011	32
1100	16
1101	8
1110	4
1111	0.5Hz

*Clock Frequencies accurate to ±TDB%.

Table 34. Slew_Rate Step Size Options

SR_STEP	AD5755-1 **(16 BIT) Step Size (LSBs)**
000	1
001	2
010	4
011	16
100	32
101	64
110	128
111	256

The following equation describes the slew rate as a function of the step size, the update clock frequency and the LSB size.

$$Slew\ Time = \frac{Output\ Change}{Step\ Size \times Update\ Clock\ Frequency \times LSB\ Size}$$

Where:

Slew Time is expressed in seconds
Output Change is expressed in Amps for I_{OUT} or Volts for V_{OUT}
When the slew rate control feature is enabled, all output changes will change at the programmed slew rate, for example if the CLEAR pin is asserted the output will slew to the clear value at the programmed slew rate (assuming that Clear channel is enabled to be cleared). The update clock frequency for any given value will be the same for all output ranges, the step size however will vary across output ranges for a given value of step size as the LSB size will be different for each output range.

POWER DISSIPATION CONTROL

The AD5755-1 contains integrated dynamic power control using a DC-DC boost circuiot allowing reductions in power consumption from standard designs when using the part in current output mode.

In standard current input module designs the load resistor values can range from typically 50 ohm to 750 ohm. Output module systems must source enough voltage to meet the compliance voltage requirement across the full range of load resistor values. For example, in a 4-20ma loop when driving 20ma a compliance voltage of >15V is required. When driving 20ma into a 50 ohm load only 1V compliance is required.

The AD5755-1 circuitry senses the output voltage and regulates this voltage to meet compliance requirements plus a small headroom voltage.

DC-DC CONVERTERS

The AD5755-1 contains 4 independent DCDC converters. These are used to provide dynamic control of the V_{boost} supply voltage for each channel (See Figure 15). Figure 21 below shows the discreet components needed for the DCDC circuitry and

the following sections describe component selection for this circuitry.

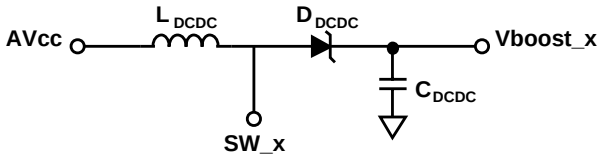


Figure 21. DC-DC Circuit

DC-DC Operation

The on-board DC-DC converters use a constant frequency, peak current mode control scheme to step-up an AV_{cc} input in the range 2.7 to 5.5v to drive the AD5755-1 output channel. These are designed to operate in discontinuous conduction mode (DCM) with a duty cycle < 85%. Discontinuous conduction mode refers to a mode of operation where the inductor current goes to zero for an appreciable % of the switching cycle. The DCDC converters are non synchronous i.e. they require an external schottky diode.

DC-DC Output Voltage

When a channel current output is enabled the converter regulates the V_{boost} supply to 7.5V or (Iout*Rload+2V), whichever is greater. The maximum V_{boost} voltage is set in the DC-DC Control Register (25, 27.3, 28.6 or 30V. See Table 26).

In voltage output mode, or in current output mode with the output disabled, the converter regulates the V_{boost} supply to +15v (±8%).

Within a channel the Vout & Iout stages share a common V_{boost} supply so that the outputs of the Iout & Vout stages can be tied together.

DC-DC On-Board Switch

The AD5755-1 contains a 0.5ohm internal switch . The switch current is monitored on a pulse by pulse basis & is limited to 0.8A peak current.

DC-DC Switching Frequency and Phase

The AD5755-1 DCDC switching frequency can be selected from the DCDC Control Register to be 250Khz, 400Khz, 649kHz or 812kHz. The phasing of the channels can also be adjusted so that the DCDCs can clock on different edges (See Table 26). For typical applications a 250Khz frequency is recommended. At light loads (low output current & small load resistor) the DCDC enters a pulse skipping mode to minimize switching power dissipation.

DC-DC Inductor Selection

For typical 4-20mA applications a 10uH inductor combined with a switching frequency of 250Khz will allow up to 24mA to be driven into a load resistance of up to 1kΩ with an AV_{cc} supply from 2.7 to 5.5v. The inductor must be able to handle the peak current without saturating at the maximum ambient temperature.

If an alternative Inductor/Switching frequency is preferred then one must ensure that the DCDC continues to operates in DCM mode and that the inductor current is less than 0.8A.

$$\frac{2\times I_{OUT\max}(V_{OUT\max}-V_{CC\min})}{I_{PEAK\max}{}^{2}\times F_{SW}}$$

$$< L < \frac{V_{IN\min}{}^{2}(V_{OUT\max}-V_{IN\min})\times\eta}{2\times I_{OUT\max}\times V_{OUT\max}{}^{2}\times F_{SW}}$$

Where:

$I_{PEAK\,max}$=Maximum Peak Current (0.8A limit)

F_{SW}=Switching Frequency set in the DCDC Control Register.

η = efficiency (Assume = 0.8)

DC-DC External schottky selection

The AD5755-1 requires an external schottky for correct operation. Ensure the schottky is rated to handle the the maximum reverse breakdown expected in operation & that the rectifier maximum junction temperature is not exceeded. The diode average current = Iload current.

DC-DC Compensation Capacitors

As the DCDC operates in DCM the uncompensated transfer function is essentially a single pole transfer function. The pole frequency is determined by Cout, Vin, Vout & Iload. The AD5755-1 uses an external capacitor in conjunction with an internal 150k resistor to compensate the regulator loop. For typical 4-20mA applications connect a 10nF capacitor from each of the $COMP_{DCDC\_A/\_B/\_C/\_D}$ pins to GND.

DC-DC Input and Output Capacitor Selection

The output capacitor effects ripple voltage of the DCDC converter & also indirectly limits the maximum slew rate at which the channel output current can rise. The ripple voltage is caused by a combination of the capacitance & ESR (equivalent series resistance) of the capacitor. For the AD5755-1 a ceramic capacitor of 4.7µF is recommended for typical applications. Larger capacitors or paralled capacitors will improve the ripple at the expense of reduced slew rate.

The input capacitor will provide much of the dynamic current required for the DCDC converter & should also be a low ESR component. For the AD5755-1 a ceramic capacitor of 10µF is recommended for typical applications. Ceramic capacitors must be chosen carefully as they can exhibit a large sensitivity to DC bias voltages & temperature. X5R or X7R dielectrics are preferred as these capacitors remain stable over wider operating voltage & temperature ranges.

Iout Slew Rate when using the DC-DC

When the AD5755-1 is configured in Iout mode & a step increase in output current is programmed then the DCDC converter must increase its output voltage so that Vboost ≈ Iout*Rload+2v. This requires that the output capacitor of the DCDC circuit must also be charge to the new voltage. The amount of power required to do this is 0.5*C*(Vnew-Vold). Figure 7. And Figure 8.show Iout settling for a 0 to 24mA step into a 1kohm load for different caps & inductor/switching frequency.

APPLICATIONS INFORMATION

PRECISION VOLTAGE REFERENCE SELECTION

To achieve the optimum performance from the AD5755-1 over its full operating temperature range, a precision voltage reference must be used. Thought should be given to the selection of a precision voltage reference. The voltage applied to the reference inpus is used to provide a buffered reference for the DAC cores. Therefore, any error in the voltage reference is reflected in the outputs of the device.

There are four possible sources of error to consider when choosing a voltage reference for high accuracy applications: initial accuracy, temperature coefficient of the output voltage, long term drift, and output voltage noise.

Initial accuracy error on the output voltage of an external reference could lead to a full-scale error in the DAC. Therefore, to minimize these errors, a reference with low initial accuracy error specification is preferred. Choosing a reference with an output trim adjustment, such as the ADR425, allows a system designer to trim system errors out by setting the reference voltage to a voltage other than the nominal. The trim adjustment can also be used at temperature to trim out any error.

Long-term drift is a measure of how much the reference output voltage drifts over time. A reference with a tight long-term drift specification ensures that the overall solution remains relatively stable over its entire lifetime.

The temperature coefficient of a reference's output voltage affects INL, DNL, and TUE. A reference with a tight temperature coefficient specification should be chosen to reduce the dependence of the DAC output voltage on ambient conditions.

In high accuracy applications, which have a relatively low noise budget, reference output voltage noise needs to be considered. Choosing a reference with as low an output noise voltage as practical for the system resolution required is important. Precision voltage references such as the ADR435 (XFET design) produce low output noise in the 0.1 Hz to 10 Hz region. However, as the circuit bandwidth increases, filtering the output of the reference may be required to minimize the output noise.

Table 35. Some Recommended Precision References

Part No.	Initial Accuracy (mV Max)	Long-Term Drift (ppm Typ)	Temp Drift (ppm/°C Max)	0.1 Hz to 10 Hz Noise (µV p-p Typ)
ADR435	±6	30	3	3.4
ADR425	±6	50	3	3.4
ADR02	±5	50	3	15
ADR395	±6	50	25	5
AD586	±2.5	15	10	4

DRIVING INDUCTIVE LOADS

When driving inductive or poorly defined loads connect a 0.01µF capacitor between I_{OUT} and GND. This will ensure stability with loads beyond 50mH. There is no maximum capacitance limit. The capacitive component of the load may cause slower settling, though this may be masked by the settling time of the AD5755-1.

TRANSIENT VOLTAGE PROTECTION

The AD5755-1 contains ESD protection diodes which prevent damage from normal handling. The industrial control environment can, however, subject I/O circuits to much higher transients. In order to protect the AD5755-1 from excessively high voltag etransients , external power diodes and a surge current limiting resistor may be required, as shown in Figure 22. The constraint on the resistor value is that during normal operation the output level at IOUT must remain within its voltage compliance limit of $AV_{DD} - 2.5V$ and the two protection diodes and resistor must have appropriate power ratings.

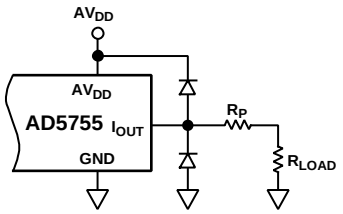


Figure 22. Output Transient Voltage Protection

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5755-1 is via a serial bus that uses a protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire minimum interface consisting of a clock signal, a data signal, and a latch signal. The AD5755-1 require a 24-bit data-word with data valid on the falling edge of SCLK.

The DAC output update is initiated on either the rising edge of LDAC or, if LDAC is held low, on the rising edge of SYNC. The contents of the registers can be read using the readback function.

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5755-1 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5755-1 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device.

The AD5755-1 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI) such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD5755-1 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near the reference inputs. A ground line routed between the SDIN and SCLK lines helps reduce crosstalk between them (not required on a multilayer board that has a separate ground plane, but separating the lines helps). It is essential to minimize noise on the REFIN line because it couples through to the DAC output.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feed through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane, while signal traces are placed on the solder side.

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that might occur. Isocouplers provide voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5755-1 makes it ideal for isolated interfaces, because the number of interface lines is kept to a minimum. Figure 23 shows a 4-channel isolated interface to the AD5755-1 using an ADuM1400. For more information, go to www.analog.com.

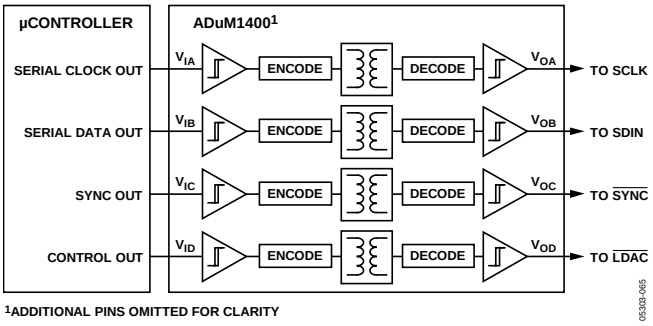
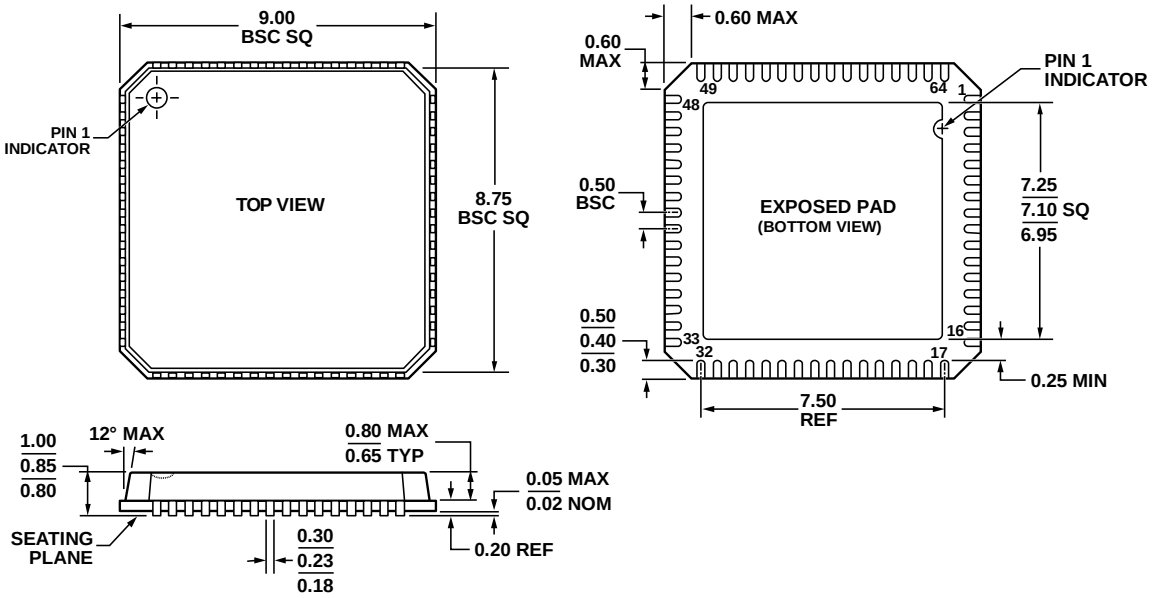


Figure 23. Isolated Interface

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4

Figure 24. 64-Lead Frame Chip Scale Package, 9x9 Quad. [LFCSP]

Dimensions shown in millimeters

ORDERING GUIDE

Model	Resolution	Temperature Range	Package Description	Package Option
AD5755-1x	16bit	–40°C to +105°C	64-lead LFCSP	CP-64-3