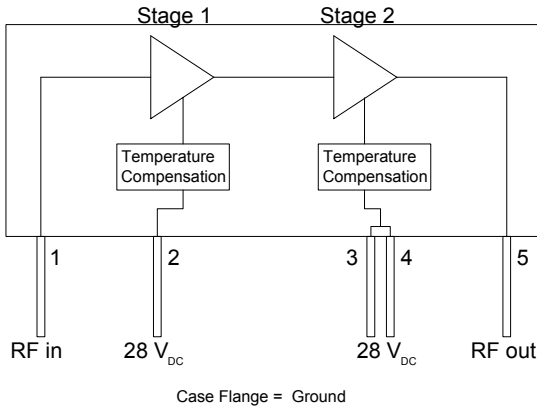




Product Description

The **XD010-35S-D2F** 10W power module is a 2-stage Class A/AB RF amplifier module for use in the driver stages of WCDMA power amplifiers. The power transistors are fabricated using Sirenza's latest, high performance LDMOS II process. The unit operates from a single voltage and has internal temperature compensation of the bias voltage to ensure stable performance over the full temperature range.

Functional Block Diagram



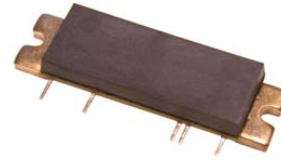
Key Specifications

Parameter	Description: Test Conditions $Z_{in} = Z_{out} = 50\Omega$, $V_{DD} = 28.0V$, $I_{DD1} = 240mA$, $I_{DD2} = 150mA$, $T_{Flange} = 25^{\circ}C$	Unit	Min.	Typ.	Max.
Frequency	Frequency of Operation	MHz	2110		2170
P_{1dB}	Output Power at 1dB Compression, 2140MHz	W		10	
Gain	Gain at 1W Output Power, 2140MHz	dB		26.5	
Gain Flatness	Peak to Peak Gain Variation, 2110-2170MHz	dB		0.4	
IRL	Input Return Loss 1W Output Power, 2110-2170MHz	dB		14	
Efficiency	Drain Efficiency at 10W CW	%		29	
	Drain Efficiency at 1W CDMA (Single Carrier)	%		6.5	
Linearity	ACPR at 1W SC W-CDMA Output	dB		-50	
	3 rd Order IMD at 8W PEP (Two Tone)	dBc		-30	
Delay	Signal Delay from Pin 1 to Pin 5	nS		3.0	
Phase Linearity	Deviation from Linear Phase (Peak to Peak)	Deg		0.5	
$R_{TH, j-1}$	Thermal Resistance Stage 1 (Junction to Case)	$^{\circ}C/W$		11	
$R_{TH, j-2}$	Thermal Resistance Stage 2 (Junction to Case)	$^{\circ}C/W$		4	

Preliminary

XD010-35S-D2F

**2110-2170 MHz Class A/AB
10W Power Amplifier Module**



Product Features

- 50 Ω RF impedance
- 10W Output P_{1dB}
- Single Voltage Operation
- High Gain: 26.5 dB Typical
- High Efficiency
- Advanced, XeMOS II LDMOS FETS
- Temperature Compensation

Applications

- Base Station PA driver
- Repeater
- WCDMA

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522 Almanor Ave., Sunnyvale, CA 94085

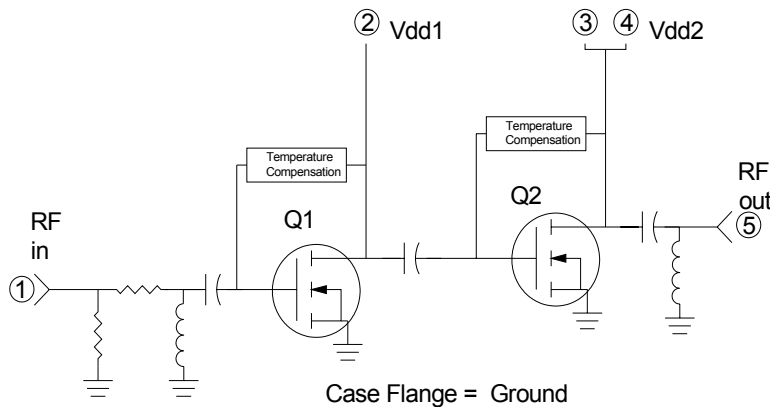
Phone: (800) SMI-MMIC

<http://www.sirenza.com>
EDS-102978 Rev A

Pin Out Description

Pin #	Function	Description
1	RF Input	Module RF input. This pin is internally connected to DC ground. Do not apply DC voltages to the RF leads. Care must be taken to protect against video transients that may damage the active devices.
2	V _{DD1}	This is the bias feed for the 1 st stage of the amplifier module. The gate bias is temperature compensated to maintain constant current over the operating temperature range. See Note 1.
3,4	V _{DD2}	This is the bias feed for the 2 nd stage of the amplifier module. The gate bias is temperature compensated to maintain constant current over the operating temperature range. See Note 1.
5	RF Output	Module RF output. This pin is internally connected to DC ground. Do not apply DC voltages to the RF leads. Care must be taken to protect against video transients that may damage the active devices.
Flange	Gnd	Exposed area on the bottom side of the package needs to be mechanically attached to the ground plane of the board for optimum thermal and RF performance. See mounting instructions for recommendation.

Simplified Device Schematic



Absolute Maximum Ratings

Parameters	Value	Unit
1 st Stage Bias Voltage (V _{DD1})	35	V
2 nd Stage Bias Voltage (V _{DD2})	35	V
RF Input Power	+23	dBm
Load Impedance for Continuous Operation Without Damage	5:1	VSWR
Output Device Channel Temperature	+200	°C
Lead Temperature During Solder Reflow	+210	°C
Operating Temperature Range	-20 to +90	°C
Storage Temperature Range	-40 to +100	°C

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation see typical setup values specified in the table on page one.

Note 1:

The internal generated gate voltage is thermally compensated to maintain constant quiescent current over the temperature range listed in the data sheet. No compensation is provided for gain changes with temperature. This can only be provided with AGC external to the module.

Note 2:

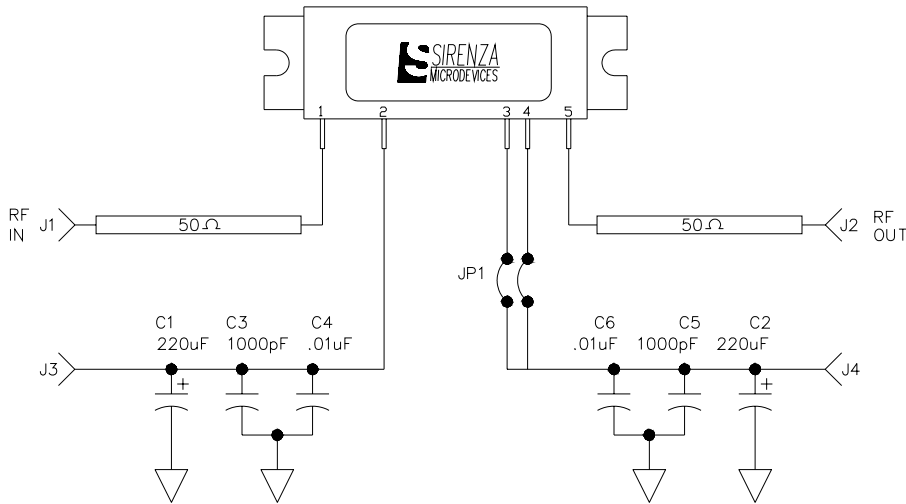
Internal RF decoupling is included on all bias leads. No additional bypass elements are required, however some applications may require energy storage on the drain leads to accommodate time-varying waveforms.



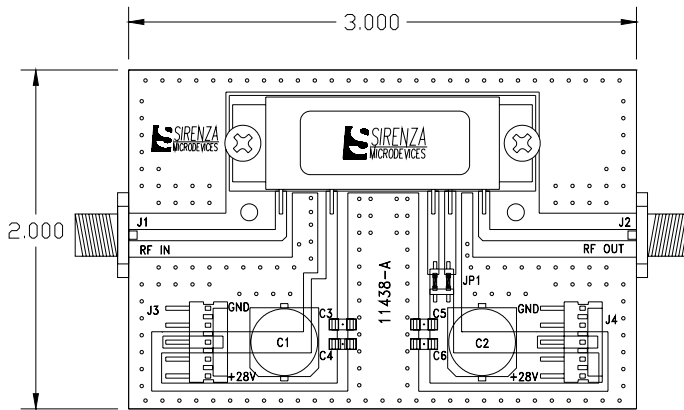
Caution: ESD Sensitive

Appropriate precaution in handling, packaging and testing devices must be observed.

Test Board Schematic with module attachments shown



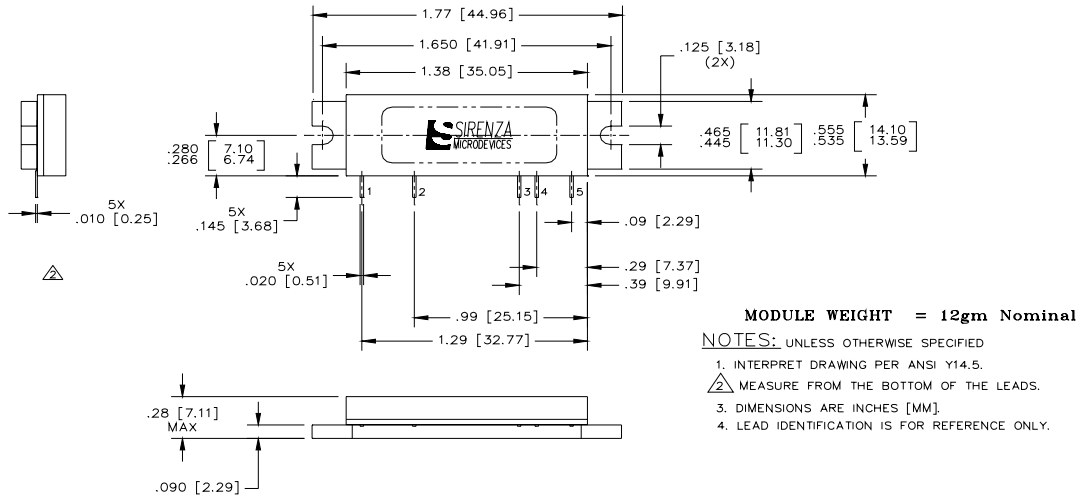
Test Board Layout and Bill of Materials



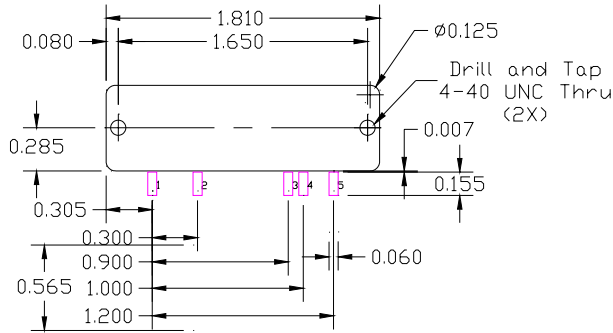
Component	Description	Manufacturer
PCB	Rogers 4350, $\epsilon_r=3.5$ Thickness=30mils	Rogers
J1, J2	SMA, RF, Panel Mount Tab W / Flange	AMP
J3, J4	MTA Post Header, 5 Pin, Rectangle, Polarized, Surface Mount	AMP
C1, C2	Cap, 220 μ F 50V, -40 to 85 $^{\circ}$ C, Electrolytic, G	Panasonic
C4, C6	Cap, 0.01 μ F, 100V, 10%, 1206	Johanson
C3, C5	Cap, 1000pF, 100V, 10%, 1206	Johanson
JP1 Header	SMT Header, Low Profile, 2mm	Specialty Electronics
JP1 Shunt	Shunt, Mate to Header, 2mm	Specialty Electronics
Mounting Screws	4-40 X 0.250"	Various

To download Gerber files, DXF drawings, a detailed BOM, and assembly recommendations for the test board with fixture [click here](#)

Package Outline Drawing



Recommended PCB Cutout and Landing Pads for the D2F Package



Note 3: Dimensions are in inches