



1GB- 128Mx64 SDRAM, UNBUFFERED W/PLL

FEATURES

- PC100 and PC133 compatible
- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- 3.3 volt \pm 0.3v Power Supply
- 144 Pin SO-DIMM JEDEC

DESCRIPTION

The WED3DG64128V is a 128Mx64 synchronous DRAM module which consists of eight 128Mx8 stack SDRAM components in TSOP- 11 package, and one 2K EEPROM in an 8- pin TSSOP package for Serial Presence Detect which are mounted on a 144 Pin SO-DIMM multilayer FR4 Substrate.

PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

PINOUT											
PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	VSS	2	VSS	49	DQ13	50	DQ45	97	DQ22	98	DQ54
3	DQ0	4	DQ32	51	DQ14	52	DQ46	99	DQ23	100	DQ55
5	DQ1	6	DQ33	53	DQ15	54	DQ47	101	VCC	102	VCC
7	DQ2	8	DQ34	55	VSS	56	VSS	103	A6	104	A7
9	DQ3	10	DQ35	57	NC	58	NC	105	A8	106	BA0
11	VCC	12	VCC	59	NC	60	NC	107	VSS	108	VSS
13	DQ4	14	DQ36	61	CLK0	62	CKE0	109	A9	110	BA1
15	DQ5	16	DQ37	63	VCC	64	VCC	111	A10	112	A11
17	DQ6	18	DQ38	65	RAS\	66	CAS\	113	VCC	114	VCC
19	DQ7	20	DQ39	67	WE\	68	CKE1	115	DQM2	116	DQM6
21	VSS	22	VSS	69	CS0\	70	A12	117	DQM3	118	DQM7
23	DQM0	24	DQM4	71	CS1\	72	NC	119	VSS	120	VSS
25	DQM1	26	DQM5	73	NC	74	NC	121	DQ24	122	DQ56
27	VCC	28	VCC	75	VSS	76	VSS	123	DQ25	124	DQ57
29	A0	30	A3	77	NC	78	NC	125	DQ26	126	DQ58
31	A1	32	A4	79	NC	80	NC	127	DQ27	128	DQ59
33	A2	34	A5	81	VCC	82	VCC	129	VCC	130	VCC
35	VSS	36	VSS	83	DQ16	84	DQ48	131	DQ28	132	DQ60
37	DQ8	38	DQ40	85	DQ17	86	DQ49	133	DQ29	134	DQ61
39	DQ9	40	DQ41	87	DQ18	88	DQ50	135	DQ30	136	DQ62
41	DQ10	42	DQ42	89	DQ19	90	DQ51	137	DQ31	138	DQ63
43	DQ11	44	DQ43	91	VSS	92	VSS	139	VSS	140	VSS
45	VCC	46	VCC	93	DQ20	94	DQ52	141	SDA	142	SCL
47	DQ12	48	DQ44	95	DQ21	96	DQ53	143	VCC	144	VCC

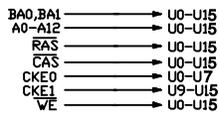
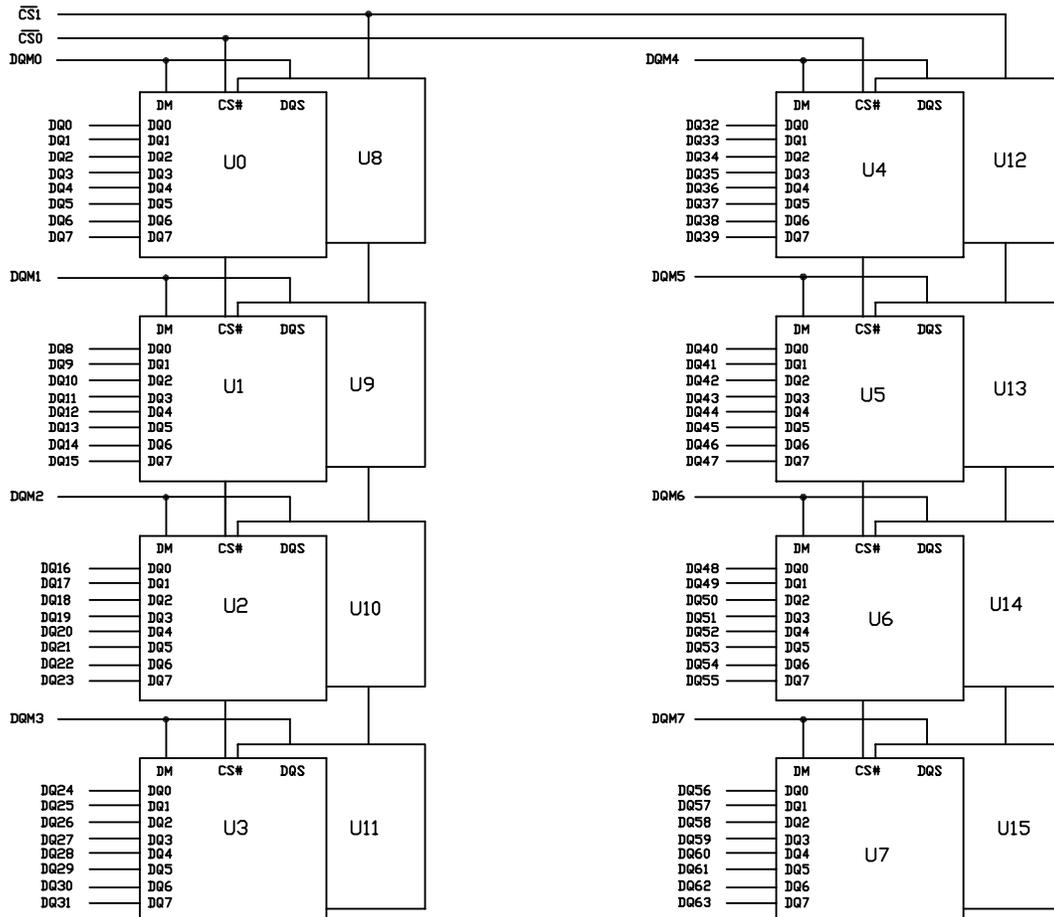
PIN NAMES

A0 – A12	Address input (Multiplexed)
BA0-1	Select Bank
DQ0-63	Data Input/Output
CLK0	Clock input
CKE0, CKE1	Clock Enable input
CS0, CS1	Chip select Input
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
DQM0-7	DQM
VDD	Power Supply (3.3V)
VSS	Ground
SDA	Serial data I/O
SCL	Serial clock
DNU	Do not use
NC	No Connect

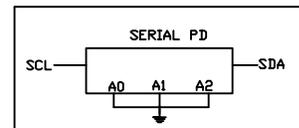
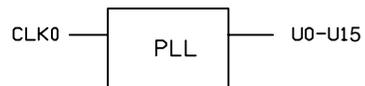
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FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor values are 22 ohms unless otherwise specified.



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Units
Voltage on any pin relative to VSS	V _{IN} , V _{out}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V
Storage Temperature	TSTG	-55 ~ +150	°C
Power Dissipation	PD	16	W
Short Circuit Current	IOS	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(Voltage Referenced to: V_{SS} = 0V, T_A = 0°C to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	VDD	3.0	3.3	3.6	V	
Input High Voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input Low Voltage	V _{IL}	-0.3	—	0.8	V	2
Output High Voltage	V _{OH}	2.4	—	—	V	I _{OH} = -2mA
Output Low Voltage	V _{OL}	—	—	0.4	V	I _{OL} = -2mA
Input Leakage Current	I _{LI}	-10	—	10	µA	3

Note: 1. V_{IH} (max)= 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min)= -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ VDDQ
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE

(T_A = 23°C, f = 1MHz, VDD = 3.3V, VREF=1.4V ± 200mV)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A12)	CIN1	-	15	pF
Input Capacitance (R _{AS} , C _{AS} , W _E)	CIN2	-	15	pF
Input Capacitance (CKE0)	CIN3	-	15	pF
Input Capacitance (CLK0)	CIN4	-	20	pF
Input Capacitance (CS0)	CIN5	-	15	pF
Input Capacitance (DQM0-DQM7)	CIN6	-	15	pF
Input Capacitance (BA0-BA1)	CIN7	-	15	pF
Data input/output capacitance (DQ0-DQ63)	Cout	-	22	pF
Data input/output capacitance (CB0-7)	Cout 1	-	22	pF

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**OPERATING CURRENT CHARACTERISTICS**(V_{CC} = 3.3V, T_A = 0°C to +70°C)

Parameter	Symbol	Conditions	Version		Units	Note
			133	100		
Operating Current (One bank active)	ICC1	Burst Length = 1 t _{RC} ≥ t _{RC} (min) IOL = 0mA	1,680	1,520	mA	1
Precharge Standby Current in Power Down Mode	ICC2P	CKE ≤ VIL(max), t _{CC} = 10ns	130		mA	
	ICC2PS	CKE & CLK ≤ VIL(max), t _{CC} = ∞	120			
Precharge Standby Current in Non-Power Down Mode	icc2N	CKE ≥ VIH(min), CS ≥ VIH(min), t _{cc} = 10ns Input signals are charged one time during 20	320		mA	
	icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), t _{cc} = ∞ Input signals are stable	160			
Active standby current in power-down mode	ICC3P	CKE ≥ VIL(max), t _{CC} = 10ns	160		mA	
	ICC3PS	CKE & CLK ≤ VIL(max), t _{cc} = ∞	130			
Active standby current in non power-down mode	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), t _{cc} = 10ns Input signals are changed one time during 20ns	480		mA	
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), t _{cc} = ∞ input signals are stable	360			
Operating current (Burst mode)	ICC4	I _o = mA Page burst 4 Banks activated t _{CCD} = 2CLK	1,680	1,440	mA	1
Refresh current	ICC5	t _{RC} ≥ t _{RC} (min)	2,720	2,560	mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	115		mA	

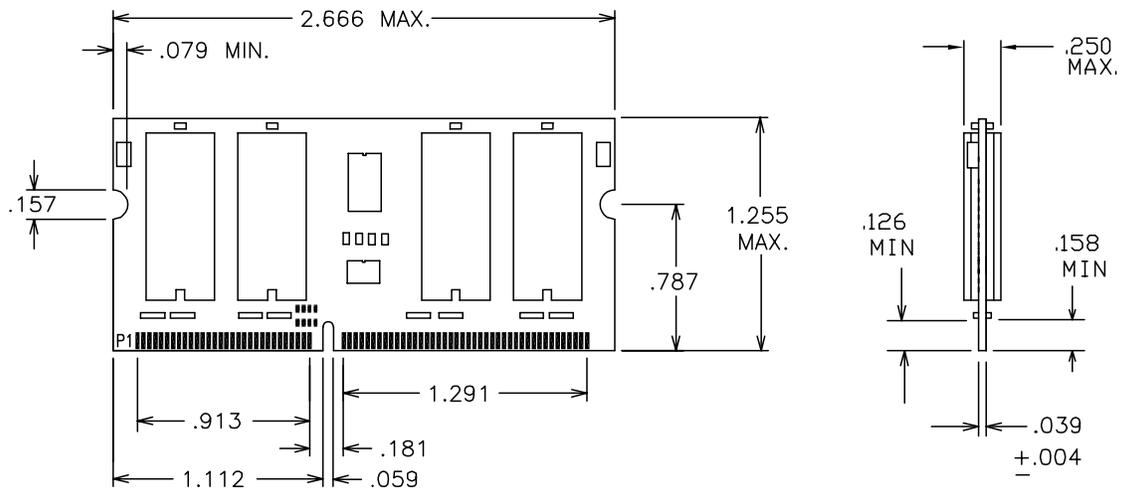
- Notes: 1. Measured with outputs open.
 2. Refresh period is 64ms.
 3. Unless otherwise noticed, input swing level is CMOS (VIH/VIL = VDDQ/VssQ)



Part number	Speed	Gas Latency
WED3DG64128V10D1	100MHz	CL=2
WED3DG64128V7D1	133MHz	CL=2
WED3DG64128V75D1	133MHz	CL=3

Note: For industrial temperature range product, add an "I" to the end of the part number.

PACKAGE DIMENSIONS



ALL DIMENSIONS ARE IN INCHES

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