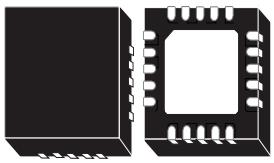
STA1102R

3 Gbps, 2 differential-pair channel eSATA signal re-driver

Preliminary data

Features

- Supports eSATA data rate of 1.5 Gbps and 3 Gbps
- Supports complete eSATA bus of two 2-wire differential-pair channels
- Squelch detector for validity of input differential signal
- Single operating supply (V_{CC}) range of 3.3 V ± 10%
- Low power mode
- 100 Ω CML I/Os
- eSATA hot-plug capable
- Low capacitance on all channels
- 1-bit input equalizer regenerates the receiver attenuated signal
- 1-bit adjustable pre-emphasis and driver to drive the transmitter outputs over long PCB track lengths
- Low output skew and jitter
- Low ground bounce
- Available in QFN20 (4 x 4 mm) package footprint with flow-through pinout
- -40 °C to 85 °C operating temperature range



QFN20
(4 x 4 mm)

Description

The STA1102R is a serial data signal re-driver. It integrates two differential-pair channels suitable for eSATA signals up to a 3 Gbps data rate, in compliance with the SATA rev 2.6 specification.

An input detector is available at each channel, which constantly monitors the input signal level for output squelch functionality. If the detected differential input is below a defined threshold, the output is biased to the common mode voltage.

High-speed data paths and the flow-through pinout minimize internal device jitter and simplify board layout. The integrated input equalizer improves signal integrity at the receiver due to effects from lossy cables. A 1-bit adjustable pre-emphasis is also integrated to drive the transmitter outputs over long PCB track lengths.

The device can be set to a low-power mode by disabling the output current drivers through the EN pin.

Table 1. Device summary

Order code	Package	Packing
STA1102RQTR	QFN20 (4 x 4 mm)	Tape and reel

1 Block diagram

Figure 1. STA1102R block diagram

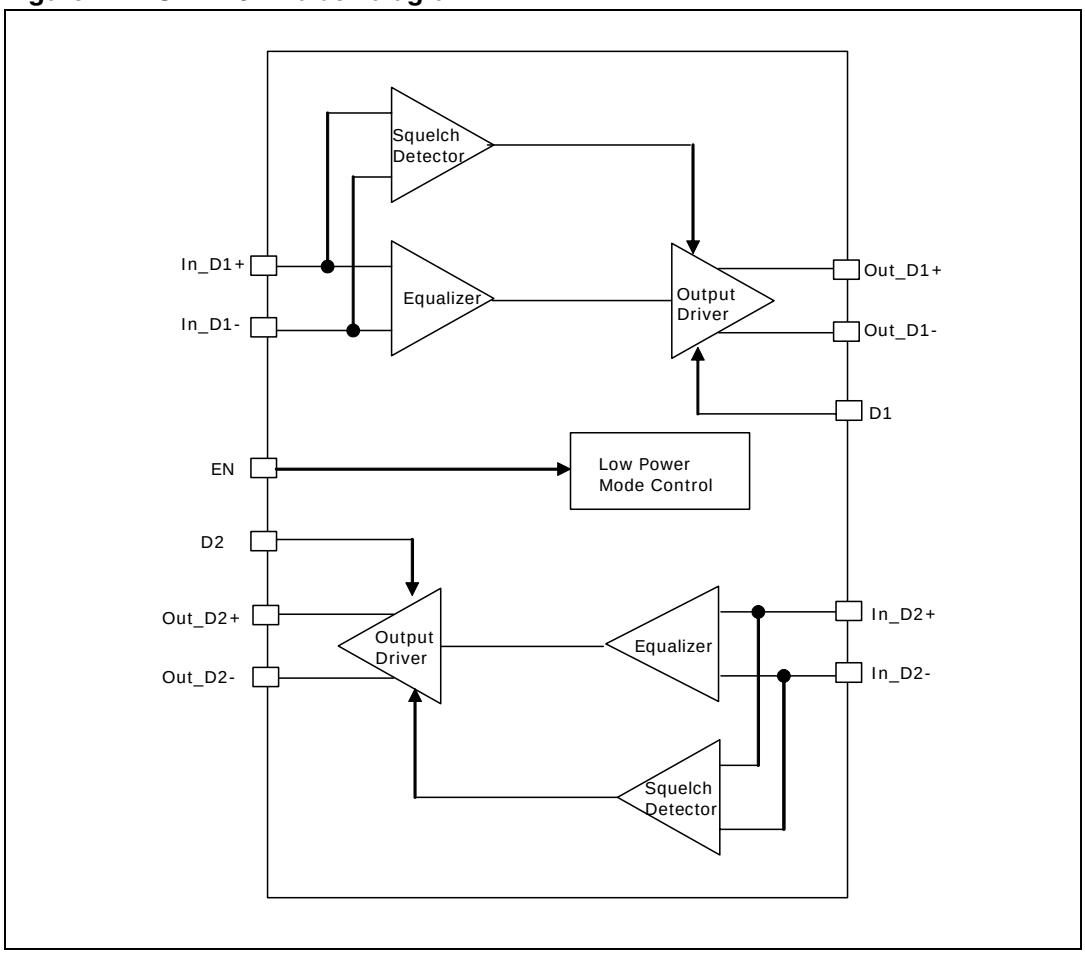


Figure 2. Pin configuration - top view

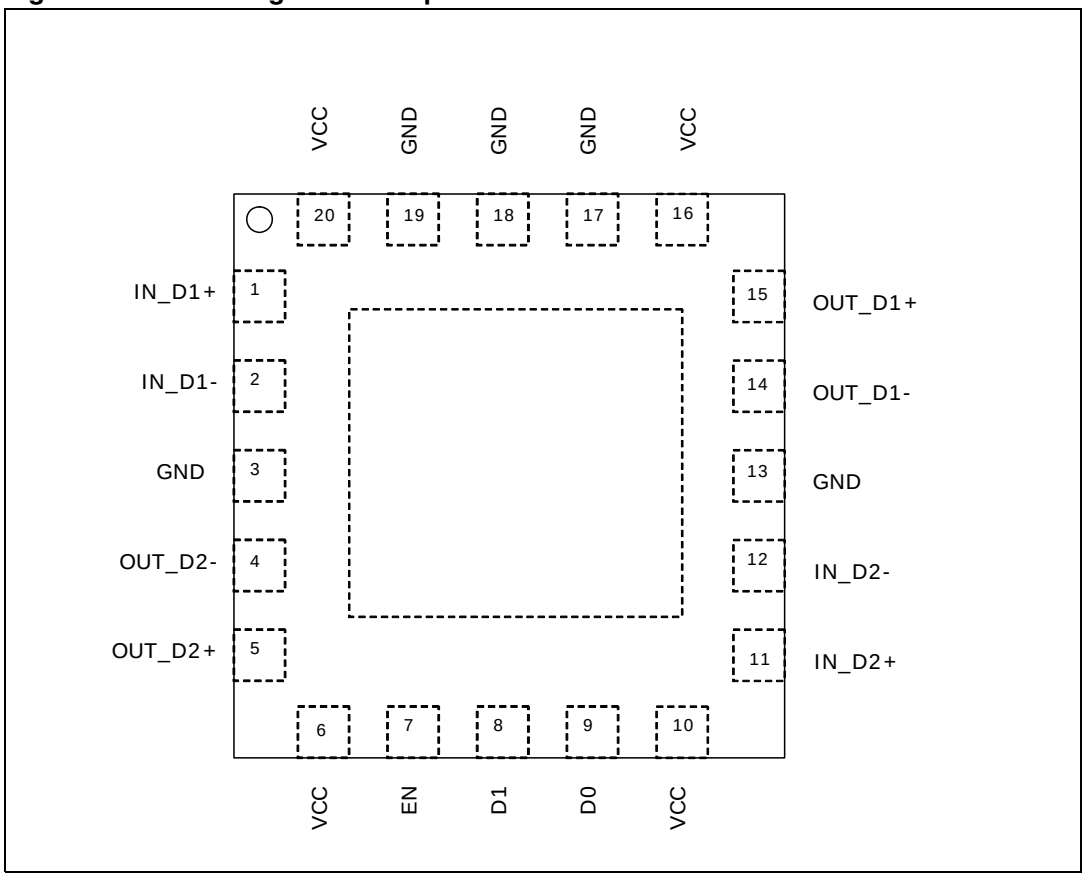


Table 2. Pin description

Pin number	Pin name	Type	Function
1	IN_D1+	Input	IN_D1+ makes a differential pair with IN_D1-
2	IN_D1-	Input	IN_D1- makes a differential pair with IN_D1+
3	GND	Power	Ground
4	OUT_D2-	Output	OUT_D2- makes a differential pair with OUT_D2+
5	OUT_D2+	Output	OUT_D2+ makes a differential pair with OUT_D2-
6	VCC	Power	3.3 V DC supply
7	EN	Input	Output driver enable pin; When low, device enters low power mode (internal 360 kΩ pull-up resistor to VCC)
8	D2	Input	Channel 2 pre-emphasis selection (internal 360 kΩ pull-down resistor to GND)
9	D1	Input	Channel 1 pre-emphasis selection (internal 360 kΩ pull-down resistor to GND)

Table 2. Pin description (continued)

Pin number	Pin name	Type	Function
10	VCC	Power	3.3 V DC supply
11	IN_D2+	Input	IN_D2+ makes a differential pair with IN_D2-
12	IN_D2-	Input	IN_D2- makes a differential pair with IN_D2+
13	GND	Power	Ground
14	OUT_D1-	Output	OUT_D1- makes a differential pair with OUT_D1+
15	OUT_D1+	Output	OUT_D1+ makes a differential pair with OUT_D1-
16	VCC	Power	3.3 V DC supply
17	GND	Power	Ground
18	GND	Power	Ground
19	GND	Power	Ground
20	VCC	Power	3.3 V DC supply

2 Functional description

2.1 Equalizer

The integrated input equalizer reduces system jitter and attenuation from long or lossy cables. Shaping is performed by the gain stage of the equalizer to compensate the signal.

2.2 Pre-emphasis

The STA1102R provides at each output a differential pair of 1-bit programmable preemphasis to compensate for losses across long PCB tracks and interconnects after the re-driver output. Below, the truth table of the pre-emphasis control is shown:

Table 3. Pre-emphasis truth table

EN	D0	D1	Functions
0	x	x	Low power mode: Output driver disabled; output driven to HiZ
1	0	0	Normal operation mode: both CH1 and CH2 0 dB pre-emphasis
1	0	1	Normal operation mode: CH1 0 dB pre-emphasis; CH2 2.5 dB pre-emphasis
1	1	0	Normal operation mode: CH1 2.5 dB pre-emphasis; CH2 0 dB pre-emphasis
1	1	1	Normal operation mode: Both CH1 and CH2 2.5 dB pre-emphasis

2.3 Input termination

The STA1102R integrates precise 50 Ω ± 10% termination resistors, pulled up to V_{Cm}, on all its differential input channels. External terminations are not required. This gives improved performance and also minimizes the PCB board space. These on-chip termination resistors should match the differential characteristic impedance of the transmission line.

2.4 Low power modes

There are 2 types of low power modes in the STA1102R: hardware low and auto low power modes.

2.4.1 Hardware low power mode

The EN input activates a hardware low power mode. There is an internal pull-up resistor to maintain the EN in the default (HIGH) state. When this low power mode is activated (EN=L), all input and output buffers and internal bias circuitry are powered off and disabled. Outputs are driven to HiZ in low power mode. There is a delay associated with entering (max 2 µs) and exiting (max 20 µs) this hardware low power mode.

2.4.2 Auto low power mode

The auto low power mode is activated when differential voltage at either or both of the channels is < 50 mV for more than 3 µs. During this low power mode, output of the associated channel is driven to V_{cm} and the selective circuit block is disabled to lower power consumption. The delay associated with exiting the auto low power mode is 50 ns max.

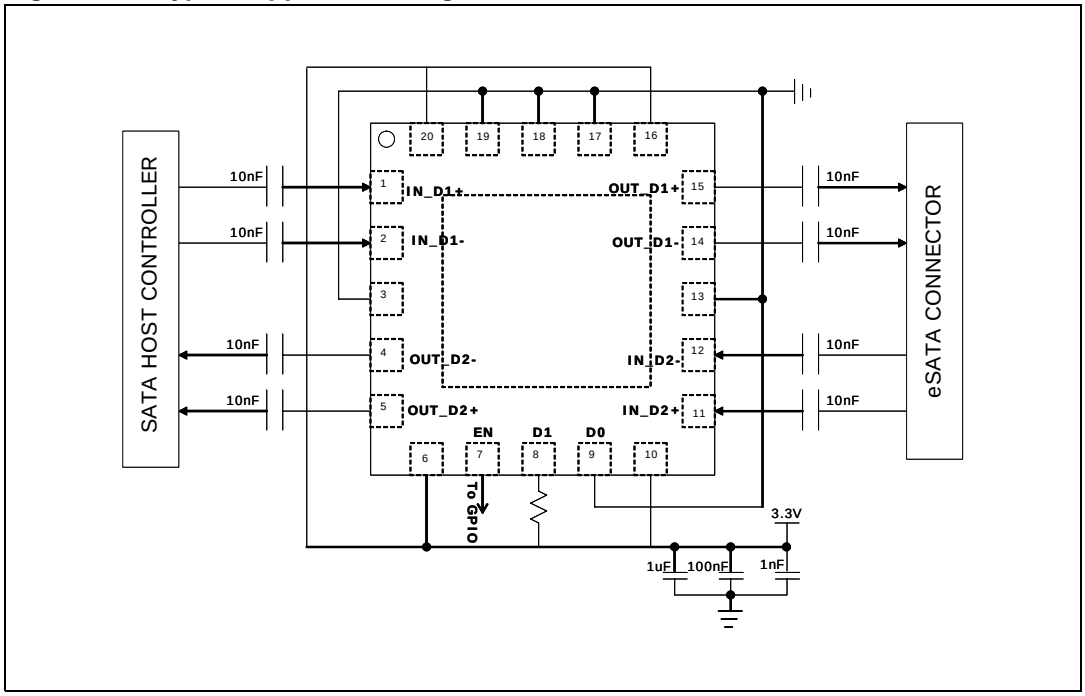
2.5 Squelch detector

A squelch detector is integrated on the input of each of the 2 data paths. The squelch detector is a high-speed amplitude comparator that is turned on when EN=H. The differential input signal is monitored by the detector. When the differential input is detected to be less than or equal to 50 mV, the input signal is considered an invalid signal and is not passed to the output. When this happens, the corresponding output is biased to V_{CM}. When the differential input is greater than or equal to 150 mV, the input signal is considered valid signal and is passed to the output.

The integration of the squelch detector helps the system to prevent responding to noises. As such, it enables the device to fully support OOB signaling.

3 Application diagram

Figure 3. Typical application diagram



Typical circuit above is shown with CH1 pre-emphasis of 0 dB and CH2 pre-emphasis of 2.5 dB.

4 Absolute maximum ratings

Absolute maximum ratings are those values above which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referenced to GND.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage to ground	-0.5 to + 4.0	V
V_I	Differential pair IOs voltage range	-0.5 to + 4.0	V
	Control IOs voltage range	-0.5 to + 4.0	V
T_{STG}	Storage temperature	-65 to + 150	°C
V_{ESD}	Electrostatic discharge voltage (human body model)	±12	kV

5 Thermal data

Table 5. QFN20 package thermal data

Symbol	Parameter	QFN20	Unit
θ_{JA}	Thermal coefficient (junction-ambient)	60	°C/Ω

6 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CC}	Supply voltage	-	3.0	3.3	3.6	V
T_A	Operating ambient temperature	-	0	-	85	°C
C_C	Coupling capacitor	-	-	12	-	nF
D_R	Data rate	-	-	-	3.0	Gbps

6.1 Electrical characteristics

(T_A = 0 to 85 °C, V_{CC} = 3.0 V to 3.6 V unless otherwise specified).

Table 7. DC electrical characteristic

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
General parameter characteristics						
$I_{CC\_standby}$	Standby mode supply current	EN = L	-	-	300	µA
I_{CC_active}	Active mode supply current	V_{DIFF_RX}=700 mV, K28.5 pattern running at 3 Gbps EN=H, D1=D0=H	-	-	80	mA
$I_{CC\_squelch}$		$V_{DIFF\_RX} \leq V_{TH}$, EN=H D1=D0=H	-	-	45	mA
T_{PD}	Data propagation delay	-	-	-	400	ps
T_{DIS}	Device disable time	EN = H to L	-	-	2	µs
T_{EN}	Device enable time	EN = L to H	-	-	20	µs
Control logic characteristics						
V_{IH}	Input logic high voltage	-	1.4	-	-	V
V_{IL}	Input logic low voltage	-	-	-	0.5	V
I_{IH}	Input logic high current	-	-15	-	15	µA
I_{IL}	Input logic low current	-	-15	-	15	µA
Squelch detector characteristics						
V_{TH}	Squelch threshold voltage	-	50	-	150	mV_{pp}
T_{ENTER}	Squelch mode enter	-	-	-	5	ns
T_{EXIT}	Squelch mode exit	-	-	-	5	ns

Table 7. DC electrical characteristic (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
AC/DC specifications for receiver						
V_{DIFF_RX}	Differential input peak-to-peak voltage	D_R = 3.0 Gbps	200	-	1600	mV_{pp}
V_{CM_RX}	Common mode voltage	-	-	0	-	V
Z_{DIFF_RX}	Differential input impedance	-	85	100	115	Ω
Z_{SE_RX}	Single-ended input impedance	-	40	-	-	Ω
RL_{DIFF_RX}	Differential input return loss	f = 100 MHz to 300 MHz	18	-	-	dB
		f = 300 MHz to 600 MHz	14	-	-	dB
		f = 600 MHz to 1200 MHz	10	-	-	dB
		f = 1.2 GHz to 2.4 GHz	8	-	-	dB
		f = 2.4 GHz to 3.0 GHz	3	-	-	dB

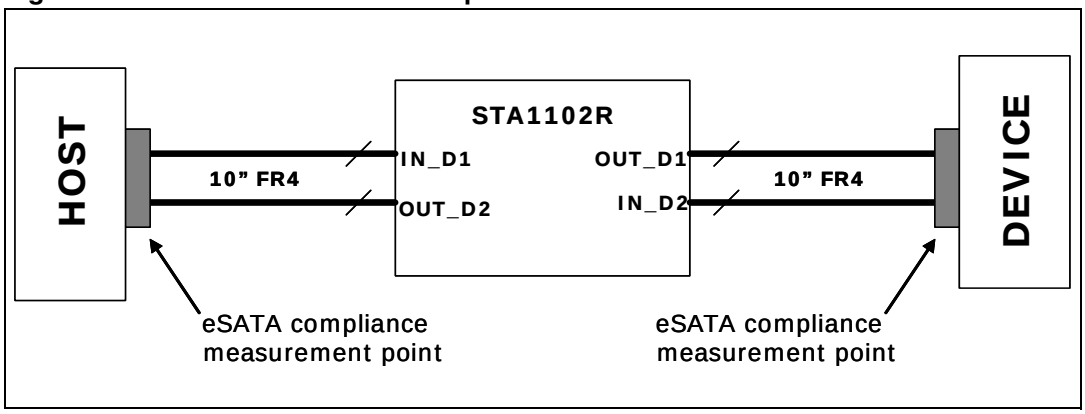
Table 8. AC electrical characteristic

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
RL_{CM_RX}	Common mode input return loss	f = 100 MHz to 300 MHz	5	-	-	dB
		f = 300 MHz to 600 MHz	5	-	-	dB
		f = 600 MHz to 1200 MHz	2	-	-	dB
		f = 1.2 GHz to 2.4 GHz	1	-	-	dB
		f = 2.4 GHz to 3.0 GHz	1	-	-	dB
T_{R/F_RX}	Input rise/fall time	20% to 80%	67	-	136	ps
T_{Skew_RX}	Input differential skew	Mid-point of RX+ to mid-point of RX-	-	-	50	ps
AC/DC specifications for transmitter						
V_{DIFF_TX}	Differential output peak-to-peak voltage	f = 1.5 GHz; D0/D1 = L	400	-	600	mV_{pp}
		f = 1.5 GHz; D0/D1 = H	600	-	800	mV_{pp}
V_{CM_TX}	Common mode voltage	-	-	2.1	-	V
Z_{DIFF_TX}	Differential output impedance	-	85	100	115	Ω

Table 8. AC electrical characteristic (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Z_{SE_TX}	Single-ended output impedance	-	40	-	-	Ω
RL_{DIFF_TX}	Differential output return loss	f = 100 MHz to 300 MHz	14	-	-	dB
		f = 300 MHz to 600 MHz	8	-	-	dB
		f = 600 MHz to 1200 MHz	6	-	-	dB
		f = 1.2 GHz to 2.4 GHz	6	-	-	dB
		f = 2.4 GHz to 3.0 GHz	3	-	-	dB
RL_{CM_TX}	Common mode output return loss	f = 100 MHz to 300 MHz	5	-	-	dB
		f = 300 MHz to 600 MHz	5	-	-	dB
		f = 600 MHz to 1200 MHz	2	-	-	dB
		f = 1.2 GHz to 2.4 GHz	1	-	-	dB
		f = 2.4 GHz to 3.0 GHz	1	-	-	dB
T_{R/F_TX}	Output rise/fall time	20% to 80%	67	-	136	ps
T_{Skew_TX}	Output differential skew	Mid-point of RX+ to mid-point of RX-	-	-	20	ps
TJ_{TX}	Total jitter	D_R = 3 Gbps; K28.5 pattern	-	0.2	0.3	UI_{pp}
DJ_{TX}	Deterministic jitter	D_R = 3 Gbps; K28.5 pattern	-	0.13	0.2	UI_{pp}
RJ_{TX}	Random jitter	D_R = 3 Gbps; K28.7 pattern	-	2.0	2.15	ps_{rms}

Figure 4. Jitter measurement setup



7 Package mechanical data

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Figure 5. Package outline for QFN20 (4 x 4 x 0.8 mm) - pitch 0.5 mm

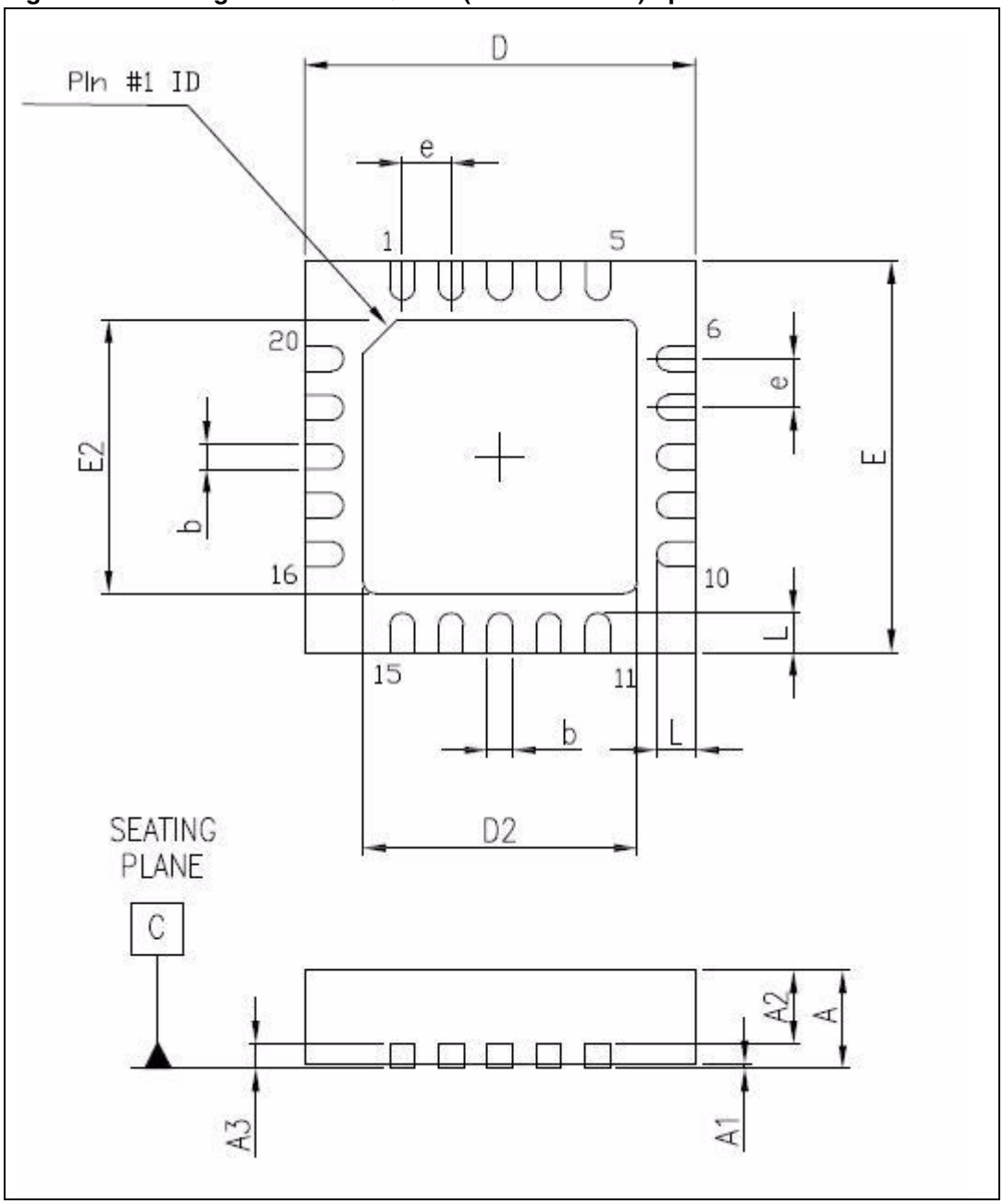


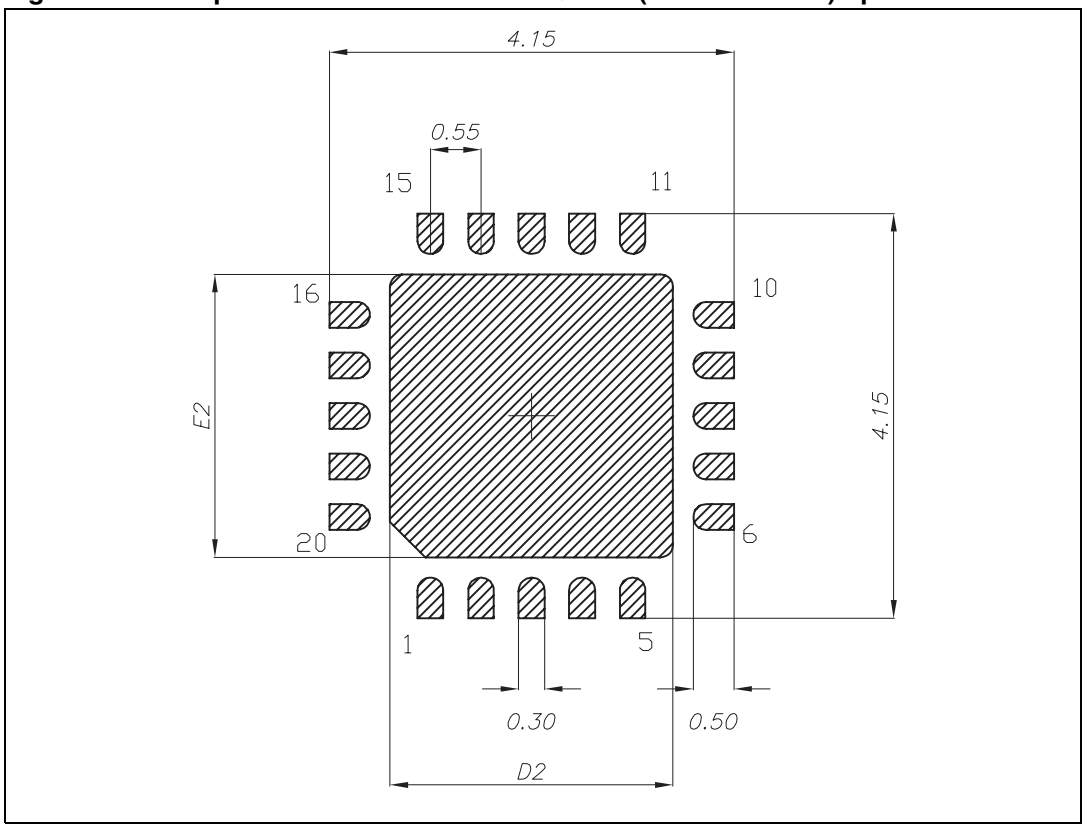
Table 9. Mechanical data for QFN20 (4 x 4 x 0.8 mm) - pitch 0.5 mm

Symbol	Millimeters		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	-	0.02	-
A2	-	0.65	-
A3	-	0.25	-
b	0.18	0.23	0.30
D	3.85	4.00	4.15
D2	See exposed pad variations		
E	3.85	4.00	4.15
E2	See exposed pad variations		
e	0.45	0.50	0.55
L	0.30	0.40	0.50

Table 10. Exposed pad variations

Variation	D2			E2		
	Min	Typ	Max	Min	Typ	Max
A	2.70	2.80	2.90	2.70	2.80	2.90

Figure 6. Footprint recommendation for QFN20 (4 x 4 x 0.8 mm) - pitch 0.5 mm



8 Revision history

Table 11. Document revision history

Date	Revision	Changes
19-Oct-2009	1	Initial release.

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