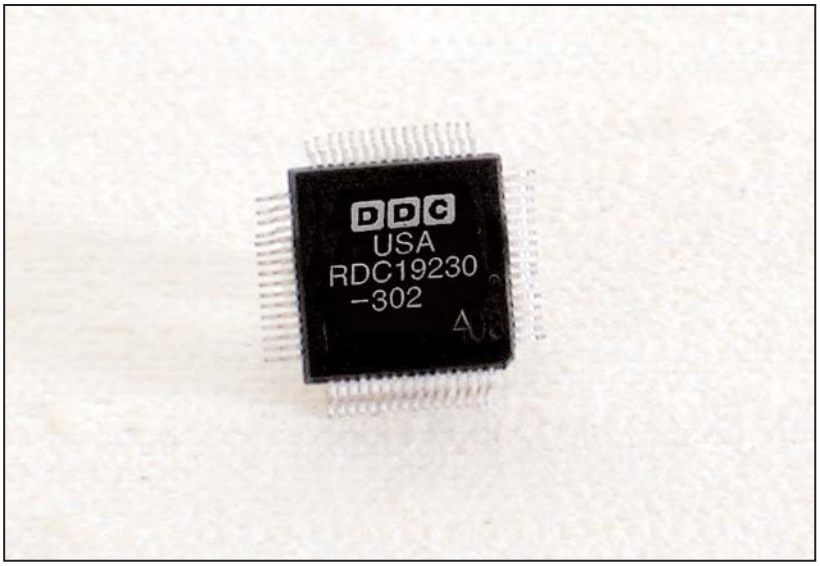
RD-19230

16-BIT MONOLITHIC TRACKING RESOLVER-TO-DIGITAL CONVERTER



DESCRIPTION

The RD-19230 is a small and versatile, low cost, state-of-the-art 16-bit monolithic Resolver-to-Digital Converter. This single chip converter offers programmable features such as resolution, bandwidth, velocity output scaling and encoder emulation.

Resolution programming allows selection of 10, 12, 14, or 16 bit, with accuracies to 1.3 minutes. The parallel digital data and the internal encoder emulation signals ($\overline{A}$ $\overline{QUAD}$ $\overline{B}$) have independent resolution control. Internal encoder emulation will permit inhibiting (freezing) the parallel digital data without interrupting the A and B outputs.

The internal Synthesized Reference section eliminates errors due to quadrature voltage and ensures operation with a rotor-to-stator phase shift of up to 45 degrees. The velocity output (VEL) can be used in place of a tachometer. It has a range of ±4 V relative to analog ground. The velocity scale factor/tracking rate is programmed with a single resistor. This converter provides the option of using a second set of filter components which can be used in dual bandwidth or switch on the fly applications.

APPLICATIONS

With its low cost, small size, high accuracy, and versatile performance, the RD-19230 converter is ideal for use in modern high performance industrial control systems. It is ideal for users who wish to use a resolver input in their encoder based system. Typical applications include motor control, machine tool control, robotics, and process control.

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FEATURES

- Accuracy up to 1.3 Arc Minutes
- Internal Synthesized Reference
- +5 Volt Only Option
- Programmable Resolution, Dual Bandwidth and Tracking Rate
- Internal Encoder Emulation with Independent Resolution Control
- Differential Resolver Input Mode
- Velocity Output Eliminates Tachometer
- Built-In-Test (BIT) Output, No 180° Hangup with AC Reference
- -40° to +85°C Operating Temperature
- Programmable for LVDT Input

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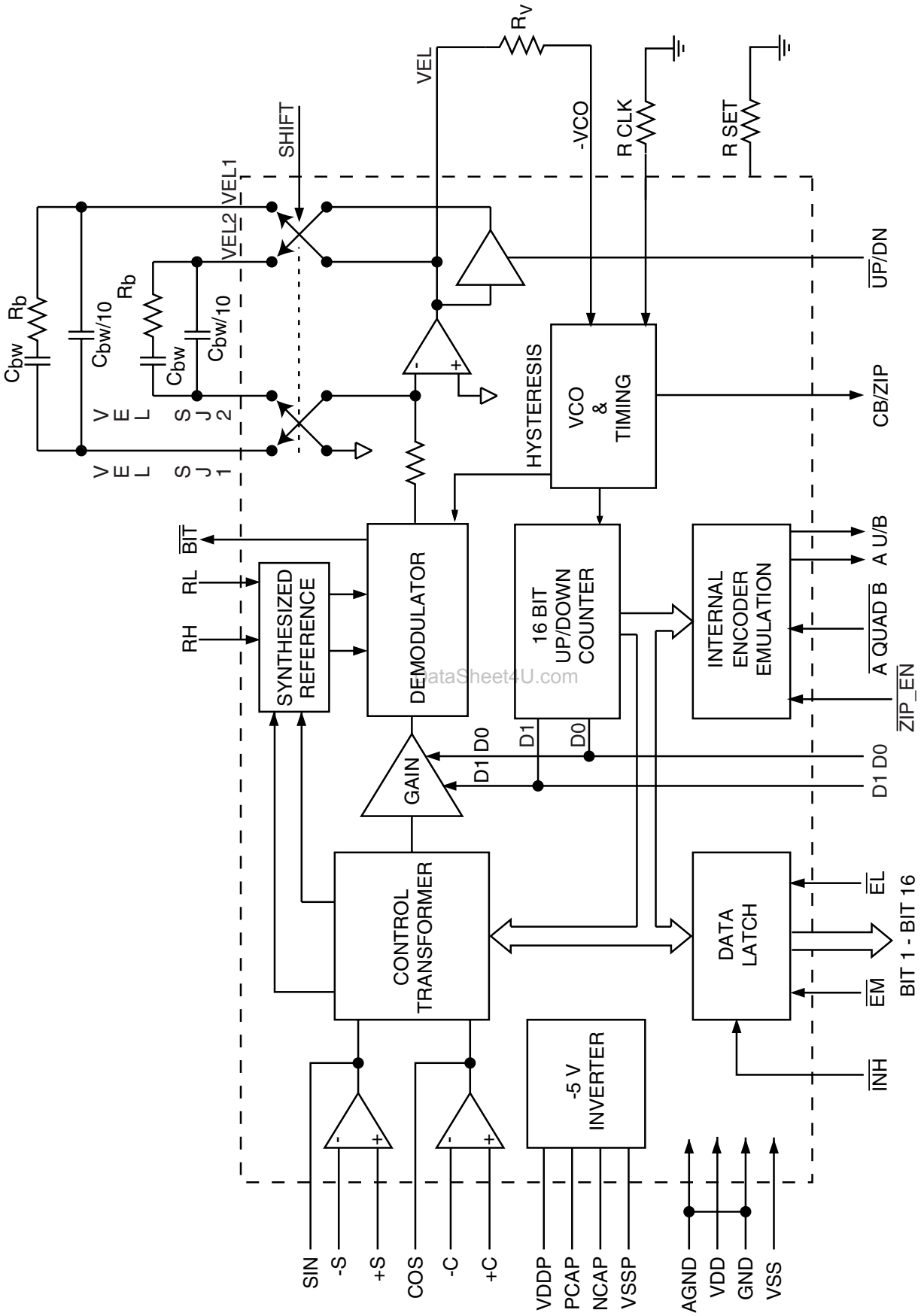


FIGURE 1. RD-19230 SERIES BLOCK DIAGRAM

TABLE 1. RD-19230 SPECIFICATIONS

These specs apply over the rated power supply, temperature,and reference frequency ranges; 10% signal amplitude variation, and 10% harmonic distortion.

PARAMETER	UNIT	VALUE		
RESOLUTION	Bits	10, 12, 14, or 16 (Note 1 & 2)		
FREQUENCY RANGE	Hz	47-1k (Note 4)	1k - 4k	4k - 10k
ACCURACY -XX2 (Note 3)	minutes	4 +1 LSB	4 +1 LSB	5 +1 LSB
-XX3 (Note 3)	minutes	2 +1 LSB	2 +1 LSB	3 +1 LSB
Repeatability	LSB	± 1	± 1	± 2
Differential Linearity	LSB	± 1	± 1	± 2
FREQUENCY RANGE	Hz	47-1k (Note 4)	1k - 5k (Note 12)	
ACCURACY -XX5 (Note 3)	minutes	1 +1 LSB	1 +1 LSB	
Repeatability	LSB	± 1	± 1	
Differential Linearity	LSB	± 1	± 1	
REFERENCE		(+RH, -RL)		
Type		Differential		
Voltage: differential	Vp-p	10 max. (Note 11)		
single ended	Vp	±5 max. (1.5 min.)(Note 11)		
overload	Vp	±25 continuous; ±100 transient		
Frequency	Hz	DC to 10k (Note 12)		
Input Impedance	Ω	10M minutes. || 20 pf		
Common Mode Range	Vp	3		
SYNTHESIZED REFERENCE		(note 5)		
±Sig/Ref Phase Shift Correction	deg	45 max. from 400 Hz to 10kHz		
SIGNAL INPUT		(+S, -S, SIN, +C, -C, COS)		
Type		Resolver, differential, groundbased		
Voltage: operating	Vrms	2 ±15%		
overload	Vp	±25 continuous		
Input impedance	Ω	10M minutes || 10 pF.		
DIGITAL INPUTS (Note 10)				
TTL / CMOS COMPATIBLE INPUTS		Logic 0 = 0.8 V max. / Logic 1 = 2.0 V minutes.		
		Loading=10 µA max P.U. current source to +5 V || 5 pF max., CMOS transient protected		
Inhibit ($\overline{\text{INH}}$)		Logic 0 inhibits; Data stable within 150 ns (Logic 1 = Transparent)		
Enable Bits 1 to 8 ($\overline{\text{EM}}$) }		{ Logic 0 enables; Data stable within 150 ns (Logic 0 = Transparent)		
Enable Bits 9 to 16 ($\overline{\text{EL}}$) }		{ Logic 1 = High Impedance; Data High Z within 100 ns (Note 8)		
Resolution and Mode Control (D1 & D0) (See Notes 1 & 2)		Mode / D1 / D0 / Resolution		
		Resolver / 0 / 0 / 10 bits		
		" / 0 / 1 / 12 bits		
		" / 1 / 0 / 14 bits		
		" / 1 / 1 / 16 bits (Preset, Note 10)		
		LVDT / -5 V / 0 / 8 bits		
		" / 0 / -5 V / 10 bits		
		" / 1 / -5 V / 12 bits		
		" / -5 V / -5 V / 14 bits		
$\overline{\text{ZIP\_EN}}$		Logic 0 enables ZIP, Logic 1 enables CB		
CMOS Compatible Inputs		Logic 0 = 1.5 V max., Logic 1 = 3.5 V minutes., negative voltage = -3.5 V minutes.		
SHIFT		Logic 1 selects VEL1 components, Logic 0 selects VEL2 components		

Notes:
1. As parallel resolution is reduced, pairs of bits are disabled. (Unused bits are set to a logic "0.")
   • 14 bit resolution: 15/16 disabled, • 12 bit resolution: 13/14, 15/16 disabled, • 10 bit resolution: 11/12, 13/14, 15/16 disabled
2. In LVDT mode, Bit 3 is the MSB and resolution is programmable to 8, 10, 12, and 14 bits.
3. Accuracy specification below for LVDT mode, null to + full scale travel (45 degrees) (2-wire configuration).
   4 Minute part = 0.15% + 1 LSB of full scale "resolution set"
   2 Minute part = 0.07% + 1 LSB of full scale "resolution set"
   1 Minute part = 0.035% + 1 LSB of full scale "resolution set"
   Accuracy specification below for LVDT mode, full scale travel (90 degrees) (3-wire configuration).
   4 Minute part = 0.07% + 1 LSB of full scale "resolution set"
   2 Minute part = 0.035% + 1 LSB of full scale "resolution set"
   1 Minute part = 0.017% + 1 LSB of full scale "resolution set"
   Note that these accuracy specifications are for the converter and do not consider any front end external resistor tolerances.
4. In the frequency range of 47Hz to 1kHz, there will be 1 LSB of jitter at quadrant boundaries.
5. The maximum phase shift tolerance will degrade linearly from 45 degrees at 400 Hz to 30 degrees at 60 Hz.
6. When using the -5V inverter, the VDD supply current will double and VSSP can be up to 20% low, or -4V.
7. || = in parallel with.
8. High Z refers to parallel data only.
9. Normal ESD (Electro Static Device) handling precautions should be observed.
10. Any unused pins may be left floating (unconnected). All TTL & CMOS input pins are internally pulled up to +5 Volts.
11. A signal less than 500 mV will assert BIT.
12. -XX5 accuracy is 1 minute + 1 LSB up to 5 kHz max.
13. For Ka definition, see the RDC-19220/RD-19230 application manual acceleration lag section.

TABLE 1. RD-19230 SPECIFICATIONS (CONTINUED)

These specs apply over the rated power supply, temperature, and reference frequency ranges; 10% signal amplitude variation, and 10% harmonic distortion.

PARAMETER	UNIT	VALUE
CMOS Compatible Inputs (cont)		
$\overline{UP}$/DN		Logic 0, precharged components gain is 4 Logic 1, precharged components gain is 1/4
$\overline{A\ QUAD\ B}$		Logic 0 enables encoder emulation, Falling edge latches encoder resolution
DIGITAL OUTPUTS		
Drive Capability		50 pF+ Logic 0: 1 TTL load, 1.6 mA at 0.4 V max. Logic 1; 10 TTL loads, = 0.4 mA at 2.8 V minutes. Logic 0; 100 mV max. driving CMOS Logic 1; +5 V supply minus 100 mV minutes. driving CMOS High Z; 10 µA ‖ 5 pF max. (Note 8)
Parallel Data (1-16)		10, 12, 14, or 16 parallel lines; natural binary angle positive logic (see note 2)
Converter Busy (CB)		0.25 to 0.75 µs positive pulse leading edge initiates counter update. (CB functions with $\overline{ZIP\_EN}$ pin tied to +5 V or NC), Logic 1 at all 0's
Zero Index Pulse (ZIP)		This output is active when the $\overline{ZIP\_EN}$ pin is tied to GND (Logic 0).
Built-In-Test ($\overline{BIT}$)		The $\overline{BIT}$ error is triggered if any of the following conditions exist: ~ ±100 LSB's of error, Loss of Signal (LOS), or Loss of Reference (LOR) is less than 500 mVp, or a false null occurs when the phase detect circuitry causes a $\overline{BIT}$ and corrects the error. Logic 0 for fault condition.
A, B		Incremental Encoder Output
DYNAMIC CHARACTERISTICS		(at maximum bandwidth)
Resolution	bits	**10** / **12** / **14** / **16**
Tracking Rate (minutes)	rps	1152 / 288 / 72 / 18
Bandwidth (Closed Loop)	Hz	1200 / 1200 / 600 / 300
Ka(Acceleration Constant) Note 13	$1/sec^2$	5.7M / 5.7M / 1.4M / 360k
A1	1/sec	19.5 / 19.5 / 4.9 / 1.2
A2	1/sec	295k / 295k / 295k / 295k
A	1/sec	2400 / 2400 / 1200 / 600
B	1/sec	1200 / 1200 / 600 / 300
Acceleration (1 LSB lag)	deg/sec^2	2M / 500k / 30k / 2k
Settling Time (179° step)	msec	2 / 8 / 20 / 50
VELOCITY CHARACTERISTICS		
Polarity		Positive for increasing angle
Voltage Range (Full Scale)	V	±4 (at nominal power supply)
Scale Factor Error	%	10 typ / 20 max
Scale Factor TC	PPM/°C	100 typ / 200 max
Reversal Error	%	0.75 typ / 1.3 max
Linearity	%	0.25 typ / 0.50 max
Zero Offset	mV	5 typ / 10 max
Zero Offset TC	µV/°C	15 typ / 30 max
Load	kΩ	8 min
POWER SUPPLIES		(note 6)
Nominal Voltage	V	+5 (VDD) / -5 (VSS)
Voltage Range	%	±5 / ±5
Max Volt. w/o Damage	V	+7 / -7
Current	mA	25 max. (each), 17 typ.* (* Typical current is when a 30K resistor is used for the current set.)
TEMPERATURE RANGE		
Operating (case)		
-30X	°C	0 to +70
-20X	°C	-40 to +85
Storage	°C	-65 to +150
Junction-to-Case	°C/W	20
Junction-to-Ambient	°C/W	50
Junction Temp Max	°C	150
MOISTURE SENSITIVITY LEVEL		Level 1 Tested in accordance with JEDEC SPEC J-STD-020
PHYSICAL CHARACTERISTICS		
Size: 64-pin Quad Flat Pack	in(mm)	0.52 x 0.52 (13.2 x 13.2)
WEIGHT	oz(g)	0.018 (0.5)

THEORY OF OPERATION

The RD-19230 is a mixed signal CMOS IC containing analog input and digital output sections. Precision analog circuitry is merged with digital logic to form a complete high-performance tracking resolver-to-digital converter. For user flexibility and convenience, the converter bandwidth, dynamics, and velocity scaling are externally set with passive components.

The RD-19230 Functional Block Diagram is shown in FIGURE 1. The analog conversion electronics require ±5 VDC power supplies, and the converter contains a charge pump to provide the user with the option of a single-ended +5 VDC supply. The converter front-end consists of differential sine and cosine input amplifiers which are protected up to ±25 V with 2 kΩ resistors and diode clamps to the ±5 VDC supplies. By performing the following trigonometric identity, $SIN\theta(COS\phi) - COS\theta(SIN\phi) = SIN(\theta-\phi)$, the Control Transformer (CT) compares the analog input signals (θ) with the digital output (ϕ), resulting in an error signal proportional to the sine of the angular difference. The CT uses a combination of amplifiers, switches, logic and capacitors in precision ratios to perform the calculation.

Note: The error output of the CT is normally sinusoidal, but in LVDT mode, it is triangular (linear) and can be used to convert any linear transducer output.

The converter accuracy is limited by the precision of the computing elements in the CT. Instead of a traditional precision resistor network, this converter uses capacitors with precisely controlled ratios. Sampling techniques are used to eliminate errors due to voltage drift and op-amp offsets.

The error processing is performed using the industry standard technique for Type II tracking converters. The DC error is integrated yielding a velocity voltage which in turn drives a voltage controlled oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output) which, together with the velocity integrator, forms a Type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and another lag at higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above. The settings of the various error processor gains and break frequencies are done with external resistors and capacitors so that the converter loop dynamics can be easily controlled by the user.

TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its Transfer Function Block Diagrams and Bode Plots (open and closed loop). These are shown in FIGURES 2, 3, and 4.

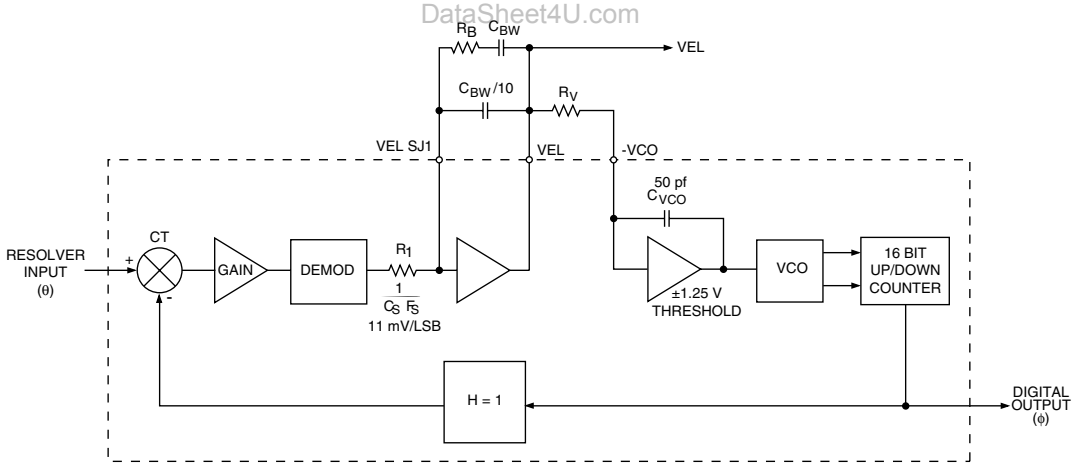


FIGURE 2. TRANSFER FUNCTION BLOCK DIAGRAM #1

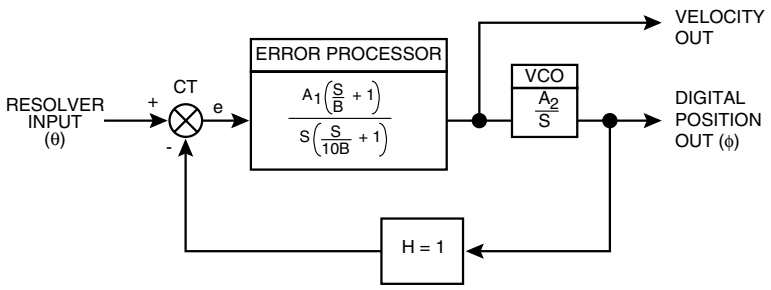


FIGURE 3. TRANSFER FUNCTION BLOCK DIAGRAM #2

The open loop transfer function is as follows:

$$\text{Open Loop Transfer Function} = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}$$

where A is the gain coefficient and $A^2=A_1A_2$
and B is the frequency of lead compensation.

The components of gain coefficient are error gradient, integrator gain, and VCO gain. These can be broken down as follows:

- Error Gradient = 0.011 volts per LSB (CT + Error Amp + Demod with 2 Vrms input)

- Integrator Gain = $\frac{Cs\ Fs}{1.1\ C_{BW}}$ volts per second per volt

- VCO Gain = $\frac{1}{1.25\ R_V\ C_{VCO}}$ LSBs per second per volt

where: Cs = 10 pF
Fs = 67 kHz when R CLK = 30 kΩ
C_{VCO} = 50 pF

R_V, R_B, and C_{BW} are selected by the user to set velocity scaling and bandwidth.

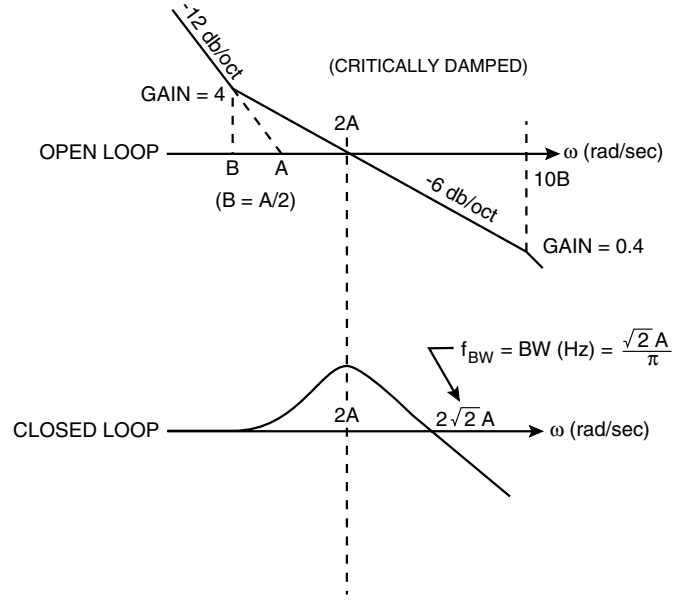


FIGURE 4. BODE PLOTS

GENERAL SETUP CONDITIONS

(Note: For detailed application and technical information see the RDC-19220 & RD-19230 series converter applications manual (Document # MN-19220XX-001) which is available for download from the DDC web site at www-ddc-web.com.)

DDC has external component selection software which considers all the criteria below. In a simple fashion, it asks the key system parameters (carrier frequency, resolution, bandwidth, and tracking rate) needed to derive the external component values.

The following recommendations should be considered when installing the RD-19230 R/D converter:

1) In setting the bandwidth (BW) and Tracking Rate (TR) (selecting five external components), the system requirements need to be considered. For the greatest noise immunity, select the minimum BW and TR the system will allow. Selecting a f_{BW} that is too low relative to the maximum application tracking rate can create a spin-around condition in which the converter never settles. The relationship to insure against this condition is detailed in TABLE 2. Verify your system does not exceed this parts dynamic specs RATIO = RPS/BW. Perform this calculation and verify the ratio does not exceed TABLE 2.

TABLE 2. TRACKING / BW RELATIONSHIP

RPS (MAX)/BW	RESOLUTION
1	10
0.50	12
0.25	14
0.125	16

2) Power supplies are ±5 VDC. For lowest noise performance it is recommended that a 0.1 µF or larger cap be connected from each supply to ground near the converter package. When using +5V and -5V supplies to power the converter, pins 23, 24, 26 and 27 must be no connection.

3) There are two internal ground planes to reduce noise to the analog input due to digital ground currents. The resolver inputs and velocity output are referenced to AGND. The digital inputs and outputs are referenced to GND. The AGND and GND pins must be tied together as close to the package as possible, or unstable results may occur.

4) This device has several high impedance amplifier inputs (+C, -C, +S, -S, -VCO, VEL SJ1, and VEL SJ2) that are sensitive to noise coupling. External components should be connected as close to the converter as possible.

5) Setup of bandwidth and velocity scaling for the optimized critically damped case should proceed as follows:

- Select the desired f_{BW} (closed loop) based on overall system dynamics.

- Select $f_{carrier} \geq 3.5 f_{BW}$

- Select the applications tracking rate (in accordance with TABLE 3), and use appropriate values for R SET and R CLK

- Compute $Rv = \frac{\text{Full Scale Velocity Voltage}}{\text{Tracking Rate (rps)} \times 2^{\text{resolution}} \times 50\text{ pF} \times 1.25\text{ V}}$

- Compute $C_{BW}\text{ (pF)} = \frac{3.2 \times Fs\text{ (Hz)} \times 10^8}{Rv \times (f_{BW})^2}$

- Where Fs = 67 kHz for R CLK = 30 KΩ
  100 kHz for R CLK = 20 KΩ
  125 kHz for R CLK = 15 KΩ

- Compute $R_B = \frac{0.9}{C_{BW} \times f_{BW}}$

- Compute $\frac{C_{BW}}{10}$

As an example:

Calculate component values for a 16-bit converter with 100Hz bandwidth, a tracking rate of 10 RPS and a full scale velocity of 4 Volts.

- $Rv = \frac{4\text{ V}}{10\text{ rps} \times 2^{16} \times 50\text{ pF} \times 1.25\text{ V}} = 97655\ \Omega$

- Compute $C_{BW}\text{ (pF)} = \frac{3.2 \times 67\text{ kHz} \times 10^8}{97655 \times 100\text{ Hz}^2} = 21955\text{ pF}$

- Compute $R_B = \frac{0.9}{21955 \times 10^{-12} \times 100\text{ Hz}} = 410\text{ k}\Omega$

6) Using the -5V Inverter will eliminate the need for a -5 V supply. Refer to FIGURE 5 for the necessary connections.

When using the built-in -5 V inverter, the maximum tracking rate should be scaled for a full-scale velocity output of 3.5 V max.

Notes:

1) Use of the -5 V inverter is not recommended for applications that require the highest BW and Tracking Rates.
2) When using the RD-19230FX with the -5V inverter, the negative velocity output voltage should be limited to -3.5 Volts. When performing tracking rate calculations this must be taken into consideration.

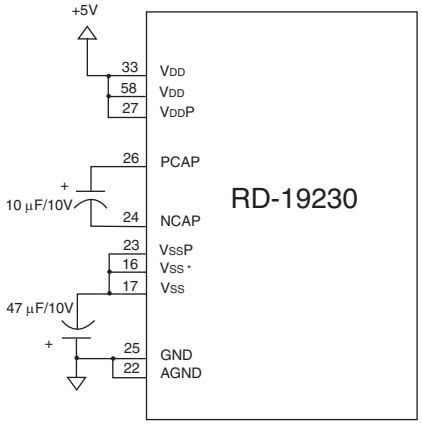
HIGHER TRACKING RATES AND CARRIER FREQUENCIES

Maximum tracking rate is limited by the velocity voltage saturation (nominally 4 V) and the maximum internal clock rate (nominally 1,333,333 Hz for R CLK = 30k). To achieve higher tracking rates, a higher internal counting rate must be programmed by setting RCLK to a value less than 30k. See TABLE 4 for the appropriate values.

Select frequency/resolution from TABLE 4 then reference TABLE 3 for max tracking rate. The Rv resistor and an internal 50pF capacitor are configured as an integrating circuit that resets to zero after a count occurs in either direction. This circuit acts as a VCO with velocity as its input and CB as its output. The Rv resistor and an internal 50pF capacitor determine the maximum rate of the VCO. Rv must be chosen such that the maximum rate of the VCO is less than the maximum internal clock rate. Choose the tracking rate in accordance with TABLE 3 to insure this relationship. The rates shown in TABLE 3 are based on ~90% of the nominal internal clock rate.

The relationship between the velocity voltage and the VCO rate is given by:

$$\frac{\text{Velocity Voltage}}{\text{VCO Frequency}} = \frac{1}{(Rv \times 50\text{ pF} \times 1.25)}$$



* Pin 16 has been renamed Vss since it will typically be connected to -5 VDC. Applications requiring a differential front-end configuration must connect this pin to Vss. Voltage follower mode can be implemented with pin 16 tied to Vss by making external connections between the output of the SIN/COS amplifiers and their respective inputs. When left unconnected, the RD-19230 will internally configure the front-end amplifiers in voltage follower mode.

FIGURE 5. -5V INVERTER CONNECTIONS

INPUT TRANSFORMERS

Refer to TABLE 5 to select the proper transformer for Reference, Synchro and Resolver inputs.

INPUT CONFIGURATION

The converter input can be configured using either transformers or thin film networks per the following tables and figures.

Signal input configuration using thin film networks with a tolerance of 0.02% adds 1 LSB of additional error to accuracy.

Signal input configuration using transformers adds 1 minute of additional error to accuracy.

TABLE 3. MAX TRACKING RATE (MINUTES) IN RPS

RC / RSET (Ω)	RS / RCLK (Ω)	RESOLUTION			
		10	12	14	16
30k** or open	30k	1152	288	72	18
23k	20k	1200	432	108	27
23k	15k	*	576	*	*

* Not recommended.
** The use of a high quality thin-film resistor will provide better temperature stability than leaving open.
Note: RC "Rcurrent" = RSET
RS "Rsample" = RCLK

TABLE 4. CARRIER FREQUENCY (MAX) IN KHZ

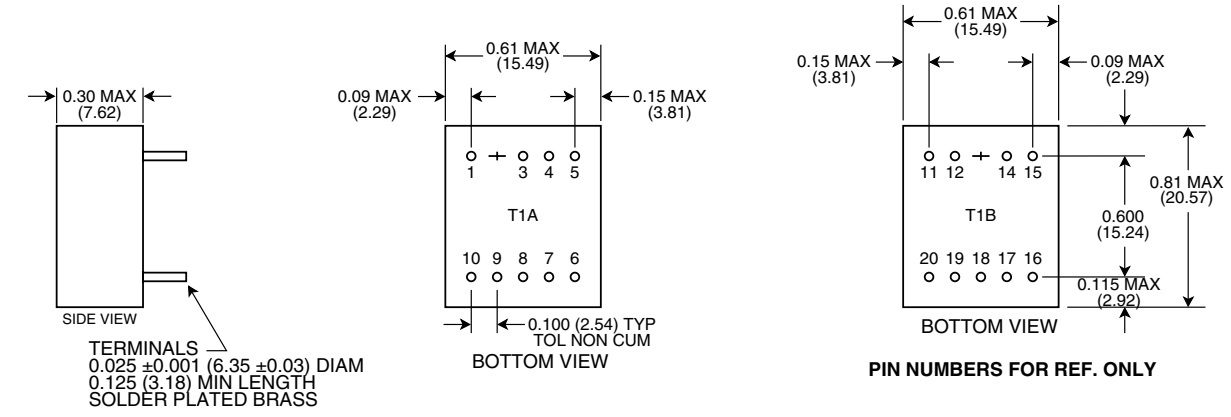
RC / RSET (Ω)	RS/ RCLK (Ω)	RESOLUTION			
		10	12	14	16
30k** or open	30k	10	10	7	5
23k	30k	10	10	10	7
23k	20k	10	10	10	10
23k	15k	10	10	*	*

* Not recommended.
** The use of a high quality thin-film resistor will provide better temperature stability than leaving open.
Note: RC "Rcurrent" = RSET
RS "Rsample" = RCLK

TABLE 5. TRANSFORMERS

P/N	TYPE	FREQUENCY (HZ)*	IN (VRMS)*	OUT (VRMS)**	ANGLE ACCURACY***	LENGTH (IN)	WIDTH (IN)	HEIGHT (IN)	FIGURE NUMBER
52034	S - R	400	11.8	2	1	0.81	0.61	0.3	6
52035	S - R	400	90	2	1	0.81	0.61	0.3	6
52036	R - R	400	11.8	2	1	0.81	0.61	0.3	7
52037	R - R	400	26	2	1	0.81	0.61	0.3	7
52038	R - R	400	90	2	1	0.81	0.61	0.3	7
B-426	Reference	400	115	3.4	N/A	0.81	0.61	0.32	8
52039-X	Synchro	60	90	2	1	1.1	1.14	.42	9
24133-X	Reference	60	115	3/6 ****	N/A	1.125	1.125	.42	9

* ±10% Frequency (Hz) and Line-to-Line input voltage (Vrms) tolerances
** 2 Vrms Output Magnitudes are -2 Vrms ±0.5% full scale
*** Angle Accuracy (Max Minutes)
**** 3 Vrms to ground or 6 Vrms differential (±3% full scale)
Dimensions are for each individual main and teaser
60 Hz Synchro transformers are active (requires ±15 Vdc power supplies)
400 Hz transformer temperature range: -55°C to +125°C
60 Hz transformer (52039-X, 24133-X) temperature ranges: add to part number -1 or -3,
-1 = -55°C to +85°C
-3 = 0 to +70°C
The following transformers can be ordered directly from DDC, Tel (631) 567-5600:
P/N 52039-X, 24133-X
The following transformers can be ordered directly from Beta Transformer Technology Corporation (BTTC), Tel (631) 244-7393:
P/N 52034, 52035, 52036, 52037, 52038, and B-426.



Dimensions are shown in inches (mm).

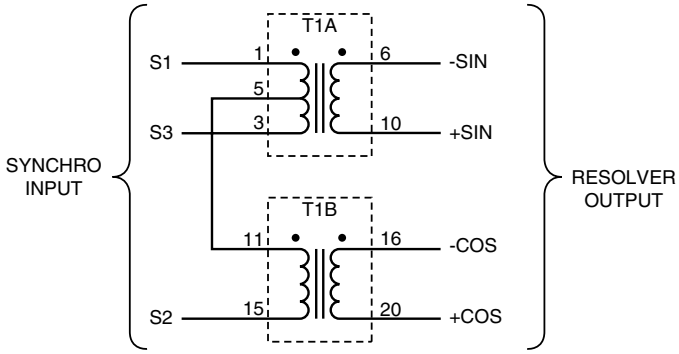
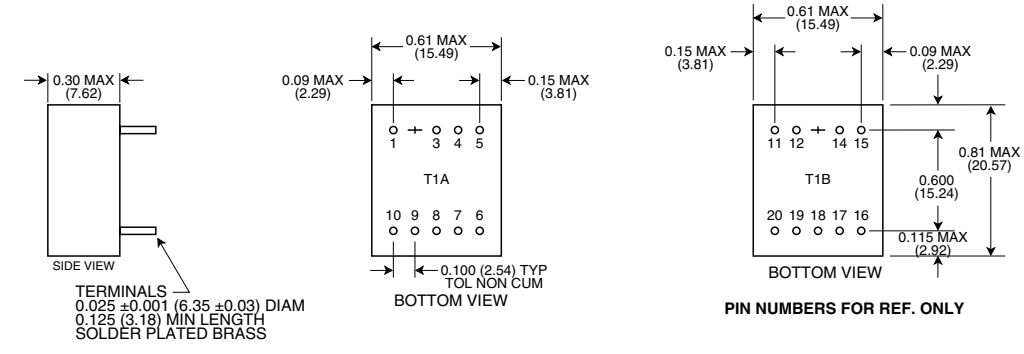


FIGURE 6. TRANSFORMER LAYOUT AND SCHEMATIC (SYNCHRO INPUT - 52034/52035)



Dimensions are shown in inches (mm).

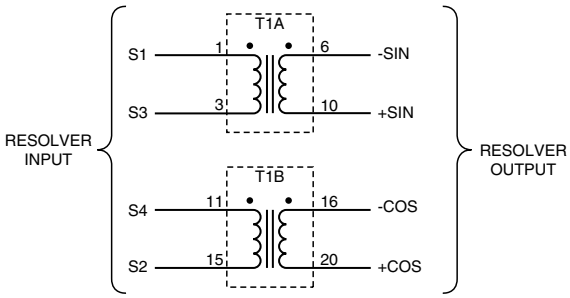
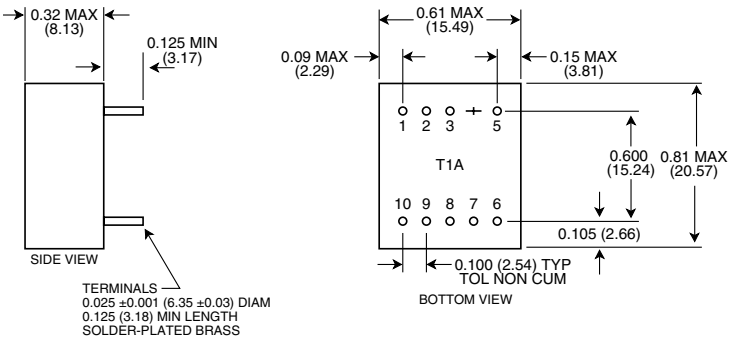


FIGURE 7. TRANSFORMER LAYOUT AND SCHEMATIC (RESOLVER INPUT - 52036/52037/52038)



Dimensions are shown in inches (mm).

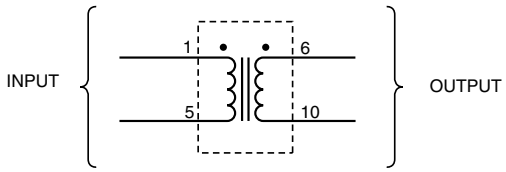
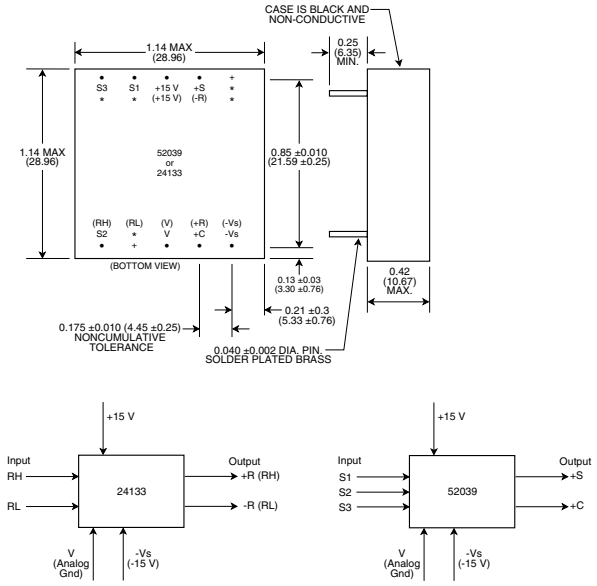


FIGURE 8. TRANSFORMER LAYOUT AND SCHEMATIC (REFERENCE INPUT - B-426)

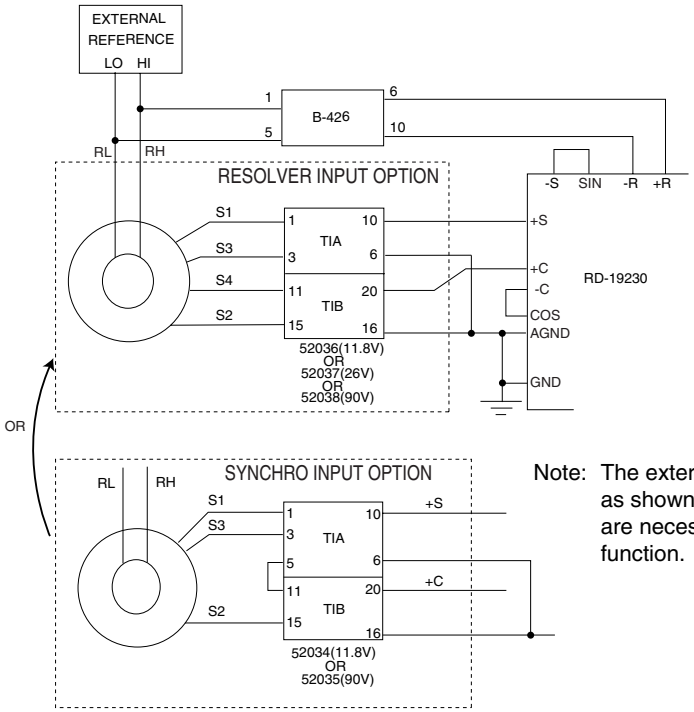


The mechanical outline is the same for the synchro input transformer (52039) and the reference input transformer (24133), except for the pins. Pins for the reference transformer are shown in parenthesis ( ) below. An asterisk * indicates that the pin is omitted.

FIGURE 9. 60 HZ SYNCHRO AND REFERENCE TRANSFORMER DIAGRAMS (SYNCHRO INPUT - 52039 / REFERENCE INPUT - 24133)

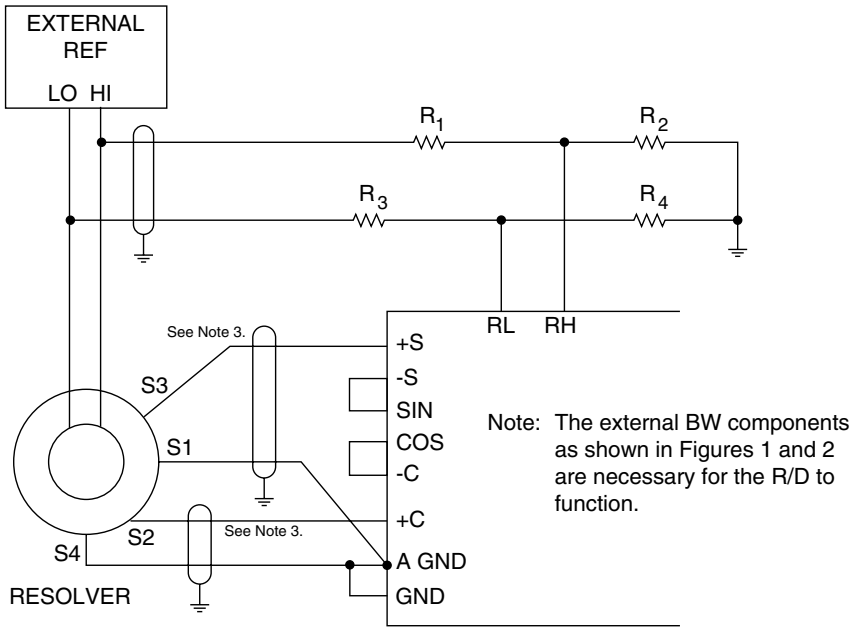
TYPICAL INPUTS

FIGURES 10 through 14 illustrate typical input configurations.



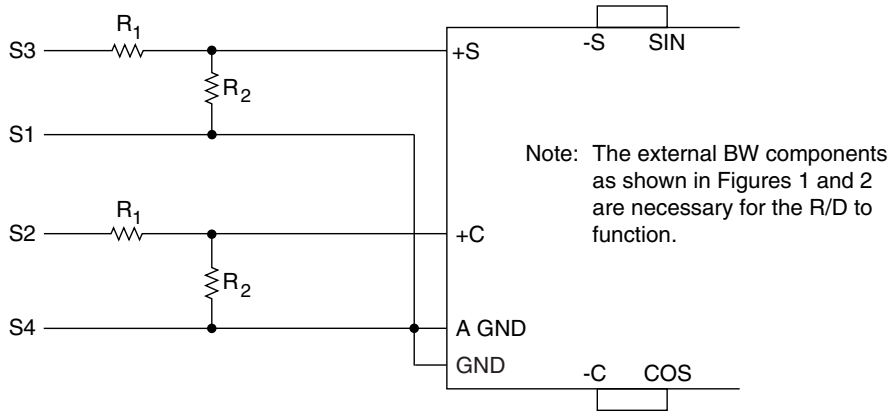
Note: The external BW components as shown in Figures 1 and 2 are necessary for the R/D to function.

FIGURE 10. TYPICAL TRANSFORMER CONNECTIONS



1) Resistors selected to limit Vref peak to between 1.5 V and 5 V.
2) External reference LO is grounded, then R3 and R4 are not needed, and -R is connected to GND.
3) 10k ohms, 1% series current limit resistors are recommended.

FIGURE 11. TYPICAL CONNECTIONS, 2 V RESOLVER, DIRECT INPUT

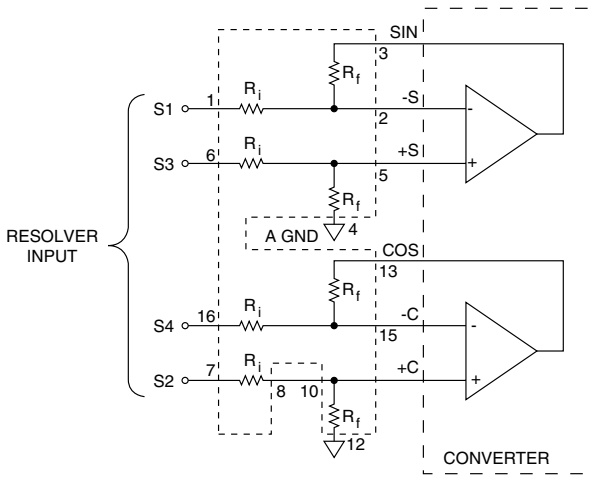


$$\frac{R_2}{R_1 + R_2} = \frac{2}{X\ Volt}$$

$R_1 + R_2$ should not load the Resolver; it is recommended to use an $R_2 = 10\ k\Omega$

$R_1 + R_2$ Ratio errors will result in Angular errors,
2 cycle, 0.1% Ratio error = 0.029° Peak Error.

FIGURE 12. TYPICAL CONNECTIONS, X- VOLT RESOLVER, DIRECT INPUT



Examples of Component Calculations:
(1) 2V in, need gain of 1, use 10k for R1 &R2
Gain = $\frac{RF}{Ri}$
(2) 4V in, need gain of 0.5, Ri = 20k, Rf = 10k

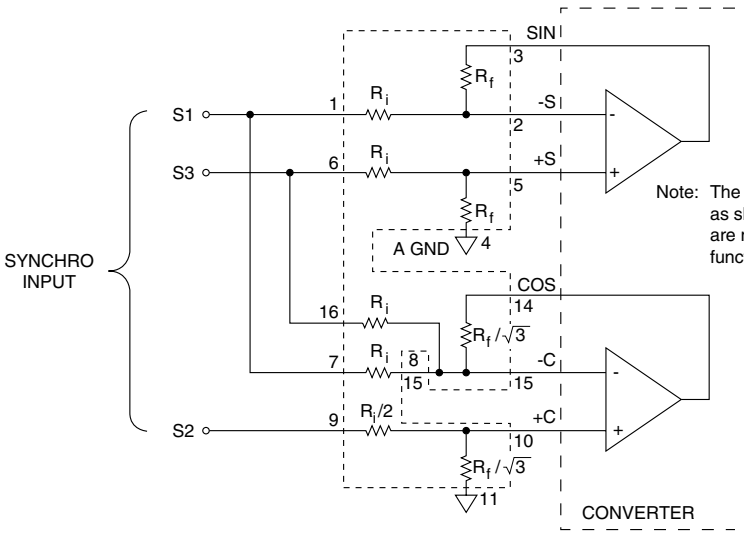
To Calculate Ri:
Select 10k for Rf
Ri = Rf x 0.5 (input L-L volt)
Ri = 10k x 0.5 x (L-L volt)

Note: The external BW components as shown in Figures 1 and 2 are necessary for the R/D to function.

S1 and S3, S2 and S4, and RH and RL should be ideally twisted shielded, with the shield tied to GND at the converter.
For DDC-49530: R_i = 70.8 KΩ, 11.8 V input, synchro or resolver.
For DDC-49590: R_i = 270 KΩ, 90 Volt input, synchro or resolver.
Maximum additional error is 1 minute.
When using discrete resistors: Resolver L-L voltage = $\frac{R_i}{R_f}$ x 2 Vrms, where $R_f \geq 6$ kΩ.
For 2V direct input, use 10kΩ matched resistors for Ri and Rf.

Input options affect DC offset gains and therefore carrier frequency ripple and jitter. Offset gains associated with differential mode (offset gain for differential configuration = 1+Rf/Ri) and direct mode (offset gain for direct configuration = 1) show differential mode will always be higher. Higher DC offsets cause higher carrier frequency ripple due to the demodulation process. This carrier frequency ripple rides on top of the DC error signal, causing jitter. A higher carrier frequency versus bandwidth ratio will help to decrease ripple and jitter associated with offsets. In summary, R/Ds with differential inputs are more susceptible to offset problems than R/Ds in single-ended mode. R/Ds in higher resolutions, such as 16 bit, will further compound offset issues due to higher internal voltage gains. Although the differential configuration has a higher DC offset gain, the differential configuration's common mode noise rejection makes it the preferred input option. The tradeoffs should be considered on a design to design basis.

FIGURE 13. DIFFERENTIAL RESOLVER INPUT, USING DDC-49530/57470 (11.8 V) OR DDC-49590 (90 V), DDC-73089 (2 V) USING DISCRETE RESISTORS



Note: The external BW components as shown in Figures 1 and 2 are necessary for the R/D to function.

S1, S2, S3 should be triple twisted shielded; RH and RL should be twisted shielded;
In both cases the shield should be tied to GND at the converter.
11.8 Volt input = DDC-49530: R_i = 70.8 KΩ, 11.8 V input, synchro or resolver.
90 Volt input = DDC-49590: R_i = 270 KΩ, 90 Volt input, synchro or resolver.
Maximum additional error is 1 minute using recommended thin film package.
When using discrete resistors: Resolver L-L voltage = $\frac{R_i}{R_f}$ x 2 Vrms, where $R_f \geq 6$ kΩ

FIGURE 14. SYNCHRO INPUT, USING DDC-49530/57470 (11.8 V), DDC-49590 (90 V) OR DDC-73089 (2V)

DC INPUTS

As noted in TABLE 1, the RD-19230 accepts DC inputs. DC input operation is from 0° to 180° or 180° to 359° only, due to the possibility of an unstable false null, i.e., 180° hangup. The false null condition will only happen on power up and an instantaneous 180° step, therefore once the converter moves it will go to the correct answer. In real world applications where an instantaneous 180° change is impossible, the converter will always be correct within 360°. The problem arises at power up in real systems. If the converter powers up at exactly 180° from the applied input, the converter will not move. This is very unlikely, although it is theoretically possible. This condition is most often encountered during wraparound verification tests, simulations, or troubleshooting.

It is recommended that the synthesized reference option be disabled for DC input operation. Disable the synthesized reference by connecting pin 52, $\overline{DSR}$, to ground through a 10 ohm resistor.

The reference input is set to DC by tying RH to +5V and RL to ground or -5V.

Set the COS and SIN inputs such that the maximum signal is equal to 1.8VDC. For example, at 90° the SIN input should equal to 1.8VDC. This will keep the BW hysteresis consistent with AC operation.

Input offsets will affect accuracy. Verify the COS and SIN inputs do not have DC offsets. If offsets are present, a differential op amp configuration can be used to minimize differential offset problems.

When operating with DC inputs the converter BIT will remain at Logic 0.

Choose the bandwidth value of the converter based on the rate of change of the systems input amplitude variation. It should be large enough to minimize it's effect on the system dynamics. Note that if the bandwidth is too high the system will be more susceptible to noise.

The accuracy of a converter using a DC input will be degraded from the rated accuracy. Consider the best case where the input is single ended and no additional DC offsets are present on the input of the converter - the accuracy will degrade by about 2 arc minutes. For example, if a part is rated at 2 arc minutes, a DC input will degrade the accuracy to approximately 4 arc minutes.

VELOCITY TRIMMING

The RD-19230 specifications for velocity scaling, reversal error, and offset are listed in TABLE 1. Velocity scaling and offset are externally trimmable for applications requiring tighter specifications than those available from the standard unit. FIGURE 15 shows the setup for trimming these parameters with external pots. It should also be noted that when the resolution is changed, velocity scaling is also changed.

OPTIONAL BANDWIDTH COMPONENTS

The RD-19230 provides the option of using a second set of bandwidth components. The second set of components can be used for switch-on-the-fly or dual-bandwidth applications. The SHIFT and $\overline{UP}$/DN inputs are used when switching bandwidth components, and their operation is described below. Refer to the block diagram, FIGURE 1.

SHIFT

The SHIFT pin is an input that chooses between the VEL1 and VEL2 bandwidth components. This pin has an internal pull-up to +5V. When the SHIFT pin is left open, or a logic 1 is applied, the VEL1 components are selected. When a Logic 0 is applied, the VEL2 components are selected. The deselected set of bandwidth components are driven by an amplifier, with programmable gain, that follows the velocity amplifier. This amplifier can be used to precharge the deselected set of components to the voltage level that is expected after a change in resolution. (See description on BENEFIT OF SWITCHING RESOLUTION ON THE FLY.)

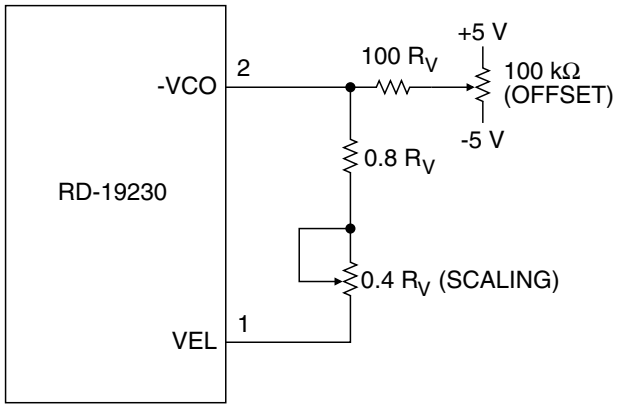


FIGURE 15. VELOCITY TRIMMING

TABLE 6. PRECHARGE AMPLIFIER GAIN PROGRAMMING		
UP/DN	**GAIN**	**FUNCTION**
Logic 0	4	preset resolution to increase
Logic 1	1/4	preset resolution to decrease
-5 V	1	dual bandwidth

$\overline{UP}$/DN

The $\overline{UP}$/DN input selects the gain of the amplifier driving the deselected set of bandwidth components. $\overline{UP}$/DN has three input states. See TABLE 6 to relate input to gain.

BENEFIT OF SWITCHING RESOLUTION ON THE FLY

Switching resolution on the fly can be used in applications that require high resolution for accurate position control, and tracking rates or settling times that are faster than the high resolution mode will allow.

The RD-19230 can track four times faster for each step down in resolution (i.e., a step from 16 bits to 14 bits). The velocity output will be scaled down by a factor of four with each step down in resolution. For example, if the velocity output is scaled such that 4 Volts = 10 RPS in 16 bit resolution, then the same converter will output 1 Volt for 10 RPS in 14 bit resolution. To avoid glitches in the velocity output, the second set of bandwidth components can be precharged to the expected voltage, and switched in using the SHIFT input at the same time the resolution is changed. This will allow for a smooth velocity transition, resulting in reduced errors and minimal settling time after the change.

FIGURE 17 shows the way the converter behaves during a change in resolution while tracking at a constant velocity. The first illustration shows the benefits of switching in precharged components while changing resolution. The second illustration shows the result without the benefits of switching on the fly.

The signals that have been recorded are:

1) VEL: velocity output pin on the RD-19230

2) ERROR: this is the analog representation of the error between the input and the output of the RD-19230

3) D0: an input resolution control line to the RD-19230

4) $\overline{BIT}$: built-in-test output pin of the RD-19230

When this system uses the switch resolution on the fly implementation, the velocity signal immediately assumes the precharged level of the second set of components, resulting in small errors and reduced settling times. Notice that the $\overline{BIT}$ output in FIGURE 17, does not indicate a fault condition.

When this system type does not use the switch resolution on the fly implementation, large errors and increased settling times result. The errors exceed 100 LSBs causing the $\overline{BIT}$ to flag for a fault condition.

SWITCH ON THE FLY IMPLEMENTATION

The following steps detail switching resolution on the fly. For additional information refer to the Application Note #AN/MFT-3 “SWITCHING RESOLUTIONS ON THE FLY” available on the DDC web site at www.ddc-web.com.

1) The SHIFT pin should be controlled synchronously with the change in resolution. When shift is logic high, the VEL1 components will be selected. When shift is logic 0, the VEL2 components will be selected.

2) The second set of BW components (C_{BW2}, R_{B2}, $C_{BW2/10}$) should typically be of the same value as the first set (C_{BW1}, R_{B1}, $C_{BW1/10}$,) and should be installed on VEL_2 and VEL SJ_2.

Note: Each set of bandwidth components must be chosen to insure that the tracking rate to BW ratio (listed in TABLE 2) is not exceeded for the resolution in which it will be used.

3) The $\overline{UP}$/DN line programs the gain of the precharged components/amplifier. If the resolution is increasing ($\overline{UP}$/DN logic 0), the gain of the precharge amplifier is set to four. If the resolution is decreasing ($\overline{UP}$/DN logic 1), the gain of the precharge amplifier is set to 1/4. The gain of the precharge amplifier should be programmed prior to switching the resolution of the converter, allowing enough time for the components to settle to the precharged level. This time will depend on the time constant of the bandwidth components being charged. If switching is limited to two adjacent resolutions (i.e., 14 and 16) then the precharge amplifier can be set up to continuously maintain the appropriate velocity voltage on the deselected components, resulting in the fastest possible switching times. See

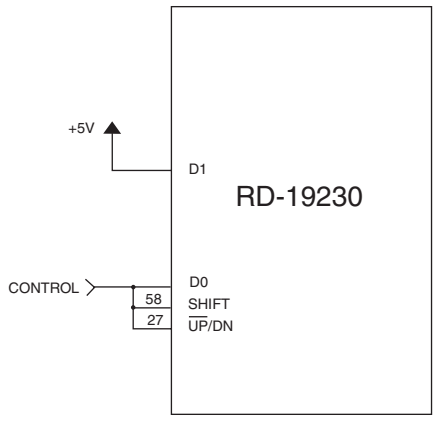


FIGURE 16. INPUT WIRING - SWITCHING ON THE FLY BETWEEN 14 AND 16 BIT RESOLUTION

FIGURE 16 for an example of the input wiring connections necessary for switching on the fly between 14 and 16 bit resolution.

DUAL BANDWIDTHS

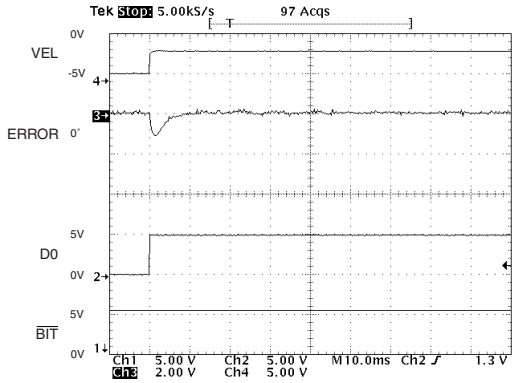
With the second set of BW component pins, the user can set two bandwidths for the RD-19230 and choose between them. To use two bandwidths, proceed as follows:

1) Tie $\overline{UP}$/DN to pin -5V.

2) Choose the two bandwidths following the guidelines in the General Setup Considerations; the R_V resistor must be the same value for both bandwidths.

3) Use the SHIFT pin to choose between bandwidths. A logic 1 selects the VEL1 components and a logic 0 selects the VEL2 components.

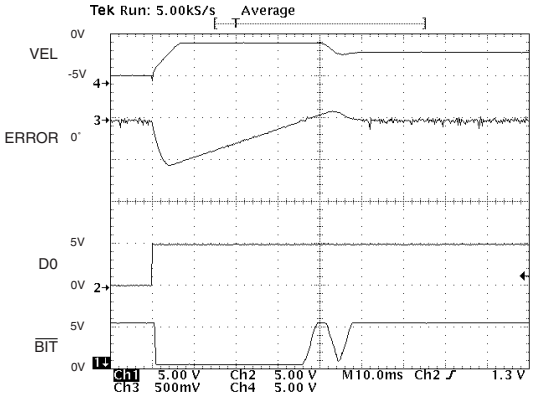
With Switch Resolution on the Fly Implemented



ERROR = 13.6 LSBs per box

Depending on the bandwidth, the step error may be greater. Also, less velocity / movement will lessen the error glitch. The graphs above shows a worst case condition based on one bandwidth and tracking rate setup. Worst case is when the velocity overshoot hits the saturations point.

Without Switch Resolution on the Fly Implemented



ERROR = 1500 LSBs per box

FIGURE 17. BENEFIT OF SWITCHING RESOLUTION ON THE FLY

INHIBIT, ENABLE, AND CB TIMING

The Inhibit ($\overline{INH}$) signal is used to freeze the digital output angle in the transparent output data latch while data is being transferred. Application of an Inhibit signal does not interfere with the continuous tracking of the converter. As shown in FIGURE 18, angular output data is valid 150 ns maximum after the application of the negative inhibit pulse.

Output angle data is enabled onto the tri-state data bus in two bytes. Enable MSBs ($\overline{EM}$) is used for the most significant 8 bits and Enable LSBs ($\overline{EL}$) is used for the least significant 8 bits. As shown in FIGURE 19, output data is valid 150 ns maximum after the application of a negative enable pulse. The tri-state data bus returns to the high impedance state 100 ns maximum after the rising edge of the enable signal.

The Converter Busy (CB) signal indicates that the tracking converter output angle is changing 1 LSB. As shown in FIGURE 20, output data is valid 50 nS maximum after the middle of the CB pulse. CB pulse width is 1/40 F_S, which is nominally 375 ns.

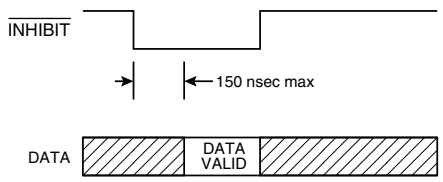
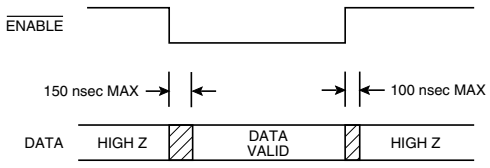


FIGURE 18. INHIBIT TIMING



For 16-bit bus, EM/EL may be tied to ground for transparent mode, as long as only 1 R/D channel is used on the data bus.

FIGURE 19. ENABLE TIMING

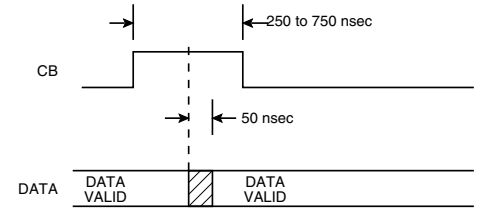


FIGURE 20. CONVERTER BUSY TIMING

Note: The converter $\overline{INH}$ may be applied regardless of the CB line state. If the CB is busy the converter $\overline{INH}$ will wait for timing referenced to CB (Fig.20), before setting the $\overline{INH}$ latch. Therefore when applying an inhibit signal to the converter there is no need to monitor the CB line.

INTERNAL ENCODER EMULATION

The RD-19230 can be programmed to encoder emulation mode by toggling the A_QUAD_B input to a logic 0. The U/B output pin becomes B (LSB XOR LSB + 1). The A (LSB + 1) and B output signals can be used in control systems that are designed to interface with incremental optical encoders. To enable the Zero Index pulse, ZIP_EN should be tied to a logic 0.

An example circuit to create a low going edge of A_QUAD_B is depicted in Figure 23B. If the power supply takes longer than 50ms to start up then the time constant of 50ms set in FIGURE 23B must be extended. Alternatively a system logic reset signal or internally generated logic 'load' pulse can be generated to latch in the encoder resolution.

The resolution of the incremental outputs is latched from the D0 and D1 inputs on the low going edge of A_QUAD_B. The resolution of the parallel data outputs may be changed any time after the encoder resolution is latched (see FIGURE 23).

When in A_QUAD_B mode, the resolution of the parallel data can be changed to a resolution equal to or greater than the A_QUAD_B resolution setting only. For example if the A_QUAD_B mode is active and the resolution is set to 12 bits, the resolution of the parallel programmed data can be changed from 12 bits to 14- or 16-bits by setting D0 & D1. If 10-bit mode is required for the parallel data, the A_QUAD_B resolution must also be programmed to 10-bits.

Note: The encoder resolution must be less than or equal to the resolution of the parallel data outputs. Refer to FIGURE 21.

The timing of the A, B and ZIP (or North Reference Pole [NRP]) output is dependent on the rate of change of the synchro/resolver position (rps or degrees per second) and the encoder resolution latched into the RD-19230 (refer to FIGURE 22). The calculations for the timing are:

n = resolution of parallel data

$t = 1 / (2^{n*} \text{ Velocity(RPS)})$

T = 1 / (Velocity(RPS))

Note: The Z1 pulse is high when all the bits of the counter are zero. If the resolution of the counter, (parallel data) is programmed differently than that of the A_QUAD_B then the resolution of the counter will determine the resolution of the ZIP.

CLARIFICATION OF A_QUAD_B, U/B AND ZIP_EN FUNCTIONS

The RD-19230 is a tracking converter which is designed with a Type II closed servo loop. The Type II closed servo loop has an internal incremental integrator. This integrator acts as an up-down position counter. An AC error (e) within the RD-19230 represents the difference between θ (current angle to be digitized) and ϕ (the angle stored in digital form in the up-down counter). Because the RD-19230 constitutes in itself a Type II closed loop servomechanism, it continuously attempts to null the error to zero. This is accomplished by counting up or down 1 LSB until ϕ is equal to θ thus having an error of zero.

TABLE 7. A_QUAD_B (PIN 30) FUNCTION

A_QUAD_B (PIN 30)	U/B (PIN 29)
0	B
1	U

TABLE 8. ZIP_EN (PIN 55) FUNCTION

ZIP_EN (PIN 55)	CB/ZI (PIN 31)
0	ZI
1	CB

When A_QUAD_B is logic 0, encoder emulation mode is selected (i.e. The U/B output [Pin 29] is programmed to B). The encoder emulator resolution is set on the falling edge of A_QUAD_B (see TABLE 7).

When A_QUAD_B is logic 1, encoder emulation mode is not selected (i.e. The U/B output is set to U, which indicates the direction of the internal position counter).

Note: U indicates the "UP" direction of the counter. If the RD-19230 is at a static angle awaiting a new angle θ, U indicates the direction the counter was going to get to the current angle ϕ. As the error is approaching zero, the internal analog circuitry voltage may overshoot before settling - which would then indicate an incorrect direction. Because of this overshoot, the U output should not be relied on after settling to a static state. Only during active resolver movement will the U output state be reliable. U is a logic 1 when going in the positive direction (increasing angle). It is a logic 0 when going in the negative direction (decreasing angle).

ZIP_EN chooses between the CB and Zero Index pulse outputs and is independent of encoder emulation mode. A logic 1 enables the CB pulse, a logic 0 enables the Zero Index pulse (see TABLE 8).

Note: When the RD-19230FX is set for 16-bit mode, the LSB is bit 16. When the RD-19230FX is set for 14-bit mode, the LSB is bit 14 and bits 15 and 16 are set to logic "0". (See TABLE 1, NOTE 1).

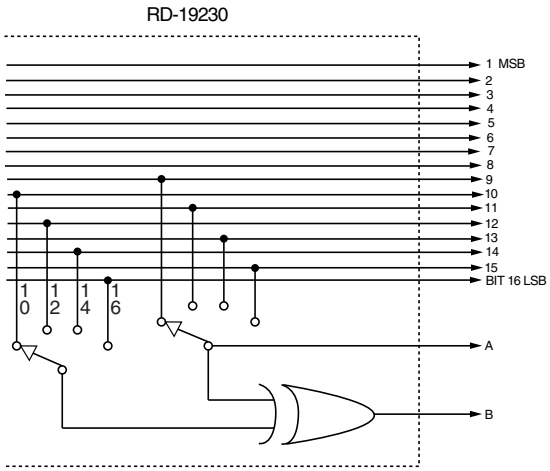


FIGURE 21. INCREMENTAL ENCODER EMULATION RESOLUTION CONTROL

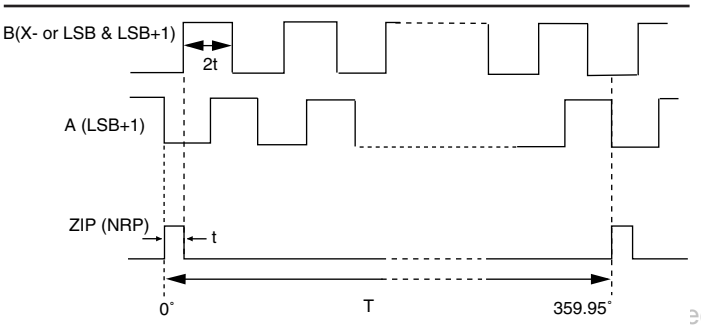


FIGURE 22. INCREMENTAL ENCODER EMULATION

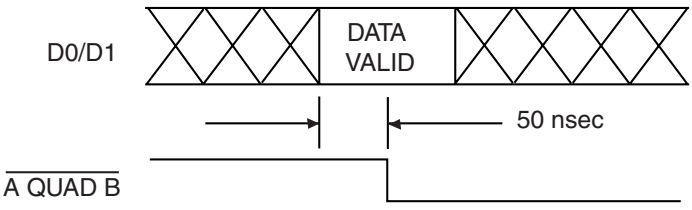
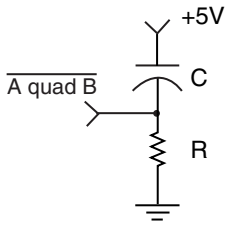


FIGURE 23A. TIMING FOR INCREMENTAL ENCODER EMULATION RESOLUTION CONTROL



$\tau = RC$

(ie. 50ms = 50Kohms x 1µf)

FIGURE 23B. EXAMPLE CIRCUIT FOR A QUAD B RESET

SYNTHESIZED REFERENCE

The synthesized reference section of the RD-19230 eliminates errors due to phase shift between the reference and signal inputs. Quadrature voltages in a resolver or synchro are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. Due to the inductive nature of synchros and resolvers, their output signals lead the reference input signal (RH and RL). When an uncompensated reference signal is used to demodulate the control transformer's output, quadrature voltages are not completely eliminated. As shown in the block diagram, FIGURE 1, the converter synthesizes its own internal reference signal based on the SIN and COS signal inputs. Therefore, the phase of the synthesized (internal) reference is determined by the signal input, resulting in reduced quadrature errors.

BUILT-IN-TEST ($\overline{\text{BIT}}$)

The $\overline{\text{BIT}}$ output is active low, and is triggered if any of the following conditions exist:

1) Loss of Signal (LOS) - SIN and COS inputs both less than 500mV.

2) Loss of Reference (LOR) - Reference Input less than 500 mV.

3) Excessive Error - This error is detected by monitoring the demodulator output, which is proportional to the difference between the analog input and digital output. When it exceeds approximately 100 LSBs (in the selected resolution), $\overline{\text{BIT}}$ will be asserted. This condition can occur any time the analog input changes at a rate in excess of the maximum tracking rate. During power up, the converter may see a large difference between the SIN/COS inputs and the digital output angle held in its counter. $\overline{\text{BIT}}$ will be asserted until the converter settles within ~ 100 LSB's of the final result.

4) 180° phase error input signal to reference input (false null) causes a BIT plus kickstarts the converter counter to correct the error.

The LOS has a filter on it to filter out the reference. Since the lowest specified reference frequency is 47 Hz (~21 ms), the filter must have a time constant long enough to filter this out. Time constants of 50 ms or more are possible.

A 500 µs dynamic delay occurs before the error $\overline{\text{BIT}}$ becomes active. This dynamic delay is responsive to the active filter loop.

LVDT MODE

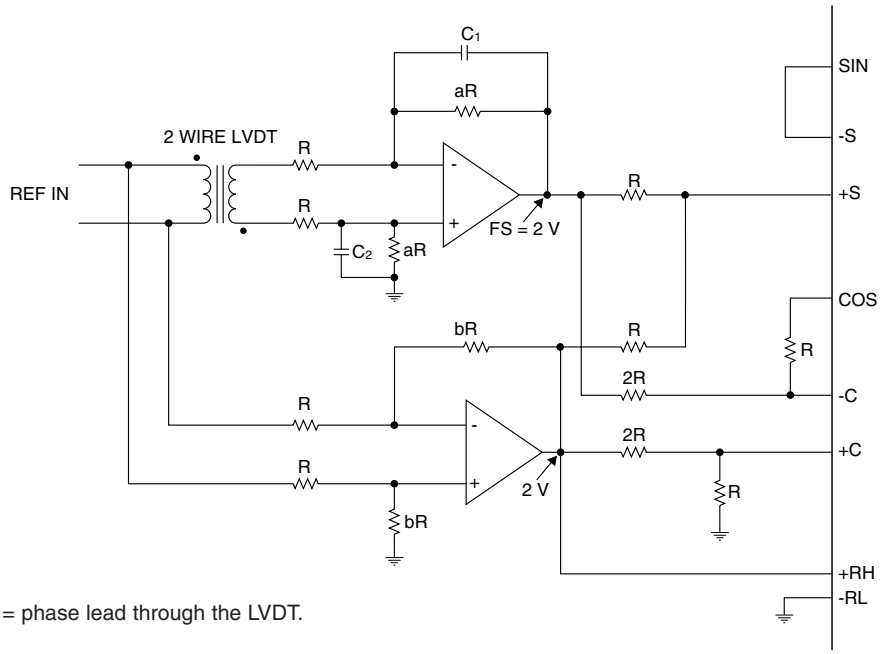
As shown in TABLE 1, the RD-19230 unit can be made to operate as an LVDT-to-digital converter. In this mode the RD-19230 functions as a ratiometric tracking linear converter. When linear AC inputs are applied from a LVDT the converter operates over one quarter of its range. This results in two less bits of resolution for LVDT mode than are provided in resolver mode.

LVDT output signals need to be scaled to be compatible with the converter input. FIGURE 25 is a schematic of an input scaling circuit applicable to 3-wire LVDTs. The value of the scaling constant "a" is selected to provide an input of 2 Vrms at full stroke of the LVDT. The value of scaling constant "b" is selected to provide an input of 1 Vrms at null of the LVDT. Suggested components for implementing the input scaling circuit are a quad op-amp, such as a OP11 type, and precision thin-film resistors of 0.1% tolerance. FIGURE 24 illustrates a 2-wire LVDT configuration.

Data output of the RD-19230 is Binary Coded in LVDT mode. The most negative stroke of the LVDT is represented by ALL ZEROS and the most positive stroke of the LVDT is represented by ALL ONES. The most significant 2 bits (2 MSBs) may be used as overrange indicators. Positive overrange is indicated by code "01" and negative overrange is indicated by code "11" (see TABLE 9).

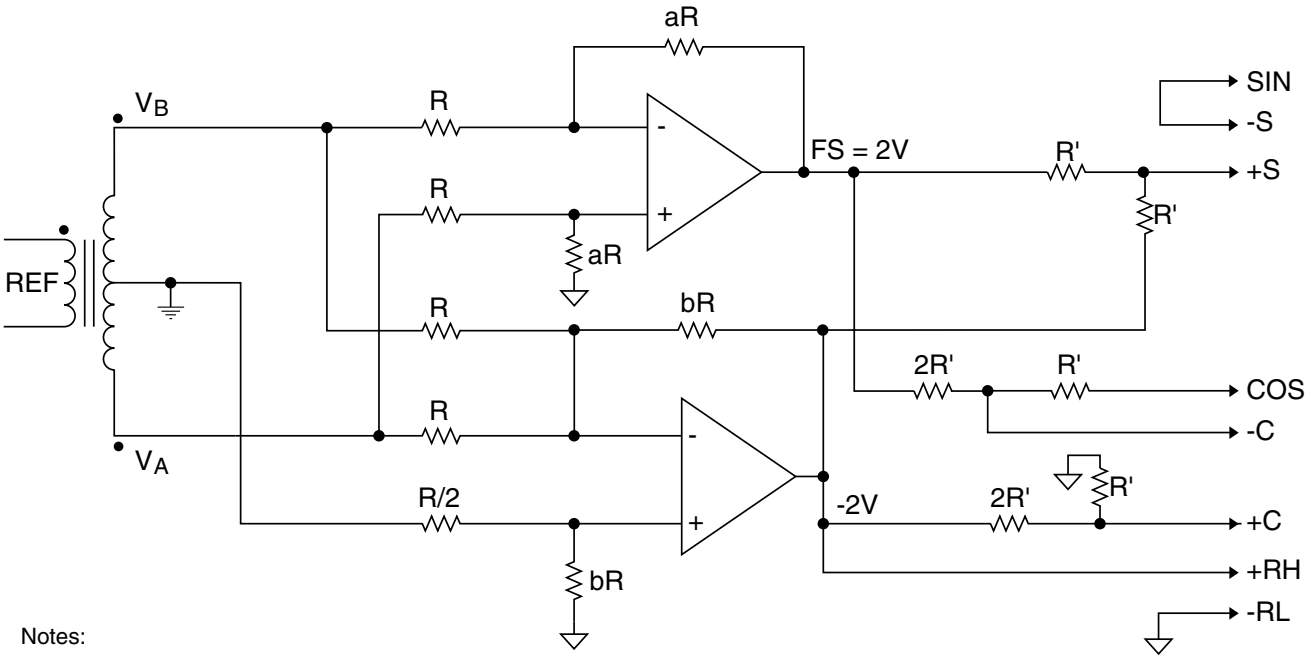
TABLE 9. 12-BIT LVDT OUTPUT CODE FOR FIGURE 25

LVDT OUTPUT	OVER RANGE	MSB DATA		LSB
+ over full travel	01	xxxx	xxxx	xxxx
+ full travel -1 LSB	00	1111	1111	1111
+0.5 travel	00	1100	0000	0000
+1 LSB	00	1000	0000	0001
null	00	1000	0000	0000
- 1 LSB	00	0111	1111	1111
-0.5 travel	00	0100	0000	0000
- full travel	00	0000	0000	0000
- over full travel	11	xxxx	xxxx	xxxx



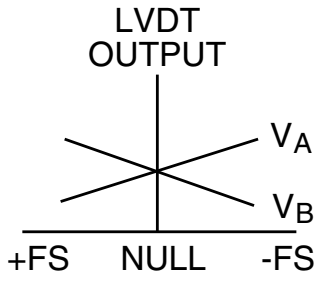
$C_1 = C_2$, set for phase lag = phase lead through the LVDT.

FIGURE 24. 2-WIRE LVDT DIRECT INPUT



Notes:

1. R' $\geq$ 10 kΩ
2. Consideration for the value of R is LVDT loading.
3. RMS values given.
4. Use the absolute values of Va and Vb when subtracting per the formula for calculating resistance values, and then use the calculated sign of "Va and Vb" for calculating SIN and COS. The calculations shown are based upon full scale travel being to the Va sideof the LVDT.
5. See the RDC application manual for calculation examples.
6. Negative voltages are 180 degrees phase from reference.



$$b = \frac{1}{V_{Anull}} = \frac{1}{V_{Bnull}}$$

$$a = \frac{2}{(V_A - V_B)_{max}}$$

$$SIN = -1V + \frac{a}{2}(V_A - V_B)$$

$$COS = -1V - \frac{a}{2}(V_A - V_B)$$

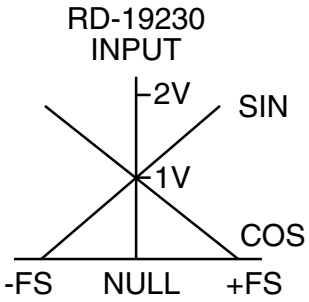


FIGURE 25. 3-WIRE LVDT SCALING CIRCUIT & CALCULATIONS

TABLE 10. RD-19230 PINOUTS							
#	NAME	#	NAME	#	NAME	#	NAME
1	VEL	17	VSS (-5V)	33	VDD (+5V)	49	Bit 8
2	-VCO	18	TP3 (test point)	34	N/C	50	Bit 16 (LSB)
3	SJ1	19	R CLK	35	Bit 9	51	A (LSB + 1)
4	SJ2	20	R SET	36	Bit 2	52	$\overline{\text{DSR}}$
5	SHIFT	21	$\overline{\text{ENM}}$	37	Bit 10	53	N/C
6	VEL2	22	AGND	38	Bit 3	54	N/C
7	TP1 (test point)	23	VSSP	39	Bit 11	55	$\overline{\text{ZIP\_EN}}$
8	VEL1	24	NCAP	40	Bit 4	56	TP6 (test point)
9	TP2 (test point)	25	GND	41	N/C	57	$\overline{\text{ENL}}$
10	+C	26	PCAP	42	Bit 12	58	VDD (+5V)
11	COS	27	VDDP	43	Bit 5	59	$\overline{\text{UP}}$/DN
12	-C	28	$\overline{\text{BIT}}$	44	Bit 13	60	D0
13	+S	29	U/B	45	Bit 6	61	D1
14	SIN	30	$\overline{\text{A\_QUAD\_B}}$	46	Bit 14	62	$\overline{\text{INH}}$
15	-S	31	CB (ZI)	47	Bit 7	63	RH
16	VSS (-5V)	32	Bit 1 (MSB)	48	Bit 15	64	RL

NOTES:
1. See FIGURE 5 for +5 V only operation.
2. Unless otherwise specified, pins TP1 through TP4 are for factory use only, and should be left unconnected.

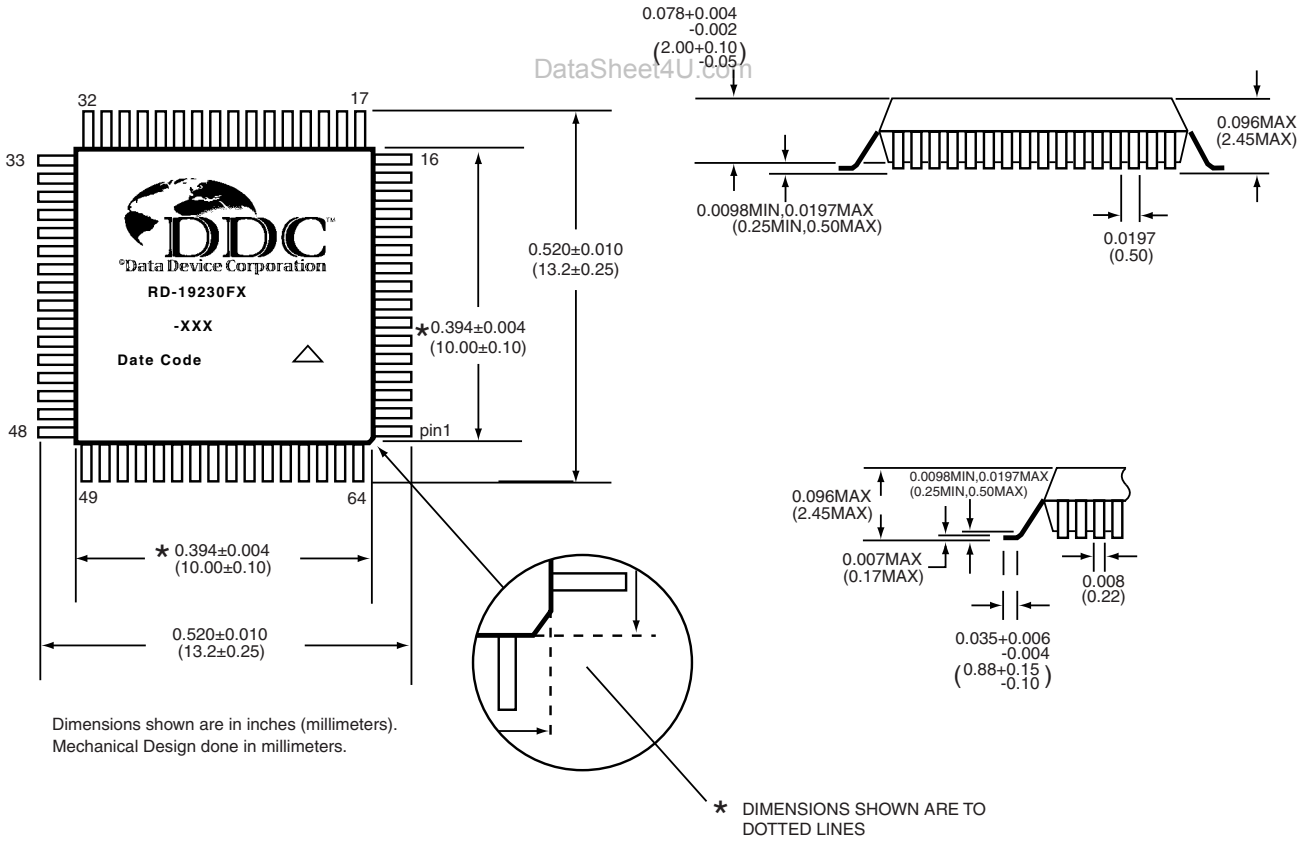


FIGURE 26. RD-19230 MECHANICAL OUTLINE (PLASTIC PACKAGE)

THIN-FILM RESISTOR NETWORKS

FOR MOTION FEEDBACK PRODUCTS

DDC converters such as the RDC-19220/2S and RD-19230 require closely matched 2Vrms SIN/COS input voltages to minimize digital error. DDC has custom thin-film resistor networks that provide the correctly matched 2Vrms converter outputs for 11.8Vrms Resolver/Synchro or 90Vrms synchro applications.

Any imbalance of the resistance ratio between the SIN/COS inputs will create errors in the digital output. DDC's custom thin-film resistor networks have very low imbalance percentages. The networks are matched to 0.02%, which equates to 1 LSB of error for a 16-bit application.

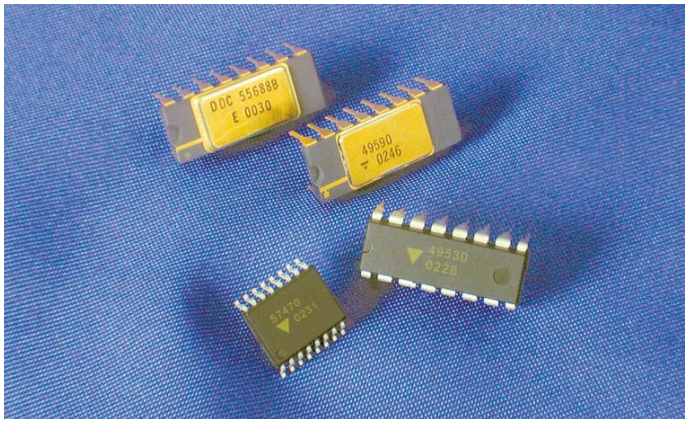


FIGURE 27. THIN-FILM RESISTOR NETWORKS

TABLE 11. THIN-FILM RESISTOR NETWORKS

THIN FILM RESISTOR NETWORK	INPUT VOLTAGE (VRMS)	OUTPUT VOLTAGE (VRMS)	PACKAGE TYPE
DDC-55688-1	2 Single Ended	2	Ceramic DIP
DDC-49530	11.8	2	Plastic DIP
DDC-57470	11.8	2	Surface Mount
DDC-49590	90	2	Ceramic DIP
DDC-73089	2 Differential	2	Surface Mount
DDC-57471	90	2	Surface Mount

Notes:
1. For thin-film network specifications see the "Thin-Film Network Specifications for Motion Feedback Products" Data Sheet available from the DDC web site.
2. Operating temperature range is -55°C to +125°C.

ORDERING INFORMATION

RD-19230FX-X X X X

Supplemental Process Requirements:
T = Tape and Reel (note 1) (50 pc. minimum order)

Accuracy:
2 = 4 minutes + 1 LSB
3 = 2 minutes + 1 LSB
5 = 1 minutes + 1 LSB (maximum reference frequency = 5 kHz)

Reliability:
0 = Standard DDC Procedures

Operating Temperature Range:
2 = -40° to +85°C
3 = 0° to +70°C

Package Options:
X = Standard
G = Lead Free

Notes:
1) DDC does not recommend Tape and Reel due to potential lead damage.

COMPONENT SELECTION SOFTWARE:

Component selection software can be downloaded from our web site at www.ddc-web.com

Evaluation Card Available

P/N RD19230EX-300 (See the DDC web site for this card's User's Guide)

STANDARD DDC PROCESSING FOR PLASTIC MONOLITHIC PRODUCTS		
TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION / WORKMANSHIP	2017	—
ELECTRICAL TEST	DDC ATP	—

Please visit our web site at **www.ddc-web.com** for the latest information.

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