FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-22002-1E

ASSP Communication Control

IEEE 1394 Bus Controller (for DVC)

MB86615

■ DESCRIPTION

The MB86615 is 1394 serial bus controller compatible with the IEEE 1394 “FireWire” standard (IEEE Standard 1394-1995). One built-in port plus a differential transceiver and comparator are provided to enable formation of networks in a 1394 cable environment. The MB86615 supports s100 data transfer speeds.

By integrating the physical layer and link layer on one chip, The MB86615 is designed to reduce mounting area as well as power consumption.

The MB86615 has an exclusive data port for isochronous transfer, provides automatic packetizing for sending and separation of header and data units at receiving, and is optimized for continuity of transfer processing.

The MB86615 supports DVC AV/C protocols, and includes the necessary built-in automatic operations and CSR’s for providing the necessary operations for DVC data transfer.

■ FEATURES

- Compatible with IEEE 1394 high-performance serial bus standards
- Physical layer and link layer integrated on one chip
- 1 cable ports
- Supports s100 transfer speed (98.304 Mbit/sec)
- 3.3V single power supply operation
- Built-in PLL (for crystal oscillator) for internal clock signal generation
- Power saving modes
  1) Forced sleep mode at instruction from MPU
  2) Automatic sleep mode for non-connected ports
- Header and data units automatically separated at receiving and automatic packetizing for sending
- Supports cycle master functions

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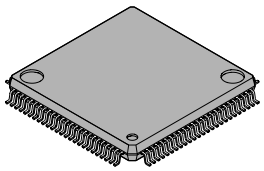
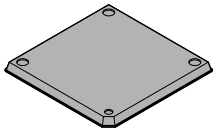
■ PACKAGES

100-pin plastic LQFP



(FPT-100P-M05)

120-pin plastic FBGA



(BGA-120P-M01)

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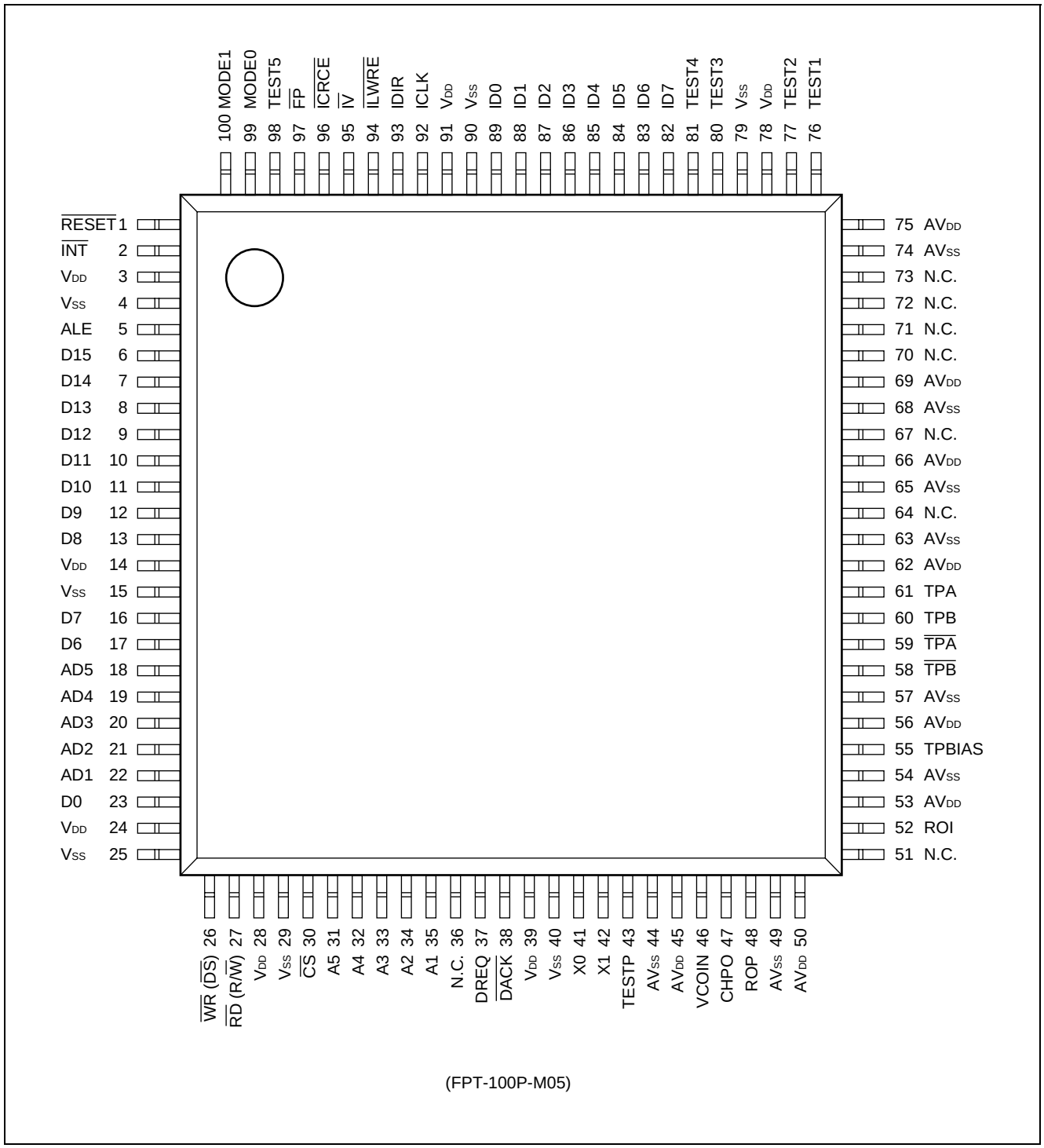
- Built-in CSR's to provide isochronous resource manager functions
- 32-bit CRC generation and check functions
- General purpose port for asynchronous transfer and control (16-bit MPU/DMA common bus)
- Exclusive built-in ports for isochronous transfer (8-bit bus)
- Built-in CRS's and automatic processes to support DVC
  1) Automatic separation of CIP headers at receiving, and automatic packetizing at sending.
  2) Automatic generation and match detection of time stamp by FP signal.
  3) DBC area automatic increment function
  4) No-data packet sending and receiving
  5) On-chip PCR (input/output 1 channel each)
  6) Each CSR with automatic C&S lock processing and read processing
- Compatible with 4-core cable
- Packages: LQFP-100, FBGA-120

■ PIN ASSIGNMENTS

1. LQFP-100



(FPT-100P-M05)

2. FBGA-120

13	12	11	10	9	8	7	6	5	4	3	2	1	
N.C.	AV_{DD}	AV_{SS}	VCOIN	TESTP	XO	$\overline{DACK}$	N.C.	A3	A5	V_{DD}	N.C.	$\overline{WR}$ ($\overline{DS}$)	N
N.C.	ROI	N.C.	CHPO	AV_{SS}	X1	V_{DD}	DREQ	A2	A4	V_{SS}	$\overline{RD}$ (R/W)	V_{SS}	M
AV_{DD}	AV_{SS}	TP-BIAS	ROP	AV_{DD}	N.C.	V_{SS}	N.C.	A1	N.C.	$\overline{CS}$	N.C.	V_{DD}	L
AV_{DD}	AV_{SS}	$\overline{TPB}$								D0	AD1	AD2	K
$\overline{TPA}$	TPB	N.C.								AD3	AD4	AD5	J
TPA	AV_{DD}	AV_{SS}								D6	N.C.	D7	I
N.C.	N.C.	AV_{SS}				TOP VIEW				V_{SS}	V_{DD}	D8	H
AV_{DD}	N.C.	N.C.								N.C.	D9	D10	G
AV_{SS}	AV_{DD}	N.C.								D11	D12	N.C.	E
N.C.	N.C.	N.C.								D13	D14	D15	D
N.C.	AV_{SS}	TEST3	ID7	ID4	ID1	V_{SS}	IDIR	$\overline{IV}$	TEST5	ALE	V_{SS}	V_{DD}	C
AV_{DD}	TEST2	V_{SS}	N.C.	ID5	ID2	ID0	ICLK	N.C.	$\overline{FP}$	N.C.	$\overline{INT}$	N.C.	B
TEST1	N.C.	V_{DD}	TEST4	ID6	ID3	N.C.	V_{DD}	$\overline{ILWRE}$	$\overline{ICRCE}$	MODE 0	MODE 1	$\overline{RESET}$	A

△
1 pin

■ PIN LIST

1. LQFP-100

NO.	I/O	Pin Name	NO.	I/O	Pin Name
1	I	$\overline{\text{RESET}}$	36	—	N.C.
2	O	$\overline{\text{INT}}$	37	O	DREQ
3	—	V_{DD}	38	I	$\overline{\text{DACK}}$
4	—	V_{SS}	39	—	V_{DD}
5	I	ALE	40	—	V_{SS}
6	IU/O	D15	41	I/O	X0
7	IU/O	D14	42	I	X1
8	IU/O	D13	43	O	TESTP
9	IU/O	D12	44	—	AV_{SS}
10	IU/O	D11	45	—	AV_{DD}
11	IU/O	D10	46	I	VCOIN
12	IU/O	D9	47	O	CHPO
13	IU/O	D8	48	O	ROP
14	—	V_{DD}	49	—	AV_{SS}
15	—	V_{SS}	50	—	AV_{DD}
16	IU/O	D7	51	—	N.C.
17	IU/O	D6	52	O	ROI
18	IU/O	AD5	53	—	AV_{DD}
19	IU/O	AD4	54	—	AV_{SS}
20	IU/O	AD3	55	O	TPBIAS
21	IU/O	AD2	56	—	AV_{DD}
22	IU/O	AD1	57	—	AV_{SS}
23	IU/O	D0	58	I/O	$\overline{\text{TPB}}$
24	—	V_{DD}	59	I/O	$\overline{\text{TPA}}$
25	—	V_{SS}	60	I/O	TPB
26	I	$\overline{\text{WR}}$ ($\overline{\text{DS}}$)	61	I/O	TPA
27	I	$\overline{\text{RD}}$ (R/W)	62	—	AV_{DD}
28	—	V_{DD}	63	—	AV_{SS}
29	—	V_{SS}	64	—	N.C.
30	I	$\overline{\text{CS}}$	65	—	AV_{SS}
31	I	A5	66	—	AV_{DD}
32	I	A4	67	—	N.C.
33	I	A3	68	—	AV_{SS}
34	I	A2	69	—	AV_{DD}
35	I	A1	70	—	N.C.

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NO.	I/O	Pin Name	NO.	I/O	Pin Name
71	—	N.C.	86	I/O	ID3
72	—	N.C.	87	I/O	ID2
73	—	N.C.	88	I/O	ID1
74	—	AV_{SS}	89	I/O	ID0
75	—	AV_{DD}	90	—	V_{SS}
76	IU/O	TEST1	91	—	V_{DD}
77	IU/O	TEST2	92	I	ICLK
78	—	V_{DD}	93	I	IDIR
79	—	V_{SS}	94	O	$\overline{\text{ILWRE}}$
80	IU/O	TEST3	95	I	$\overline{\text{IV}}$
81	IU/O	TEST4	96	O	$\overline{\text{ICRCE}}$
82	I/O	ID7	97	I/O	$\overline{\text{FP}}$
83	I/O	ID6	98	O	TEST5
84	I/O	ID5	99	I	MODE0
85	I/O	ID4	100	I	MODE1

2. FBGA-120

Pin No.	Ball No.	I/O	Pin Name	Pin No.	Ball No.	I/O	Pin Name	Pin No.	Ball No.	I/O	Pin Name
1	A1	I	$\overline{\text{RESET}}$	37	N4	I	A5	73	H13	I/O	TPA
2	B1	—	N.C.	38	M4	I	A4	74	H12	—	AV_{DD}
3	B2	O	$\overline{\text{INT}}$	39	L4	—	N.C.	75	H11	—	AV_{SS}
4	C1	—	V_{DD}	40	N5	I	A3	76	G13	—	N.C.
5	C2	—	V_{SS}	41	M5	I	A2	77	G12	—	N.C.
6	C3	I	ALE	42	L5	I	A1	78	G11	—	AV_{SS}
7	D1	IU/O	D15	43	N6	—	N.C.	79	F13	—	AV_{DD}
8	D2	IU/O	D14	44	M6	O	DREQ	80	F12	—	N.C.
9	D3	IU/O	D13	45	L6	—	N.C.	81	F11	—	N.C.
10	E1	—	N.C.	46	N7	I	$\overline{\text{DACK}}$	82	E13	—	AV_{SS}
11	E2	IU/O	D12	47	M7	—	V_{DD}	83	E12	—	AV_{DD}
12	E3	IU/O	D11	48	L7	—	V_{SS}	84	E11	—	N.C.
13	F1	IU/O	D10	49	N8	I/O	X0	85	D13	—	N.C.
14	F2	IU/O	D9	50	M8	I	X1	86	D12	—	N.C.
15	F3	—	N.C.	51	L8	—	N.C.	87	D11	—	N.C.
16	G1	IU/O	D8	52	N9	O	TESTP	88	C13	—	N.C.
17	G2	—	V_{DD}	53	M9	—	AV_{SS}	89	C12	—	AV_{SS}
18	G3	—	V_{SS}	54	L9	—	AV_{DD}	90	B13	—	AV_{DD}
19	H1	IU/O	D7	55	N10	I	VCOIN	91	A13	IU/O	TEST1
20	H2	—	N.C.	56	M10	O	CHPO	92	A12	—	N.C.
21	H3	IU/O	D6	57	L10	O	ROP	93	B12	IU/O	TEST2
22	J1	IU/O	AD5	58	N11	—	AV_{SS}	94	A11	—	V_{DD}
23	J2	IU/O	AD4	59	M11	—	N.C.	95	B11	—	V_{SS}
24	J3	IU/O	AD3	60	N12	—	AV_{DD}	96	C11	IU/O	TEST3
25	K1	IU/O	AD2	61	N13	—	N.C.	97	A10	IU/O	TEST4
26	K2	IU/O	AD1	62	M13	—	N.C.	98	B10	—	N.C.
27	K3	IU/O	D0	63	M12	O	ROI	99	C10	I/O	ID7
28	L1	—	V_{DD}	64	L13	—	AV_{DD}	100	A9	I/O	ID6
29	L2	—	N.C.	65	L12	—	AV_{SS}	101	B9	I/O	ID5
30	M1	—	V_{SS}	66	L11	O	TPBIAS	102	C9	I/O	ID4
31	N1	I	$\overline{\text{WR}}$ ($\overline{\text{DS}}$)	67	K13	—	AV_{DD}	103	A8	I/O	ID3
32	N2	—	N.C.	68	K12	—	AV_{SS}	104	B8	I/O	ID2
33	M2	I	$\overline{\text{RD}}$ (R/$\overline{\text{W}}$)	69	K11	I/O	$\overline{\text{TPB}}$	105	C8	I/O	ID1
34	N3	—	V_{DD}	70	J13	I/O	$\overline{\text{TPA}}$	106	A7	—	N.C.
35	M3	—	V_{SS}	71	J12	I/O	TPB	107	B7	I/O	ID0
36	L3	I	$\overline{\text{CS}}$	72	J11	—	N.C.	108	C7	—	V_{SS}

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Pin No.	Ball No.	I/O	Pin Name	Pin No.	Ball No.	I/O	Pin Name	Pin No.	Ball No.	I/O	Pin Name
109	A6	—	V_{DD}	113	B5	—	N.C.	117	C4	O	TEST5
110	B6	I	ICLK	114	C5	I	$\overline{IV}$	118	A3	I	MODE0
111	C6	I	IDIR	115	A4	O	$\overline{ICRCE}$	119	B3	—	N.C.
112	A5	O	$\overline{ILWRE}$	116	B4	I/O	$\overline{FP}$	120	A2	I	MODE1

■ PIN DESCRIPTION

1. 1394 Interface

Pin name	I/O	Function
TPA	I/O	1394 Cable port TPA positive signal I/O pin
$\overline{\text{TPA}}$	I/O	1394 Cable port TPA negative signal I/O pin
TPB	I/O	1394 Cable port TPB positive signal I/O pin
$\overline{\text{TPB}}$	I/O	1394 Cable port TPB negative signal I/O pin
TPBIAS	O	1394 Cable port common voltage reference voltage output pin
ROI	O	Connect to GND through 4.7 kΩ resistance

2. Isochronous-data Interface

Pin name	I/O	Function
ICLK	I	Isochronous data interface CLK signal input pin (4 MHz to 16 MHz).
IDIR	I	Isochronous transfer transmission/reception switching signal input pin. 0 input: The device clears the ISO-FIFO buffer and enters the transmission mode. The device asserts the $\overline{\text{ILWRE}}$ signal and starts transmission after receiving one packet of data according to the “data-length” setting (bank 0: 10h). 1 input: The device clears the ISO-FIFO buffer and enters the reception mode. If any packet being transmitted exists, the device enters the reception mode after completing transmission of the packet. The $\overline{\text{ILWRE}}$ signal is asserted upon reception of one packet. Note: The IDIR signal should normally be left at “1” and switched to “0” only for transmission.
$\overline{\text{ILWRE}}$	O	ISO-FIFO access enable signal output pin. Transmission mode: The signal is asserted when the FIFO buffer is not full. The signal is negated when the FIFO buffer becomes full. When it is negated, data is accepted only up to the rising edge of the next ICLK signal. When a bus reset is detected, the signal is negated after accepting data of up to the packet boundary. After the bus reset, the signal is asserted again upon completion of transmission of one source packet remaining in the FIFO buffer. Reception mode: The signal is asserted upon completion of one packet of data. The signal is negated once when one packet of data is read from the FIFO buffer and asserted back if the FIFO buffer still contains any packet of data which has been received completely.
ID7 to ID0	I/O	Isochronous transfer data input/output bits. (MSB is ID7, LSB is ID0)
$\overline{\text{IV}}$	I	ID7 to ID0 enable signal input pin Transmission mode: While the $\overline{\text{IV}}$ signal is active, data from the ID7 to ID0 pins is loaded into the ISO-FIFO buffer at the rising edge of the ICLK signal. Reception mode: While the signal becomes active, the device starts sending data from the ISO-FIFO buffer to the ID7 to ID0 pins. Data is then switched at the rising edge of the ICLK signal.

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Pin name	I/O	Function
$\overline{\text{ICREC}}$	O	This pin outputs a signal indicating that data sent in the reception mode is data in a packet from which a data-CRC error has been detected.
$\overline{\text{FP}}$	I/O	Time stamp trigger signal I/O pin. Transmission mode: This pin inputs the time stamp trigger signal. The value in the internal cycle timer register is fetched upon detection of the falling edge of the $\overline{\text{FP}}$ signal. Reception mode: Time stamp match detection signal output pin.

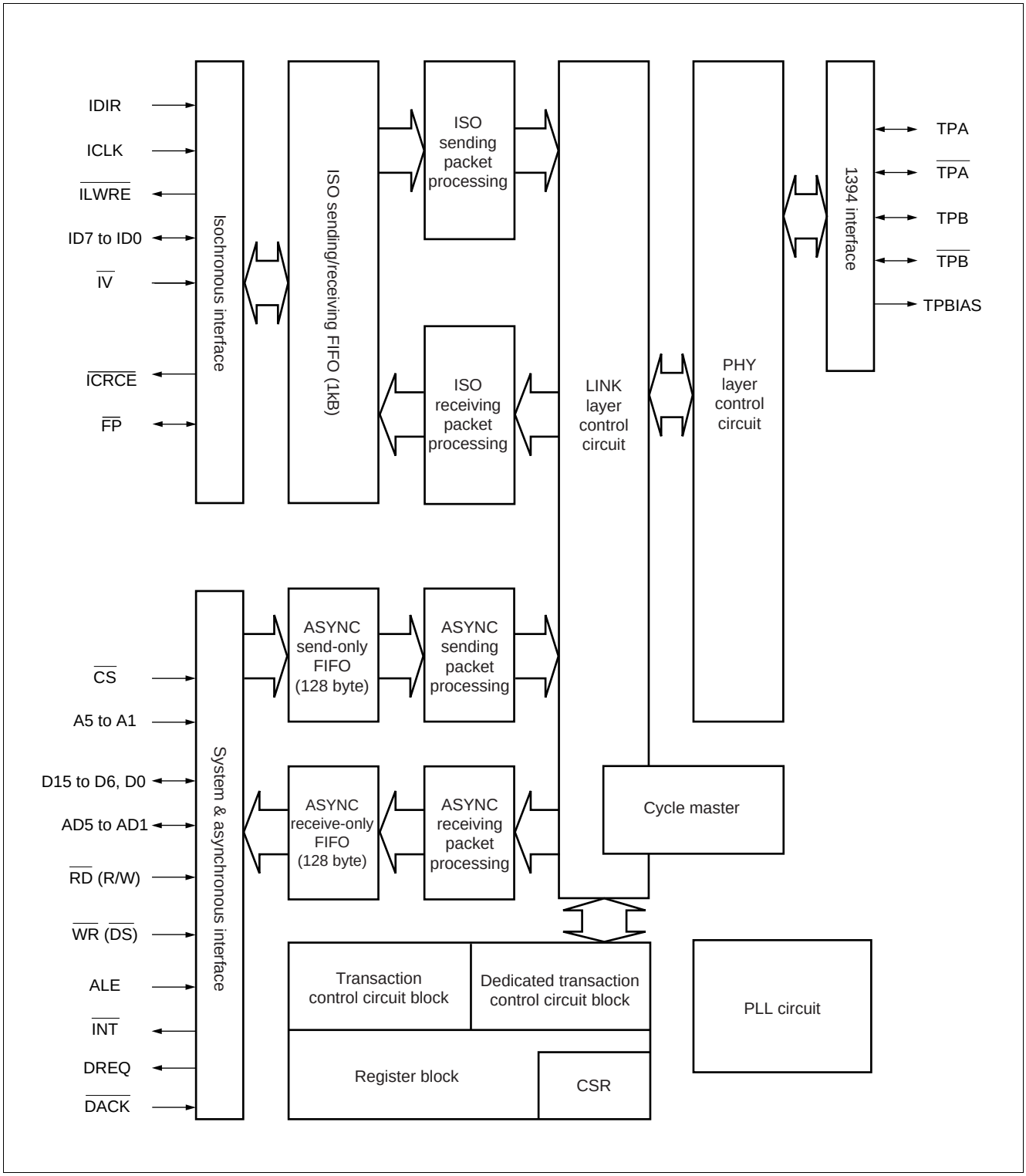
3. System Interface

Pin name	I/O	Function
$\overline{\text{CS}}$	I	Input pin for signals used by the MPU to select the MB86615 as an I/O device.
A5 to A1	I	Address input pins for internal register selection. Valid only in non-multiplexed mode. If multiplexed mode is selected these pins should be fixed at '0'.
D15 to D6, D0	I/O	16-bit data bus input/output pins (MSB is D15, LSB is D0).
AD5 to AD1	I/O	16-bit data bus input/output pins (MSB is AD5, LSB is AD1). Used for address input signals when multiplexed mode is selected.
$\overline{\text{RD}}$ (R/W)	I	80-series mode: Read strobe signal input pin, used to output data from the MB86615 to the data bus. 68-series mode: Control signal input pin, used for data input/output operations to the MB86615.
$\overline{\text{WR}}$ ($\overline{\text{DS}}$)	I	80-series mode: Write strobe signal input pin, used to input data from the data bus to the MB86615. 68-series mode: $\overline{\text{DS}}$ signal input pin, output when data bus is enabled.
ALE	I	ALE signal input pin, for signal output when addresses are enabled in multiplexed mode. In non-multiplexed mode, this signal should be fixed at '0'.
DREQ	O	This pin outputs the DMA transfer request signal to the DMAC for asynchronous transfer in DMA mode. The signal requests DMA transfer between the device and memory.
$\overline{\text{DACK}}$	I	This pin inputs the DMA enable signal from the DMAC for asynchronous transfer in DMA mode.
$\overline{\text{INT}}$	O	Interrupt output pin.

4. Other

Pin name	I/O	Function
X0	I/O	External crystal connection pins for oscillator circuits.
X1	I	
VCOIN	I	VCO input pin for internal PLL.
CHPO	O	Charge pump output pin for internal PLL.
ROP	O	Connect to GND through 4.7 kΩ resistance.
$\overline{\text{RESET}}$	I	Reset signal input pin. The device enters the forced sleep mode automatically upon detection of the $\overline{\text{RESET}}$ signal asserted.
MODE0	I	Input ‘0’ for 80-series mode. Input ‘1’ for 68-series mode.
MODE1	I	Input ‘0’ for non-multiplexed mode. Input ‘1’ for multiplexed mode.
TESTP	O	Test pin. Do not connect.
TEST1 to TEST4	IU/O	Test pin. Do not connect.
TEST5	O	Test pin. Do not connect.
AV_{DD}	—	Analog power supply
AV_{SS}	—	Analog ground
V_{DD}	—	Digital power supply
V_{SS}	—	Digital ground
N.C.	—	Unused pin. Do not connect.

■ BLOCK DIAGRAM



■ BLOCK DESCRIPTIONS

- PHY Layer Control Circuit
  This block contains the IEEE 1394 physical layer control circuits.
  Both asynchronous transfer and isochronous transfer in a cable environment are supported.
  The transfer speed is 100 Mbit/sec.
  One analog transceiver/receiver ports are built-in.
  This block provides bus status monitoring initialization operation after a bus reset is applied, as well as arbitration and encoding/decoding functions for data sending and receiving.

- LINK Layer Control Circuit
  This block controls the generation and transfer of IEEE 1394 standard packets.
  32-bit CRC generation and checking is performed for packet headers and data.
  A 32-bit cycle timer register is built-in to provide cycle master functions.

- Sending/Receiving FIFO
  Contains built-in 1-byte FIFO areas, used for isochronous transfer for both sending and receiving.
  Contains independent sending and receiving 128-byte FIFO areas for asynchronous transfer.

- Packet Processing
  Sending: Performs packetizing of headers, data and CRC. Automatically generates and attaches CRC.
  Receiving: Separates 1394 packet headers and data, strips CRC.

- Transaction Control Circuit Block
  This block controls the 1394 bus protocol based on a variety of instructions.

- Dedicated Transaction Circuit Block
  This block packetizes data from the isochronous interface for DVC and rebuilds received data for the isochronous interface in conjunction with the packet processing block.

- Register Block
  This block contains various device control registers, as well as registers for setting parameters required for transfer, DVC registers and CSR.
  The built-in CSR provides isochronous resource manager functions.

- PLL Circuit
  This block uses the reference clock signal generated by the crystal oscillator circuit to create internal operating clock and transfer clock signals.
  Reference oscillator frequency: 8.192 MHz.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage*1	V_{DD}	V_{SS} – 0.5	4.0	V
Input voltage*1	V_I	V_{SS} – 0.5	V_{DD} + 0.5	V
Output voltage*1	V_O	V_{SS} – 0.5	V_{DD} + 0.5	V
Strage temperature	Tst	–55	+125	°C
Operating temperature*2	Top	–40	+85	°C
Output current*3	I_O	–14	+14	mA
Overshoot*4	—	—	V_{DD} + 1.0	V
Undershoot*4	—	—	V_{SS} – 1.0	V

*1: Voltage values are based on Vss = 0 V.
*2: Not warranted for continuous operation.
*3: Normal output current flow (Minimum at Vo = 0 V, maximum at Vo = V_{DD}).
*4: 50 ns or less.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Value		Unit
			Min.	Max.	
Power supply voltage*		V_{DD}	3.0	3.6	V
“H” level input voltage	CMOS input	V_{IH}	$V_{DD} \times 0.65$	V_{DD}	V
“L” level input voltage	CMOS input	V_{IL}	V_{SS}	$V_{DD} \times 0.25$	V
Differential input voltage (for data transfer)	Cable input	V_{ID}	142	260	mV
Differential input voltage (for arbitration)	Cable input	V_{IDA}	173	260	mV
Common mode input voltage	Cable input	V_{CM}	1.165	2.515	V
Receiving input jitter	Cable input	—	—	1.08	ns
Receiving input skew	Cable input	—	—	0.8	ns
Output current	CMOS output	I_{OH}/I_{OL}	–4	+4	mA
	TPBIAS	Iot	–2	+10	mA
Operating temperature		Ta	0	+70	°C

* : Voltage values are based on Vss = 0 V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

1.1 1394 Interface Driver

(V_{DD} = 3 to 3.6 V , V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter	Symbol	Conditions	Value		Unit
			Min.	Max.	
Differential output voltage	V_{OD}	R_1 = 56 Ω	172	265	mV
Common phase current	I_{CM}	Driver enabled	–0.81	0.44	mA
Off state voltage	V_{OFF}	Driver disabled	—	20	mV
TPBIAS output voltage	V_O	—	1.665	2.015	V

1.2 1394 Interface - Comparator

(V_{DD} = 3 to 3.6 V , V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter	Symbol	Conditions	Value		Unit
			Min.	Max.	
Common phase input current	I_{IC}	Driver disabled	–20	20	µA
Arbitration comparator “H” level detection offset	V_{SCH}	Driver disabled	168	—	mV
Arbitration comparator “Z” level detection offset	V_{SCZ}	Driver disabled	–30	30	mV
Arbitration comparator “L” level detection offset	V_{SCL}	Driver disabled	—	–168	mV
Port status comparator disconnection detect voltage	V_{SD}	Driver disabled	—	0.6	V
Port status comparator connection detect voltage	V_{SC}	Driver disabled	1.0	—	V

1.3 System Interface, etc

(V_{DD} = 3 to 3.6 V , V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.	Max.	
"H" level input voltage		V_{IH}	CMOS	$V_{DD} \times 0.65$	—	V_{DD}	V
"L" level input voltage		V_{IL}	CMOS	V_{SS}	—	$V_{DD} \times 0.25$	V
"H" level output voltage		V_{OH}	I_{OH} = –4 mA	V_{DD} – 0.5	—	V_{DD}	V
"L" level output voltage		V_{OL}	I_{OL} = +4 mA	V_{SS}	—	0.4	V
Input leak current	Input pins	I_{LI}	V_I = 0V to V_{DD}	–5	—	5	µA
	3-state pin input	I_{LZ}		–5	—	5	µA
Input pull-up resistance		Rp	V_{IH} = 0	25	50	200	kΩ
Power supply current		I_{DD1}	1394 port connected	—	—	200	mA
		I_{DD0}	1394 port non connected	—	—	180	mA
		I_{DDS}	Forced sleep	—	—	30	mA

2. AC Characteristics

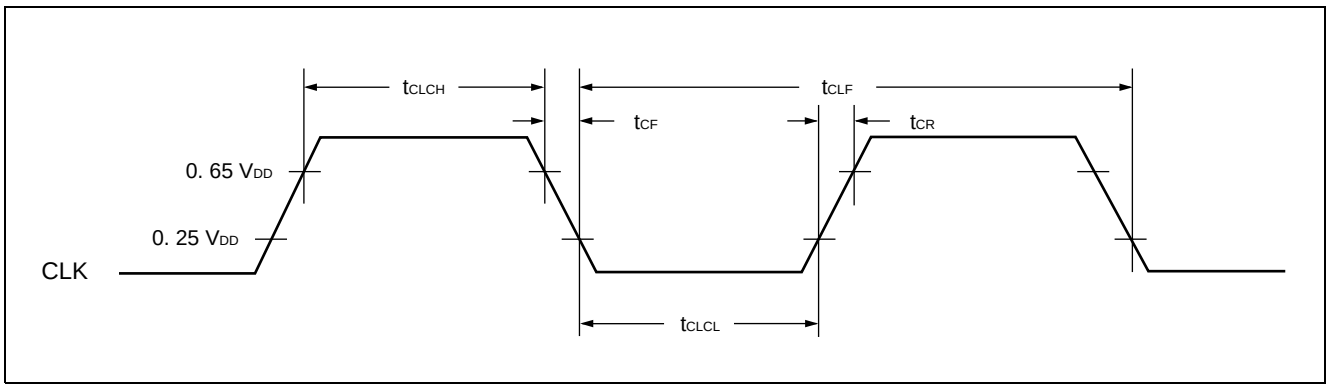
2.1 1394 Driver

Parameter		Symbol	Value		Unit
			Min.	Max.	
Sending jitter		t_{JT}	—	±0.8	ns
Sending skew		t_{SK}	—	±0.8	ns
Sending rise time*	Conditions C_L = 10 pF. R_L = 56 Ω	t_{DR}	—	3.2	ns
Sending fall time*		t_{DF}	—	3.2	ns

* : 10 to 90% value.

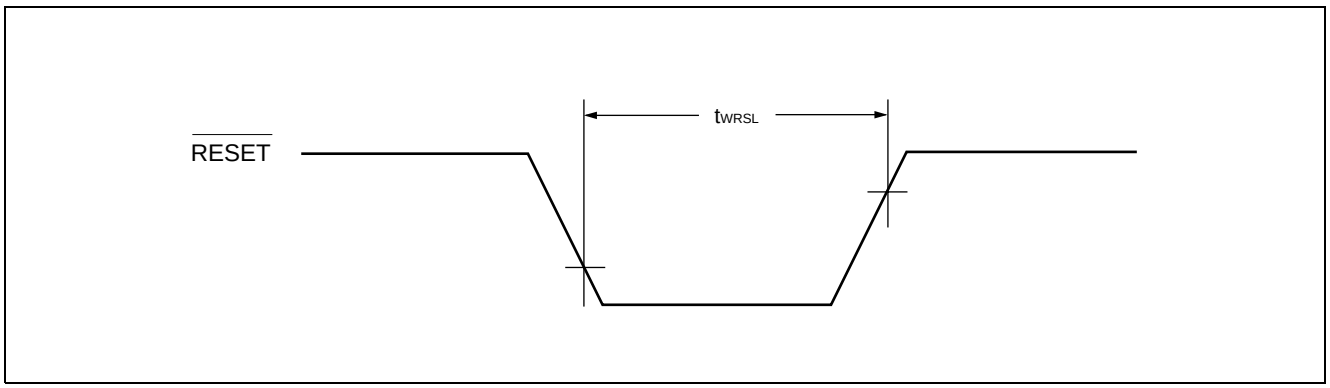
2.2 System Clock

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Clock frequency		f_C	8.191992	8.192	8.192008	MHz
Clock cycle time		t_{CLF}	—	1/fc	—	ns
Clock pulse width	High	t_{CLCH}	50	—	—	ns
	Low	t_{CLCL}	50	—	—	ns
Clock rise time		t_{CR}	—	—	5	ns
Clock fall time		t_{CF}	—	—	5	ns



2.3 System Reset

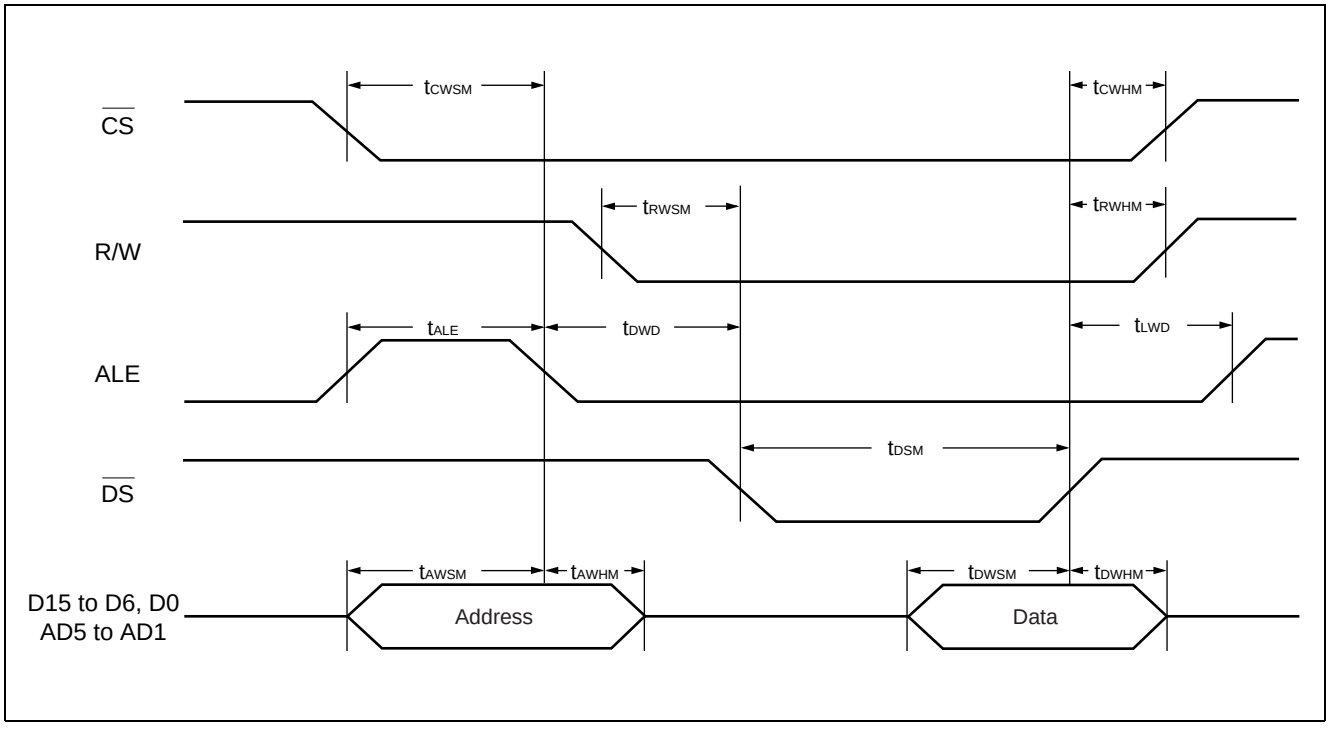
Parameter	Symbol	Value		Unit
		Min.	Max.	
Reset (RESET) “L” level pulse width	t_{WRSL}	4 tclf	—	ns



2.4 MPU Interface

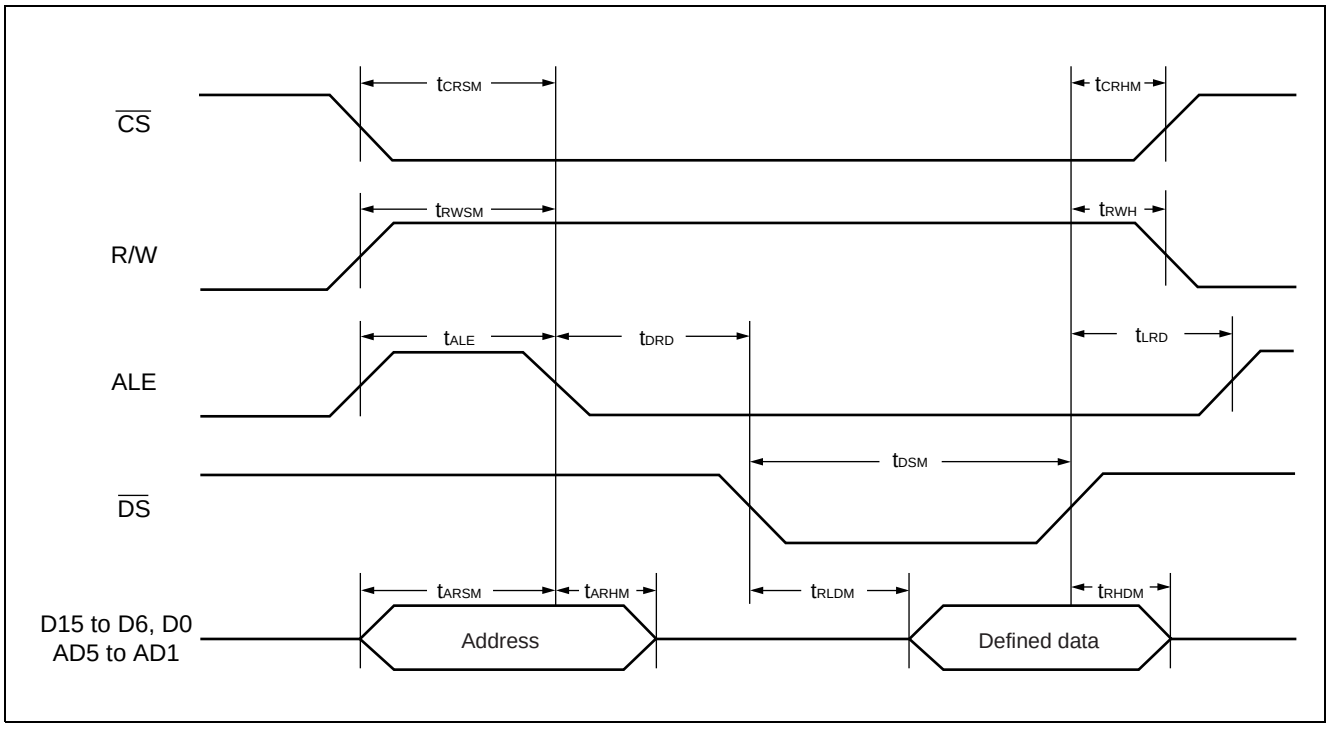
(1) **68-Series Register Write Operation (multiplexed)**

Parameter	Symbol	Value		Unit
		Min.	Max.	
Address setup time	t_{AWSM}	10	—	ns
Address hold time	t_{AWHM}	10	—	ns
$\overline{CS}$ setup time	t_{CWSM}	20	—	ns
$\overline{CS}$ hold time	t_{CWHM}	10	—	ns
R/W setup time	t_{RWSM}	20	—	ns
R/W hold time	t_{RWHM}	10	—	ns
ALE “H” level pulse width	t_{ALE}	15	—	ns
ALE fall to $\overline{DS}$ fall time	t_{DWD}	15	—	ns
$\overline{DS}$ “L” level pulse width	t_{DSM}	40	—	ns
Data setup time	t_{DWSM}	10	—	ns
Data hold time	t_{DWHM}	0	—	ns
$\overline{DS}$ rise to ALE rise time	t_{LWD}	20	—	ns



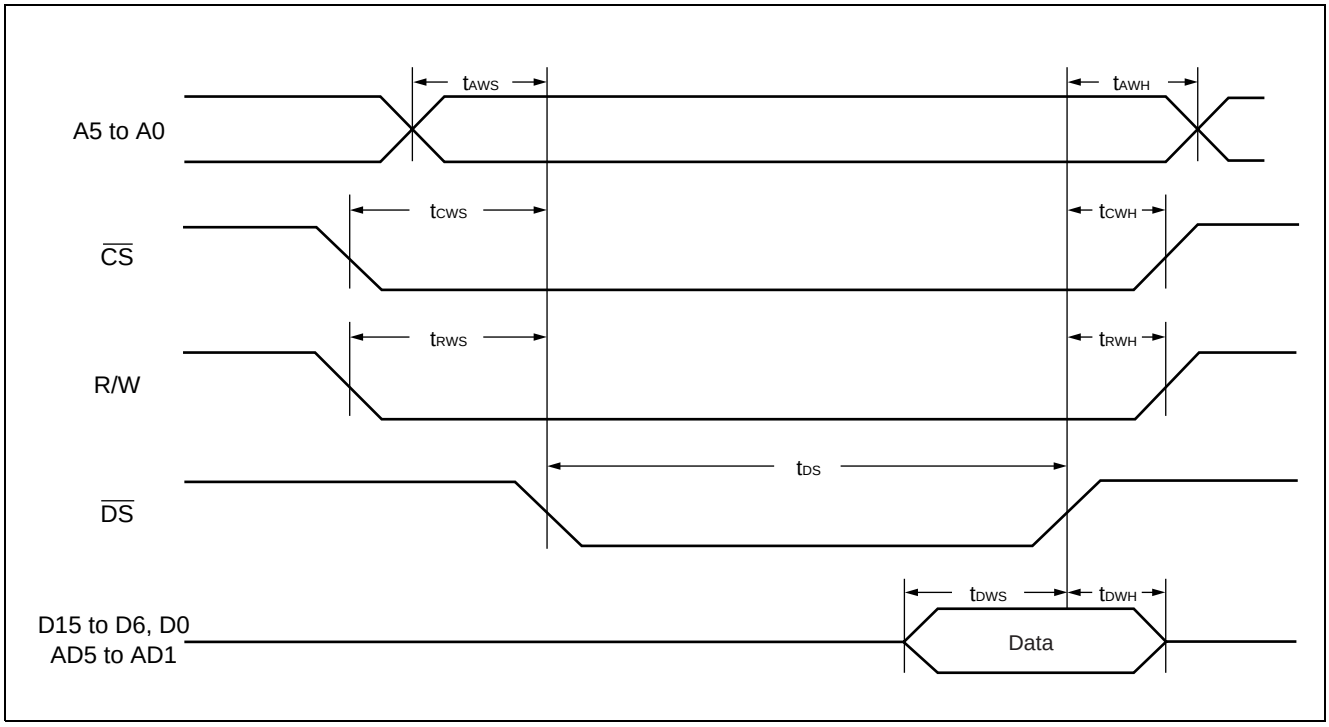
(2) 68-System Register Read Operation (multiplexed)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Address setup time	t_{ARSM}	10	—	ns
Address hold time	t_{ARHM}	10	—	ns
$\overline{CS}$ setup time	t_{CRSM}	20	—	ns
$\overline{CS}$ hold time	t_{CRHM}	10	—	ns
R/W setup time	t_{RWSM}	20	—	ns
R/W hold time	t_{RWH}	10	—	ns
ALE “H” level pulse width	t_{ALE}	15	—	ns
ALE fall to $\overline{DS}$ fall time	t_{DRD}	15	—	ns
$\overline{DS}$ “L” level pulse width	t_{DSM}	40	—	ns
Data output definition time	t_{RLDM}	—	40	ns
Data output disabled time	t_{RHDM}	5	—	ns
$\overline{DS}$ rise to ALE rise time	t_{LRD}	20	—	ns



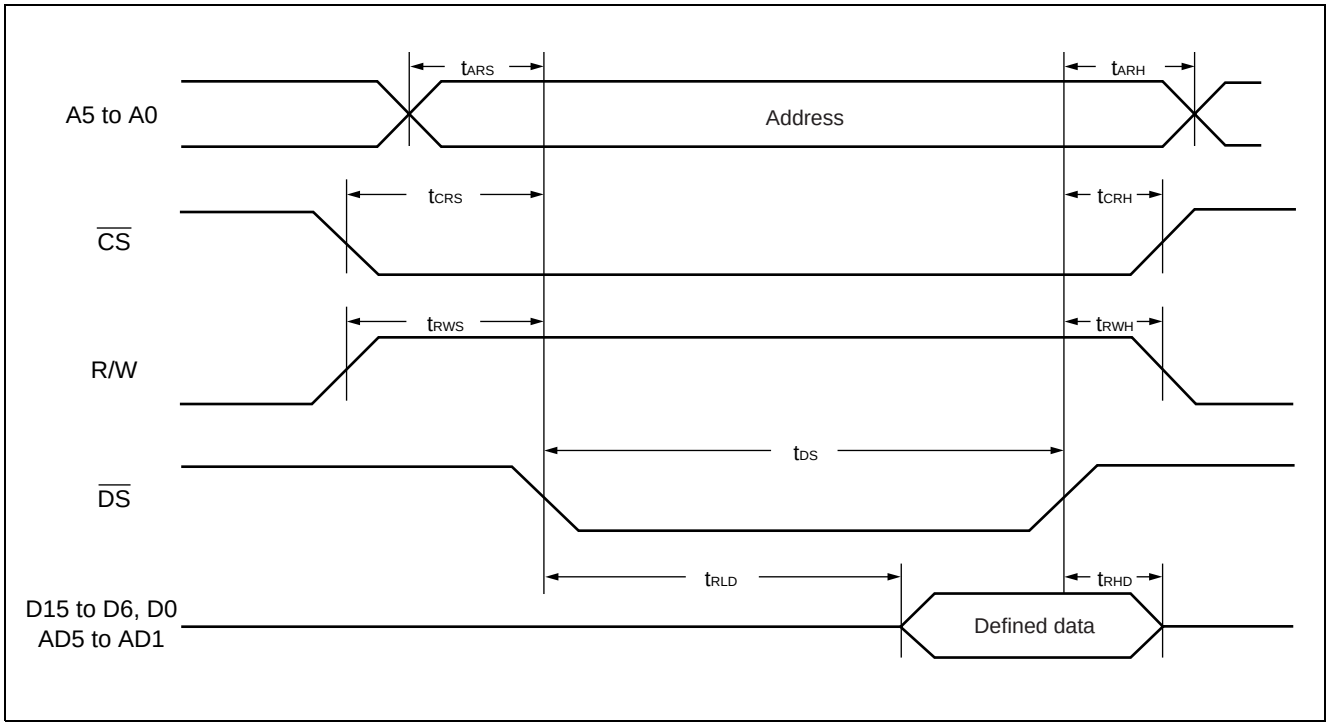
(3) 68-Series Register Write Operation (non-multiplexed)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Address setup time	t_{AWS}	10	—	ns
Address hold time	t_{AWH}	20	—	ns
$\overline{CS}$ setup time	t_{CWS}	20	—	ns
$\overline{CS}$ hold time	t_{CWH}	10	—	ns
R/W setup time	t_{RWS}	20	—	ns
R/W hold time	t_{RWH}	10	—	ns
$\overline{DS}$ "L" level pulse width	t_{DS}	40	—	ns
Data setup time	t_{DWS}	40	—	ns
Data hold time	t_{DWH}	0	—	ns



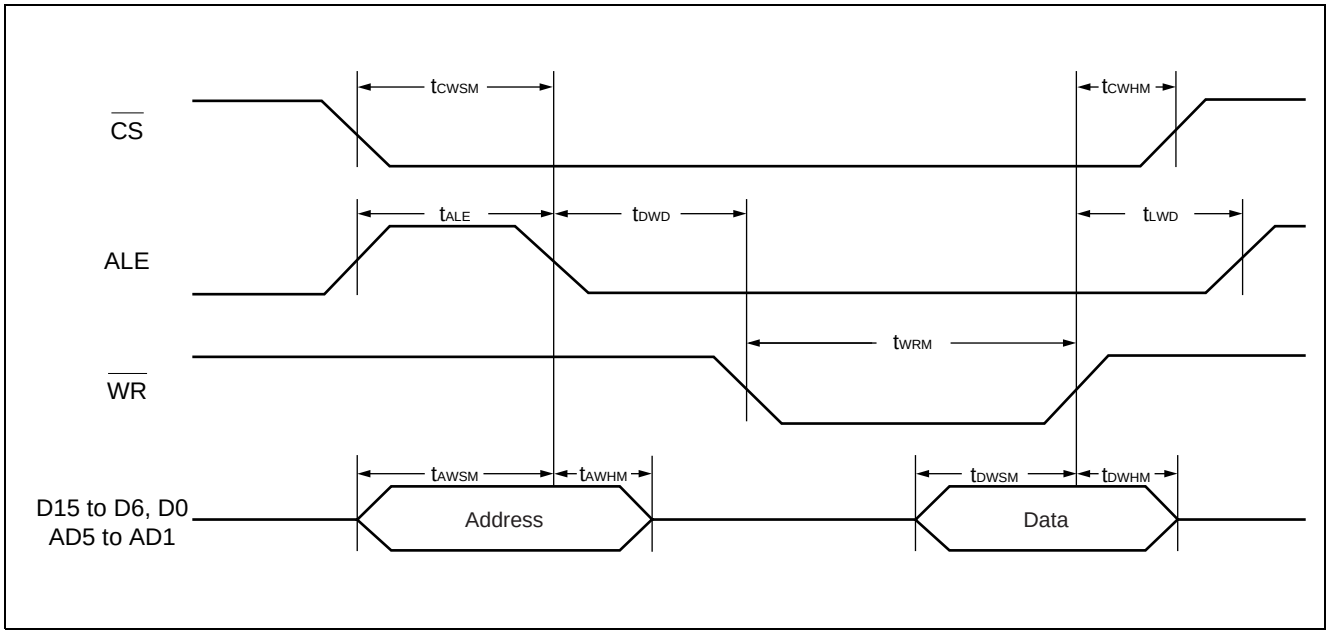
(4) 68-Series Register Read Operation (non-multiplexed)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Address setup time	t_{ARS}	10	—	ns
Address hold time	t_{ARH}	20	—	ns
$\overline{CS}$ setup time	t_{CRS}	20	—	ns
$\overline{CS}$ hold time	t_{CRH}	10	—	ns
R/W setup time	t_{RWS}	20	—	ns
R/W hold time	t_{RWH}	10	—	ns
$\overline{DS}$ "L" level pulse width	t_{DS}	40	—	ns
Data output definition time	t_{RLD}	—	40	ns
Data output disabled time	t_{RHD}	5	—	ns



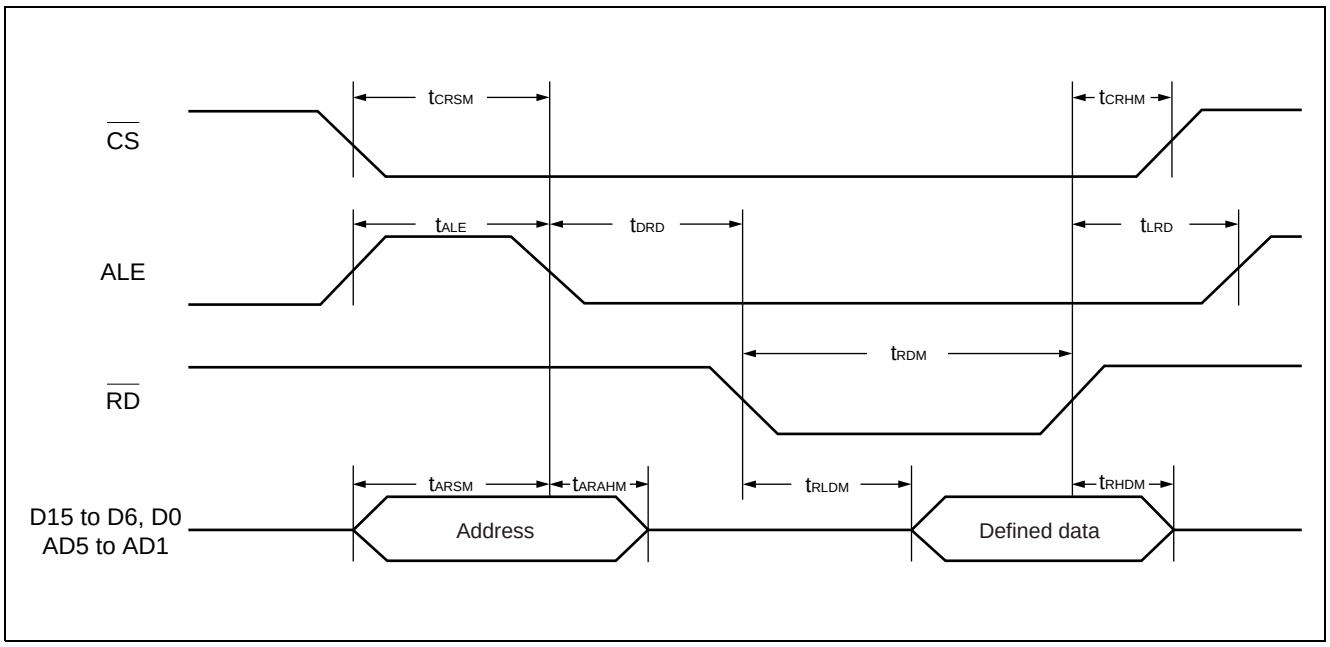
(5) 80-Series Register Write Operation (multiplexed)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Address setup time	t_{AWSM}	10	—	ns
Address hold time	t_{AWHM}	10	—	ns
$\overline{CS}$ setup time	t_{CWSM}	20	—	ns
$\overline{CS}$ hold time	t_{CWHM}	10	—	ns
ALE “H” level pulse width	t_{ALE}	15	—	ns
ALE fall to $\overline{WR}$ fall time	t_{DWD}	15	—	ns
$\overline{WR}$ “L” level pulse width	t_{WRM}	40	—	ns
Data setup time	t_{DWSM}	40	—	ns
Data hold time	t_{DWHM}	0	—	ns
$\overline{WR}$ rise to ALE rise time	t_{LWD}	20	—	ns



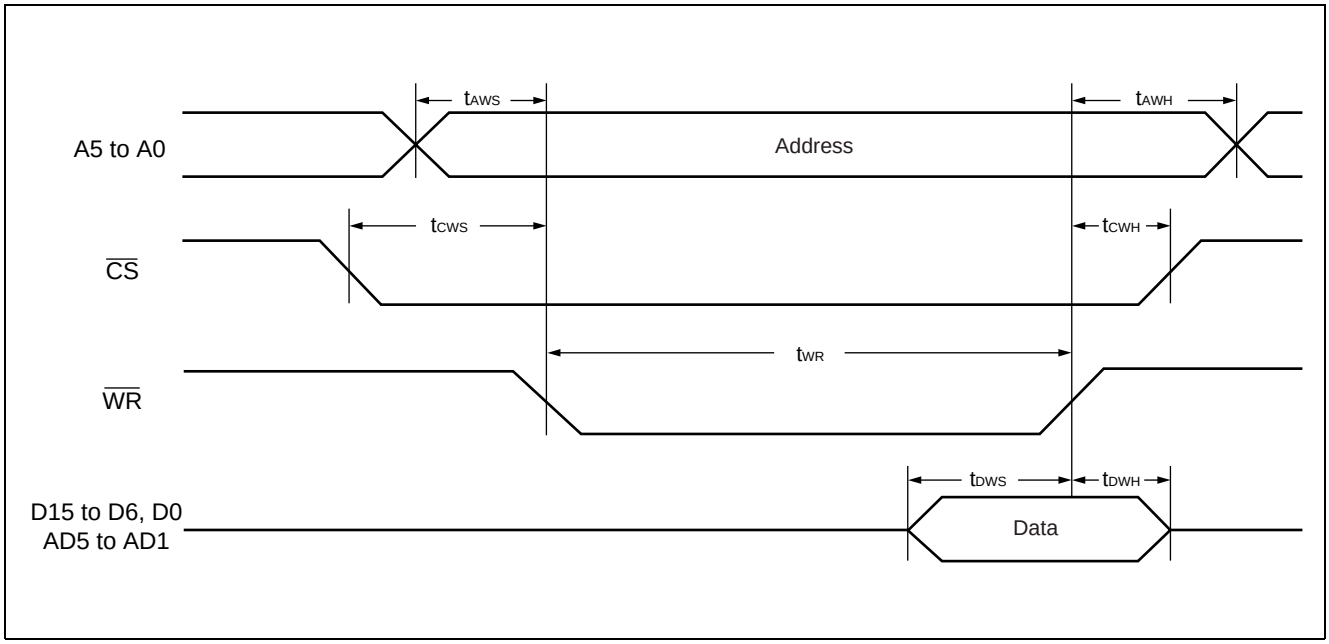
(6) 80-Series Register Read Operation (multiplexed)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Address setup time	t_{ARSM}	10	—	ns
Address hold time	t_{ARAHM}	10	—	ns
$\overline{CS}$ setup time	t_{CRSM}	20	—	ns
$\overline{CS}$ hold time	t_{CRHM}	10	—	ns
ALE “H” level pulse width	t_{ALE}	15	—	ns
ALE fall to $\overline{RD}$ fall time	t_{DRD}	15	—	ns
$\overline{RD}$ “L” level pulse width	t_{RDM}	40	—	ns
Data output definition time	t_{RLDM}	—	40	ns
Data output disabled time	t_{RHDM}	5	—	ns
$\overline{RD}$ rise to ALE rise time	t_{LRD}	20	—	ns



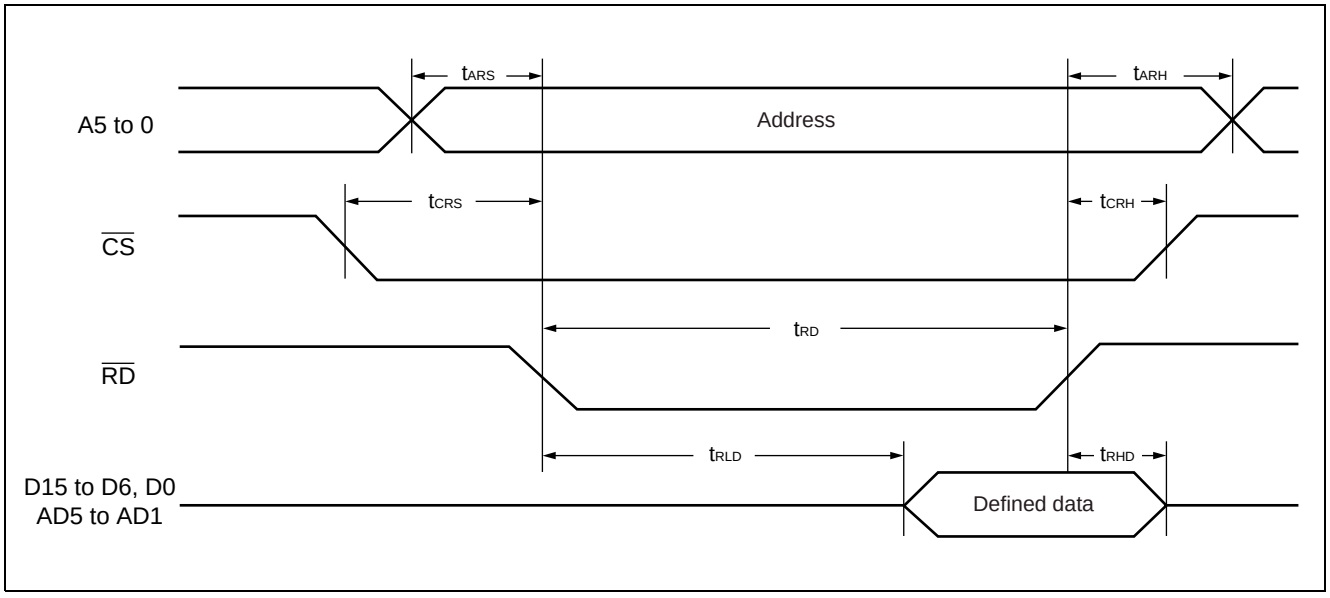
(7) 80-Series Register Write Operation (non-multiplexed)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Address setup time	t_{AWS}	10	—	ns
Address hold time	t_{AWH}	20	—	ns
$\overline{CS}$ setup time	t_{CWS}	20	—	ns
$\overline{CS}$ hold time	t_{CWH}	10	—	ns
$\overline{WR}$ "L" level pulse width	t_{WR}	40	—	ns
Data setup time	t_{DWS}	40	—	ns
Data hold time	t_{DWH}	0	—	ns



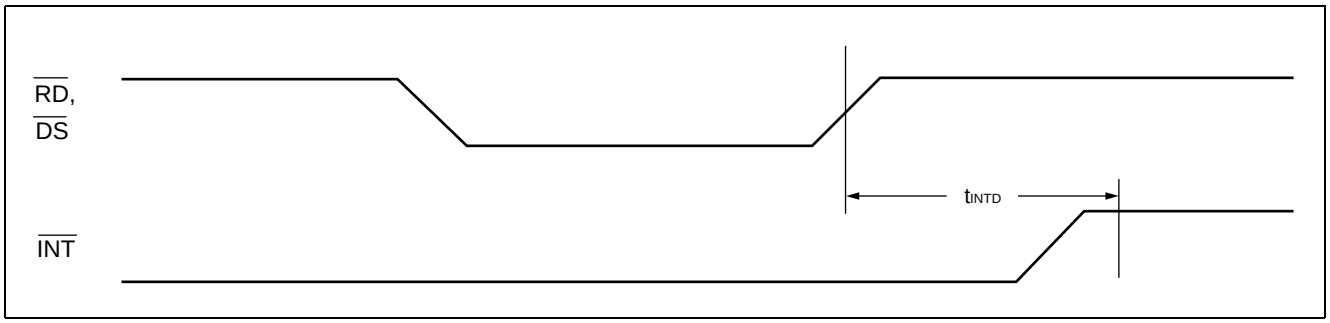
(8) 80-Series Register Read Operation (non-multiplexed)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Address setup time	t_{ARS}	10	—	ns
Address hold time	t_{ARH}	20	—	ns
$\overline{CS}$ setup time	t_{CRS}	20	—	ns
$\overline{CS}$ hold time	t_{CRH}	10	—	ns
$\overline{RD}$ "L" level pulse width	t_{RD}	40	—	ns
Data output definition time	t_{RLD}	—	40	ns
Data output disabled time	t_{RHD}	5	—	ns



(9) INT Signal Operation

Parameter	Symbol	Value		Unit
		Min.	Max.	
Interrupt read operation to $\overline{INT}$ signal negate	t_{INTD}	100	—	ns

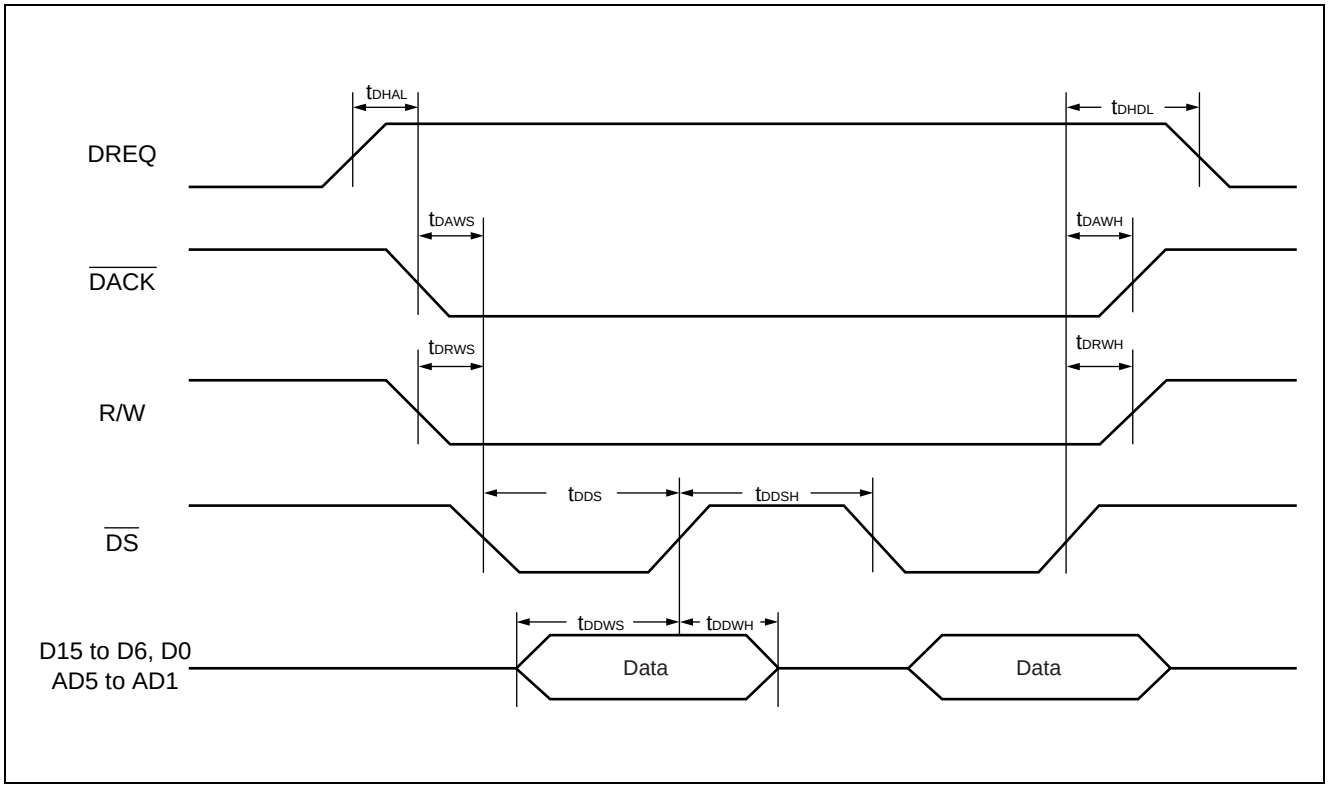


Note: This specification applies only to reading of the last data from the interrupt holding register. For other read-related specifications, conform to the respective specifications for individual modes.

2.5 DMA Access

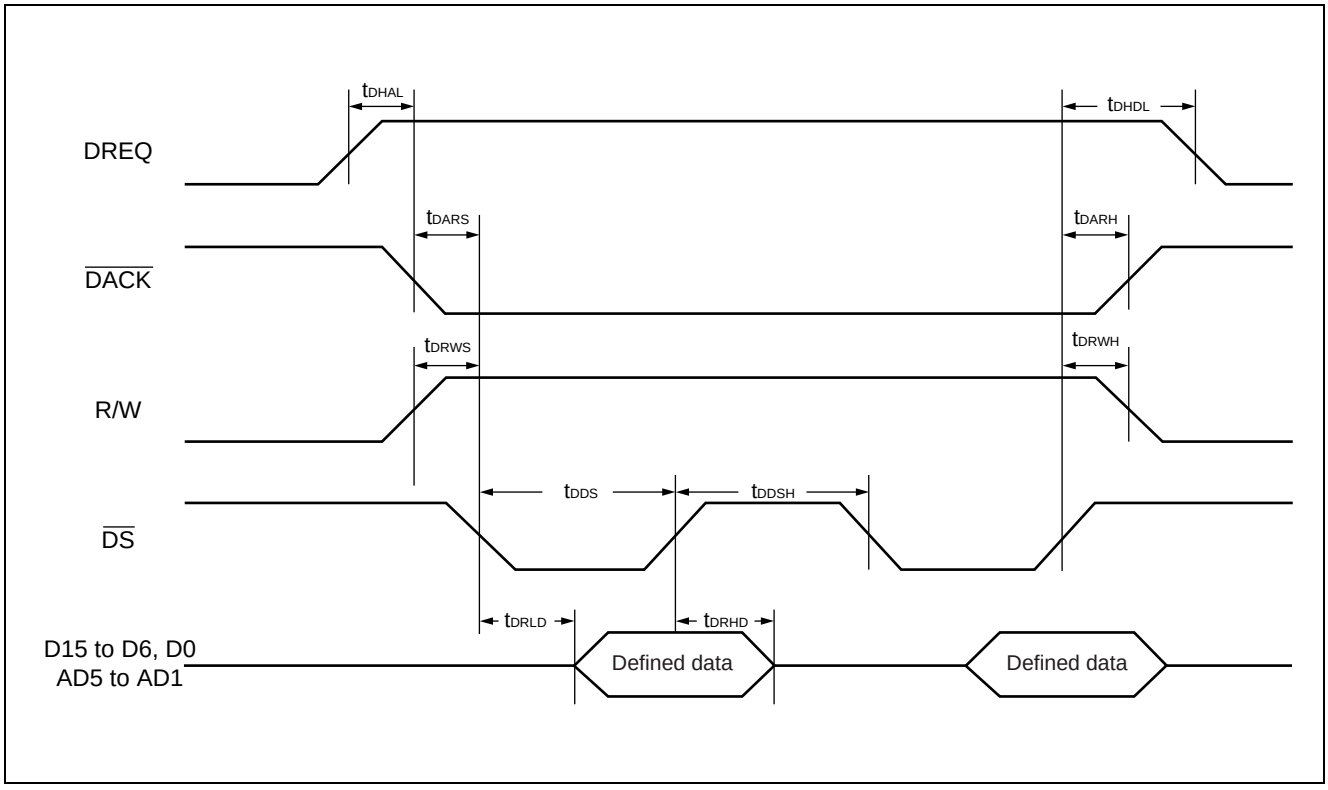
(1) 68-Series DMA Write Operation

Parameter	Symbol	Value		Unit
		Min.	Max.	
DREQ “H” to $\overline{\text{DACK}}$ “L”	t_{DHAL}	0	—	ns
$\overline{\text{DS}}$ “H” to DREQ “L”	t_{DHDL}	—	30	ns
$\overline{\text{DACK}}$ setup time	t_{DAWS}	20	—	ns
$\overline{\text{DACK}}$ hold time	t_{DAWH}	0	—	ns
R/W setup time	t_{DRWS}	20	—	ns
R/W hold time	t_{DRWH}	10	—	ns
$\overline{\text{DS}}$ “L” level pulse width	t_{DDS}	40	—	ns
$\overline{\text{DS}}$ “H” level pulse width	t_{DDSH}	30	—	ns
Input data setup time	t_{DDWS}	30	—	ns
Input data hold time	t_{DDWH}	0	—	ns



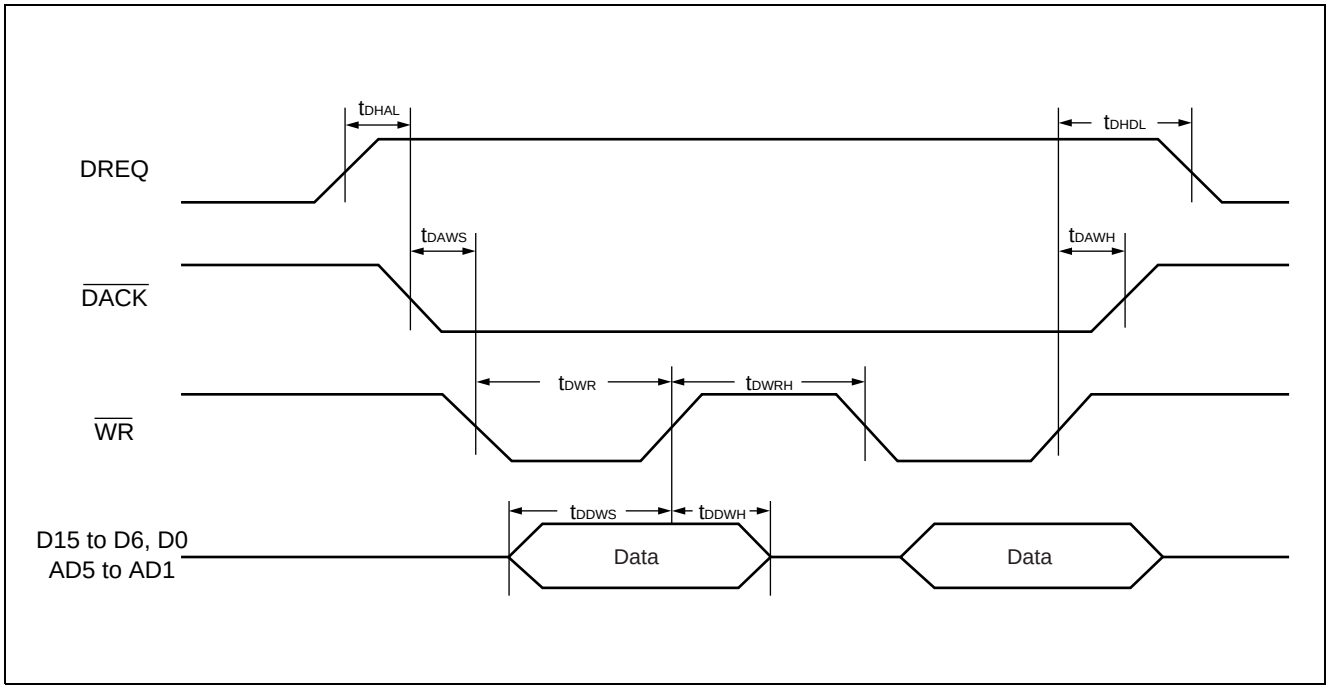
(2) 68-Series DMA Read Operation

Parameter	Symbol	Value		Unit
		Min.	Max.	
DREQ “H” to $\overline{\text{DACK}}$ “L”	t_{DHAL}	0	—	ns
$\overline{\text{DS}}$ “H” to $\overline{\text{DREQ}}$ “L”	t_{DHDL}	—	30	ns
$\overline{\text{DACK}}$ setup time	t_{DARS}	20	—	ns
$\overline{\text{DACK}}$ hold time	t_{DARH}	0	—	ns
R/W setup time	t_{DRWS}	20	—	ns
R/W hold time	t_{DRWH}	10	—	ns
$\overline{\text{DS}}$ “L” level pulse width	t_{DDS}	40	—	ns
$\overline{\text{DS}}$ “H” level pulse width	t_{DDSH}	30	—	ns
Data output definition time	t_{DRLD}	—	40	ns
Data output disabled time	t_{DRHD}	5	—	ns



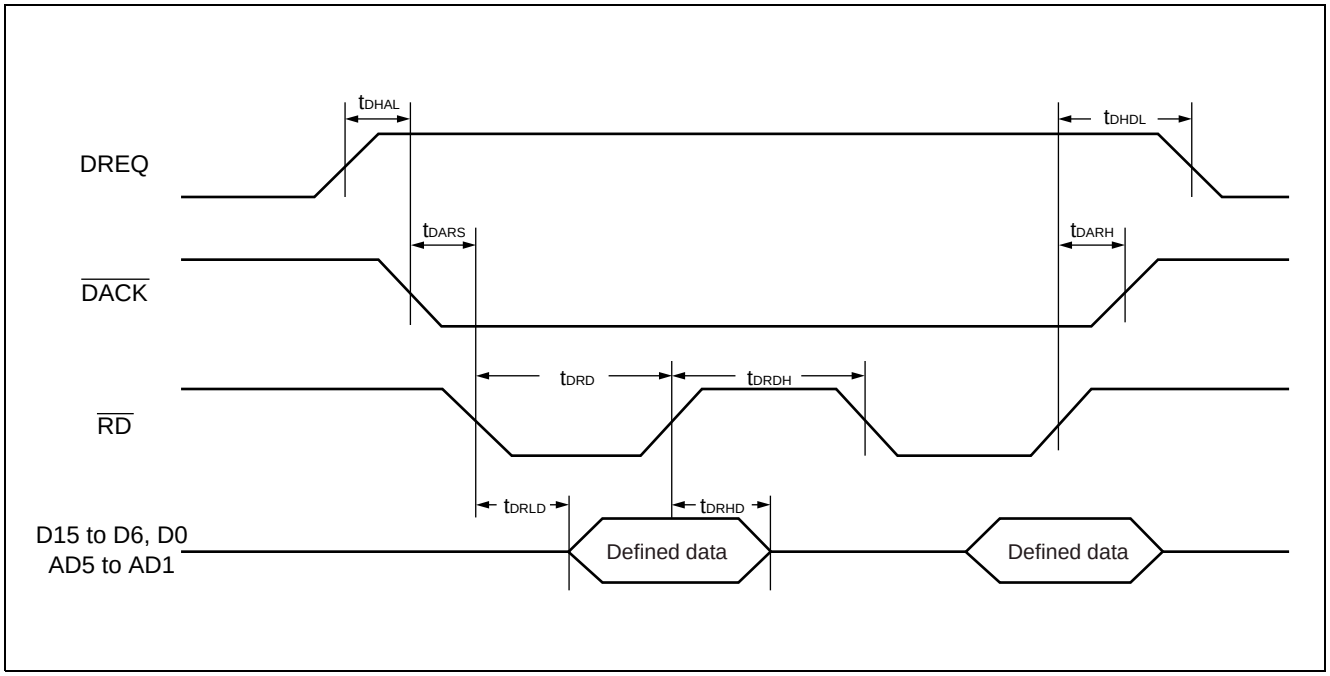
(3) 80-Series DMA Write Operation

Parameter	Symbol	Value		Unit
		Min.	Max.	
DREQ “H” to $\overline{\text{DACK}}$ “L”	t_{DHAL}	0	—	ns
$\overline{\text{WR}}$ “H” to DREQ “L”	t_{DHDL}	—	30	ns
$\overline{\text{DACK}}$ setup time	t_{DAWS}	20	—	ns
$\overline{\text{DACK}}$ hold time	t_{DAWH}	0	—	ns
$\overline{\text{WR}}$ “L” level pulse width	t_{DWR}	40	—	ns
$\overline{\text{WR}}$ “H” level pulse width	t_{DWRH}	30	—	ns
Input data setup time	t_{DDWS}	30	—	ns
Input data hold time	t_{DDWH}	0	—	ns



(4) 80-Series DMA Read Operation

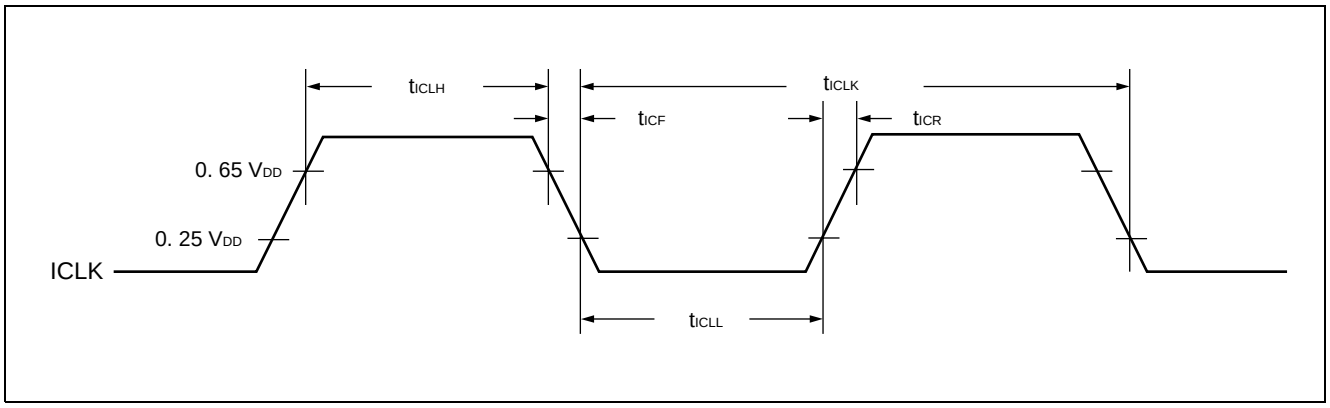
Parameter	Symbol	Value		Unit
		Min.	Max.	
DREQ “H” to $\overline{\text{DACK}}$ “L”	t_{DHAL}	0	—	ns
$\overline{\text{RD}}$ “H” to DREQ “L”	t_{DHDL}	—	30	ns
$\overline{\text{DACK}}$ setup time	t_{DARS}	20	—	ns
$\overline{\text{DACK}}$ hold time	t_{DARH}	0	—	ns
$\overline{\text{RD}}$ “L” level pulse width	t_{DRD}	40	—	ns
$\overline{\text{RD}}$ “H” level pulse width	t_{DRDH}	30	—	ns
Data output definition time	t_{DRLD}	—	40	ns
Data output disabled time	t_{DRHD}	5	—	ns



2.6 Isochronous Interface

2.6.1 ICLK

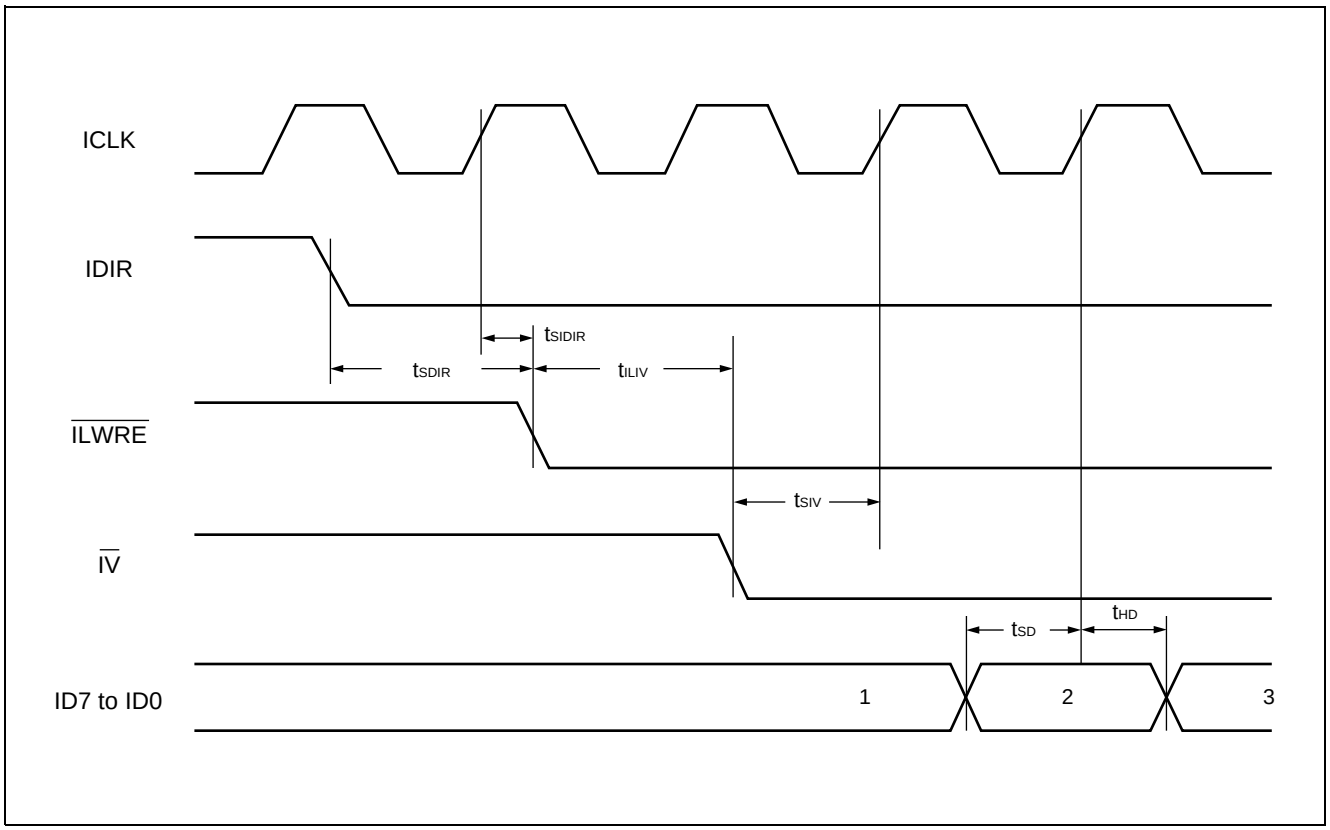
Parameter	Symbol	Value		Unit
		Min.	Max.	
Clock frequency	—	4	16	MHz
Clock cycle time	t_{ICLK}	62.5	250	ns
Clock “H” level pulse width	t_{ICLH}	20	—	ns
Clock “L” level pulse width	t_{ICLL}	20	—	ns
Clock rise time	t_{ICR}	—	7	ns
Clock fall time	t_{ICF}	—	7	ns



2.6.2 Sending Operation

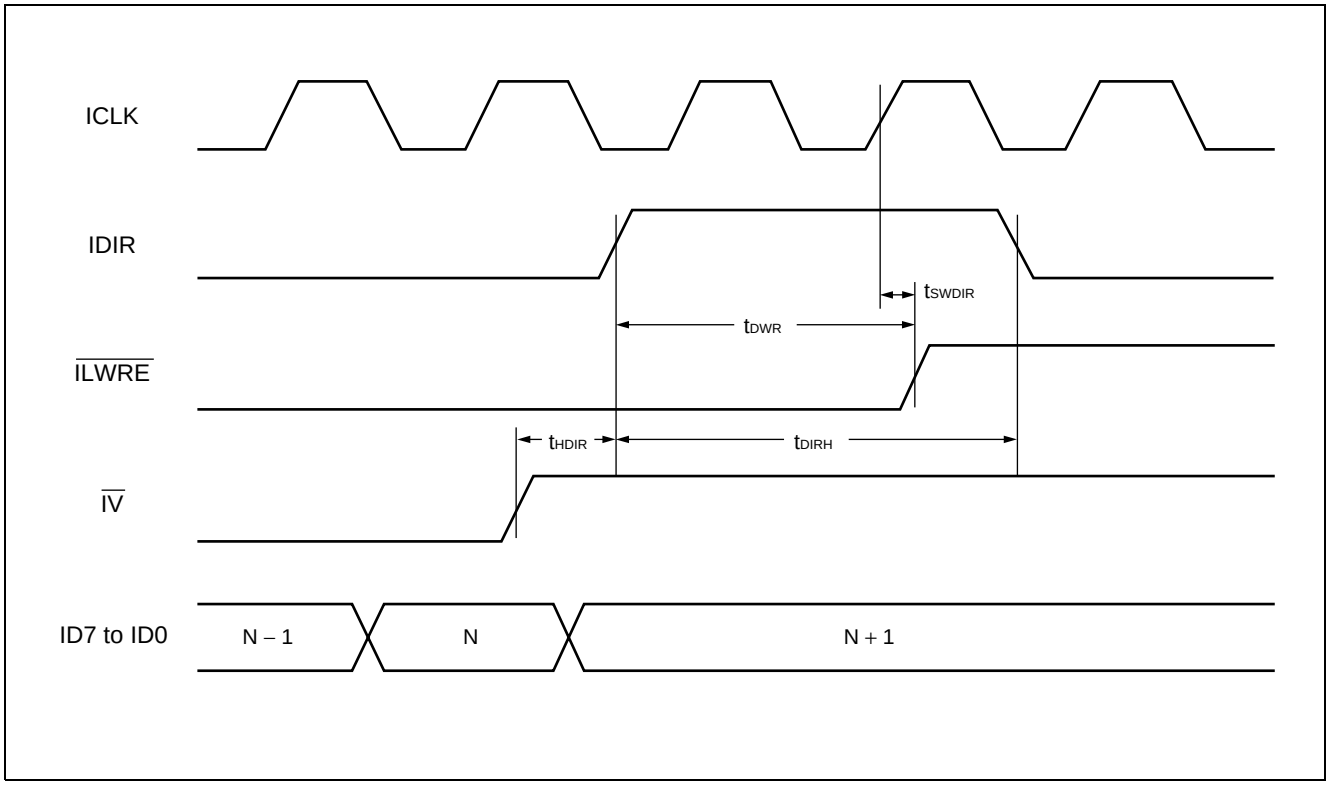
(1) Start Sending Operation

Parameter	Symbol	Value		Unit
		Min.	Max.	
IDIR fall to $\overline{\text{ILWRE}}$ fall time	t_{SDIR}	—	t_{ICLK} + 125	ns
ICLK rise to $\overline{\text{ILWRE}}$ fall time	t_{SIDIR}	—	40	ns
$\overline{\text{ILWRE}}$ fall to $\overline{\text{IV}}$ fall time	t_{ILIV}	0	—	ns
$\overline{\text{IV}}$ setup time	t_{SIV}	40	—	ns
Data setup time	t_{SD}	20	—	ns
Data hold time	t_{HD}	0	—	ns



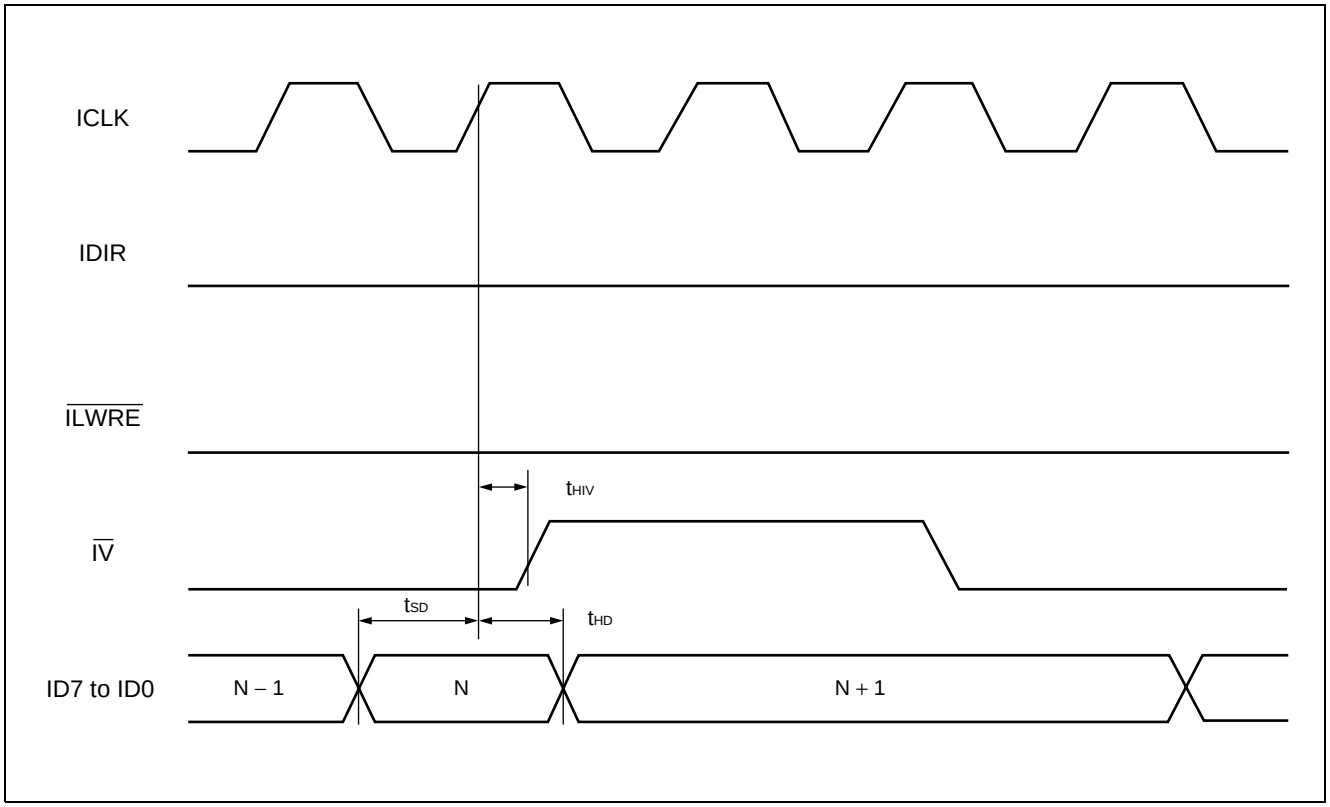
(2) End Sending Operation

Parameter	Symbol	Value		Unit
		Min.	Max.	
$\overline{IV}$ rise to IDIR rise time	t_{HDIR}	0	—	ns
IDIR rise to $\overline{ILWRE}$ rise time	t_{DWR}	—	1 t_{ICLK} + 40	ns
ICLK rise to $\overline{ILWRE}$ rise time	t_{SWDIR}	—	40	ns
IDIR rise to IDIR fall time	t_{DIRH}	250	—	µs



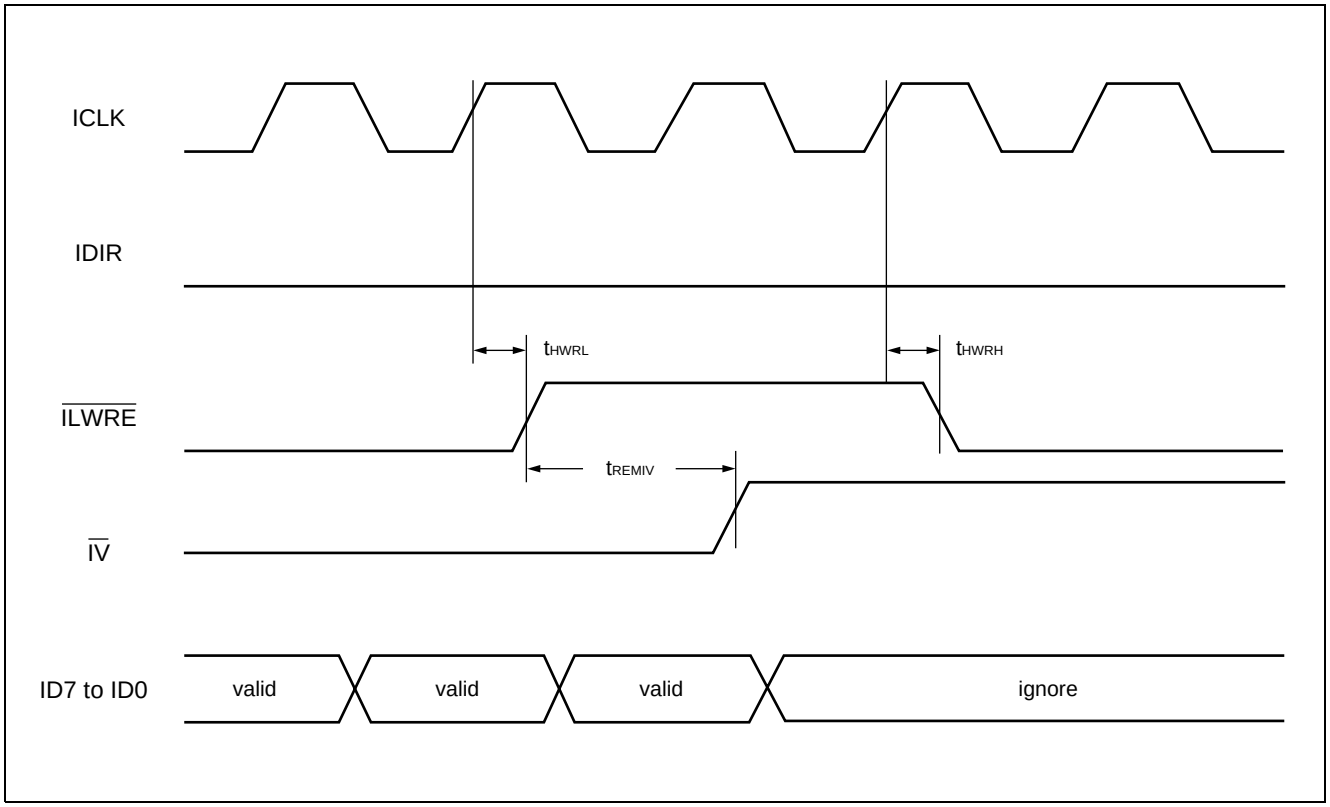
(3) $\overline{IV}$ Temporary Negation in Sending Operation

Parameter	Symbol	Value		Unit
		Min.	Max.	
$\overline{IV}$ hold time	t_{HIV}	0	t_{ICLK} – 40	ns
Date setup time	t_{SD}	20	—	ns
Data hold time	t_{HD}	0	—	ns



(4) Negating $\overline{\text{ILWRE}}$ during Transmission (with a bus reset detected or the FIFO buffer full)

Parameter	Symbol	Value		Unit
		Min.	Max.	
ICLK rise to $\overline{\text{ILWRE}}$ rise time	t_{HWRL}	—	40	ns
$\overline{\text{ILWRE}}$ rise to $\overline{\text{IV}}$ rise time	t_{REMIV}	t_{ICLK}	2 t_{ICLK} – 40	ns
ICLK rise to $\overline{\text{ILWRE}}$ fall time	t_{HWRH}	—	40	ns



Note: The $\overline{\text{ILWRE}}$ signal is negated to stop writing data to be transmitted in either of the following cases in the transmission mode

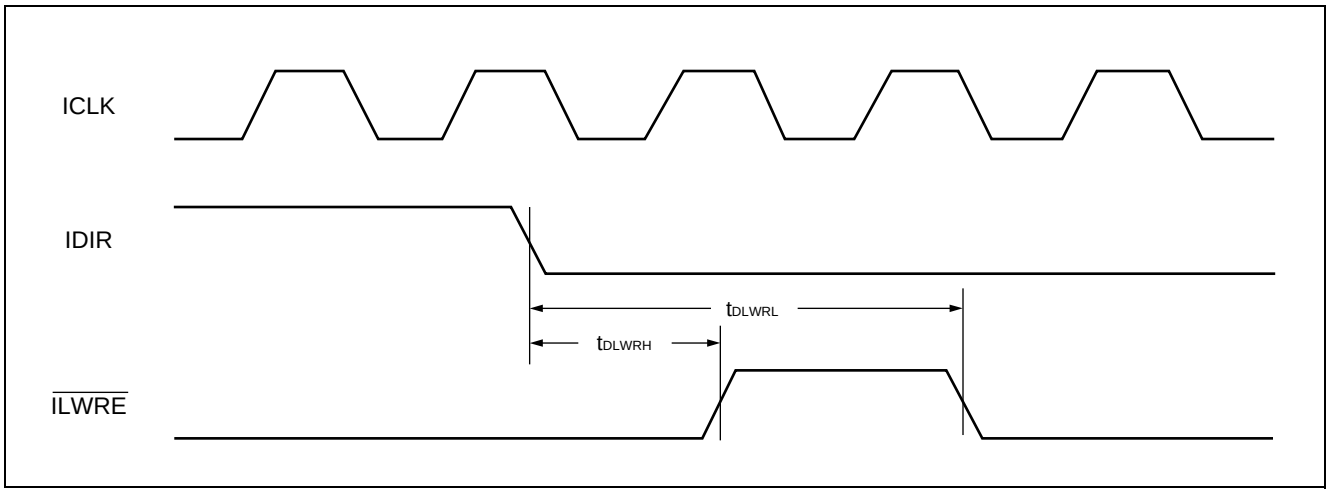
(1) When the ISO transmission/reception FIFO buffer becomes full (The $\overline{\text{ILWRE}}$ signal is negated in synchronization with the last ICLK signal generated before the FIFO buffer becomes full. Note, however, that this condition does not negate the $\overline{\text{ILWRE}}$ signal if the point-rcc bit (bit 7) in the ISO-FIFO control register (address 0Eh) has been set to “1.”

(2) When a bus reset is detected (The $\overline{\text{ILWRE}}$ signal is negated in synchronization with the last ICLK signal generated before the FIFO buffer loads one packet of data after detection of the bus reset.)

The $\overline{\text{ILWRE}}$ signal is asserted back when transmission of one packet of data to the 1394 bus is completed.

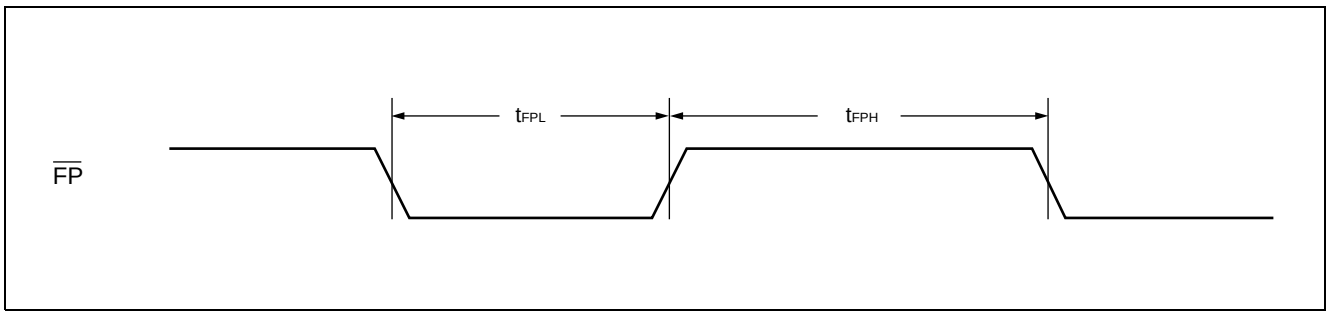
(5) Switch to Transmission from Reception in Process

Parameter	Symbol	Value		Unit
		Min.	Max.	
IDIR fall to $\overline{\text{ILWRE}}$ rise time	t_{DLWRH}	—	t_{ICLK} + 40	ns
IDIR fall to $\overline{\text{ILWRE}}$ fall time	t_{DLWRL}	—	2 t_{ICLK} + 40	ns



(6) $\overline{\text{FP}}$ Input Timing

Parameter	Symbol	Value		Unit
		Min.	Max.	
$\overline{\text{FP}}$ "L" level pulse width	t_{FPL}	100	—	ns
$\overline{\text{FP}}$ "H" level pulse width	t_{FPH}	125	—	µs
$\overline{\text{FP}}$ "H" detection to CTR value load	—	80	150	ns

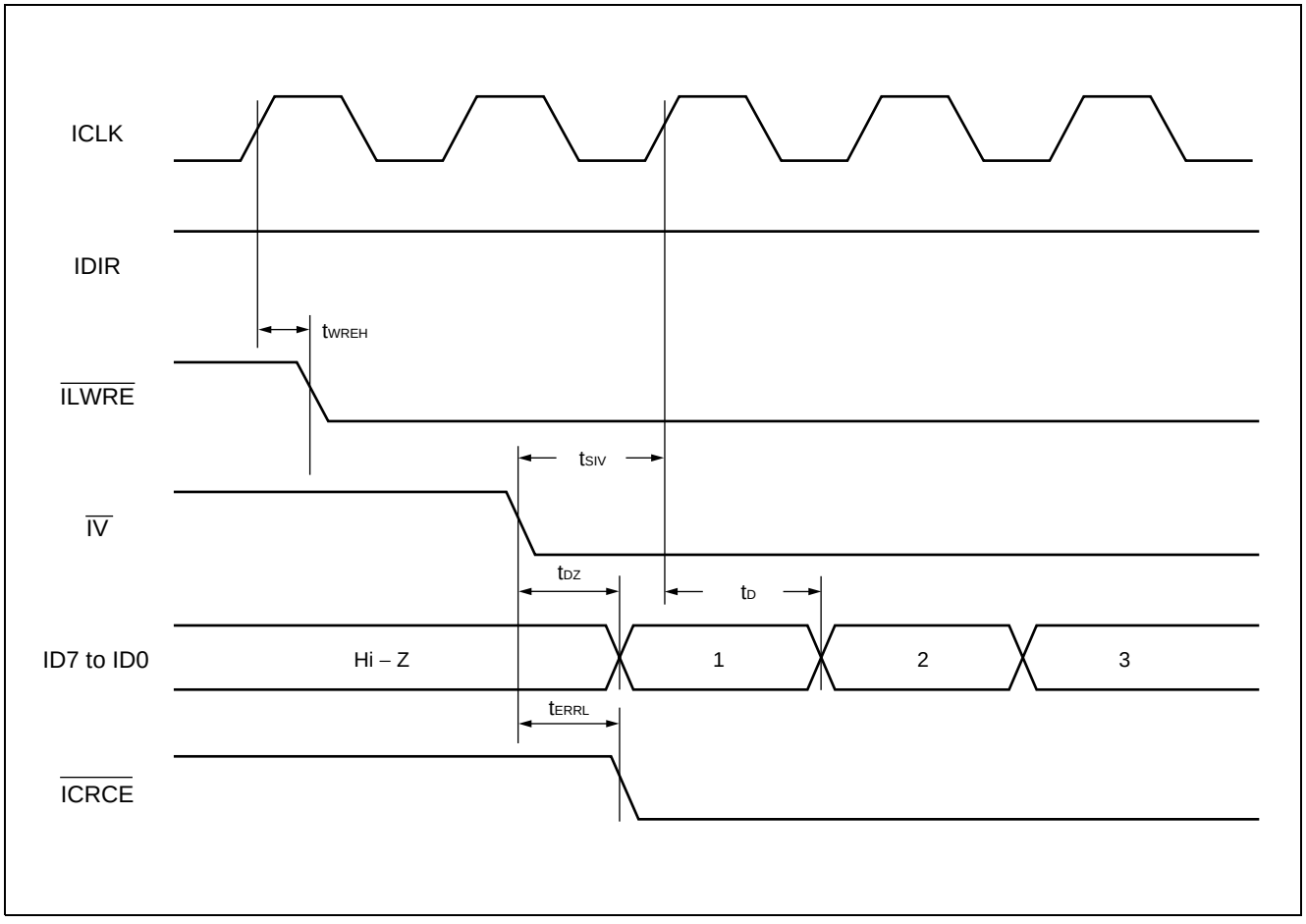


2.6.3 Receiving Operation

(1) Start Receiving Operation

Parameter	Symbol	Value		Unit
		Min.	Max.	
ICLK rise to $\overline{\text{ILWRE}}$ fall	t_{WREH}	—	40	ns
$\overline{\text{IV}}$ setup time	t_{SIV}	40	—	ns
Data output definition time	t_{DZ}	—	40	ns
Data output disable time	t_{D}	10	40	ns
$\overline{\text{IV}}$ fall to $\overline{\text{ICRCE}}$ fall time*	t_{ERRL}	—	40	ns

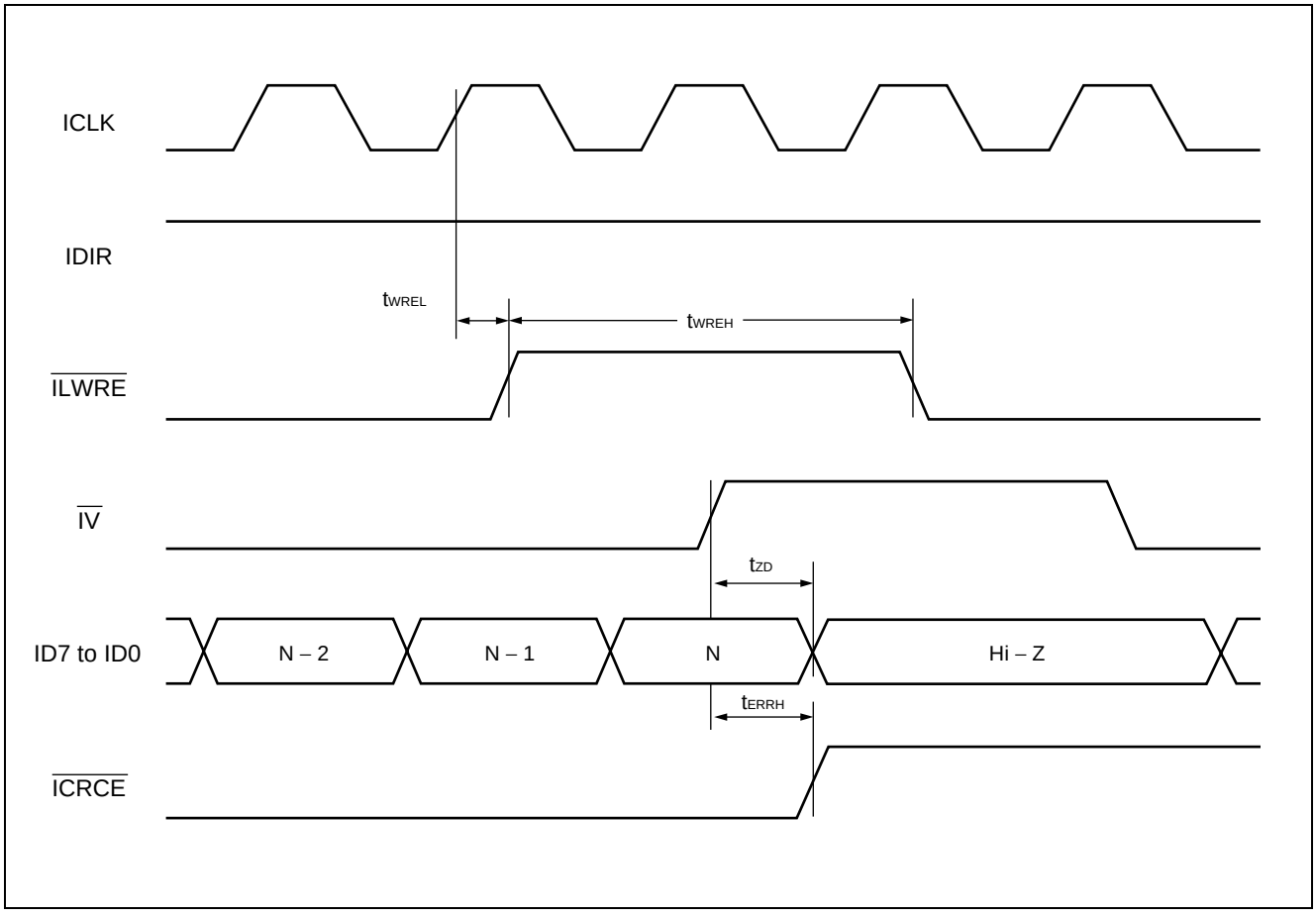
* : The $\overline{\text{ICRCE}}$ signal is output when a CRC error is detected in receiving data.



(2) End Receiving Operation

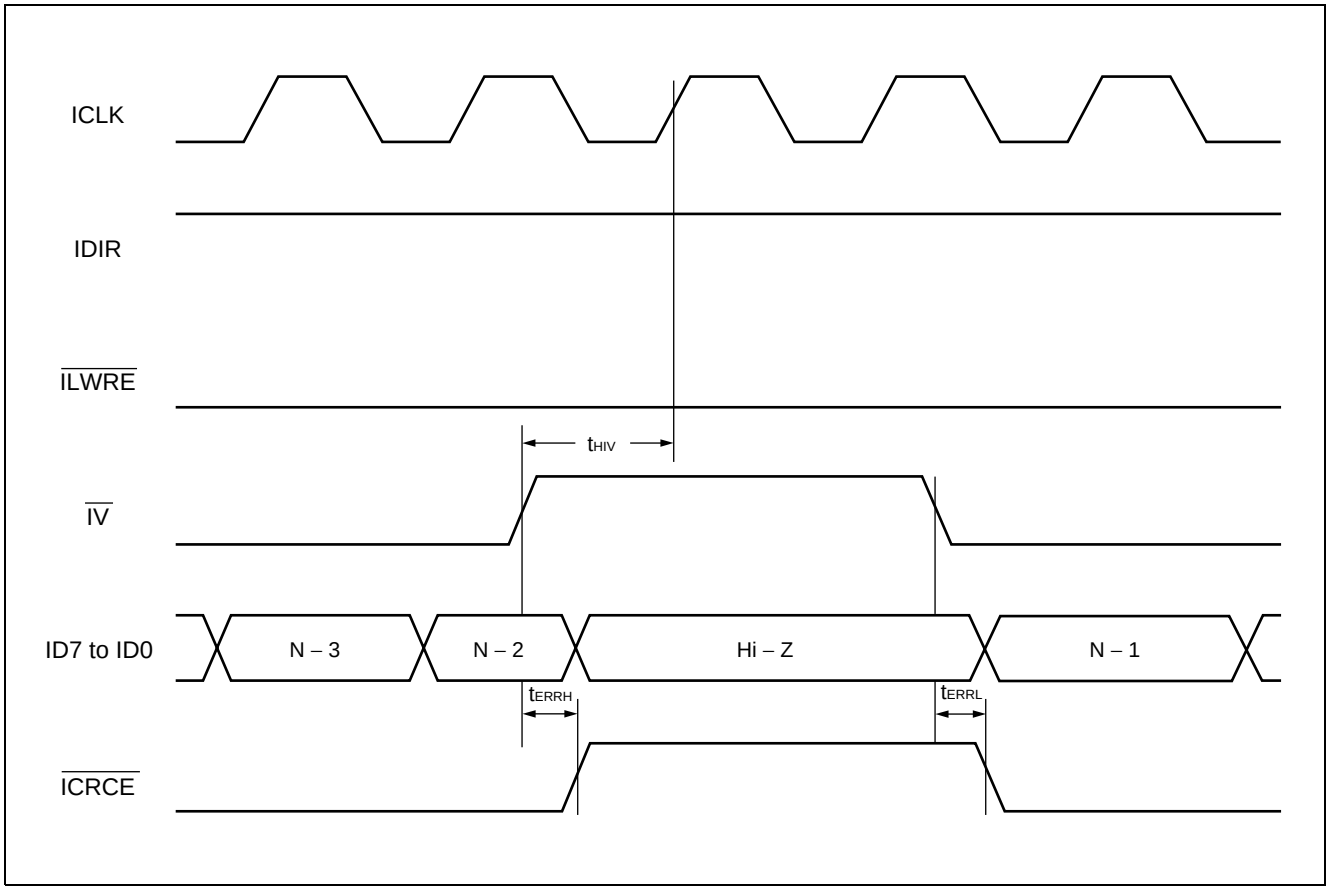
Parameter	Symbol	Value		Unit
		Min.	Max.	
ICLK rise to $\overline{\text{ILWRE}}$ rise	t_{WREL}	—	40	ns
Data output disable time	t_{ZD}	0	50	ns
$\overline{\text{ILWRE}}$ negate time*1	t_{WREH}	6 t_{ICLK}	—	ns
$\overline{\text{IV}}$ rise to $\overline{\text{ICRCE}}$ rise time*2	t_{ERRH}	—	40	ns

*1: This device negates the $\overline{\text{ILWRE}}$ signal upon completion of reading each packet of data.
*2: The $\overline{\text{ICRCE}}$ signal is asserted only when a CRC error is detected in data received.



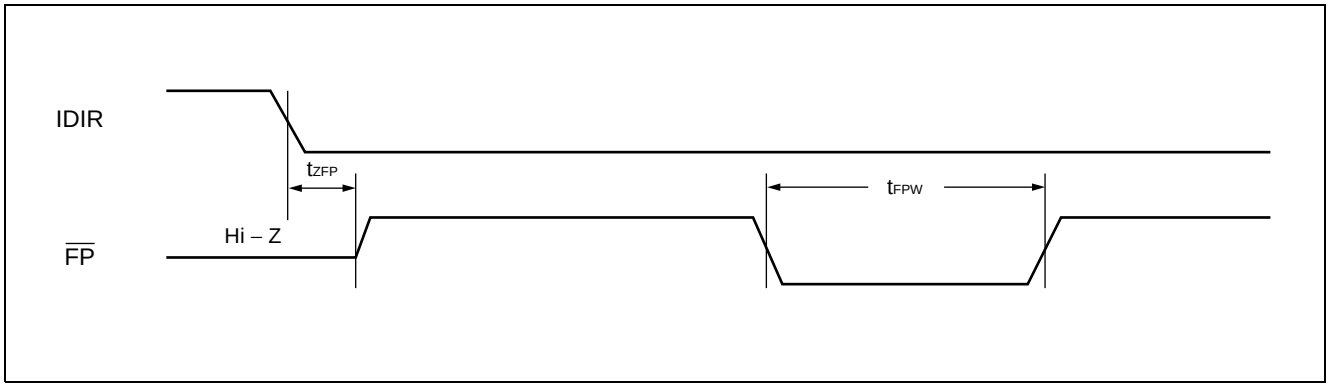
(3) $\overline{IV}$ Temporary Negation in Receiving Operation

Parameter	Symbol	Value		Unit
		Min.	Max.	
$\overline{IV}$ rise to ICLK rise	t_{HIV}	40	—	ns
$\overline{IV}$ rise to $\overline{ICRCE}$ rise time	t_{ERRH}	—	40	ns
$\overline{IV}$ fall to $\overline{ICRCE}$ fall time	t_{ERRL}	—	40	ns



(4) $\overline{FP}$ Signal Output

Parameter	Symbol	Value		Unit
		Min.	Max.	
IDIR fall to $\overline{FP}$ output enable	t_{ZFP}	—	40	ns
$\overline{FP}$ "L" level pulse width	t_{FPW}	600	730	ns
Time stamp match detect to $\overline{FP}$ output	—	—	40	ns

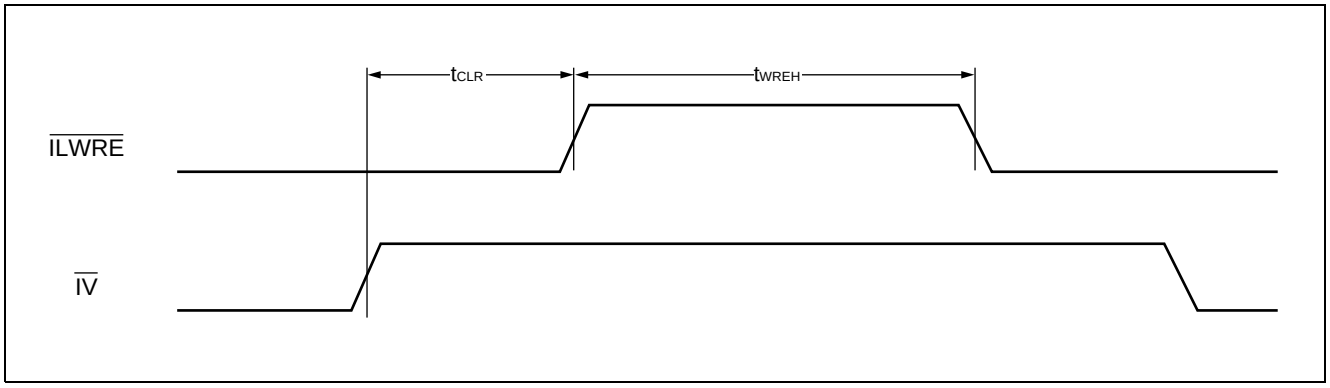


2.6.4 Clearing the ISO Transmission/Reception FIFO Buffer Using the fifo-clr Bit

The ISO transmission/reception FIFO buffer is cleared by setting the fifo-clr bit (bit 4) in the ISO-FIFO control register (address 0Eh) to "1." Given below is a timing chart for the isochronous interface when the FIFO buffer is cleared.

Note that this FIFO buffer clear function is available only when the point-rec bit (bit 7) or length-chk bit (bit 6) in the ISO-FIFO control register has been set to "1."

Parameter	Symbol	Value		Unit
		Min.	Max.	
$\overline{IV}$ rise to $\overline{ILWRE}$ rise	t_{CLR}	—	4 t_{ICLK}	ns
$\overline{ILWRE}$ negate time	t_{WREH}	—	7 t_{ICLK}	ns



* : The ISO transmission/reception FIFO buffer is cleared while the $\overline{ILWRE}$ signal is negated.

■ INTERNAL REGISTERS

The MB86615 internal registers have 3-bank construction, with 16-bit access to all registers.
Bank 0 contains registers necessary for IEEE 1394 settings and transfer, bank 1 contains registers necessary for AV/C (DVC) operation, and bank 2 contains CSR's.
In addition each bank has registers used in common for MB86615 device control.

1. Bank Common Registers

The following registers can be accessed in any bank from bank 0 to bank 2.

Address						Write operation	Read operation
HEX	A5	A4	A3	A2	A1		
00	0	0	0	0	0	mode-control register	←
02	0	0	0	0	1	(reserved)	flag & status register
04	0	0	0	1	0	instruction fetch register	←
06	0	0	0	1	1	interrupt mask register	interrupt code register
08	0	0	1	0	0	(reserved)	Receiving acknowledge display register
0A	0	0	1	0	1	ASYNC data port (sending)	ASYNC data port (receiving)
0C	0	0	1	1	0	mode-control-2 register	←
0E	0	0	1	1	1	ISO-FIFO control register	←
3E	1	1	1	1	1	bank select register	←

2. Bank 0 Registers

Bank 0 contains the registers required for 1394 settings and transfers.

Access to this bank is enabled by writing ‘0000h’ to the bank select register (3Eh).

Address						Write operation	Read operation
HEX	A5	A4	A3	A2	A1		
10	0	1	0	0	0	Sending ISO PKT header setting register (high)	Receiving ISO PKT header display register (high)
12	0	1	0	0	1	Sending ISO PKT header setting register (low)	Receiving ISO PKT header display register (low)
14	0	1	0	1	0	Sending ASYNC des ID setting register	Receiving ASYNC des ID setting register
16	0	1	0	1	1	Sending ASYNC PKT param setting register	Receiving ASYNC PKT param display register
18	0	1	1	0	0	Sending ASYNC data length setting register	Receiving ASYNC data length display register
1A	0	1	1	0	1	Sending ASYNC ex tcode setting register	Receiving ASYNC ex tcode display register
1C	0	1	1	1	0	Sending ASYNC source ID setting register	Receiving ASYNC source ID display register
1E	0	1	1	1	1	Sending ASYNC resp param setting register	Receiving ASYNC resp param display register
20	1	0	0	0	0	Sending ASYNC des offset setting register (high)	Receiving ASYNC des offset display register (high)
22	1	0	0	0	1	Sending ASYNC des offset setting register (middle)	Receiving ASYNC des offset display register (middle)
24	1	0	0	1	0	Sending ASYNC des offset setting register (low)	Receiving ASYNC des offset display register (low)
26	1	0	0	1	1	(reserved)	←
28	1	0	1	0	0	(reserved)	PHY ID display register
2A	1	0	1	0	1	(reserved)	NODE config display register
2C	1	0	1	1	0	(reserved)	←
2E	1	0	1	1	1	(reserved)	PORT config display register
30	1	1	0	0	0	state clear setting register	root ID display register
32	1	1	0	0	1	Self ID PKT param setting register	ISO resource manager ID display register
34	1	1	0	1	0	Receiving ISO-channel setting register (0, 1)	←
36	1	1	0	1	1	Receiving ISO-channel setting register (2, 3)	←
38	1	1	1	0	0	(reserved)	cycle timer monitor display register (high)
3A	1	1	1	0	1	(reserved)	cycle timer monitor display register (low)
3C	1	1	1	1	0	(reserved)	←

3. Bank 1 Registers

Bank 1 contains the registers required for AV/C (DVC) protocols.

Access to this bank is enabled by writing ‘0001h’ to the bank select register (3Eh).

Address						Write operation	Read operation
HEX	A5	A4	A3	A2	A1		
10	0	1	0	0	0	Sending time stamp offset setting register	←
12	0	1	0	0	1	Receiving time stamp offset setting register	←
14	0	1	0	1	0	Sending CIP header DBS setting register	Receiving CIP header display register (highest)
16	0	1	0	1	1	(reserved)	Receiving CIP header display register (high)
18	0	1	1	0	0	Sending CIP header FMT setting register	Receiving CIP header display register (low)
1A	0	1	1	0	1	(reserved)	Receiving CIP header display register (lowest)
1C	0	1	1	1	0	OMPR (high)	←
1E	0	1	1	1	1	OMPR (low)	←
20	1	0	0	0	0	OPCR0 (high)	←
22	1	0	0	0	1	OPCR0 (low)	←
24	1	0	0	1	0	(reserved)	←
26	1	0	0	1	1	(reserved)	←
28	1	0	1	0	0	(reserved)	←
2A	1	0	1	0	1	(reserved)	←
2C	1	0	1	1	0	IMPR (high)	←
2E	1	0	1	1	1	IMPR (low)	←
30	1	1	0	0	0	IPCR0 (high)	←
32	1	1	0	0	1	IPCR0 (low)	←
34	1	1	0	1	0	(reserved)	←
36	1	1	0	1	1	(reserved)	←
38	1	1	1	0	0	(reserved)	←
3A	1	1	1	0	1	(reserved)	←
3C	1	1	1	1	0	set-PCR & FP-timeout setting register	←

4. Bank 2 Registers

Bank 2 contains CSR's required for Isochronous resource manager.

Access to this bank is enabled by writing '0002h' to the bank select register (3Eh).

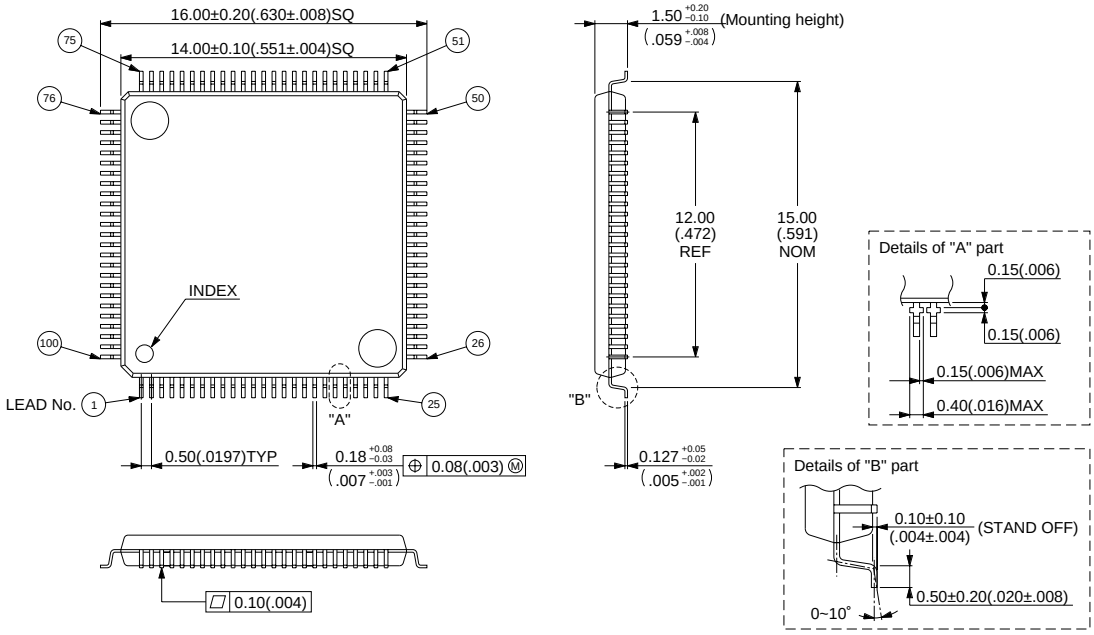
Address						Write operation	Read operation
HEX	A5	A4	A3	A2	A1		
10	0	1	0	0	0	bus manager ID register (high)	←
12	0	1	0	0	1	bus manager ID register (low)	←
14	0	1	0	1	0	bandwidth available register (high)	←
16	0	1	0	1	1	bandwidth available register (low)	←
18	0	1	1	0	0	channels available high register (high)	←
1A	0	1	1	0	1	channels available high register (low)	←
1C	0	1	1	1	0	channels available low register (high)	←
1E	0	1	1	1	1	channels available low register (low)	←
20	1	0	0	0	0	(reserved)	←
22	1	0	0	0	1	(reserved)	←
24	1	0	0	1	0	(reserved)	←
26	1	0	0	1	1	(reserved)	←
28	1	0	1	0	0	(reserved)	←
2A	1	0	1	0	1	(reserved)	←
2C	1	0	1	1	0	(reserved)	←
2E	1	0	1	1	1	(reserved)	←
30	1	1	0	0	0	(reserved)	←
32	1	1	0	0	1	(reserved)	←
34	1	1	0	1	0	(reserved)	←
36	1	1	0	1	1	(reserved)	←
38	1	1	1	0	0	(reserved)	←
3A	1	1	1	0	1	(reserved)	←
3C	1	1	1	1	0	(reserved)	←

■ ORDERING INFORMATION

Partnumber	Package	Remarks
MB86615PFV	100-pin plastic LQFP (FPT-100P-M05)	
MB86615PBT	120-pin plastic FBGA (BGA-120P-M01)	

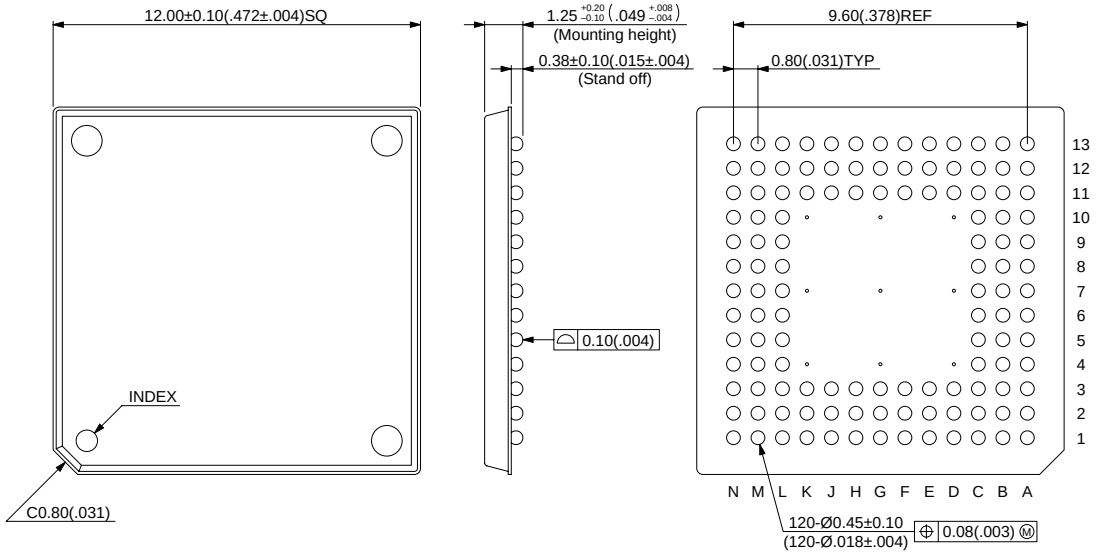
■ PACKAGE DIMENSIONS

100-pin plastic LQFP
(FPT-100P-M05)



Dimensions in mm (inches)

120-pin plastic FBGA
(BGA-120P-M01)



Dimensions in mm (inches)

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