

**MEMORY Mobile FCRAM™**  
CMOS**64M Bit (4 M word × 16 bit)***Mobile Phone Application Specific Memory***MB82DP04183C-65L****DESCRIPTION**

The FUJITSU MB82DP04183C is a CMOS Fast Cycle Random Access Memory (FCRAM\*) with asynchronous Static Random Access Memory (SRAM) interface containing 67,108,864 storages accessible in a 16-bit format. MB82DP04183C is utilized using a FUJITSU advanced FCRAM core technology and improved integration in comparison to regular SRAM.

This MB82DP04183C is suited for mobile applications such as Cellular Handset and PDA.

\*: FCRAM is a trademark of Fujitsu Limited, Japan.

**PRODUCT LINEUP**

Parameter	MB82DP04183C-65L
Access time (Max) ( $t_{CE}$ , $t_{AA}$ )	65 ns
Active current (Max) ( $I_{DDA1}$ )	40 mA
Standby current (Max) ( $I_{DDs1}$ )	90 $\mu$ A
Power down current (Max) ( $I_{DDPS}$ )	10 $\mu$ A

**FEATURES**

- Asynchronous SRAM Interface
- Fast Access Cycle Time :  $t_{AA} = t_{CE} = 65$  ns Max
- 8 words Page Access Capability :  $t_{PAA} = 20$  ns Max
- Low Voltage Operating Condition :  $V_{DD} = +2.6$  V to  $+3.1$  V
- Wide Operating Temperature :  $T_A = -30$  °C to  $+85$  °C
- Byte Control by  $\overline{LB}$  and  $\overline{UB}$
- Low Power Consumption :  $I_{DDA1} = 40$  mA Max  
 $I_{DDs1} = 90$   $\mu$ A Max (  $T_A = +40$  °C)
- Various Power Down mode : Sleep  
8M-bit Partial  
16M-bit Partial
- Shipping Form : Wafer/Chip

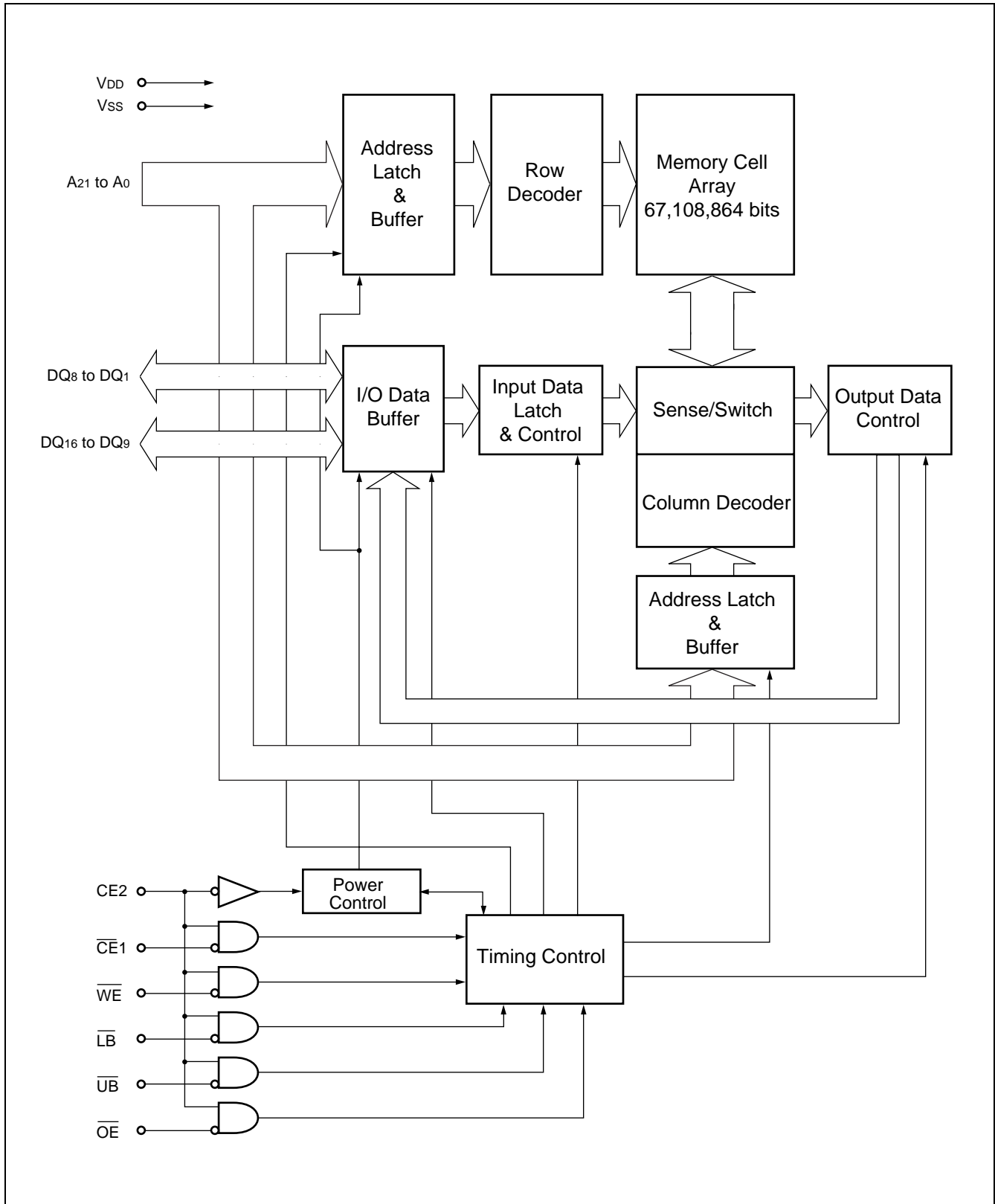
# MB82DP04183C-65L

## ■ PIN DESCRIPTION

Pin Name	Description
A <sub>21</sub> to A <sub>0</sub>	Address Input
$\overline{CE}1$	Chip Enable 1 (Low Active)
CE2	Chip Enable 2 (High Active)
$\overline{WE}$	Write Enable (Low Active)
$\overline{OE}$	Output Enable (Low Active)
$\overline{LB}$	Lower Byte Control (Low Active)
$\overline{UB}$	Upper Byte Control (Low Active)
DQ <sub>8</sub> to DQ <sub>1</sub>	Lower Byte Data Input/Output
DQ <sub>16</sub> to DQ <sub>9</sub>	Upper Byte Data Input/Output
V <sub>DD</sub>	Power Supply Voltage
V <sub>SS</sub>	Ground

Note : Refer to “■ PACKAGE FOR ENGINEERING SAMPLES” for the pin description of FBGA package supply.

## ■ BLOCK DIAGRAM



## FUNCTION TRUTH TABLE

Mode	CE2	$\overline{CE1}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	A <sub>21</sub> to A <sub>0</sub>	DQ <sub>8</sub> to DQ <sub>1</sub>	DQ <sub>16</sub> to DQ <sub>9</sub>
Standby (Deselect)	H	H	X	X	X	X	X	High-Z	High-Z
Output Disable*1	H	L	H	H	X	X	*3	High-Z	High-Z
Output Disable (No Read)			H	L	H	H	Valid	High-Z	High-Z
Read (Upper Byte)					H	L	Valid	High-Z	Output Valid
Read (Lower Byte)					L	H	Valid	Output Valid	High-Z
Read (Word)					L	L	Valid	Output Valid	Output Valid
No Write			L	H*4	H	H	Valid	Invalid	Invalid
Write (Upper Byte)					H	L	Valid	Invalid	Input Valid
Write (Lower Byte)					L	H	Valid	Input Valid	Invalid
Write (Word)					L	L	Valid	Input Valid	Input Valid
Power Down*2			L	X	X	X	X	X	X

Notes : L = V<sub>IL</sub>, H = V<sub>IH</sub>, X can be either V<sub>IL</sub> or V<sub>IH</sub>, High-Z = High Impedance

\*1 : Should not be kept this logic condition longer than 1 μs.

\*2 : Power Down mode can be entered from Standby state and all DQ pins are in High-Z state.  
Data retention depends on the selection of Power Down Program.  
Refer to "■ Power Down" for the detail.

\*3 : Can be either V<sub>IL</sub> or V<sub>IH</sub> but must be valid before Read or Write.

\*4 :  $\overline{OE}$  can be V<sub>IL</sub> during Write operation if the following conditions are satisfied;

(1) Write pulse is initiated by  $\overline{CE1}$ . See "(12) Read/Write Timing #1-1 ( $\overline{CE1}$  Control)" in "■ TIMING DIAGRAMS".

(2)  $\overline{OE}$  stays V<sub>IL</sub> during Write cycle.

## ■ POWER DOWN

### Power Down

The Power Down is low power idle state controlled by CE2. CE2 Low drives the device in power down mode and maintains low power idle state as long as CE2 is kept Low. CE2 High resumes the device from power down mode.

This device has three power down modes, Sleep, 8M-bit Partial and 16M-bit Partial. These can be programmed by series of read/write operation. Each mode has following features.

Mode	Data Retention	Retention Address
Sleep (default)	No	N/A
8M-bit Partial	8M bits	000000h to 07FFFFh
16M-bit Partial	16M bits	000000h to 0FFFFFFh

The default state is Sleep and it is the lowest power consumption but all data will be lost once CE2 is brought to Low for Power Down. It is not required to program to Sleep mode after power-up.

### Power Down Program Sequence

The program requires total six read/write operations with unique address. Between each read/write operation requires that device be in standby mode. Following table shows the detail sequence.

Cycle #	Operation	Address	Data
1st	Read	3FFFFFFh (MSB)	Read Data (RDa)
2nd	Write	3FFFFFFh	RDa
3rd	Write	3FFFFFFh	RDa
4th	Write	3FFFFFFh	Don't care (X)
5th	Write	3FFFFFFh	X
6th	Read	Address Key	Read Data (RDb)

The first cycle is to read from most significant address (MSB).

The second and third cycle are to write to MSB. If the second or third cycle is written into the different address, the program is cancelled and the data written by the second or third cycle is valid as a normal write operation. It is recommended to write back the data (RDa) read by first cycle to MSB in order to secure the data.

The fourth and fifth cycle is to write to MSB. The data of fourth and fifth cycle are don't-care. If the fourth or fifth cycle is written into different address, the program is also cancelled but write data may not be written as normal write operation.

The last cycle is to read from specific address key for power down mode selection. And read data (RDb) is invalid. Once this program sequence is performed from a Partial mode to other Partial mode, the write data stored in memory cell array may be lost. So, it should perform this program prior to regular read/write operation if Partial power down mode is used.

### Address Key

The address key has following format.

Mode	Address				
	A <sub>21</sub>	A <sub>20</sub>	A <sub>19</sub>	A <sub>18</sub> to A <sub>0</sub>	Binary
Sleep (default)	1	1	1	1	3FFFFFFh
8M-bit Partial	1	0	1	1	2FFFFFFh
16M-bit Partial	1	0	0	1	27FFFFFFh

## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Voltage of $V_{DD}$ Supply Relative to $V_{SS}^*$	$V_{DD}$	- 0.5	+ 3.6	V
Voltage at Any Pin Relative to $V_{SS}^*$	$V_{IN}, V_{OUT}$	- 0.5	+ 3.6	V
Short Circuit Output Current	$I_{OUT}$	- 50	+ 50	mA
Storage Temperature	$T_{STG}$	- 55	+ 125	°C

\* : All voltages are referenced to  $V_{SS}$ .

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min	Max	
Supply Voltage* <sup>1</sup>	$V_{DD}$	2.6	3.1	V
	$V_{SS}$	0	0	V
High Level Input Voltage * <sup>1, *2</sup>	$V_{IH}$	$V_{DD} \times 0.8$	$V_{DD} + 0.2$	V
Low Level Input Voltage * <sup>1, *3</sup>	$V_{IL}$	- 0.3	$V_{DD} \times 0.2$	V
Ambient Temperature	$T_A$	- 30	+ 85	°C

\*1 : All voltages are referenced to  $V_{SS}$ .

\*2 : Maximum DC voltage on input and I/O pins are  $V_{DD} + 0.2$  V. During voltage transitions, inputs may overshoot to  $V_{DD} + 1.0$  V for periods of up to 5 ns.

\*3 : Minimum DC voltage on input or I/O pins are -0.3 V. During voltage transitions, inputs may undershoot  $V_{SS}$  to -1.0 V for periods of up to 5 ns.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

### 1. DC CHARACTERISTICS

Parameter	Symbol	Test conditions	Value		Unit	
			Min	Max		
Input Leakage Current	$I_{LI}$	$V_{SS} \leq V_{IN} \leq V_{DD}$	-1.0	+1.0	$\mu A$	
Output Leakage Current	$I_{LO}$	$0 V \leq V_{OUT} \leq V_{DD}$ , Output Disable	-1.0	+1.0	$\mu A$	
Output High Voltage Level	$V_{OH}$	$V_{DD} = V_{DD} \text{ Min}$ , $I_{OH} = -0.5 \text{ mA}$	2.4	—	V	
Output Low Voltage Level	$V_{OL}$	$I_{OL} = 1 \text{ mA}$	—	0.4	V	
$V_{DD}$ Power Down Current	$I_{DDPS}$	$V_{DD} = V_{DD} \text{ Max}$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$ , $\overline{CE2} \leq 0.2 \text{ V}$	Sleep	—	10	$\mu A$
	$I_{DDP8}$		8M-bit Partial	—	80	$\mu A$
	$I_{DDP16}$		16M-bit Partial	—	100	$\mu A$
$V_{DD}$ Standby Current	$I_{DDS}$	$V_{DD} = V_{DD} \text{ Max}$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$ , $\overline{CE1} = \overline{CE2} = V_{IH}$	—	1.5	mA	
	$I_{DDS1}$	$V_{DD} = V_{DD} \text{ Max}$ , $V_{IN} \leq 0.2 \text{ V}$ or $V_{IN} \geq V_{DD} - 0.2 \text{ V}$ , $\overline{CE1} = \overline{CE2} \geq V_{DD} - 0.2 \text{ V}$	$T_A \leq +85 \text{ }^\circ\text{C}$	—	170	$\mu A$
		$T_A \leq +40 \text{ }^\circ\text{C}$	—	90		
$V_{DD}$ Active Current	$I_{DDA1}$	$V_{DD} = V_{DD} \text{ Max}$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$ , $\overline{CE1} = V_{IL}$ and $\overline{CE2} = V_{IH}$ , $I_{OUT} = 0 \text{ mA}$	$t_{RC}/t_{WC} = \text{Min}$	—	40	mA
	$I_{DDA2}$		$t_{RC}/t_{WC} = 1 \text{ } \mu\text{s}$	—	5	mA
$V_{DD}$ Page Read Current	$I_{DDA3}$	$V_{DD} = V_{DD} \text{ Max}$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$ , $\overline{CE1} = V_{IL}$ and $\overline{CE2} = V_{IH}$ , $I_{OUT} = 0 \text{ mA}$ , $t_{PRC} = \text{Min}$	—	10	mA	

- Notes :
- All voltages are referenced to  $V_{SS}$ .
  - DC characteristics are measured after following Power-up timing.
  - $I_{OUT}$  depends on the output load conditions.

## 2. AC CHARACTERISTICS

### (1) READ OPERATION

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Read Cycle Time	$t_{RC}$	65	1000	ns	*1, *2
$\overline{CE1}$ Access Time	$t_{CE}$	—	65	ns	*3
$\overline{OE}$ Access Time	$t_{OE}$	—	40	ns	*3
Address Access Time	$t_{AA}$	—	65	ns	*3, *5
$\overline{LB}$ , $\overline{UB}$ Access Time	$t_{BA}$	—	30	ns	*3
Page Address Access Time	$t_{PAA}$	—	20	ns	*3, *6
Page Read Cycle Time	$t_{PRC}$	20	1000	ns	*1, *6, *7
Output Data Hold Time	$t_{OH}$	5	—	ns	*3
$\overline{CE1}$ Low to Output Low-Z	$t_{CLZ}$	5	—	ns	*4
$\overline{OE}$ Low to Output Low-Z	$t_{OLZ}$	10	—	ns	*4
$\overline{LB}$ , $\overline{UB}$ Low to Output Low-Z	$t_{BLZ}$	0	—	ns	*4
$\overline{CE1}$ High to Output High-Z	$t_{CHZ}$	—	20	ns	*3
$\overline{OE}$ High to Output High-Z	$t_{OHZ}$	—	14	ns	*3
$\overline{LB}$ , $\overline{UB}$ High to Output High-Z	$t_{BHZ}$	—	20	ns	*3
Address Setup Time to $\overline{CE1}$ Low	$t_{ASC}$	-6	—	ns	
Address Setup Time to $\overline{OE}$ Low	$t_{ASO}$	10	—	ns	
Address Invalid Time	$t_{AX}$	—	10	ns	*5, *8
Address Hold Time from $\overline{CE1}$ High	$t_{CHAH}$	-6	—	ns	*9
Address Hold Time from $\overline{OE}$ High	$t_{OHAH}$	-6	—	ns	
$\overline{WE}$ High to $\overline{OE}$ Low Time for Read	$t_{WHOL}$	25	1000	ns	*10
$\overline{CE1}$ High Pulse Width	$t_{CP}$	12	—	ns	

\*1 : Maximum value is applicable if  $\overline{CE1}$  is kept at Low without change of address input of  $A_{21}$  to  $A_3$ .

\*2 : Address should not be changed within minimum  $t_{RC}$ .

\*3 : The output load 50 pF.

\*4 : The output load 5 pF.

\*5 : Applicable to  $A_{21}$  to  $A_3$  when  $\overline{CE1}$  is kept at Low.

\*6 : Applicable only to  $A_2$ ,  $A_1$  and  $A_0$  when  $\overline{CE1}$  is kept at Low for the page address access.

\*7 : In case Page Read Cycle is continued with keeping  $\overline{CE1}$  stays Low,  $\overline{CE1}$  must be brought to High within 4  $\mu$ s. In other words, Page Read Cycle must be closed within 4  $\mu$ s.

\*8 : Applicable to address access when at least two of address inputs are switched from previous state.

\*9 :  $t_{RC}(\text{Min})$  and  $t_{PRC}(\text{Min})$  must be satisfied.

\*10 : If actual value of  $t_{WHOL}$  is shorter than specified minimum values, the actual  $t_{AA}$  of following Read may become longer by the amount of subtracting actual value from specified minimum value.



## (2) WRITE OPERATION

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Write Cycle Time	$t_{WC}$	65	1000	ns	*1, *2
Address Setup Time	$t_{AS}$	0	—	ns	*3
$\overline{CE1}$ Write Pulse Width	$t_{CW}$	40	—	ns	*3
$\overline{WE}$ Write Pulse Width	$t_{WP}$	40	—	ns	*3
$\overline{LB}$ , $\overline{UB}$ Write Pulse Width	$t_{BW}$	40	—	ns	*3
$\overline{LB}$ , $\overline{UB}$ Byte Mask Setup Time	$t_{BS}$	-5	—	ns	*4
$\overline{LB}$ , $\overline{UB}$ Byte Mask Hold Time	$t_{BH}$	-5	—	ns	*5
Write Recovery Time	$t_{WR}$	0	—	ns	*6
$\overline{CE1}$ High Pulse Width	$t_{CP}$	12	—	ns	
$\overline{WE}$ High Pulse Width	$t_{WHP}$	12	1000	ns	
$\overline{LB}$ , $\overline{UB}$ High Pulse Width	$t_{BHP}$	12	1000	ns	
Data Setup Time	$t_{DS}$	12	—	ns	
Data Hold Time	$t_{DH}$	0	—	ns	
$\overline{OE}$ High to $\overline{CE1}$ Low Setup Time for Write	$t_{OHCL}$	-5	—	ns	*7
$\overline{OE}$ High to Address Setup Time for Write	$t_{OES}$	0	—	ns	*8
$\overline{LB}$ and $\overline{UB}$ Write Pulse Overlap	$t_{BWO}$	30	—	ns	

\*1 : Maximum value is applicable if  $\overline{CE1}$  is kept at Low without any address change.

\*2 : Minimum value must be equal or greater than the sum of write pulse ( $t_{CW}$ ,  $t_{WP}$  or  $t_{BW}$ ) and write recovery time ( $t_{WR}$ ).

\*3 : Write pulse is defined from High to Low transition of  $\overline{CE1}$ ,  $\overline{WE}$ ,  $\overline{LB}$  or  $\overline{UB}$ , whichever occurs last.

\*4 : Applicable for byte mask only. Byte mask setup time is defined to the High to Low transition of  $\overline{CE1}$  or  $\overline{WE}$  whichever occurs last.

\*5 : Applicable for byte mask only. Byte mask hold time is defined from the Low to High transition of  $\overline{CE1}$  or  $\overline{WE}$  whichever occurs first.

\*6 : Write recovery is defined from Low to High transition of  $\overline{CE1}$ ,  $\overline{WE}$ ,  $\overline{LB}$  or  $\overline{UB}$ , whichever occurs first.

\*7 : If  $\overline{OE}$  is Low after minimum  $t_{OHCL}$ , read cycle is initiated. In other word,  $\overline{OE}$  must be brought to High within 5 ns after  $\overline{CE1}$  is brought to Low.

\*8 : If  $\overline{OE}$  is Low after new address input, read cycle is initiated. In other word,  $\overline{OE}$  must be brought to High at the same time or before new address valid.

### (3) POWER DOWN PARAMETERS

Parameter	Symbol	Value		Unit	Note
		Min	Max		
CE2 Low Setup Time for Power Down Entry	t <sub>CSP</sub>	10	—	ns	
CE2 Low Hold Time after Power Down Entry	t <sub>C2LP</sub>	65	—	ns	
$\overline{CE1}$ High Hold Time following CE2 High after Power Down Exit [Sleep mode only]	t <sub>CHH</sub>	300	—	μs	*1
$\overline{CE1}$ High Hold Time following CE2 High after Power Down Exit [not in Sleep mode]	t <sub>CHHP</sub>	70	—	ns	*2
$\overline{CE1}$ High Setup Time following CE2 High after Power Down Exit	t <sub>CHS</sub>	0	—	ns	*1

\*1 : Applicable also to power-up.

\*2 : Applicable when 8M-bit and 16M-bit Partial mode is programmed.

### (4) OTHER TIMING PARAMETERS

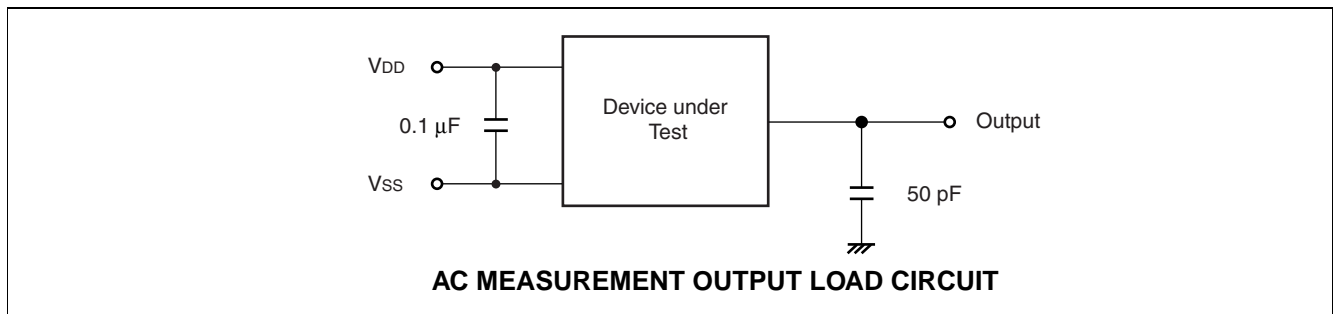
Parameter	Symbol	Value		Unit	Note
		Min	Max		
$\overline{CE1}$ High to $\overline{OE}$ Invalid Time for Standby Entry	t <sub>CHOX</sub>	10	—	ns	
$\overline{CE1}$ High to $\overline{WE}$ Invalid Time for Standby Entry	t <sub>CHWX</sub>	10	—	ns	*1
CE2 Low Hold Time after Power-up	t <sub>C2LH</sub>	50	—	μs	
$\overline{CE1}$ High Hold Time following CE2 High after Power-up	t <sub>CHH</sub>	300	—	μs	
Input Transition Time	t <sub>T</sub>	1	25	ns	*2

\*1 : Some data might be written into any address location if t<sub>CHWX</sub>(Min) is not satisfied.

\*2 : The Input Transition Time (t<sub>T</sub>) at AC testing is 5 ns as shown in below. If actual t<sub>T</sub> is longer than 5 ns, it may violate AC specification of some timing parameters.

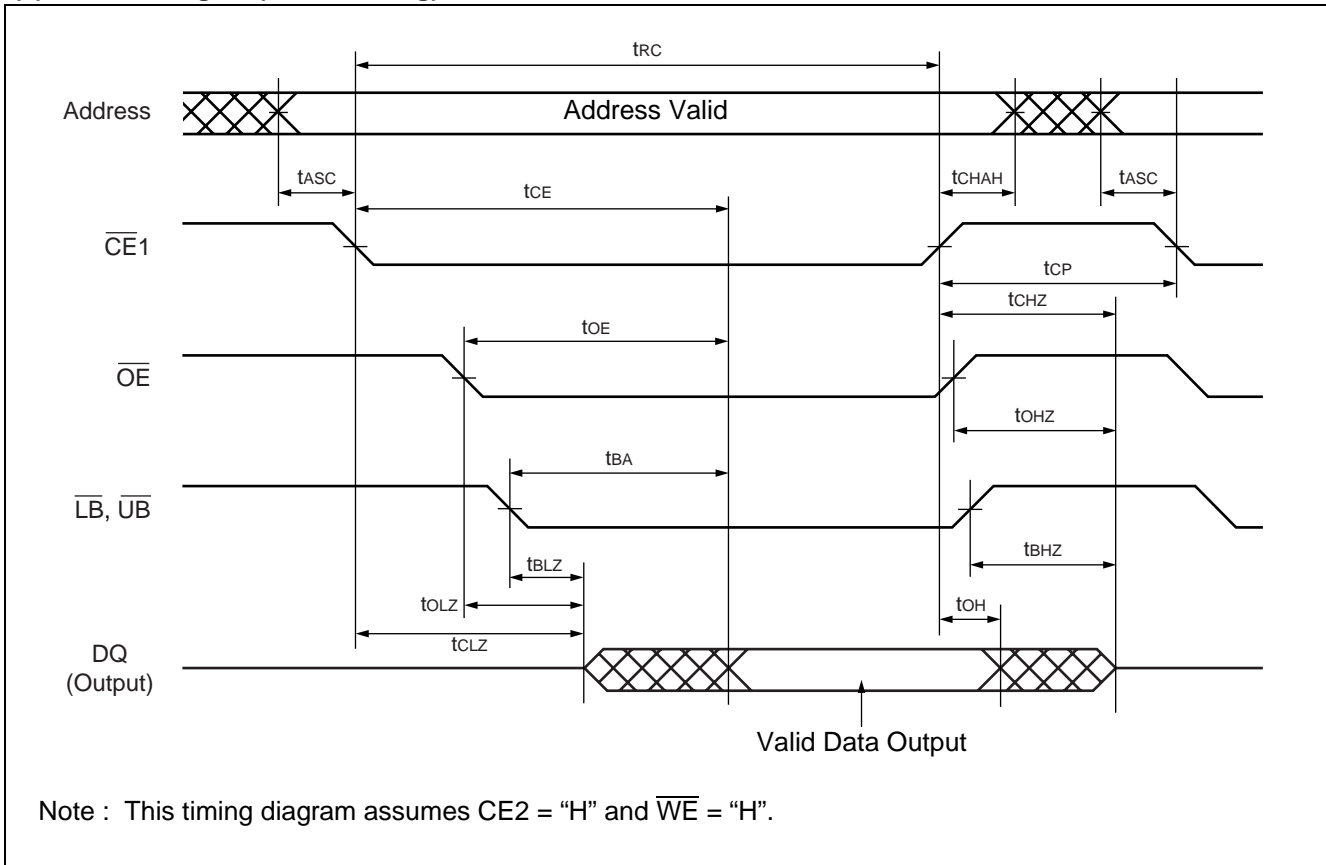
### (5) AC TEST CONDITIONS

Description	Symbol	Test Setup	Value	Unit	Note
Input High Level	V <sub>IH</sub>	—	V <sub>DD</sub> × 0.8	V	
Input Low Level	V <sub>IL</sub>	—	V <sub>DD</sub> × 0.2	V	
Input Timing Measurement Level	V <sub>REF</sub>	—	V <sub>DD</sub> × 0.5	V	
Input Transition Time	t <sub>T</sub>	Between V <sub>IL</sub> and V <sub>IH</sub>	5	ns	

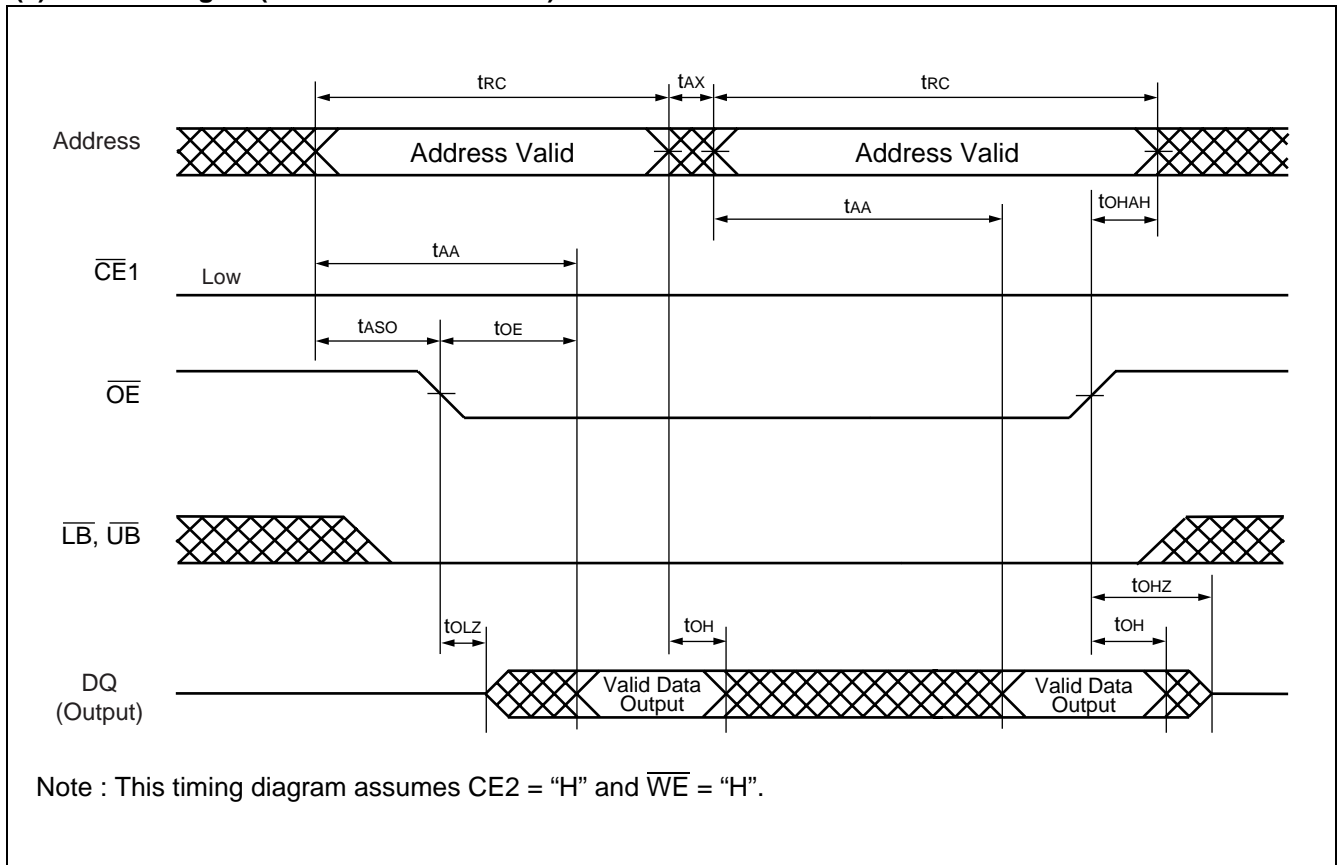


## ■ TIMING DIAGRAMS

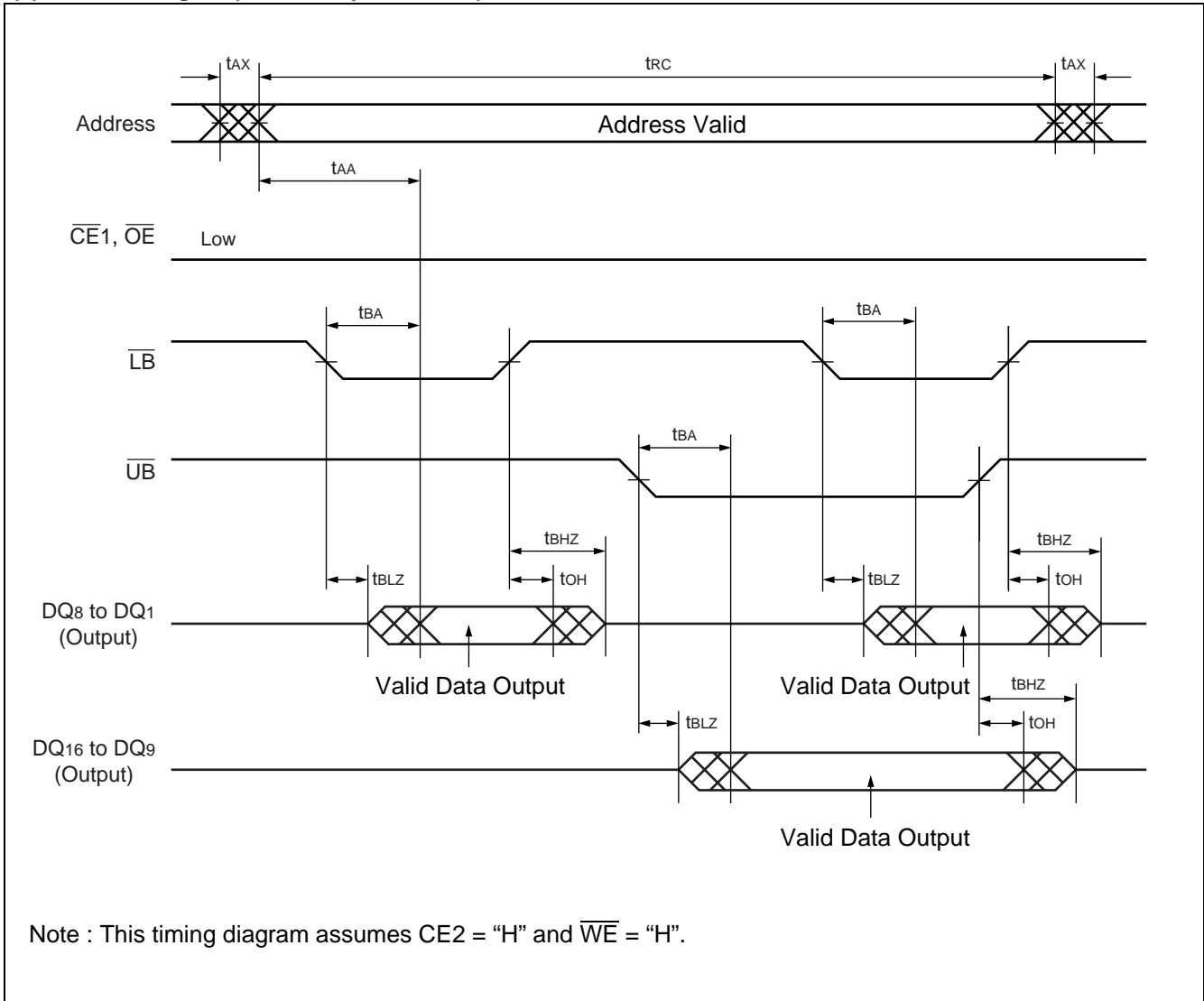
### (1) Read Timing #1 (Basic Timing)



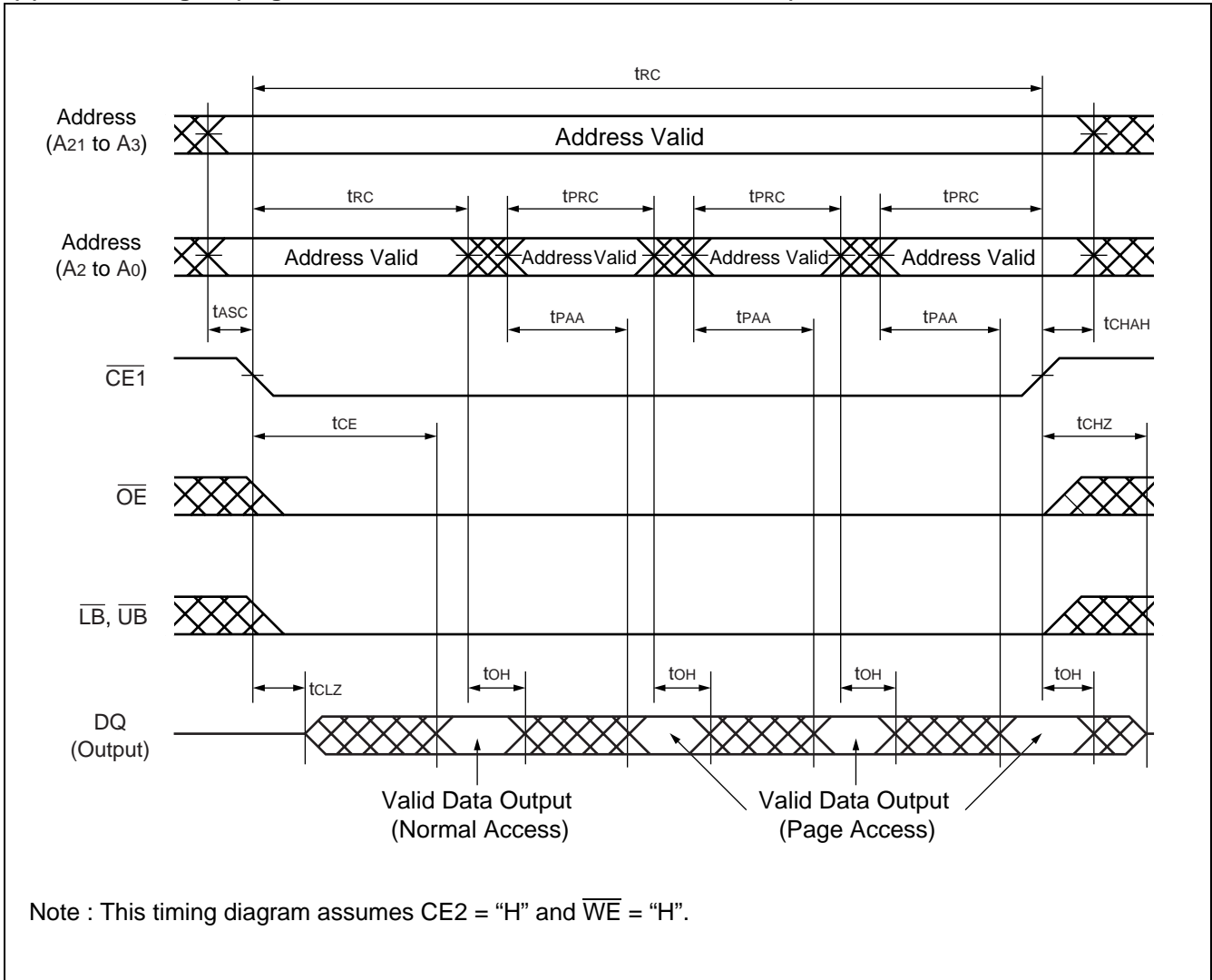
## (2) Read Timing #2 ( $\overline{\text{OE}}$ & Address Access)



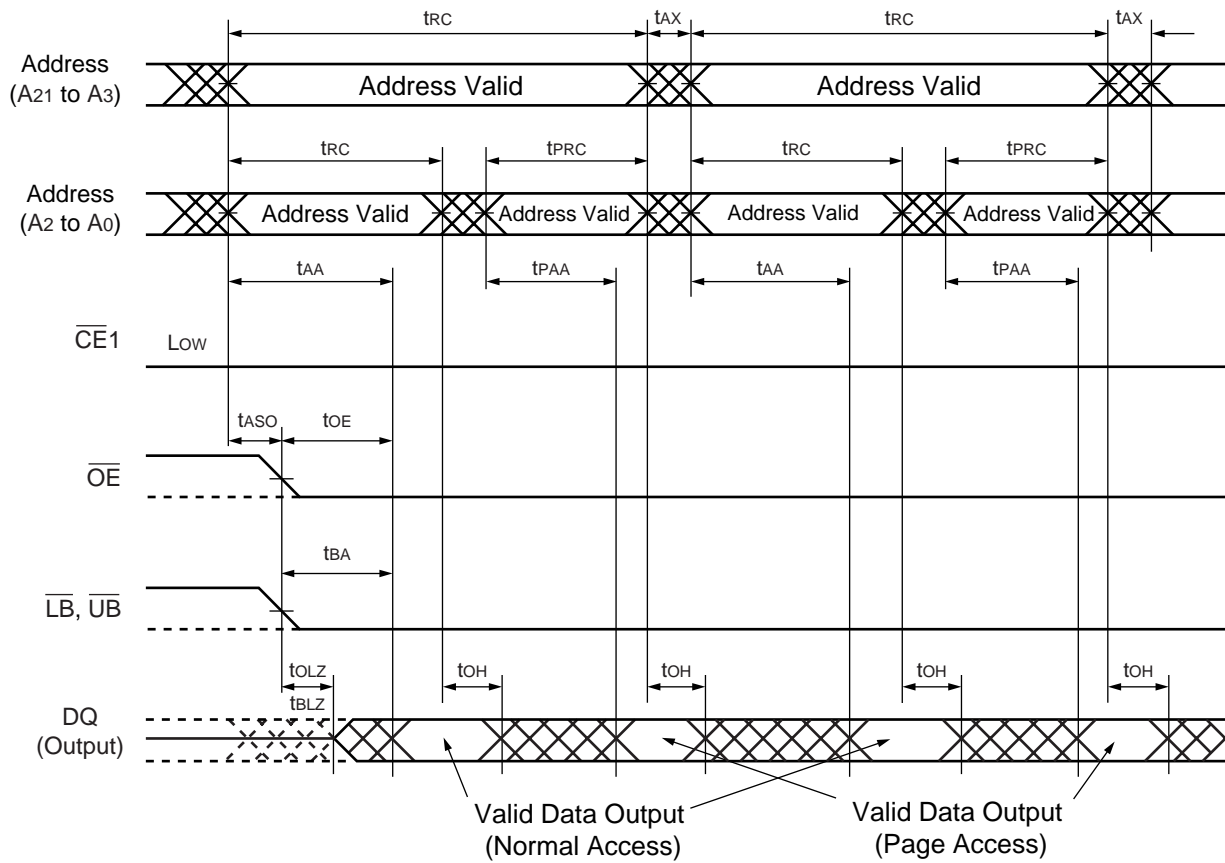
## (3) Read Timing #3 ( $\overline{\text{LB}}$ , $\overline{\text{UB}}$ Byte Access)



## (4) Read Timing #4 (Page Address Access after $\overline{CE1}$ Control Access)

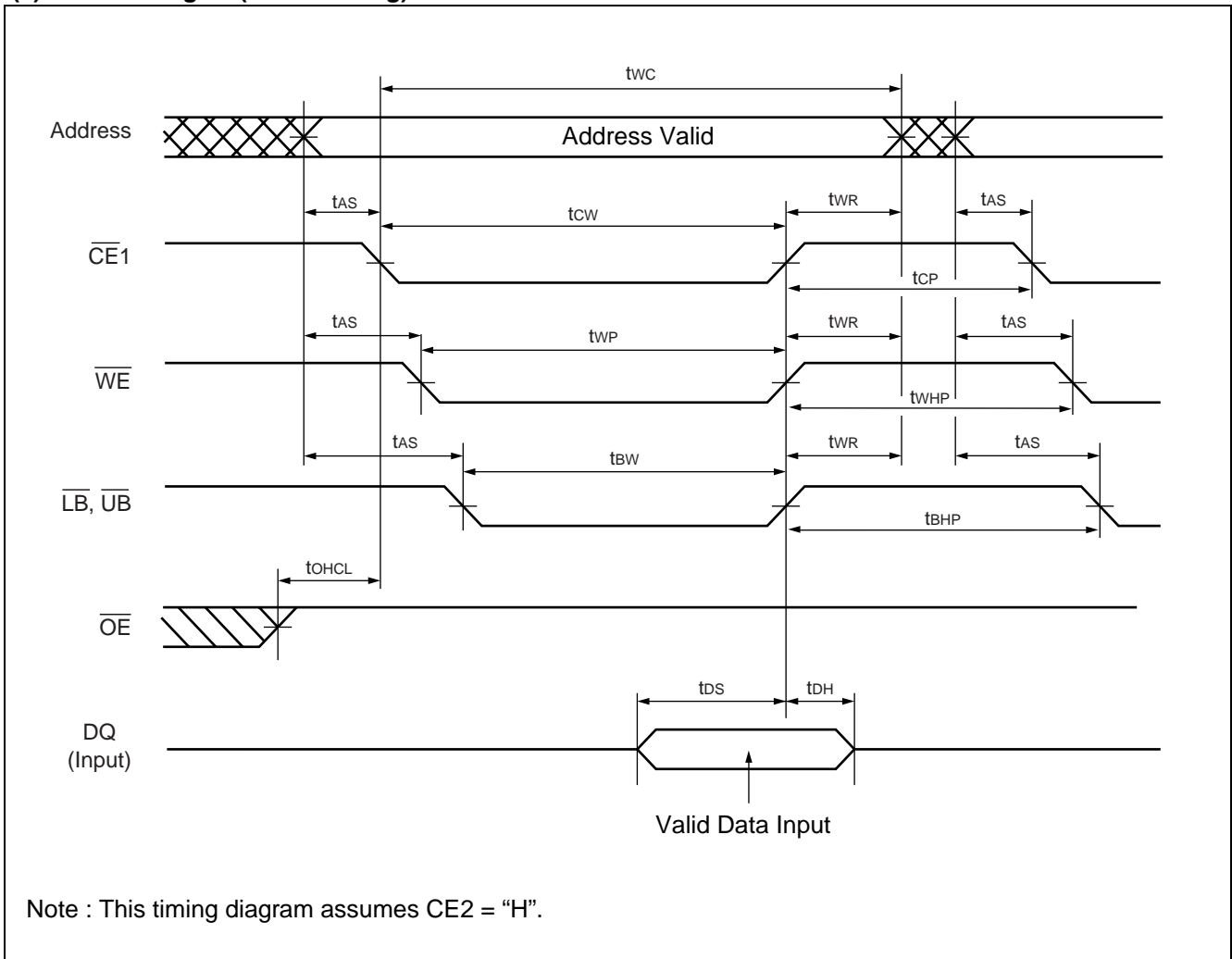


## (5) Read Timing #5 (Random and Page Address Access)



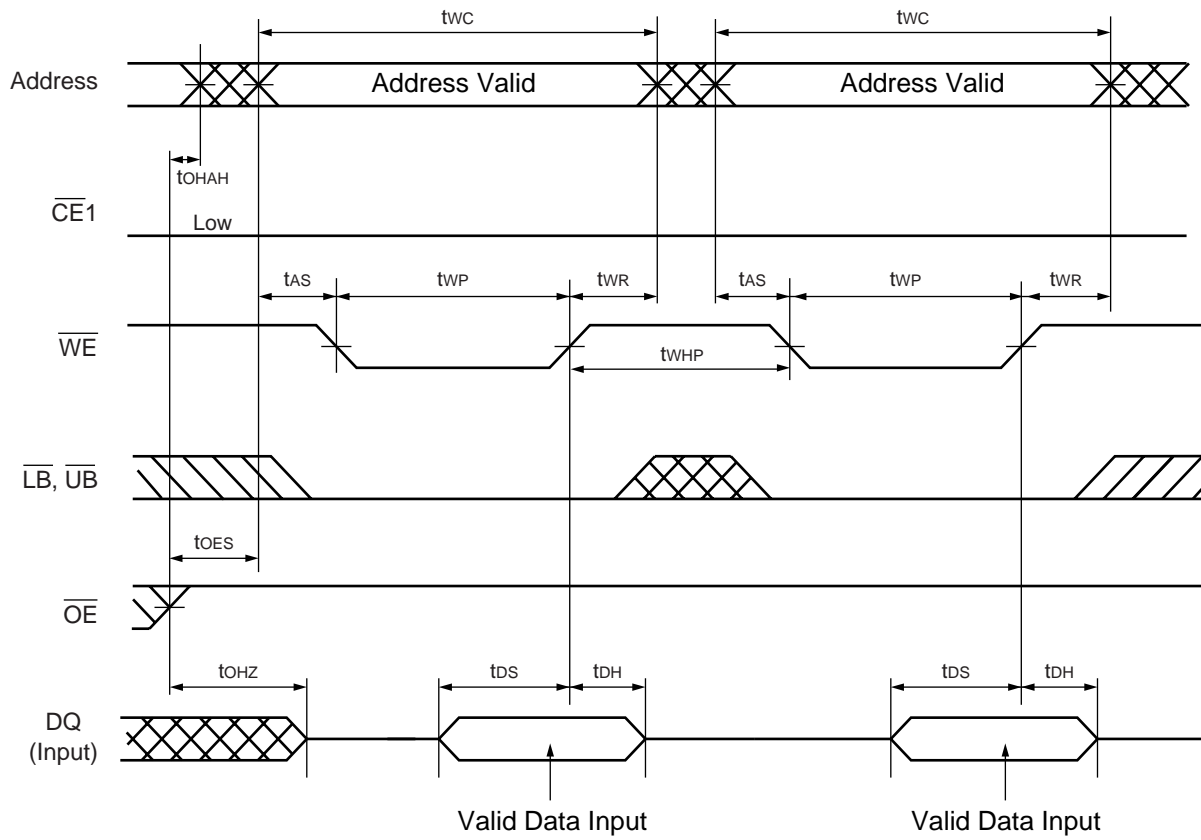
- Notes :
- This timing diagram assumes  $CE2 = "H"$  and  $\overline{WE} = "H"$ .
  - Either or both  $\overline{LB}$  and  $\overline{UB}$  must be Low when both  $\overline{CE1}$  and  $\overline{OE}$  are Low.

## (6) Write Timing #1 (Basic Timing)



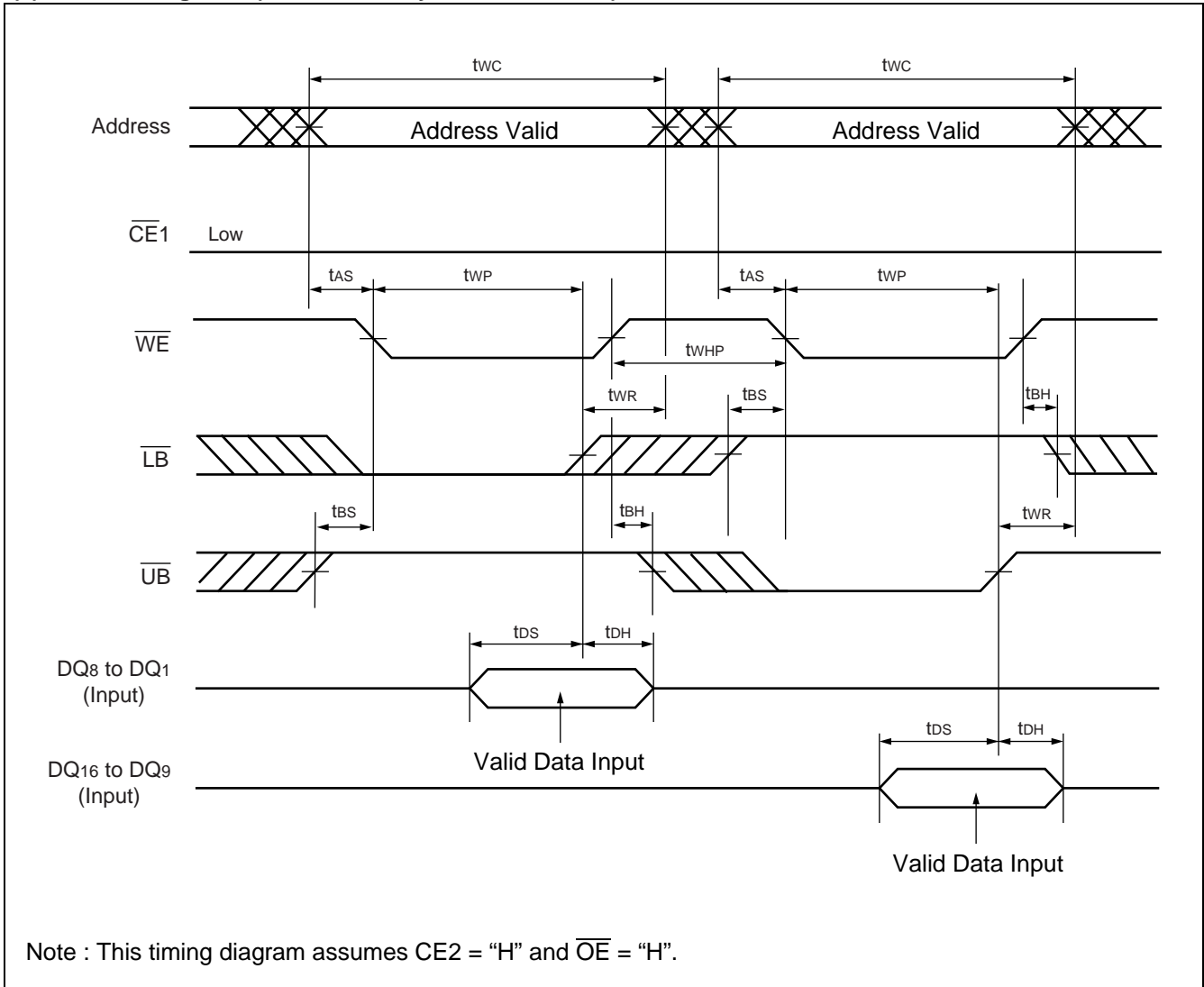


## (7) Write Timing #2 ( $\overline{WE}$ Control)

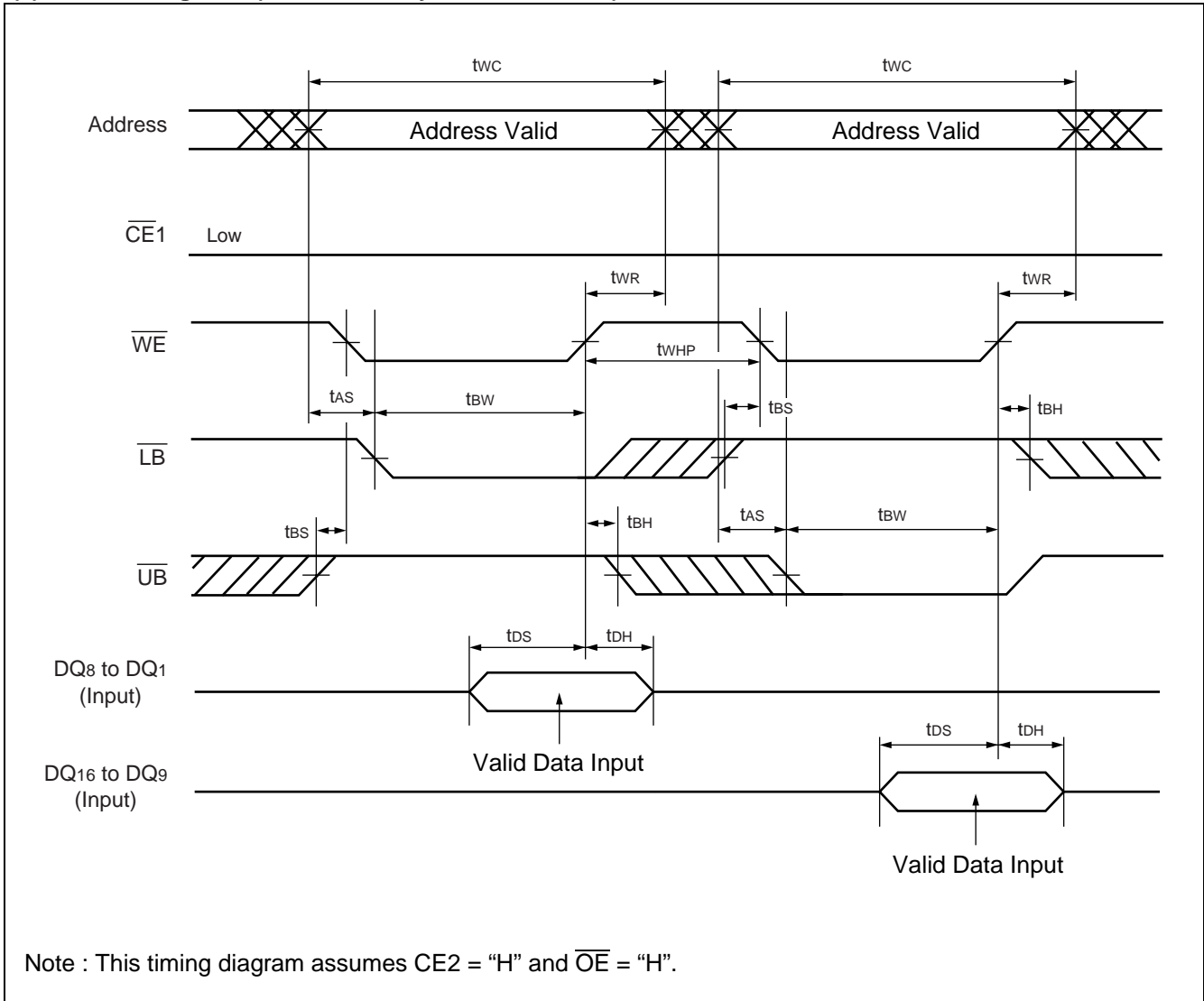


Note : This timing diagram assumes  $CE2 = "H"$ .

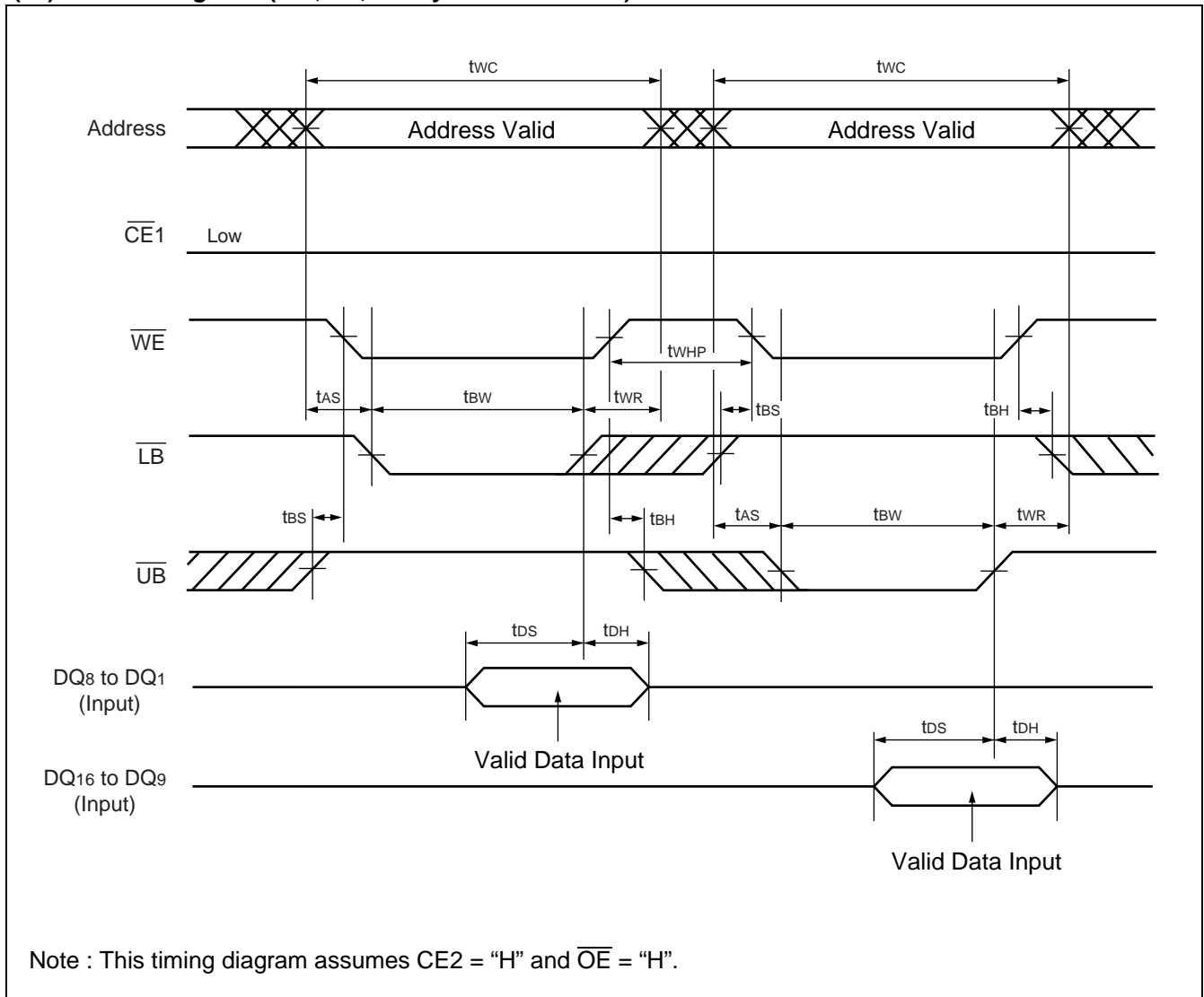
## (8) Write Timing #3-1 ( $\overline{WE}$ , $\overline{LB}$ , $\overline{UB}$ Byte Write Control)



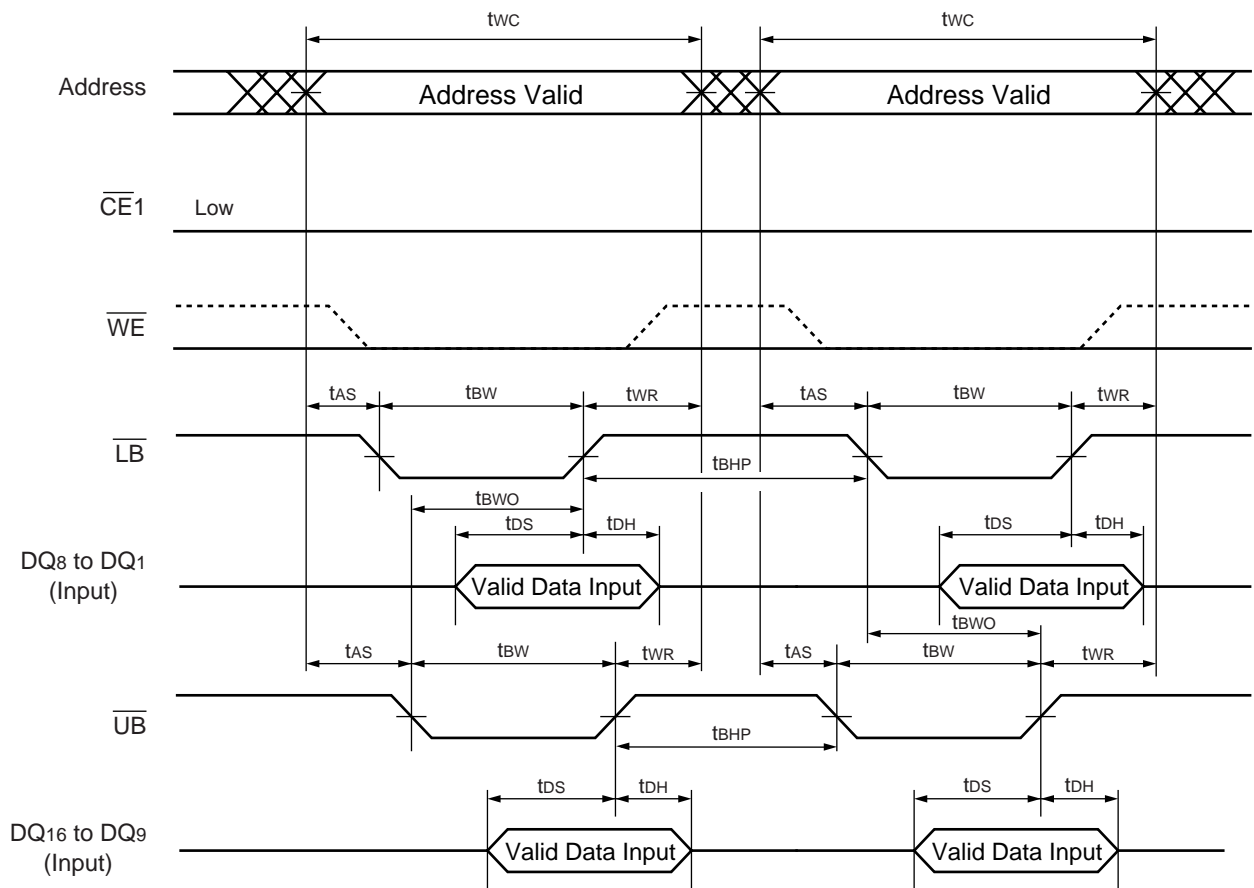
## (9) Write Timing #3-2 ( $\overline{WE}$ , $\overline{LB}$ , $\overline{UB}$ Byte Write Control)



## (10) Write Timing #3-3 ( $\overline{WE}$ , $\overline{LB}$ , $\overline{UB}$ Byte Write Control)

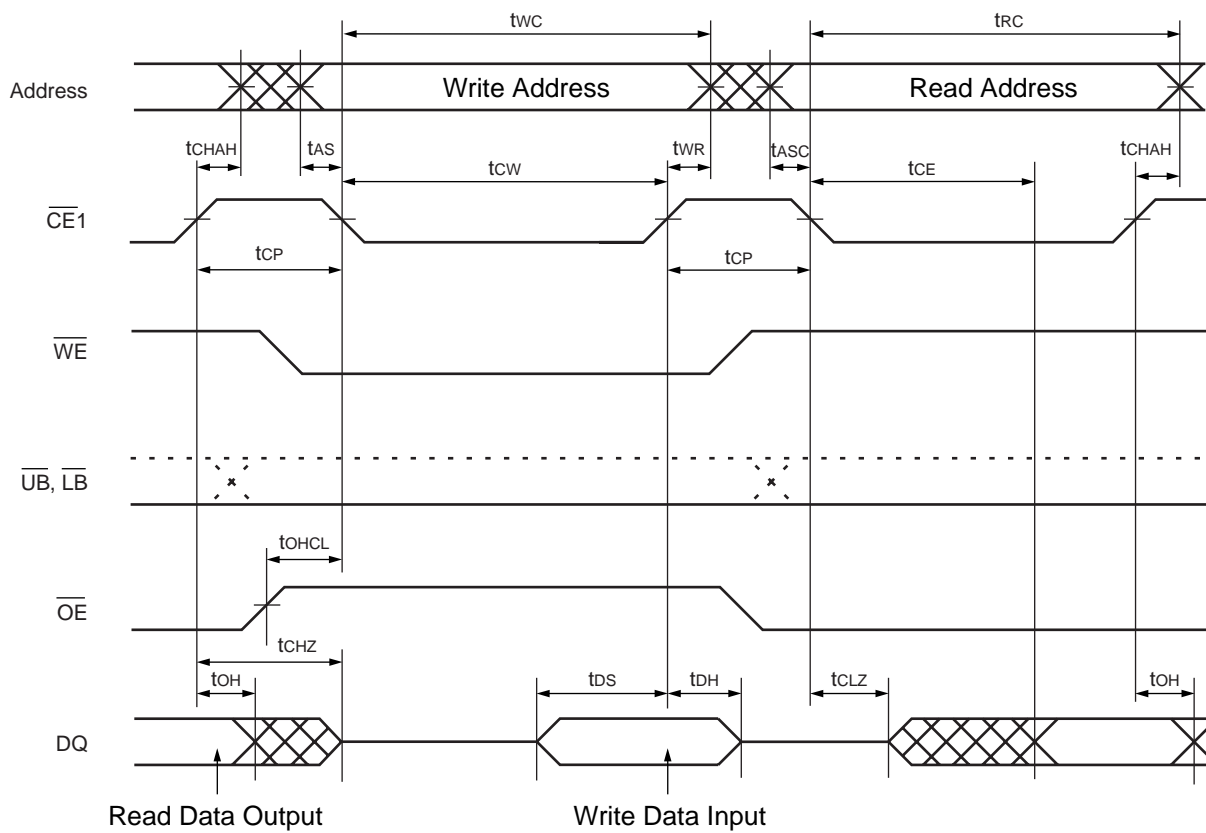


## (11) Write Timing #3-4 ( $\overline{WE}$ , $\overline{LB}$ , $\overline{UB}$ Byte Write Control)



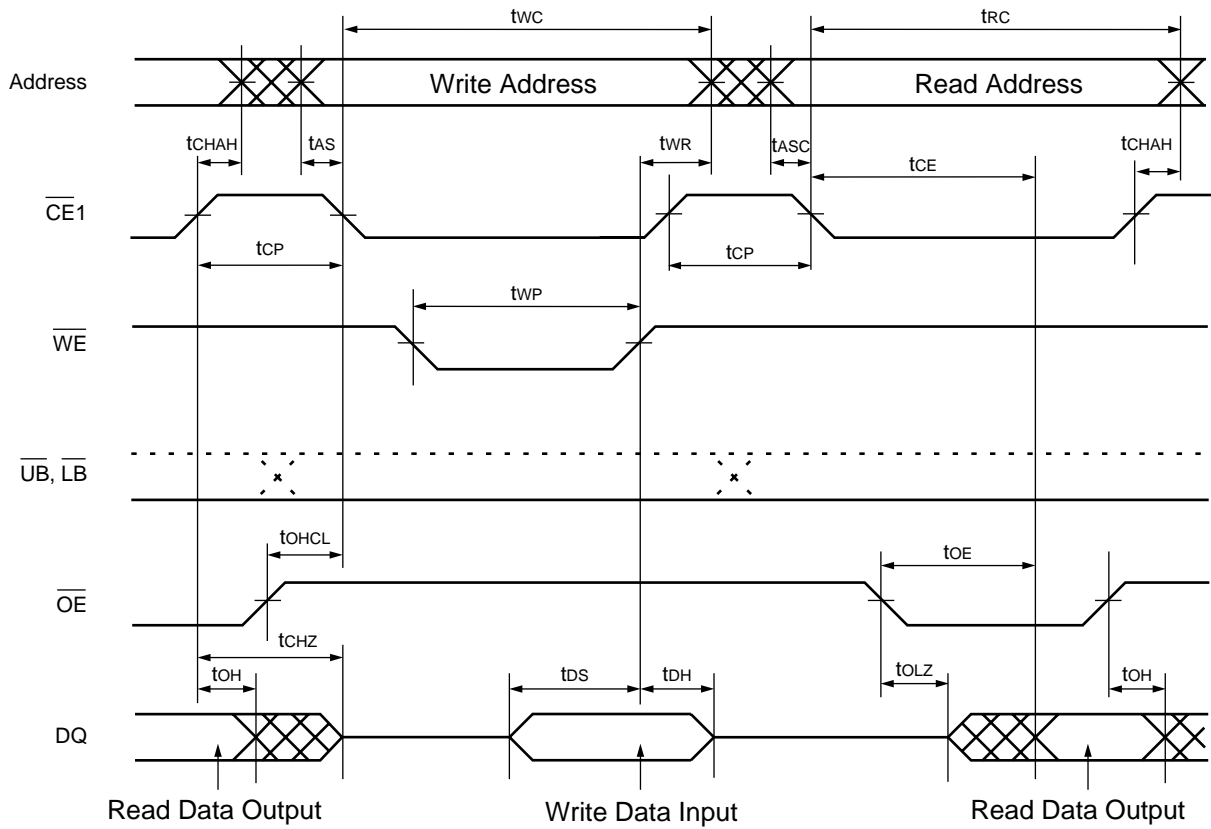
Note : This timing diagram assumes  $CE2 = "H"$  and  $\overline{OE} = "H"$ .

## (12) Read / Write Timing #1-1 ( $\overline{CE1}$ Control)



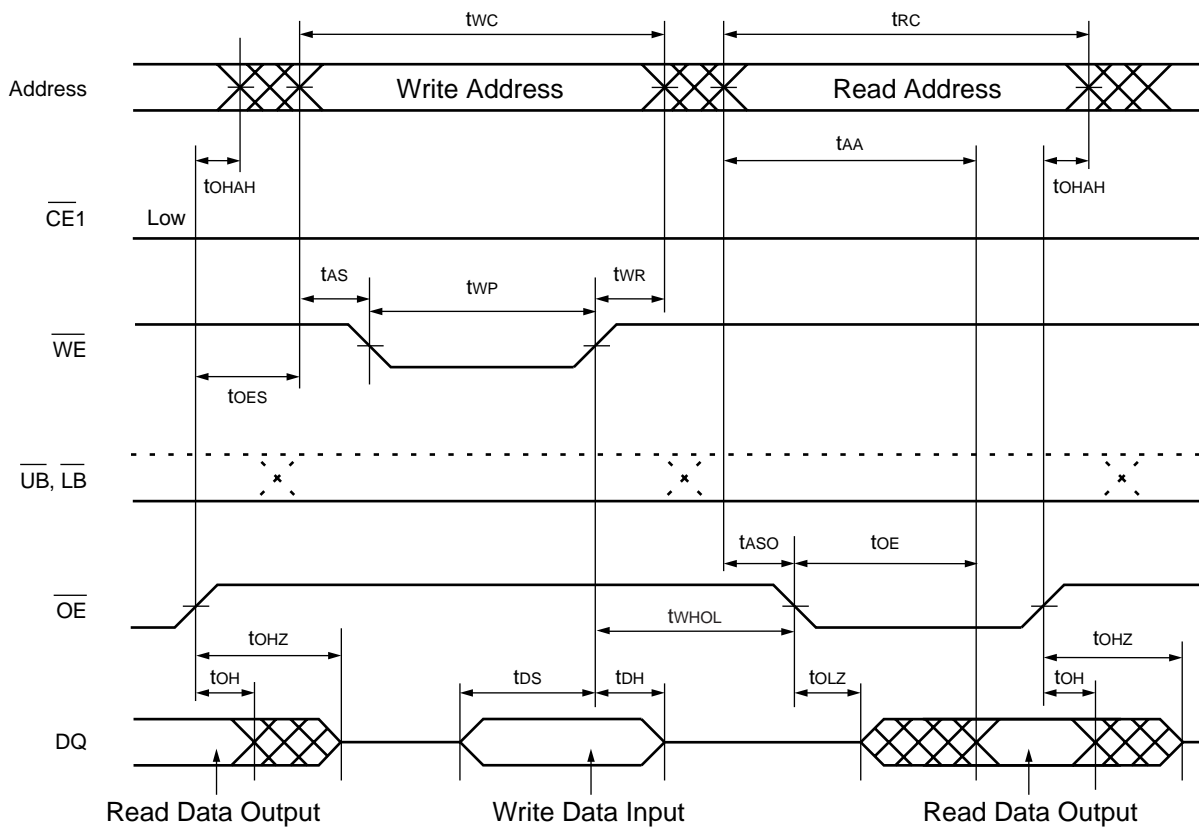
- Notes :
- This timing diagram assumes  $CE2 = "H"$ .
  - Write address is valid from either  $\overline{CE1}$  or  $\overline{WE}$  of last falling edge.

## (13) Read / Write Timing #1-2 ( $\overline{CE1}$ , $\overline{WE}$ , $\overline{OE}$ Control)



- Notes :
- This timing diagram assumes  $CE2 = "H"$ .
  - $\overline{OE}$  can be fixed Low during write operation if it is  $\overline{CE1}$  controlled write at Read-Write-Read sequence.

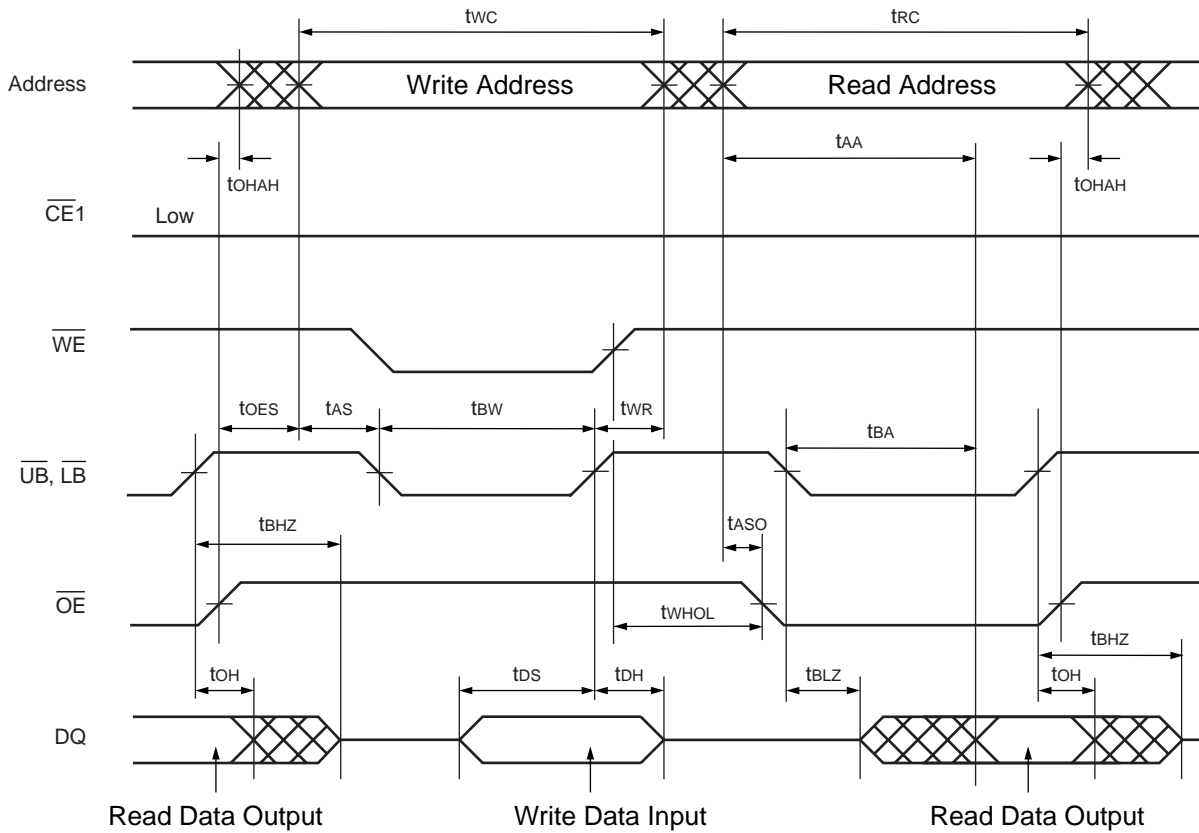
## (14) Read / Write Timing #2 ( $\overline{OE}$ , $\overline{WE}$ Control)



- Notes :
- This timing diagram assumes  $\overline{CE2} = "H"$ .
  - $\overline{CE1}$  can be tied to Low for  $\overline{WE}$  and  $\overline{OE}$  controlled operation.

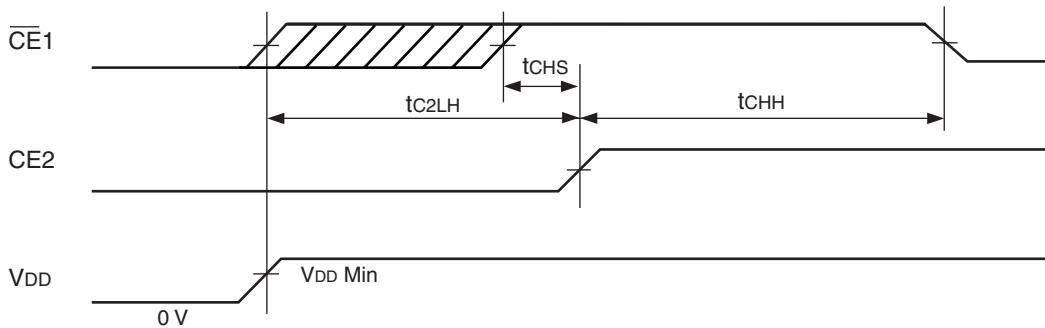


## (15) Read / Write Timing #3 ( $\overline{OE}$ , $\overline{WE}$ , $\overline{LB}$ , $\overline{UB}$ Control)



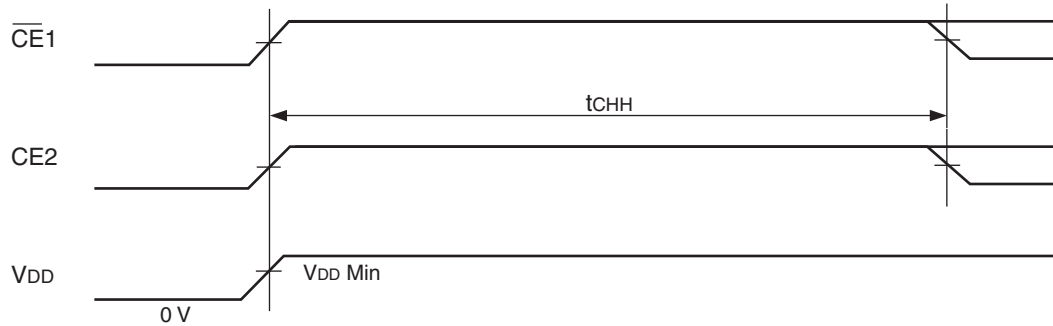
- Notes :
- This timing diagram assumes  $\overline{CE2} = "H"$ .
  - $\overline{CE1}$  can be tied to Low for  $\overline{WE}$  and  $\overline{OE}$  controlled operation.

## (16) Power-up Timing #1



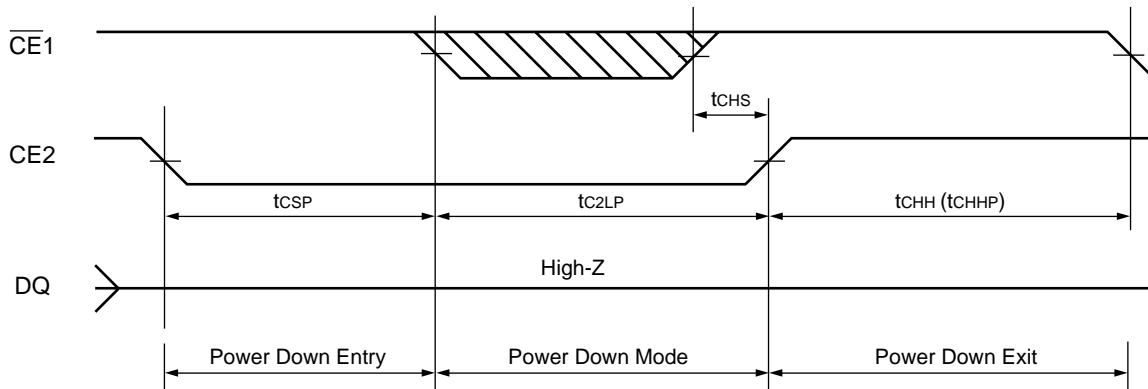
Note : The  $t_{C2LH}$  specifies after  $V_{DD}$  reaches specified minimum level.

## (17) Power-up Timing #2



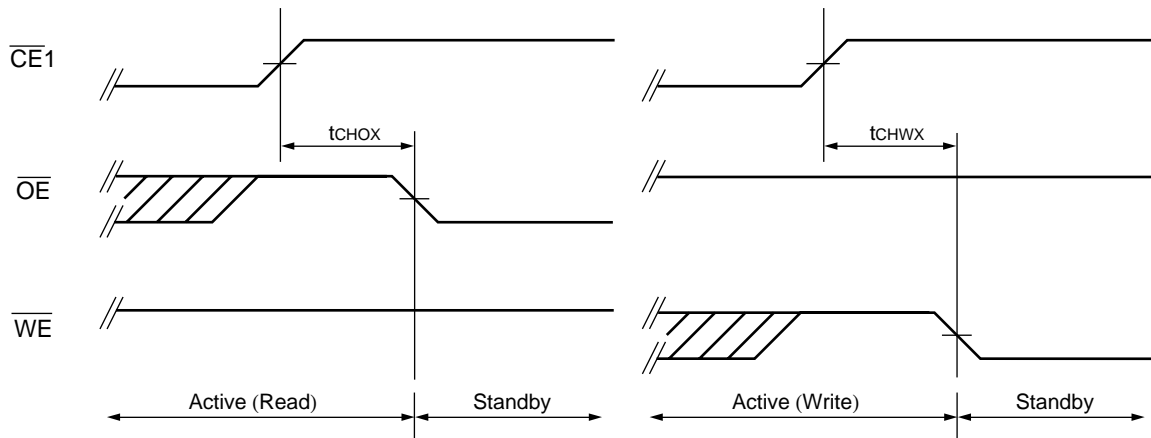
Note : The  $t_{CHH}$  specifies after  $V_{DD}$  reaches specified minimum level and applicable to both  $\overline{CE1}$  and CE2. If transition time of  $V_{DD}$  (from 0 V to  $V_{DD\ Min}$ ) is longer than 50 ms, Power-up Timing #1 must be applied.

## (18) Power Down Entry and Exit Timing



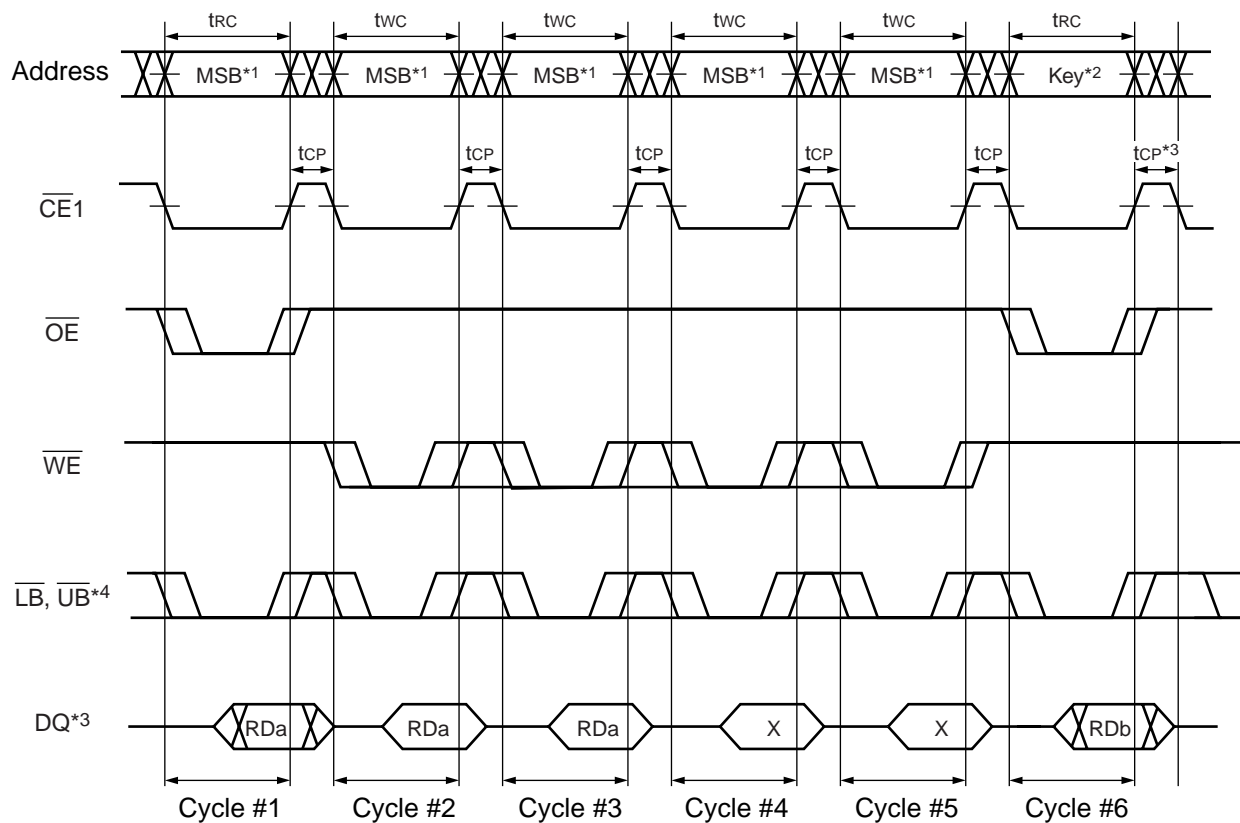
Note : This Power Down mode can be also used as a reset timing if "Power-up timing" above could not be satisfied and Power Down program was not performed prior to this reset.

## (19) Standby Entry Timing after Read or Write



Note : Both  $t_{CHOX}$  and  $t_{CHWX}$  define the earliest entry timing for Standby mode.

## (20) Power Down Program Timing



\*1 : The all address inputs must be High from Cycle #1 to #5.

\*2 : The address key must confirm the format specified in "■ POWER DOWN". If not, the operation and data are not guaranteed.

\*3 : After  $t_{CP}$  following Cycle #6, the Power Down Program is completed and returned to the normal operation.

\*4 : Byte read or write is available in addition to word read or write. At least one byte control signal ( $\overline{LB}$  or  $\overline{UB}$ ) needs to be Low.

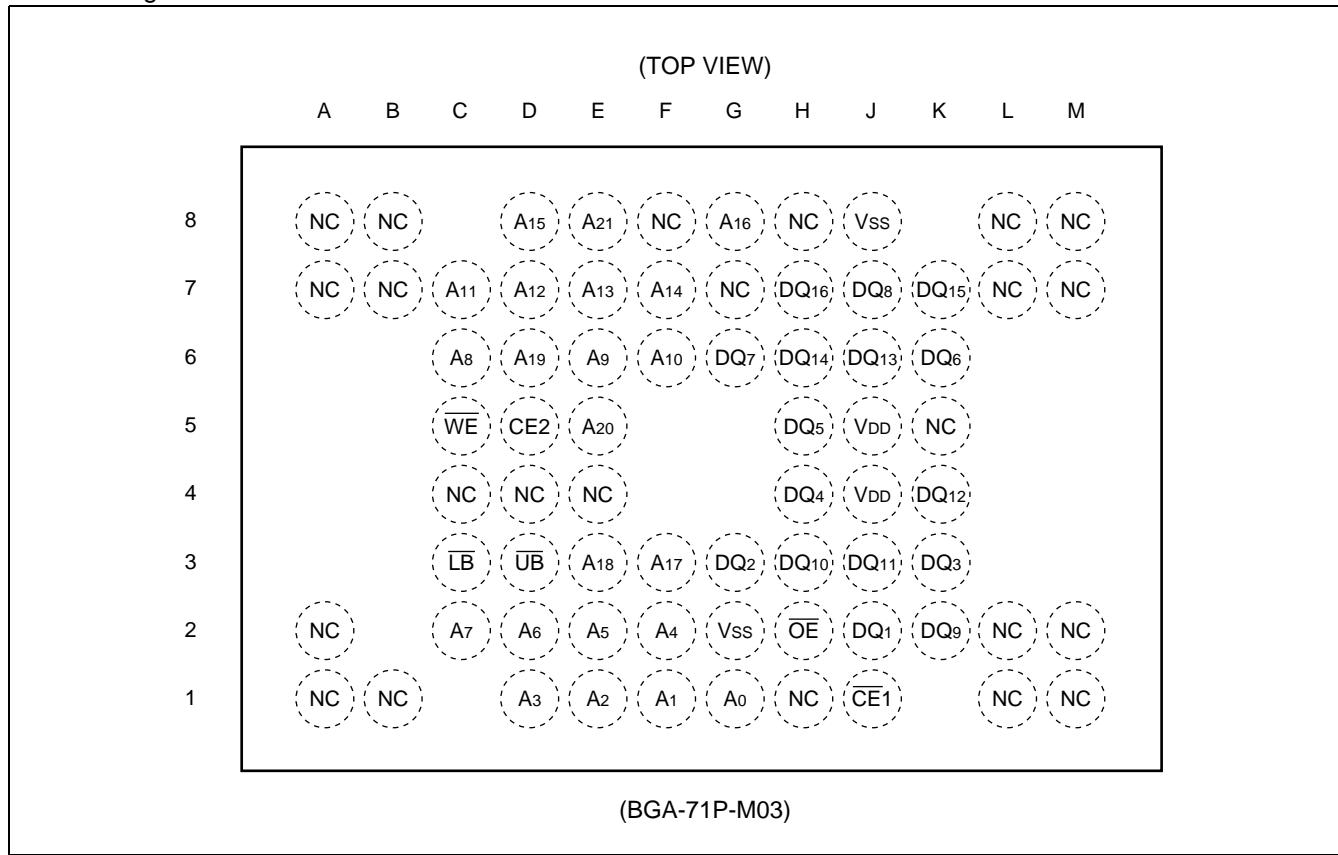
## ■ ORDERING INFORMATION

Part Number	Shipping Form	Remarks
MB82DP04183C-65LWFKT	Wafer	

# MB82DP04183C-65L

## PACKAGE FOR ENGINEERING SAMPLES

- Pin Assignment



- Pin Description

Pin Name	Description
A <sub>21</sub> to A <sub>0</sub>	Address Input
$\overline{CE}1$	Chip Enable 1 (Low Active)
CE2	Chip Enable 2 (High Active)
$\overline{WE}$	Write Enable (Low Active)
$\overline{OE}$	Output Enable (Low Active)
$\overline{LB}$	Lower Byte Control (Low Active)
$\overline{UB}$	Upper Byte Control (Low Active)
DQ <sub>8</sub> to DQ <sub>1</sub>	Lower Byte Data Input/Output
DQ <sub>16</sub> to DQ <sub>9</sub>	Upper Byte Data Input/Output
V <sub>DD</sub>	Power Supply Voltage
V <sub>SS</sub>	Ground
NC	No connection

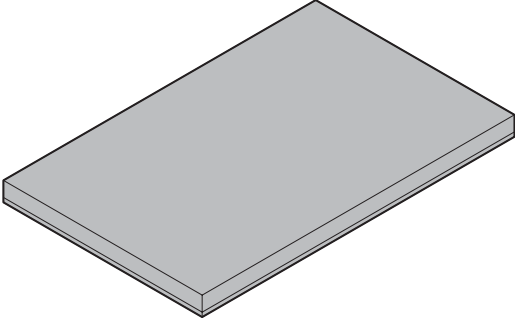
• Package Capacitance

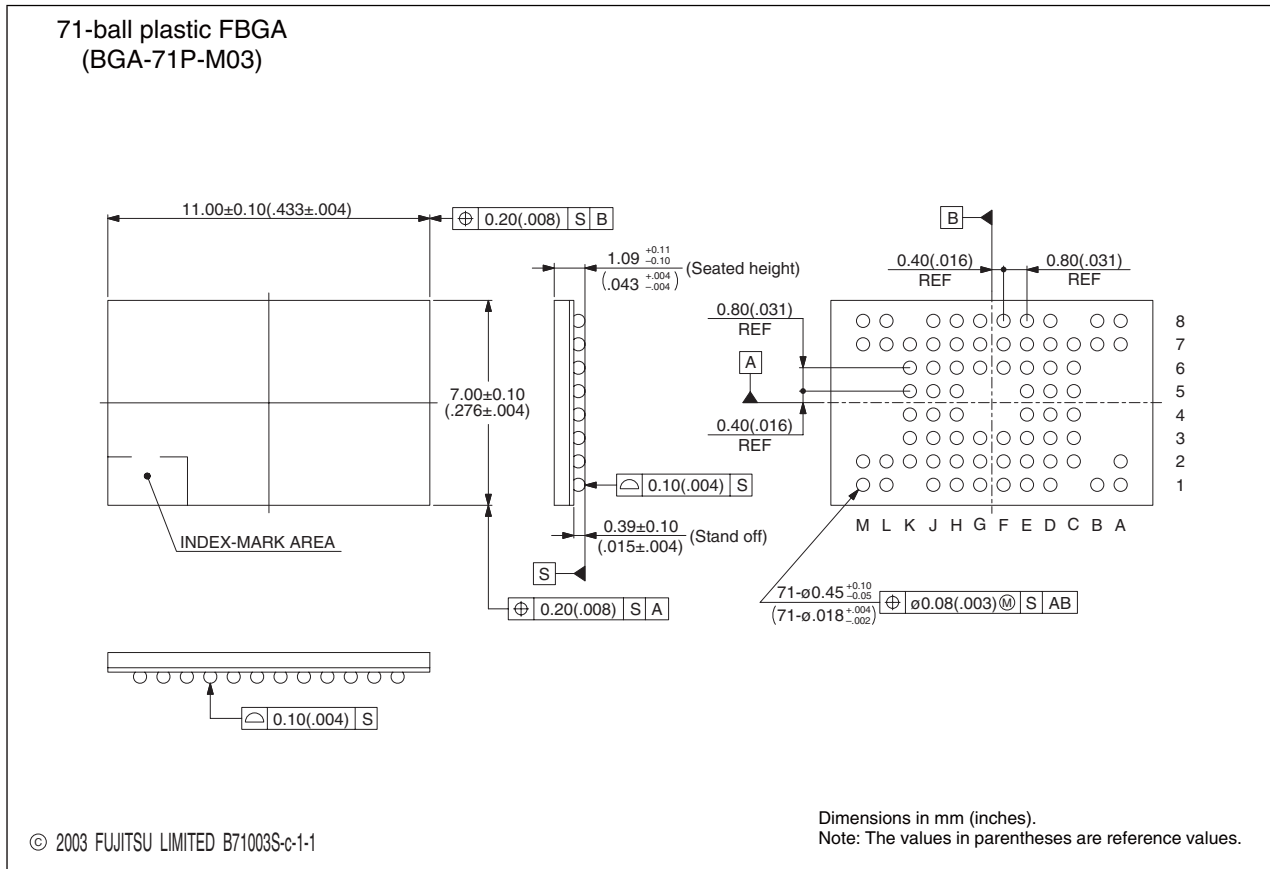
(f = 1 MHz, T<sub>A</sub> = +25 °C)

Parameter	Symbol	Test conditions	Value			Unit
			Min	Typ	Max	
Address Input Capacitance	C <sub>IN1</sub>	V <sub>IN</sub> = 0 V	—	—	5	pF
Control Input Capacitance	C <sub>IN2</sub>	V <sub>IN</sub> = 0 V	—	—	5	pF
Data Input/Output Capacitance	C <sub>I/O</sub>	V <sub>IO</sub> = 0 V	—	—	8	pF

# MB82DP04183C-65L

• Package Dimension

<p>71-ball plastic FBGA</p>  <p>(BGA-71P-M03)</p>	Ball pitch	0.80 mm
	Package width × package length	7.00 × 11.00 mm
	Lead shape	Soldering ball
	Sealing method	Plastic mold
	Ball size	∅0.45 mm
	Mounting height	1.20 mm Max.
	Weight	0.14 g





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