

CL-PS6700

Preliminary Product Bulletin

FEATURES

- Direct interface to CL-PS7111 low-power microcontroller
 - Custom multiplexed address/data bus for low pin count
 - Supports 13 and 18 MHz operating frequencies
- Fully compatible with PCMCIA Rel. 2.01 specification
- One or two CL-PS6700s per system
- Low-power states
 - Operating (25 mW, typical)
 - Idle
 - Standby (virtually zero power drain)
- Support for PC Card hot insertion and removal
- Read and write buffers
- Support for 3.3- and 5-V PC Cards
- Endian conversion
- Supports the following PC Cards:
 - Memory-only card; flash, EPROM, or SRAM
 - I/O card; modem and communications
 - Cards configured as both I/O and memory
 - DMA-capable cards (through software emulation)
- 100-pin VQFP package

Low-Power PC Card Controller for the CL-PS7111

OVERVIEW

The CL-PS6700 connects directly to a PCMCIA Rel. 2.01 socket and has a custom interface to the CL-PS7111 microcontroller. The CL-PS7111 can support up to two CL-PS6700 devices, which allows up to two PC Card sockets per system. Addresses and data are passed to the CL-PS6700 through 16 bits of the 32-bit Data bus (D[15:0]).

The PC Card socket is effectively isolated by the CL-PS6700. Except for power and ground pins, the pins on the socket only contact to the rest of the system through the CL-PS6700.

CL-PS7111-to-CL-PS6700 Interface

The PC Card interface requires a 26-bit address bus and a 16-bit data bus. The interface between the CL-PS6700 and CL-PS7111 consists of a 16-bit bus that carries the address and data information, and several control signals. This bus defines a two-clock address phase during which the 26-bit PC Card address and 6 control bits are transferred, and a one- or two-clock data phase during which 1 or 4 bytes of

(cont.)



CL-PS7111-to-CL-PS6700 Interface



OVERVIEW (cont.)

data are transferred. The data phase for reads can be deferred (for example, for a DMA access to the frame buffer of the CL-PS7111).

If a write transfer is indicated, write data appears in the third clock phase. If a word write is indicated, write data also appears in the fourth clock phase. For read transfers, the CL-PS6700 drives the bus with read data during the first one or two clocks of the data phase. This interface bus is also shared by other memory devices and up to one additional CL-PS6700 device.

The CL-PS7111 accesses the CL-PS6700 as a memorymapped peripheral on the 16-bit memory bus. A Chip Enable signal (NCS4) from the CL-PS7111 selects one CL-PS6700 device for access to a particular PC Card socket. Another Chip Enable signal (NCS5) connects a second PC Card socket.

The CL-PS6700 implements the low-level interface to the PC Card socket and provides voltage translation for mixedvoltage systems. The CL-PS6700 also provides the data buffer and interrupt controls for the PC Card. Transfers between the two devices can be either 1 or 4 bytes.

The CL-PS6700 can be programmed to assemble/disassemble CL-PS7111 transfers to the width of the PC Card. The CL-PS6700 has read and write buffers that allow posting of both reads and writes. The read queue is single entry; the write FIFO can queue up to four CL-PS7110 transactions (up to 16 bytes).

Hot Insertion Support

The CL-PS6700 PC Card controller allows PC Cards to be inserted or removed while system power is on. The CL-PS7111 controller typically applies power to a PC Card socket after it has detected a properly inserted card. The device removes the power before the card is removed (that is, when the CPU detects that the card lock is deasserted). Since each card is isolated from the system by the associated CL-PS6700, insertion and removal of cards do not cause interference on the system buses.

Card Configuration and Access

After power-on or reset, a PC Card defaults to a memoryonly card. The CL-PS7111 then reads the CIS of the card to determine the card type, access time, and so on, and configures the CL-PS6700 to access the card.

Each PC Card's V_{CC} and V_{PP} pins are individually controlled by its associated CL-PS6700. The CL-PS7111 controls the power to a card by writing to the CL-PS6700 registers. The CL-PS6700 ensures that its signals to the sockets are in the proper state before applying or removing power.

The CL-PS6700 device is available in a 100-pin VQFP package. The device can be used with both operating frequencies of the CL-PS7111 (13 and 18 MHz at 2.7 and 3.3 V).

Cirrus Logic Direct Sales Offices

Houston, TX

Andover, MA

Duluth. GA

Raleigh, NC

TEL: 713/257-2525

FAX: 713/257-2555

TEL: 508/474-9300

FAX: 508/474-9149

TEL: 770/935-6110

FAX: 770/935-6112

TEL: 919/859-5210

FAX: 919/859-5334

TEL · 407/241-2364

FAX: 407/241-7990

International

TEL: 33/1-48-12-2812 FAX: 33/1-48-12-2810

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Domestic

Fremont TEL: 510/623-8300 FAX: 510/252-6020

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TEL: 714/453-5961 FAX: 714/453-5962

Westlake Village TEL: 805/371-5860

FAX: 805/371-5861

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FAX: 82/2-565-8565

TEL: 65/743-4111 FAX: 65/742-4111

TAIWAN Taipei TEL: 886/2-718-4533 FAX: 886/2-718-4526

UNITED KINGDOM London, England

TEL: 44/1727-872424 FAX: 44/1727-875919

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Cirrus Logic Inc. 3100 West Warren Ave., Fremont, CA 94538 *TEL:* 510/623-8300 *FAX:* 510/252-6020 *Publications Order Information:* 800/359-6414 (USA) or 510/249-4200 *World Wide Web:* http://www.cirrus.com

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