## DESCRIPTION

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01 Hz to 300 kHz. It can accommodate analog signals between 2 mV and 3V, and can interface with conventional DTL, TTL and ECL logic families. The circuit consists of a basic PLL for tracking an input signal frequency within the passband, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set carrier frequency, bandwidth, and output delay.



## FEATURES

- Wide Frequency Range (0.01 Hz to 300 kHz)
- Wide Supply Voltage Range (4.5V to 20V)
- DTL/TTL/ECL Logic Compatibility
- FSK Demodulation with Carrier-Detection
- Wide Dynamic Range (2 mV to 3V rms)
- Adjustable Tracking Range (±1% to ±80%)
- Excellent Temperature Stability (20 ppm/°C, typical)

## APPLICATIONS

- FSK Demodulation
- Data Synchronization
- Tone Decoding
- FM Detection
- Carrier Detection
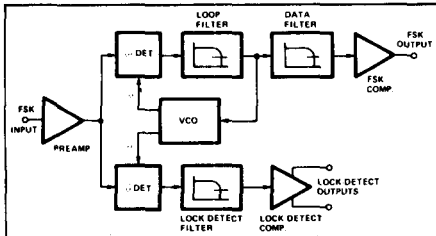
## SCHEMATIC DIAGRAM
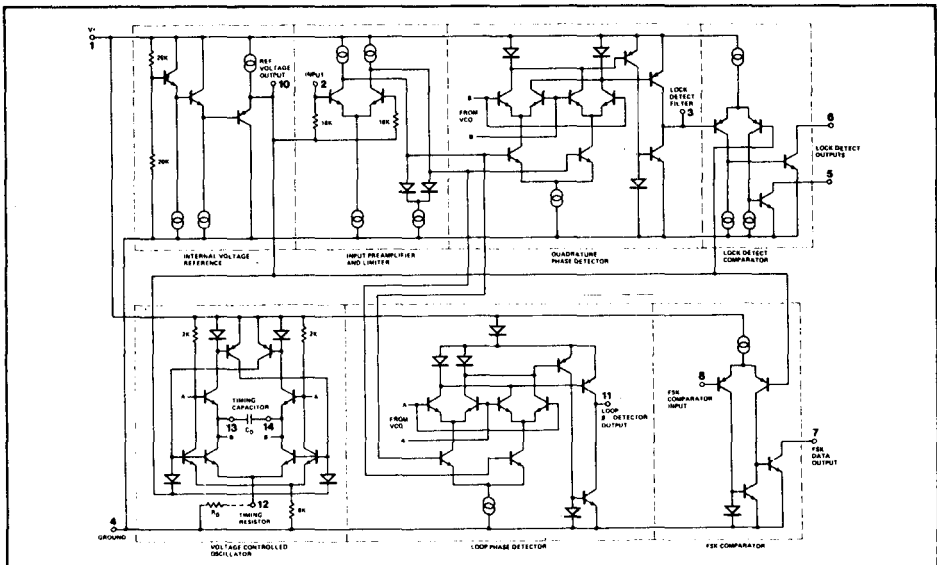
## ABSOLUTE MAXIMUM RATINGS

Power Supply . . . . . . . . . . . . . 20V

Input Signal Level . . . . . . . . . . . 3V rms

Power Dissipation
Ceramic Package . . . . . . . . . 750 mW
    Derate above $T_A$ = +25°C . . . . . . . 6 mW/°C

Plastic Package . . . . . . . . . 625 mW
    Derate above $T_A$ = +25°C . . . . . . . 5 mW/°C

## ELECTRICAL CHARACTERISTICS

**Test Conditions (see Figure 2):**
$V^+$ = +12V, $T_A$ = +25°C, $R_0$ = 30 KΩ. $C_0$ = 0.033 $\mu$F.

## CONNECTION INFORMATION
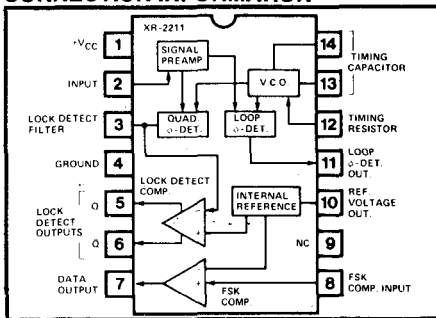


| PARAMETER | CONDITIONS | XR-2211/2211M | | | XR-2211C | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| **GENERAL** | | | | | | | | |
| Supply Voltage | | 4.5 | | 20 | 4.5 | | 20 | V |
| Supply Current | $R_0 \geq$ 10 KΩ See Fig. 4. | | 4 | 7 | | 5 | 9 | mA |
| **OSCILLATOR** | | | | | | | | |
| Frequency Accuracy | Deviation from $f_0 = 1/R_0C_0$ | | ±1 | ±3 | | ±1 | | % |
| Frequency Stability | $R_1 = \infty$ | | | | | | | |
|   Temperature Coefficient | See Fig. 8. | | ±20 | ±50 | | ±20 | | ppm/°C |
|   Power Supply Rejection | $V^+$ = 12 ±1V. See Fig. 7. | | 0.05 | 0.5 | | 0.05 | | %/V |
| | $V^+$ = 5 ±0.5V. See Fig. 7. | | 0.2 | | | 0.2 | | %/V |
| Upper Frequency Limit | $R_0$ = 8.2 KΩ, $C_0$ = 400 pF | 100 | 300 | | | 300 | | kHz |
| Lowest Practical Operating Frequency | $R_0$ = 2 MΩ, $C_0$ = 50 $\mu$F | | | 0.01 | | 0.01 | | Hz |
| Timing Resistor, $R_0$ | See Fig. 5 | | | | | | | |
|   Operating Range | | 5 | | 2000 | 5 | | 2000 | KΩ |
|   Recommended Range | See Fig. 7 and 8. | 15 | | 100 | 15 | | 100 | KΩ |
| **LOOP PHASE DETECTOR** | | | | | | | | |
| Peak Output Current | Measured at pin 11. | ±150 | ±200 | ±300 | ±100 | ±200 | ±300 | $\mu$A |
| Output Offset Current | | | ±1 | | | ±2 | | $\mu$A |
| Output Impedance | | | 1 | | | 1 | | MΩ |
| Maximum Swing | Referenced to pin 10. | ±4 | ±5 | | ±4 | ±5 | | V |
| **QUADRATURE PHASE DETECTOR** | | | | | | | | |
| Peak Output Current | Measured at pin 3. | 100 | 150 | | | 150 | | $\mu$ |
| Output Impedance | | | 1 | | | 1 | | MΩ |
| Maximum Swing | | | 11 | | | 11 | | Vpp |
| **INPUT PREAMP** | | | | | | | | |
| Input Impedance | Measured at pin 2. | | 20 | | | 20 | | KΩ |
| Input Signal Voltage Required to Cause Limiting | | | 2 | 10 | | 2 | | mV rms |
| **VOLTAGE COMPARATOR** | | | | | | | | |
| Input Impedance | Measured at pins 3 and 8. | | 2 | | | 2 | | MΩ |
| Input Bias Current | | | 100 | | | 100 | | nA |
| Voltage Gain | $R_L$ = 5.1 KΩ | 55 | 70 | | 55 | 70 | | dB |
| Output Voltage Low | $I_C$ = 3 mA | | 300 | | | 300 | | mV |
| Output Leakage Current | $V_0$ = 12V | | .01 | | | .01 | | $\mu$A |
| **INTERNAL REFERENCE** | | | | | | | | |
| Voltage Level | Measured at pin 10. | 4.9 | 5.3 | 5.7 | 4.75 | 5.3 | 5.85 | V |
| Output Impedance | | | 100 | | | 100 | | Ω |

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## TYPICAL PERFORMANCE DATA



*Typical Supply Current vs V⁺ (Logic Outputs Open Circuited)*

*VCO Frequency vs Timing Resistor*

*VCO Frequency vs Timing Capacitor*

*Typical f₀ vs Power Supply Characteristics*

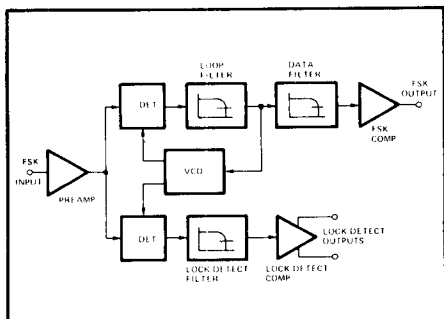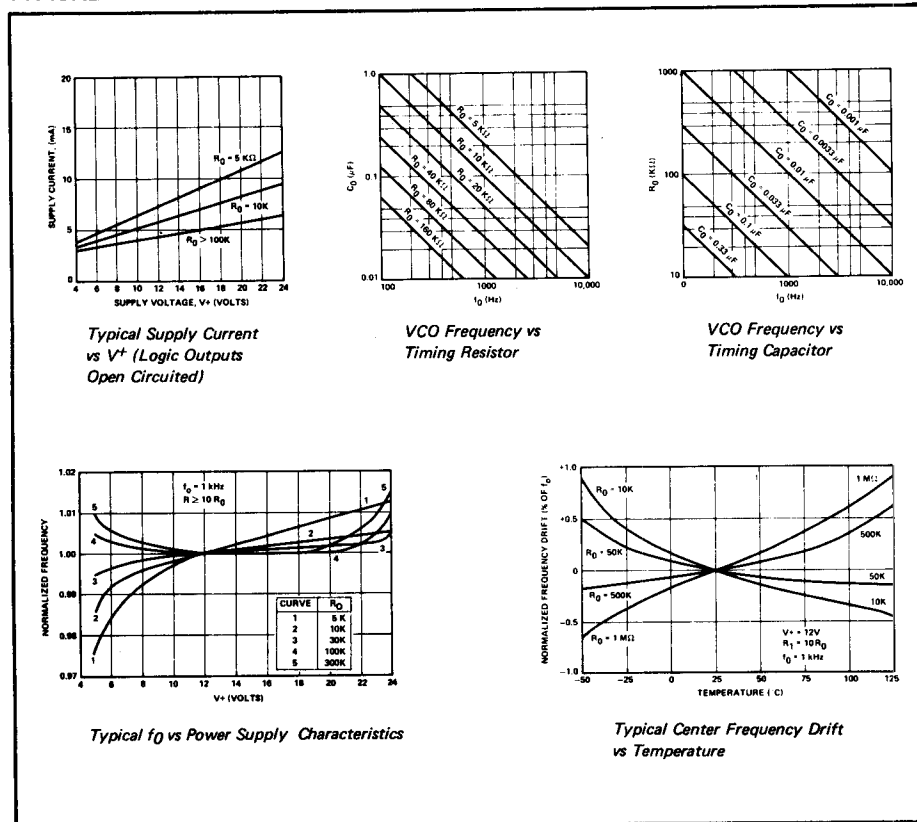*Typical Center Frequency Drift vs Temperature*



Figure 1. *Functional Block Diagram of a Tone and FSK Decoding System Using XR-2211.*

## DESCRIPTION OF CIRCUIT CONTROLS

### SIGNAL INPUT (PIN 2)

Signal is ac coupled to this terminal. The internal impedance at pin 2 is 20 K$\Omega$. Recommended input signal level is in the range of 10 mV rms to 3V rms.

### QUADRATURE PHASE DETECTOR OUTPUT (PIN 3)

This is the high-impedance output of quadrature phase detector, and is internally connected to the input of lock-detect voltage-comparator. In tone-detection applications, pin 3 is connected to ground through a parallel combination of $R_D$ and $C_D$ (see Figure 2) to eliminate the chatter at lock-detect outputs. If this tone-detect section is not used, pin 3 can be left open circuited.
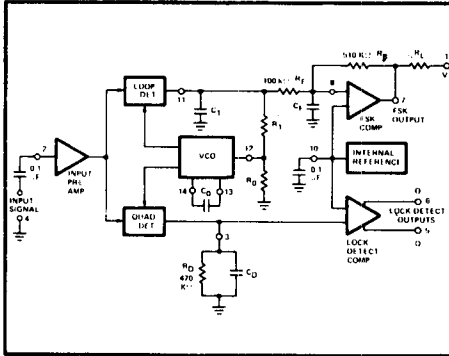
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Figure 2. *Generalized Circuit Connection for FSK and Tone Detection*

### LOCK-DETECT OUTPUT, Q (PIN 5)

The output at pin 5 is at "high" state when the PLL is out of lock and goes to "low" or conducting state when the PLL is locked. It is an open-collector type output and requires a pull-up resistor, $R_L$, to $V^+$ for proper operation. At "low" state, it can sink up to 5 mA of load current.

### LOCK-DETECT COMPLEMENT, $\overline{Q}$ (PIN 6)

The output at pin 6 is the logic complement of the lock-detect output at pin 5. This output is also an open-collector type stage which can sink 5 mA of load current at low or "on" state.

### FSK DATA OUTPUT (PIN 7)

This output is an open-collector logic stage which requires a pull-up resistor, $R_L$, to $V^+$ for proper operation. It can sink 5 mA of load current. When decoding FSK signals, FSK data output is at "high" or off state for low input frequency; and at "low" or on state for high input frequency. If no input signal is present, the logic state at pin 7 is indeterminate.

### FSK COMPARATOR INPUT (PIN 8)

This is the high-impedance input to the FSK voltage comparator. Normally, an FSK post-detection or data filter is connected between this terminal and the PLL phase-detector output (pin 11). This data filter is formed by $R_F$ and $C_F$ of Figure 2. The threshold voltage of the comparator is set by the internal reference voltage, $V_R$, available for pin 10.

### REFERENCE VOLTAGE, $V_R$ (PIN 10)

This pin is internally biased at the reference voltage level, $V_R$; $V_R = V^+/2 - 650$ mV. The dc voltage level at this pin forms an internal reference for the voltage levels at pins 3, 8, 11 and 12. Pin 10 must be bypassed to ground with a 0.1 $\mu$F capacitor, for proper operation of the circuit.

### LOOP PHASE DETECTOR OUTPUT (PIN 11)

This terminal provides a high-impedance output for the loop phase-detector. The PLL loop filter is formed by $R_1$ and $C_1$ connected to pin 11 (see Figure 2). With no input signal, or with no phase-error within the PLL, the dc level at pin 11 is very nearly equal to $V_R$. The peak voltage swing available at the phase detector output is equal to $\pm V_R$.

### VCO CONTROL INPUT (PIN 12)

VCO free-running frequency is determined by external timing resistor, $R_0$, connected from this terminal to ground. The VCO free-running frequency, $f_0$, is:

$$f_0 = \frac{1}{R_0 C_0} \text{ Hz}$$

where $C_0$ is the timing capacitor across pins 13 and 14. For optimum temperature stability, $R_0$ must be in the range of 10 K$\Omega$ to 100 K$\Omega$ (see Typical Electrical Data).

This terminal is a low-impedance point, and is internally biased at a dc level equal to $V_R$. The maximum timing current drawn from pin 12 must be limited to $\leqslant 3$mA for proper operation of the circuit.

### VCO TIMING CAPACITOR (PINS 13 AND 14)

VCO frequency is inversely proportional to the external timing capacitor, $C_0$, connected across these terminals. $C_0$ must be non-polar, and in the range of 200 pF to 10 $\mu$F

### VCO FREQUENCY ADJUSTMENT

VCO can be fine-tuned by connecting a potentiometer, $R_X$, in series with $R_0$ at pin 12 (see Figure 3).

### VCO FREE-RUNNING FREQUENCY, $f_o$.

The XR-2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase-detector sections of the circuit. However, for set-up or adjustment purposes, VCO free-running frequency can be measured at pin 3 (with $C_D$ disconnected), with no input and with pin 2 shorted to pin 10.

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## DESIGN EQUATIONS

See Figure 2 for Definitions of Components.

1.     VCO Center Frequency, $f_0$:

$$f_0 = 1/R_0C_0 \text{ Hz}$$

2.     Internal Reference Voltage, $V_R$ (measured at pin 10)

$$V_R = V^+/2 - 650 \text{ mV}$$
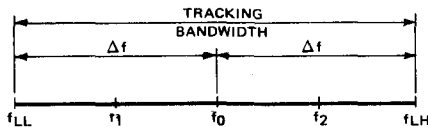
3.     Loop Lowpass Filter Time Constant, $\tau$:

$$\tau = R_1C_1$$

4.     Loop Damping, $\zeta$:

$$\zeta = 1/4\sqrt{\frac{C_0}{C_1}}$$

5.     Loop Tracking Bandwidth, $\pm\Delta f/f_0$:

$$\Delta f/f_0 = R_0/R_1$$

```
                      TRACKING
                     BANDWIDTH
          |←── Δf ──→|←── Δf ──→|

        f_LL      f_1        f_0        f_2      f_LH
```

6.     FSK Data Filter Time Constant, $\tau_F$:

$$\tau_F = R_FC_F$$

7.     Loop Phase Detector Conversion Gain, $K_\phi$: ($K_\phi$ is the differential dc voltage across pins 10 and 11, per unit of phase error at phase-detector input):

$$K_\phi = -2V_R/\pi \text{ volts/radian}$$

8.     VCO Conversion Gain, $K_0$: ($K_0$ is the amount of change in VCO frequency, per unit of dc voltage change at pin 11):

$$K_0 = -1/V_RC_0R_1 \text{ Hz/volt}$$

9.     Total Loop Gain, $K_T$:

$$K_T = 2\pi K_\phi K_0 = 4/C_0R_1 \text{ rad/sec/volt}$$

10.    Peak Phase-Detector Current, $I_A$:

$$I_A = V_R \text{ (volts)}/25 \text{ mA}$$

## APPLICATIONS

### FSK DECODING

Figure 3 shows the basic circuit connection for FSK decoding. With reference to Figures 2 and 3, the functions of external components are defined as follows: $R_0$ and $C_0$ set the PLL center frequency, $R_1$ sets the system bandwidth, and $C_1$ sets the loop-filter-time-constant and the loop damping factor. $C_F$ and $R_F$ form a one-pole post-detection filter for the FSK data output. The resistor $R_B$ (= 510 KΩ) from pin 7 to pin 8 introduces positive feedback across FSK comparator to facilitate rapid transition between output logic states.

Recommended component values for some of the most commonly used FSK bands are given in Table 1.
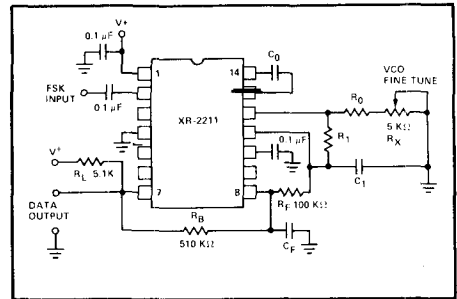


*Figure 3. Circuit Connection for FSK Decoding*

### Design Instructions

The circuit of Figure 3 can be tailored for any FSK decoding application by the choice of five key circuit components; $R_0$, $R_1$, $C_0$, $C_1$ and $C_F$. For a given set of FSK mark and space frequencies, $f_1$ and $f_2$, these parameters can be calculated as follows:

1.     Calculate PLL center frequency, $f_0$:

$$f_0 = \frac{f_1 + f_2}{2}$$

2.     Choose value of timing resistor $R_0$ to be in the range of 10 KΩ to 100 KΩ. This choice is arbitrary. The recommended value is $R_0 \cong 20$ KΩ. The final value of $R_0$ is normally fine-tuned with the series potentiometer, $R_X$.

3.     Calculate value of $C_0$ from Design Equation No. 1 or from Typical Performance Data

$$C_0 = 1/R_0f_0$$

4. Calculate $R_1$ to give a $\Delta f$ equal to the mark–space deviation:

$$R_1 = R_0 \ [f_0/f_1 - f_2)]$$

5. Calculate $C_1$ to set loop damping. (See Design Equation No. 4.)

Normally, $\zeta \approx 1/2$ is recommended.

Then: $C_1 = C_0/4$ for $\zeta = 1/2$

6. Calculate Data Filter Capacitance, $C_F$:

For $R_F = 100 \ K\Omega$, $R_B = 510 \ K\Omega$, the recommended value of $C_F$ is:

$$C_F \approx 3/Baud \ Rate) \ \mu F$$

**Note:** *All calculated component values except $R_0$ can be rounded-off to the nearest standard value, and $R_0$ can be varied to fine-tune center frequency through a series potentiometer, $R_X$. (See Figure 3.)*

**Design Example:**

75 Baud FSK demodulator with mark/space frequencies of 1110/1170 Hz:

Step 1: Calculate $f_0$: $f_0 = (1110 + 1170) \ (1/2) = 1140$ Hz

Step 2: Choose $R_0 = 20 \ K\Omega$ (13 K$\Omega$ fixed resistor in series with 5 K$\Omega$ potentiometer)

Step 3: Calculate $C_0$ from VCO Frequency vs Timing Capacitor: $C_0 = 0.044 \ \mu F$

Step 4: Calculate $R_1$: $R_1 = R_0 \ (2240/60) = 380 \ K\Omega$

Step 5: Calculate $C_1$: $C_1 = C_0/4 = 0.011 \ \mu F$

**Note:** *All values except $R_0$ can be rounded-off to nearest standard value.*

*Table 1. Recommended Component Values for Commonly Used FSK Bands (See Circuit of Figure 3)*

| FSK BAND | COMPONENT VALUES | |
|---|---|---|
| 300 Baud | $C_0 = 0.039 \ \mu F$ | $C_F = 0.005 \ \mu F$ |
| $f_1 = 1070$ Hz | $C_1 = 0.01 \ \mu F$ | $R_0 = 18 \ K\Omega$ |
| $f_2 = 1270$ Hz | $R_1 = 100 \ K\Omega$ | |
| 300 Baud | $C_0 = 0.022 \ \mu F$ | $C_F = 0.005 \ \mu F$ |
| $f_1 = 2025$ Hz | $C_1 = 0.0047 \ \mu F$ | $R_0 = 18 \ K\Omega$ |
| $f_2 = 2225$ Hz | $R_1 = 200 \ K\Omega$ | |



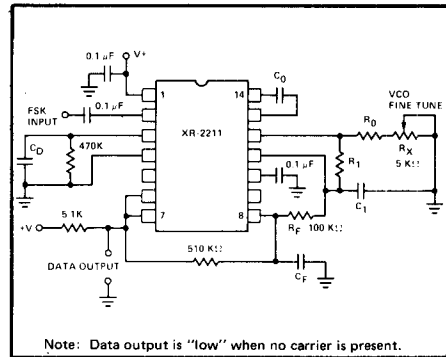Note: Data output is "low" when no carrier is present.

*Figure 4. External Connectors for FSK Demodulation with Carrier-Detect Capability*

## FSK DECODING WITH CARRIER-DETECT

The lock–detect section of the XR-2211 can be used as a carrier-detect option for FSK decoding. The recommended circuit connection for this application is shown in Figure 4. The open-collector lock-detect output, pin 6, is shorted to data output (pin 7). Thus, data output will be disabled at "low" state until there is a carrier within the detection band of the PLL and the pin 6 output goes "high" to enable the data output.

The minimum value of the lock-detect filter capacitance $C_D$ is inversely proportional to the capture range, $\pm \Delta f_c$. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by $C_1$. For most applications, $\Delta f_c > \Delta f/2$. For $R_D = 470 \ K\Omega$, the approximate minimum value of $C_D$ can be determined by:

$$C_D \ (\mu F) \geqslant 16/\text{capture range in Hz.}$$

With values of $C_D$ that are too small, chatter can be observed on the lock-detect output as an incoming signal frequency approaches the capture bandwidth. Excessively-large values of $C_D$ will slow the response time of the lock-detect output.

## TONE DETECTION

Figure 5 shows the generalized circuit connection for tone detection. The logic outputs, Q and $\bar{Q}$ at pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs become reversed for the duration of the input tone. Each logic output can sink 5 mA of load current.

Both logic outputs at pins 5 and 6 are open-collector type stages, and require external pull-up resistors $R_{L1}$ and $R_{L2}$, as shown in Figure 5.
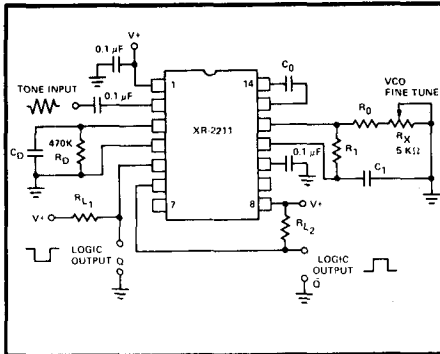
*Figure 5. Circuit Connection for Tone Detection*

With reference to Figures 2 and 5, the function of the external circuit components can be explained as follows: $R_0$ and $C_0$ set VCO center frequency; $R_1$ sets the detection bandwidth; $C_1$ sets the lowpass-loop filter time constant and the loop damping factor, $R_{L1}$ and $R_{L2}$ are the respective pull-up resistors for the Q and $\overline{Q}$ logic outputs.

**Design Instructions**

The circuit of Figure 5 can be optimized for any tone-detection application by the choice of the 5 key circuit components: $R_0$, $R_1$, $C_0$, $C_1$ and $C_D$. For a given input tone frequency, $f_S$, these parameters are calculated as follows:

1.  Choose $R_0$ to be in the range of 15 K$\Omega$ to 100 K$\Omega$. This choice is arbitrary.

2.  Calculate $C_0$ to set center frequency, $f_0$ equal to $f_S$: $C_0 = 1/R_0 f_S$.

3.  Calculate $R_1$ to set bandwidth $\pm \Delta f$; (see Design Equation No. 5):

    $R_1 = R_0(f_0/\Delta f)$

**Note:** *The total detection bandwidth covers the frequency range of $f_0 \pm \Delta f$.*

4.  Calculate value of $C_1$ for a given loop damping factor:

    $C_1 = C_0/16\zeta^2$

Normally $\zeta \approx 1/2$ is optimum for most tone-detector applications, giving $C_1 = 0.25\ C_0$.

Increasing $C_1$ improves the out-of-band signal rejection, but increases the PLL capture time.

5.  Calculate value of filter capacitor $C_D$. To avoid chatter at the logic output, with $R_D$ = 470 K$\Omega$, $C_D$ must be:

    $C_D\ (\mu F) \geqslant (16/\text{capture range in Hz})$

Increasing $C_D$ slows the logic output response time.

**Design Examples:**

Tone detector with a detection band of 1 kHz ± 20 Hz:

Step 1:  Choose $R_0$ = 20 K$\Omega$ (18 K$\Omega$ in series with 5 K$\Omega$ potentiometer).

Step 2:  Choose $C_0$ for $f_0$ = 1 kHz: $C_0 = 0.05\ \mu F$.

Step 3:  Calculate $R_1$: $R_1 = (R_0)\ (1000/20) = 1\ M\Omega$.

Step 4:  Calculate $C_1$: for $\zeta$ = 1/2, $C_1 = 0.25\ \mu F$, $C_0 = 0.013\ \mu F$.

Step 5:  Calculate $C_D$: $C_D = 16/38 = 0.42\ \mu F$.

Step 6:  Fine-tune center frequency with 5 K$\Omega$ potentiometer, $R_X$.

**LINEAR FM DETECTION**



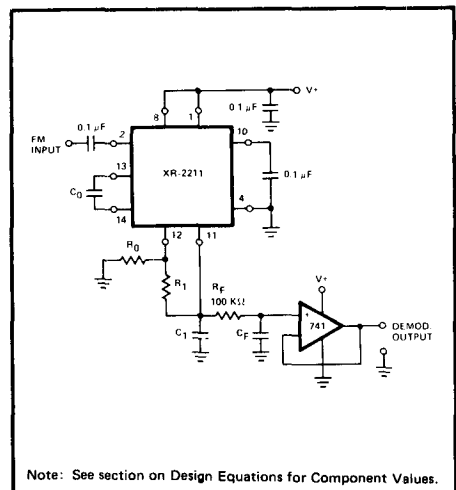Note: See section on Design Equations for Component Values.

*Figure 6. Linear FM Detector Using XR-2211 and an External Op Amp*

## LINEAR FM DETECTION

The XR-2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for the application is shown in Figure 6. The demodulated output is taken from the loop phase detector output (pin 11), through a post detection filter made up of $R_F$ and $C_F$, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Figure 6.

The FM detector gain, i.e., the output voltage change per unit of FM deviation, can be given as:

$$V_{out} = R_1 \, V_R/100 \, R_0 \text{ Volts/\%deviation}$$

where $V_R$ is the internal reference voltage. ($V_R = V^+/2 - 650$ mV). For the choice of external components $R_1$, $R_0$, $C_D$, $C_1$ and $C_F$, see section on Design Equations.

## AVAILABLE TYPES

| Part Number | Package | Operating Temperature |
|-------------|---------|----------------------|
| XR-2211M | Ceramic | $-55°C$ to $+125°C$ |
| XR-2211N | Ceramic | $-40°C$ to $+85°C$ |
| XR-2211P | Plastic | $-40°C$ to $+85°C$ |
| XR-2211CN | Ceramic | $0°C$ to $+75°C$ |
| XR-2211CP | Plastic | $0°C$ to $+75°C$ |