

MOS INTEGRATED CIRCUIT

μ PD78011B, 78012B, 78013, 78014

8-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μ PD78011B/78012B/78013/78014 are the products in the μ PD78014 subseries within the 78K/0 Series.

The μ PD78011B/78012B/78013/78014 have 8-bit resolution A/D converter, timer, serial interface, interrupt control, and many other peripheral hardware functions.

A one-time PROM or EPROM product μ PD78P014 capable of operating in the same power supply voltage range as of the mask ROM product and other development tools are also provided.

Functions are described in detail in the following User's Manual, which should be read when carrying out design work.

μ PD78014, 78014Y Series User's Manual: IEU-1343

FEATURES

- Large on-chip ROM & RAM

Item Product Name	Program Memory (ROM)	Data Memory		Package
		Internal High-Speed RAM	Buffer RAM	
μ PD78011B	8K bytes	512 bytes	32 bytes	<ul style="list-style-type: none"> • 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (\square14 mm)
μ PD78012B	16K bytes			
μ PD78013	24K bytes	1024bytes		
μ PD78014	32K bytes			

- External memory expansion space : 64K bytes
- Instruction execution time can be varied from high-speed (0.4 μ s) to ultra-low-speed (122 μ s)
- I/O ports: 53 (N-ch open-drain : 4)
- 8-bit resolution A/D converter : 8 channels
- Serial interface : 2 channels
- Timer : 5 channels
- Operating voltage range : 2.7 to 6.0 V

Application

Telephone, VCR, audio, camera, home appliances, etc.

The information in this document is subject to change without notice.

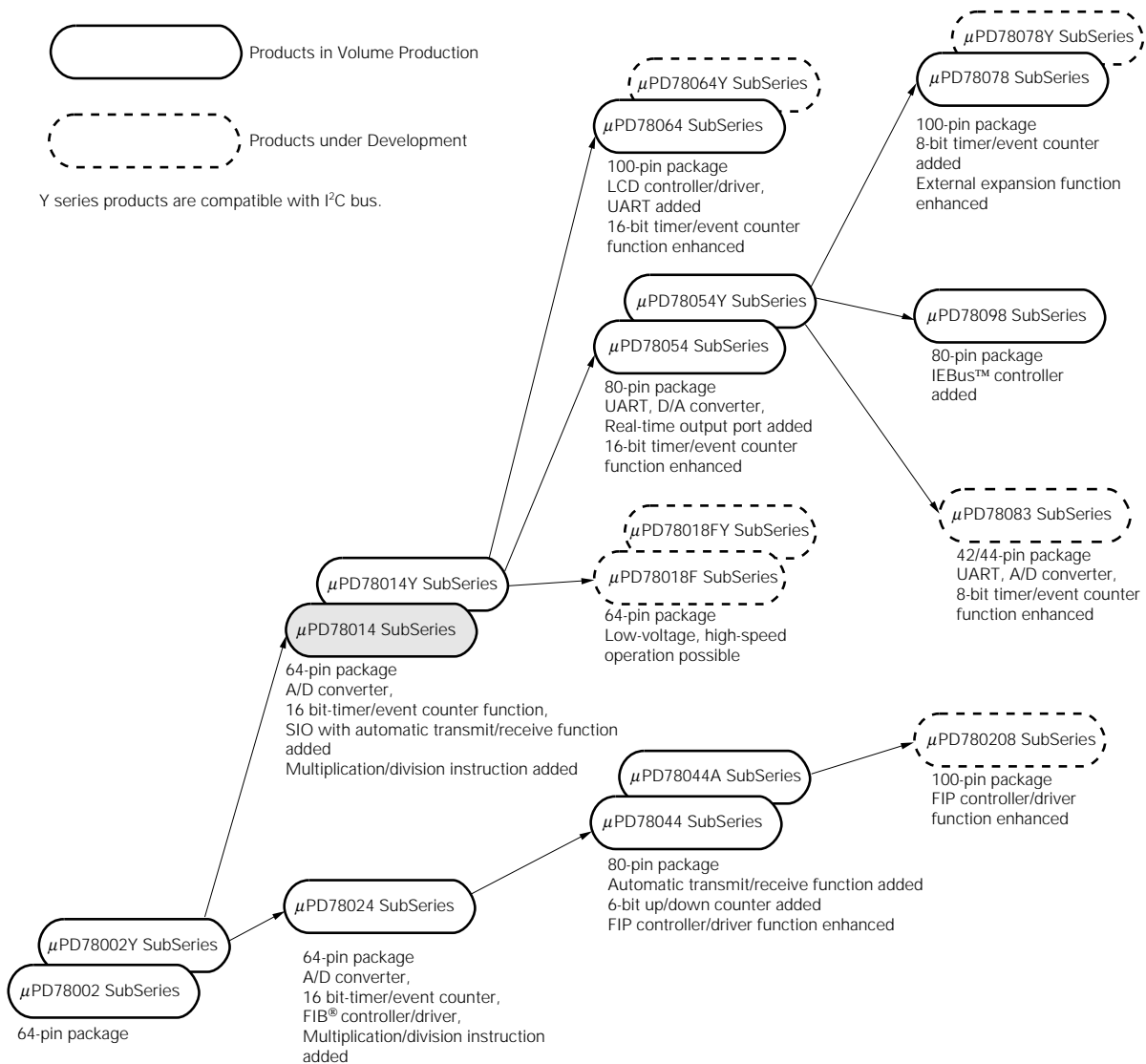
ORDERING INFORMATION

Ordering Code	Package	Quality Grade
μPD78011BCW-xxx	64-pin plastic shrink DIP (750 mil)	Standard
μPD78011BGC-xxx-AB8	64-pin plastic QFP (□14 mm)	Standard
μPD78012BCW-xxx	64-pin plastic shrink DIP (750 mil)	Standard
μPD78012GC-xxx-AB8	64-pin plastic QFP (□14 mm)	Standard
μPD78013CW-xxx	64-pin plastic shrink DIP (750 mil)	Standard
μPD78013GC-xxx-AB8	64-pin plastic QFP (□14 mm)	Standard
μPD78014CW-xxx	64-pin plastic shrink DIP (750 mil)	Standard
μPD78014GC-xxx-AB8	64-pin plastic QFP (□14 mm)	Standard

Remarks xxx indicates ROM code No.

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

★ 78K/0 SERIES DEVELOPMENT



OVERVIEW OF FUNCTION (1/2)

Product Name		Item	μPD78011B	μPD78012B	μPD78013	μPD78014
Internal memory	ROM		8K bytes	16K bytes	24K bytes	32K bytes
	Internal high-speed RAM		512 bytes		1024 bytes	
	Buffer RAM		32 bytes			
Memory space			64K bytes			
General registers			8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Instruction cycle			On-chip instruction execution time cycle modification function			
	When main system clock selected		0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (at 10.0 MHz operation)			
	When subsystem clock selected		122 μs (at 32.768 kHz operation)			
Instruction set			<ul style="list-style-type: none"> • 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD correction, etc. 			
I/O ports			Total : 53 • CMOS input : 2 • CMOS I/O : 47 • N-channel open-drain I/O (15 V withstand voltage) : 4			
A/D converter			<ul style="list-style-type: none"> • 8-bit resolution × 8 channels • Operable over a wide power supply voltage range: V_{DD} = 2.7 to 6.0 V 			
Serial interface			<ul style="list-style-type: none"> • 3-wire/SBI/2-wire mode selectable: 1 channel • 3-wire mode (on-chip max. 32 bytes automatic data transmit/receive function): 1 channel 			
Timer			<ul style="list-style-type: none"> • 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel 			
Timer output			3 (14-bit PWM output × 1)			
Clock output			39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz (at main system clock 10.0 MHz operation), 32.768 kHz (at subsystem clock 32.768 kHz operation)			
Buzzer output			2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock 10.0 MHz operation)			
Vectored interrupts	Maskable interrupts		Internal : 8 External: 4			
	Non-maskable interrupt		Internal : 1			
	Software interrupt		Internal : 1			

OVERVIEW OF FUNCTION (2/2)

Item	μPD78011B	μPD78012B	μPD78013	μPD78014
Product Name				
Test input	Internal : 1 External : 1			
Operating voltage range	V _{DD} = 2.7 to 6.0 V			
Operating temperature range	-40 to +85°C			
Package	<ul style="list-style-type: none"> • 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (□14 mm) 			

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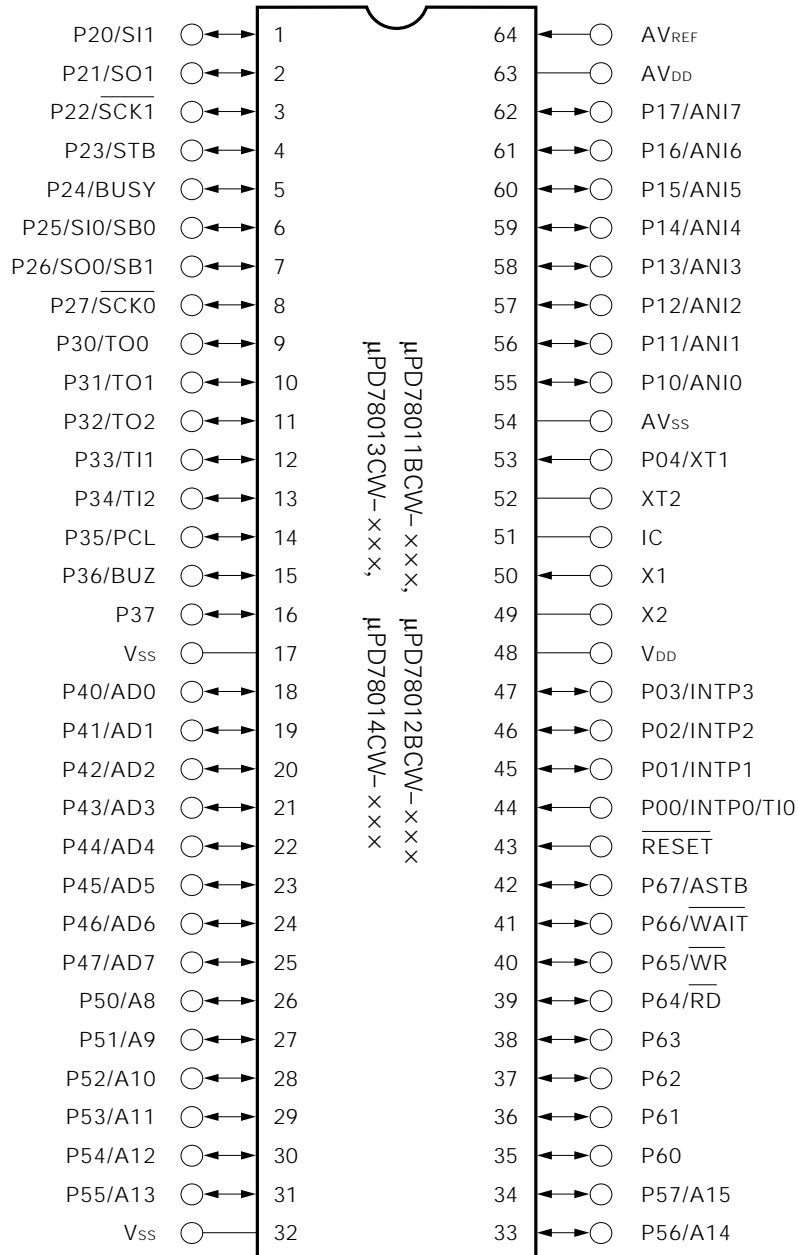
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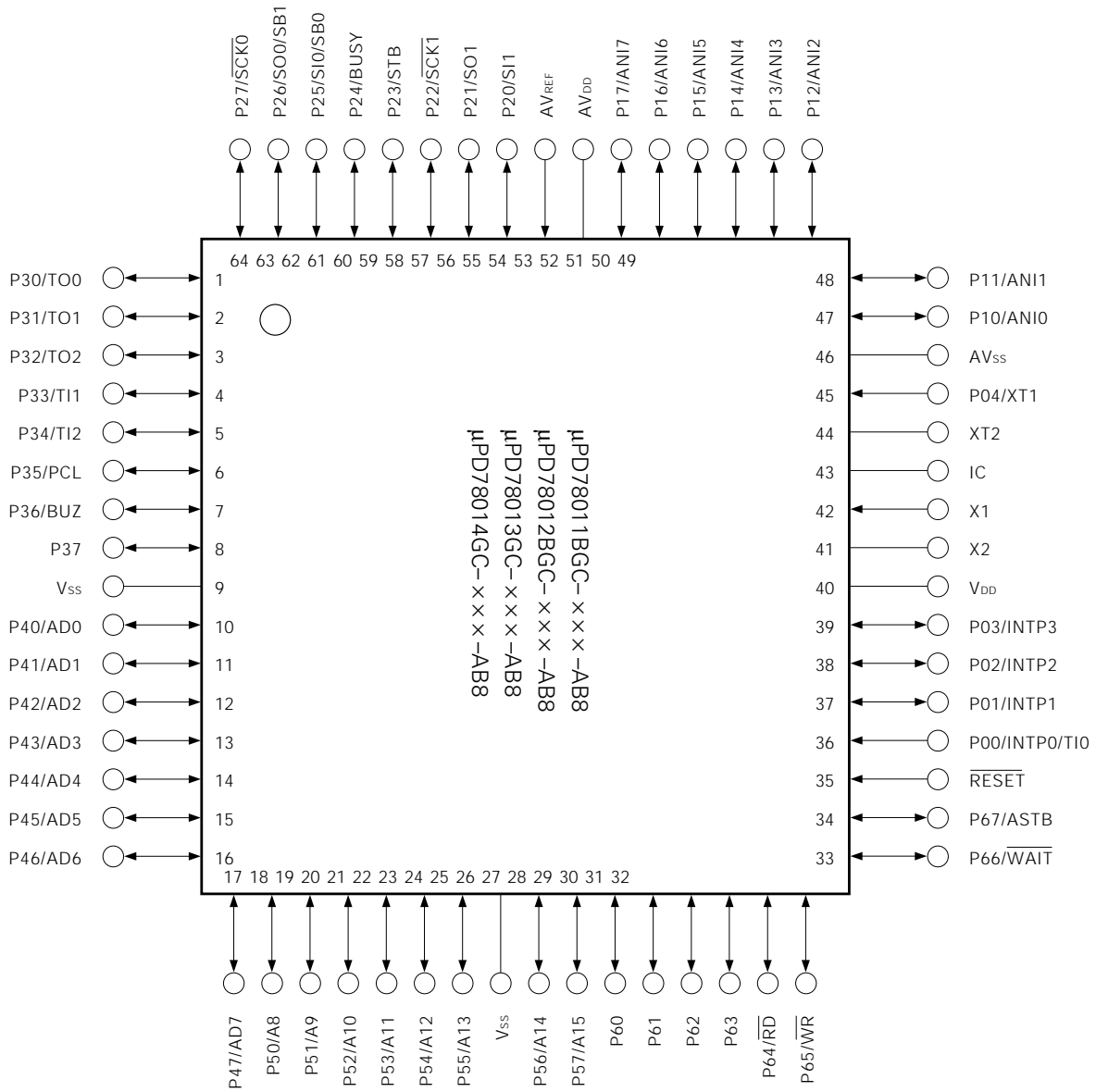
1. PIN CONFIGURATION (Top View)

64-Pin Plastic Shrink DIP (750 mil)



- Caution**
1. Always connect the IC (Internally Connected) pin to V_{SS} directly.
 2. Always connect the AV_{DD} pin to V_{DD}.
 3. Always connect the AV_{SS} pin to V_{SS}.

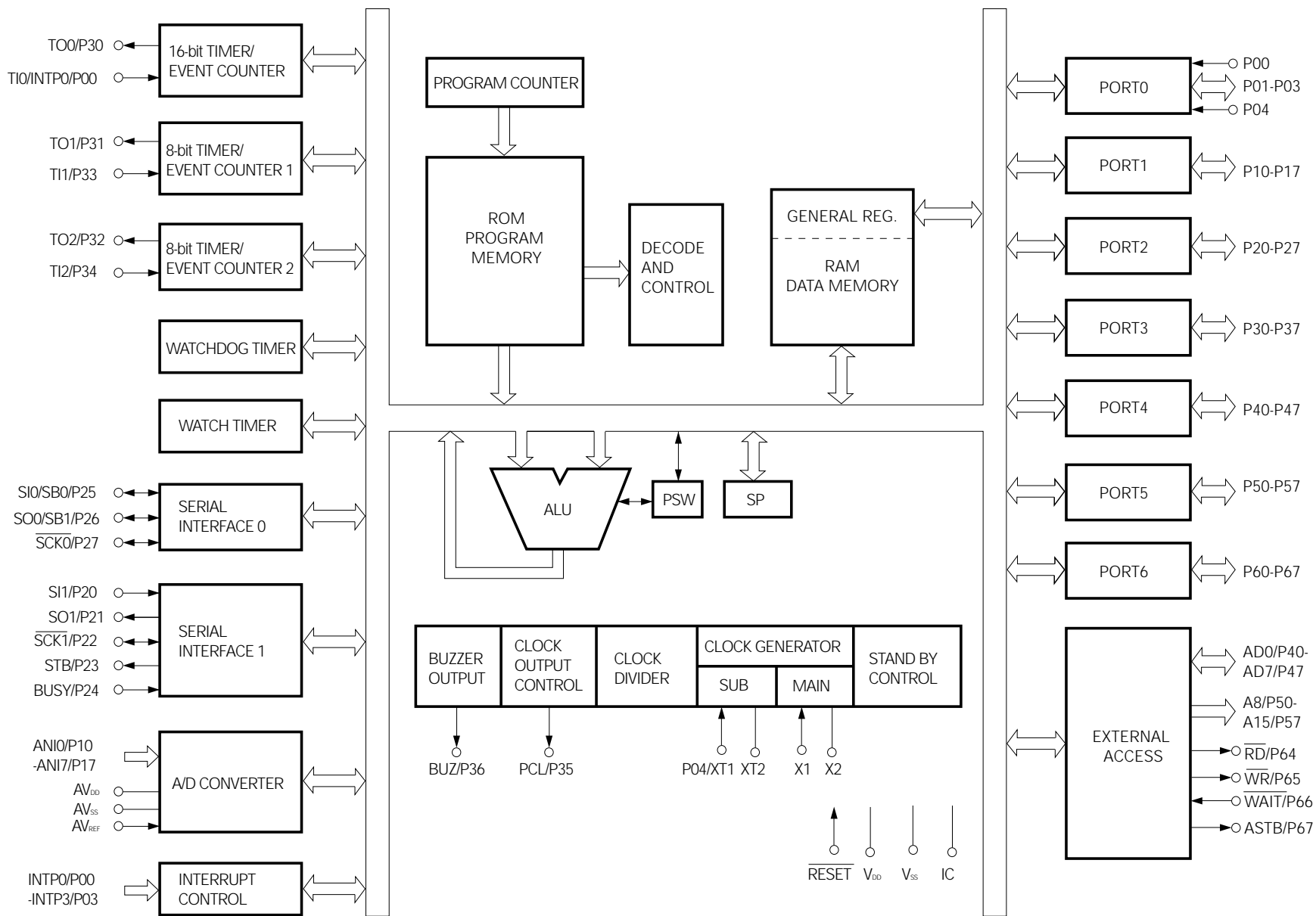
64-Pin Plastic QFP (□14 mm)



- Caution**
1. Always connect the IC (Internally Connected) pin to V_{SS} directly.
 2. Always connect the AV_{DD} pin to V_{DD}.
 3. Always connect the AV_{SS} pin to V_{SS}.

P00 to P04	: Port 0	AD0 to AD7	: Address/Data Bus
P10 to P17	: Port 1	A8 to A15	: Address Bus
P20 to P27	: Port 2	$\overline{\text{RD}}$: Read Strobe
P30 to P37	: Port 3	$\overline{\text{WR}}$: Write Strobe
P40 to P47	: Port 4	$\overline{\text{WAIT}}$: Wait
P50 to P57	: Port 5	ASTB	: Address Strobe
P60 to P67	: Port 6	X1, X2	: Crystal (Main System Clock)
INTP0 to INTP3	: Interrupt From Peripherals	$\overline{\text{XT1}}, \overline{\text{XT2}}$: Crystal (Subsystem Clock)
T10 to T12	: Timer Input	RESET	: Reset
TO0 to TO2	: Timer Output	ANI0 to ANI7	: Analog Input
SB0, SB1	: Serial Bus	AV _{DD}	: Analog Power Supply
SI0, SI1	: Serial Input	AV _{SS}	: Analog Ground
SO0, SO1	: Serial Output	AV _{REF}	: Analog Reference Voltage
$\overline{\text{SCK0}}, \overline{\text{SCK1}}$: Serial Clock	V _{DD}	: Power Supply
PCL	: Programmable Clock	V _{SS}	: Ground
BUZ	: Buzzer Clock	IC	: Internally Connected
STB	: Strobe		
BUSY	: Busy		

2. BLOCK DIAGRAM



Remarks Internal ROM & RAM capacity varies depending on the product.

3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin Name	I/O	Function		After Reset	Dual-Function Pin
P00	Input	Port 0 5-bit I/O port	Input only	Input	INTP0/TI0
P01	Input/ output		Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.	Input	INTP1
P02					INTP2
P03					INTP3
P04*1	Input		Input only	Input	XT1
P10 to P17	Input/ output	Port 1 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.*2		Input	ANI0 to ANI7
P20	Input/ output	Port 2 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.		Input	SI1
P21					SO1
P22					$\overline{\text{SCK1}}$
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					SCK0
P30	Input/ output	Port 3 8-bit input/output port. Input/output can be specified in 1-bit units. When used as an input port, pull-up resistor can be used by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—
P40 to P47	Input/ output	Port 4 8-bit input/output port. Input/output can be specified in 8-bit unit. When used as an input port, pull-up resistor can be used by software. Test input flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7

- * 1. When using the P04/XT1 pins as an input port, set 1 to bit 6 (REC) of the processor control register. Do not use the on-chip feedback register of the subsystem clock oscillator.
- 2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input, pull-up resistor is automatically unused.

3.1 PORT PINS (2/2)

Pin Name	I/O	Function		After Reset	Dual-Function Pin
P50 to P57	Input/output	Port 5 8-bit input/output port. LED can be driven directly. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.		Input	A8 to A15
P60	Input/output	Port 6 8-bit input/output port. Input/output can be specified bit-wise.	N-ch open-drain input/output port. On-chip pull-up resistor can be specified by mask option. LED can be driven directly.	Input	
P61					
P62					
P63					
P64		When used as an input port, pull-up resistor can be used by software.	RD		
P65			WR		
P66			WAIT		
P67			ASTB		

Caution When pull-up resistors are not used (specified by mask option), the low-level input leak current increases with -200 μA (MAX.) under either of the following conditions.

- ① When the external device expansion function is used and a low-level is input to the pin.
- ② During the 3-clock period when a read instruction is executed on port 6 (P6) and the port mode register (PM6).

3.2 OTHER PORTS (1/2)

Pin Name	I/O	Function		After Reset	Dual-Function Pin
INTP0	Input	External interrupt input by which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.		Input	P00/TI0
INTP1					P01
INTP2					P02
INTP3		Falling edge detection external interrupt input.	P03		
SI0	Input	Serial interface serial data input.		Input	P25/SB0
SI1					P20
SO0	Output	Serial interface serial data output.		Input	P26/SB1
SO1					P21
SB0	Input/output	Serial interface serial data input/output.		Input	P25/SI0
SB1					P26/SO0
SCK0	Input/output	Serial interface serial clock input/output.		Input	P27
SCK1					P22
STB	Output	Serial interface automatic transmit/receive strobe output.		Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input.		Input	P24

3.2 OTHER PORTS (2/2)

Pin Name	I/O	Function	After Reset	Dual-Function Pin
T10	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
T11		External count clock input to 8-bit timer (TM1).		P33
T12		External count clock input to 8-bit timer (TM2).		P34
TO0	Output	16-bit timer output (shared as 14-bit PWM output).	Input	P30
TO1		8-bit timer output.		P31
TO2				P32
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
AD0 to AD7	Input /output	Low-order address/data bus at external memory expansion.	Input	P40 to P47
A8 to A15	Output	High-order address bus at external memory expansion.	Input	P50 to P57
\overline{RD}	Output	External memory read operation strobe signal output.	Input	P64
\overline{WR}		External memory write operation strobe signal output.		P65
\overline{WAIT}	Input	Wait insertion at external memory access.	Input	P66
ASTB	Output	Strobe output which latches the address information output at port 4 and port 5 to access external memory.	Input	P67
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
AVREF	Input	A/D converter reference voltage input.	—	—
AVDD	—	A/D converter analog power supply. Connected to V _{DD} .	—	—
AVSS	—	A/D converter ground potential. Connected to V _{SS} .	—	—
\overline{RESET}	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P04
XT2	—		—	—
VDD	—	Positive power supply.	—	—
VSS	—	Ground potential.	—	—
IC	—	Internal connection. Connected to V _{SS} directly.	—	—

3.3 PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.

For the input/output circuit configuration of each type, see Fig. 3-1.

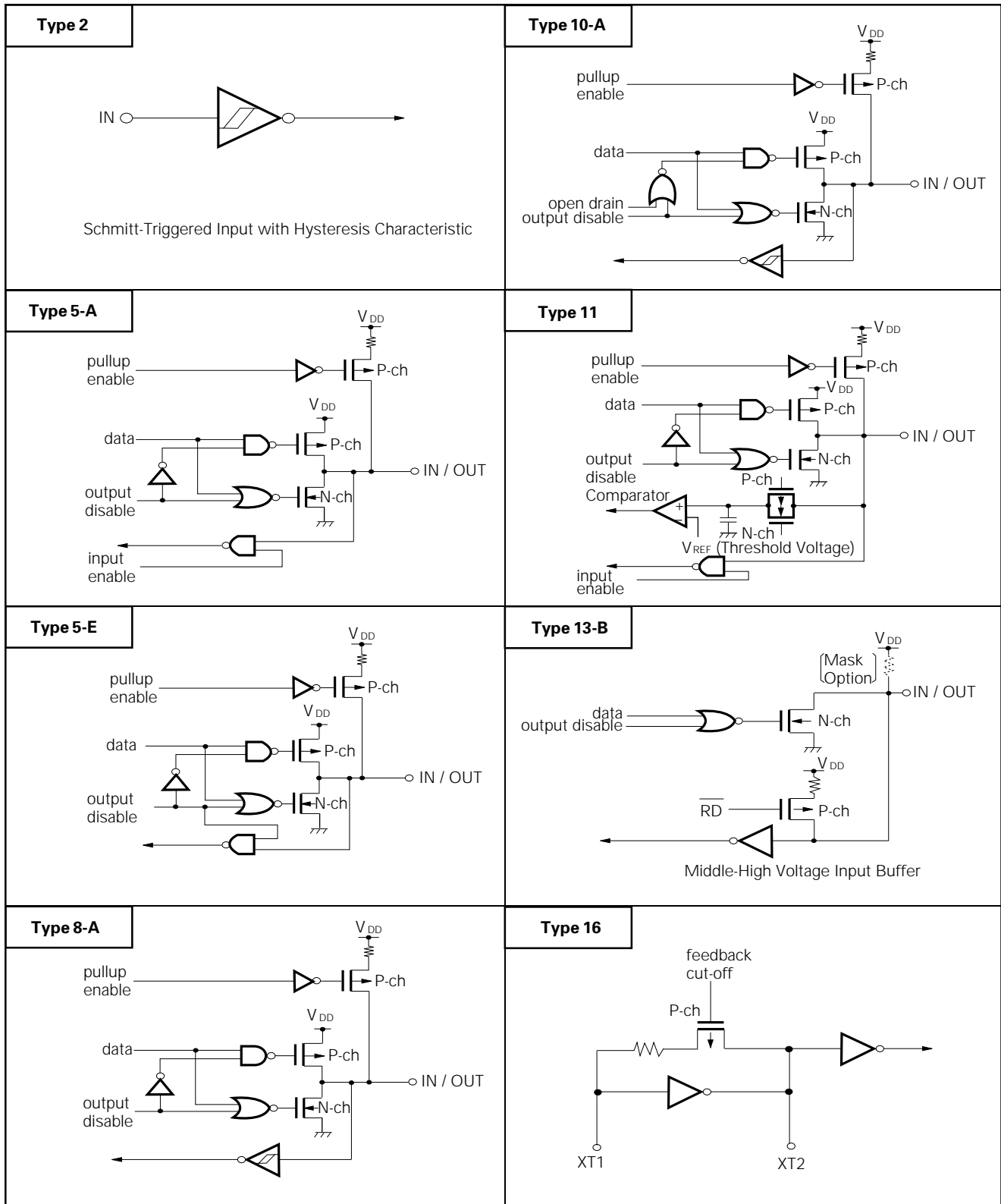
Table 3-1 Input/Output Circuit Type of Each Pin (1/2)

Pin Name	Input/output Circuit Type	I/O	Recommended Connection when Not Used
P00/INTP0/TI0	2	Input	Connected to Vss .
P01/INTP1	8-A	Input/output	Input : Connected to Vss .
P02/INTP2			Output : Leave open.
P03/INTP3			
P04/XT1	16	Input	Connected to Vss .
P10/ANI0 to P17/ANI7	11	Input/output	Input : Connected to V _{DD} or Vss . Output : Leave open.
P20/SI1	8-A	Input/output	Input : Connected to V _{DD} or Vss . Output : Leave open.
P21/SO1	5-A		
P22/ $\overline{\text{SCK1}}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/ $\overline{\text{SCK0}}$			
P30/TO0	5-A	Input/output	Input : Connected to V _{DD} or Vss . Output : Leave open.
P31/TO1			
P32/TO2			
P33/TI1	8-A	Input/output	Input : Connected to V _{DD} or Vss . Output : Leave open.
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0 to P47/AD7			
P50/A8 to P57/A15	5-A		
P60 to P63	13-B		
P64/ $\overline{\text{RD}}$	5-A		
P65/ $\overline{\text{WR}}$			
P66/ $\overline{\text{WAIT}}$			
P67/ASTB			

Table 3-1 Input/Output Circuit Type of Each Pin (2/2)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection when Not Used
RESET	2	Input	—
XT2	16	—	Leave open.
AVREF	—		Connected to Vss .
AVDD			Connected to VDD .
AVSS			Connected to Vss .
IC			Connected to Vss directly.

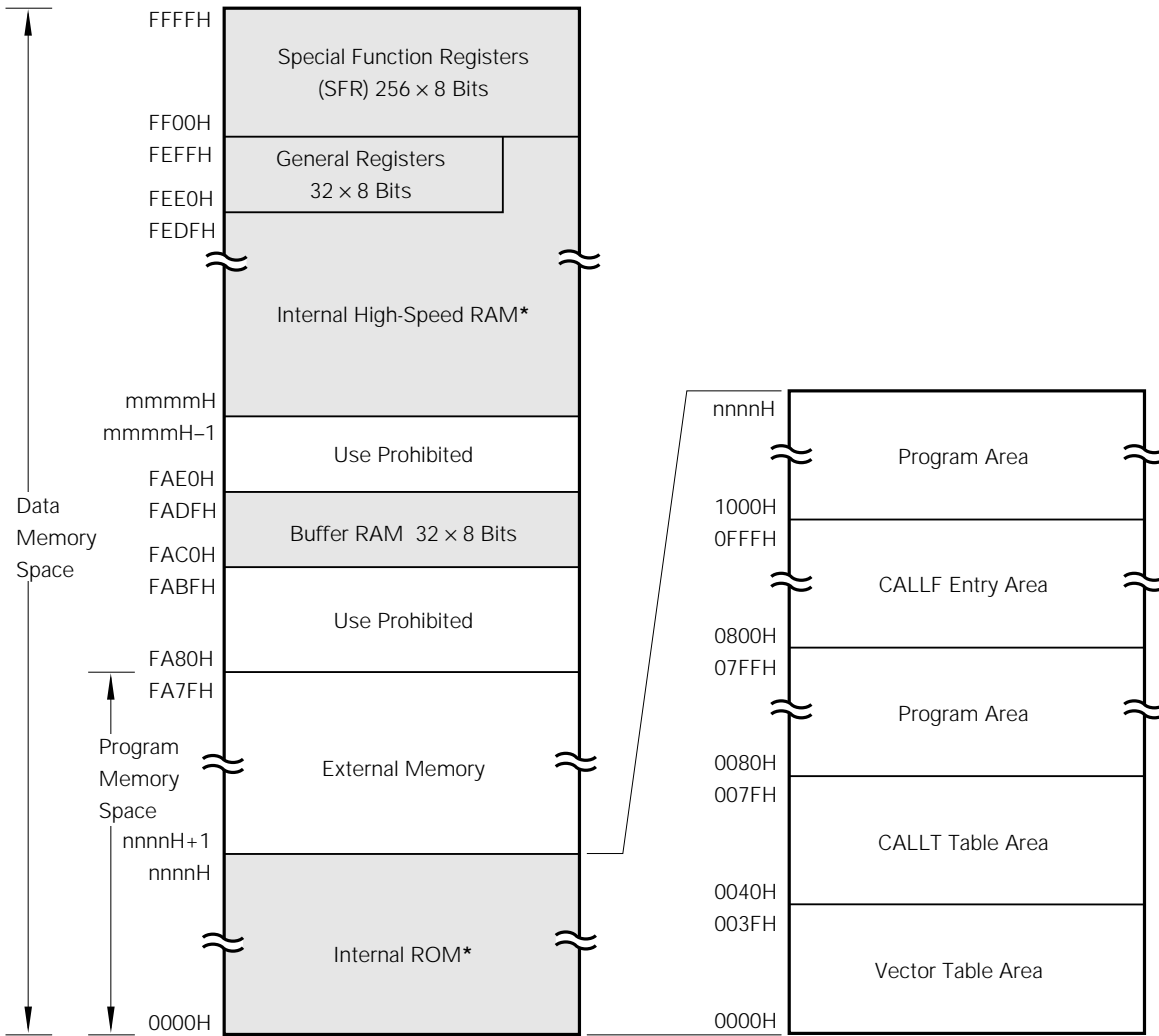
Fig. 3-1 Pin Input/Output Circuits



4. MEMORY SPACE

The memory map of μPD78011B/78012B/78013/78014 is shown in Fig 4-1.

Fig.4-1 Memory Map



Remarks Shaded area indicates internal memory.

* Internal ROM and internal high-speed RAM capacities vary depending on the product (see the table below).

Product Name	Internal ROM End Address nnnnH	Internal High-Speed RAM StartAddress mmmmH
μPD78011B	1FFFH	FD00H
μPD78012B	3FFFH	
μPD78013	5FFFH	FB00H
μPD78014	7FFFH	

5 PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 PORTS

The I/O port has the following three types

- CMOS input (P00, P04) : 2
 - CMOS input/output (P01 to P03, port 1 to port 5, P64 to P67) : 47
 - N-ch open-drain input/output(15V withstand voltage) (P60 to P63) : 4
-
- Total : 53

Table 5-1 Functions of Ports

Port Name	Pin Name	Function
Port 0	P00, P04	Dedicated Input port
	P01 to P03	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.
Port 1	P10 to P17	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.
Port 2	P20 to P27	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.
Port 3	P30 to P37	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.
Port 4	P40 to P47	Input/output ports. Input/output can be specified in 8-bit units. When used as an input port, pull-up resistor can be used by software. Test input flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software. LED can be driven directly.
Port 6	P60 to P63	N-ch open-drain input/output port. Input/output can be specified bit-wise. On-chip pull-up resistor can be specified by mask option. LED can be driven directly.
	P64 to P67	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.

Caution When pull-up resistors are not used (specified by mask option), low-level input leak current increases with – 200 mA (MAX.) under either of the following conditions.

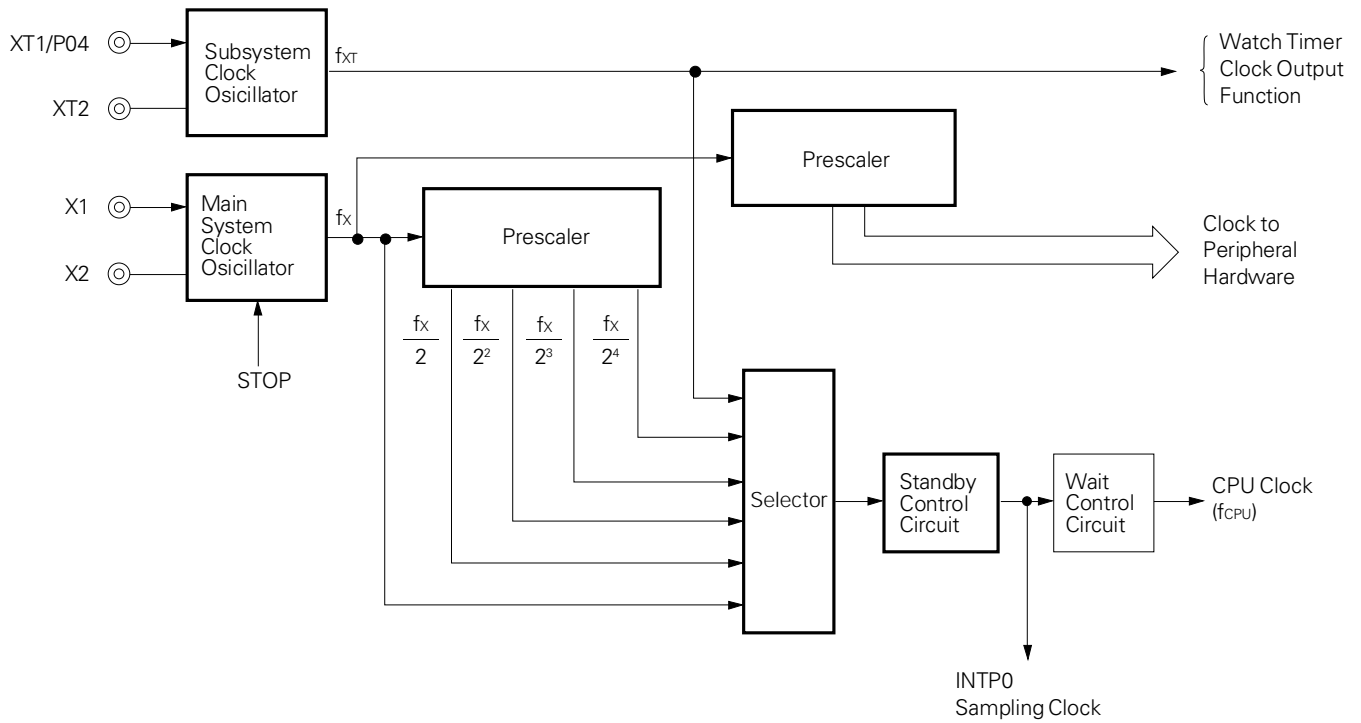
- ① When the external device expansion function is used and a low-level is input to the pin.
- ② During the 3-clock period when a read instruction is executed on port 6 (P6) and the port mode register (PM6).

5.2 CLOCK GENERATOR

There are two types of clock generator: main system clock and subsystem clock.
The instruction execution time can be changed.

- 0.4μs/0.8μs/1.6μs/3.2μs/6.4μs (Main system clock: at 10.0 MHz operation)
- 122μs (Subsystem clock: at 32.768 KHz operation)

Fig. 5-1 Clock Generator Block Diagram



5.3 TIMER/EVENT COUNTER

The following five channels are incorporated in the timer/event counter.

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2 Types and Features of Timer/Event Counter

		16-bit Timer/Event Counter	8-bit Timer/Event Counter	Watch Timer	Watchdog Timer
Type	Interval timer	1 channel	2 channels	1channel	1 channel
	Externanal event counter	1 channel	2 channels	–	–
Functions	Timer output	1 output	2 outputs	–	–
	PWM output	1 output	–	–	–
	Pulse width mesurement	1 input	–	–	–
	Sqare wave output	1 output	2 outputs	–	–
	Interrupt request	2	2	2	1

Fig. 5-2 16-bit Timer/Event Counter Block Diagram

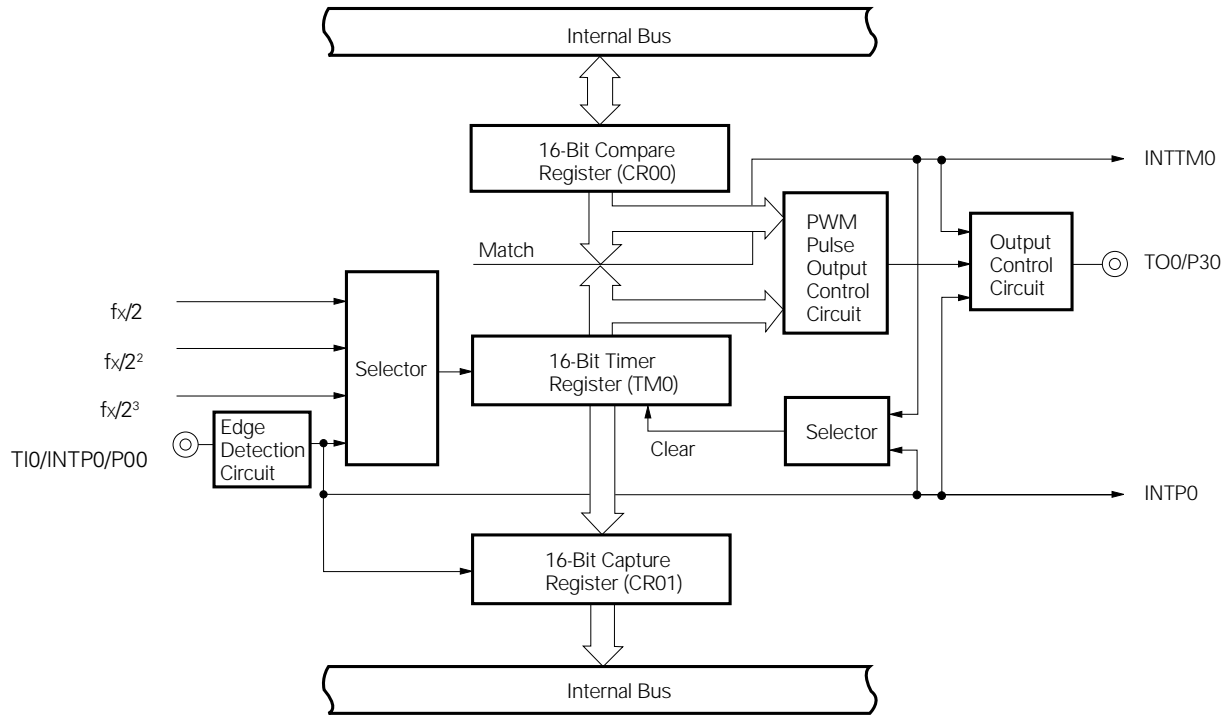


Fig. 5-3 8-bit Timer/Event Counter Block Diagram

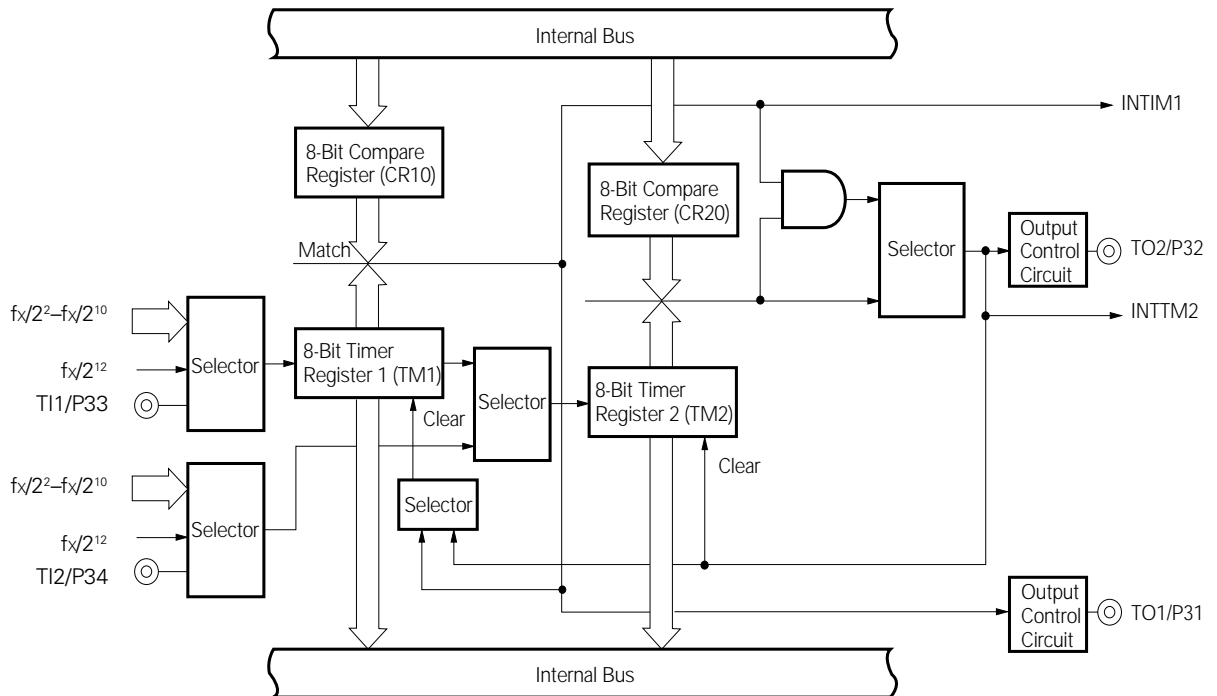


Fig. 5-4 Watch Timer Block Diagram

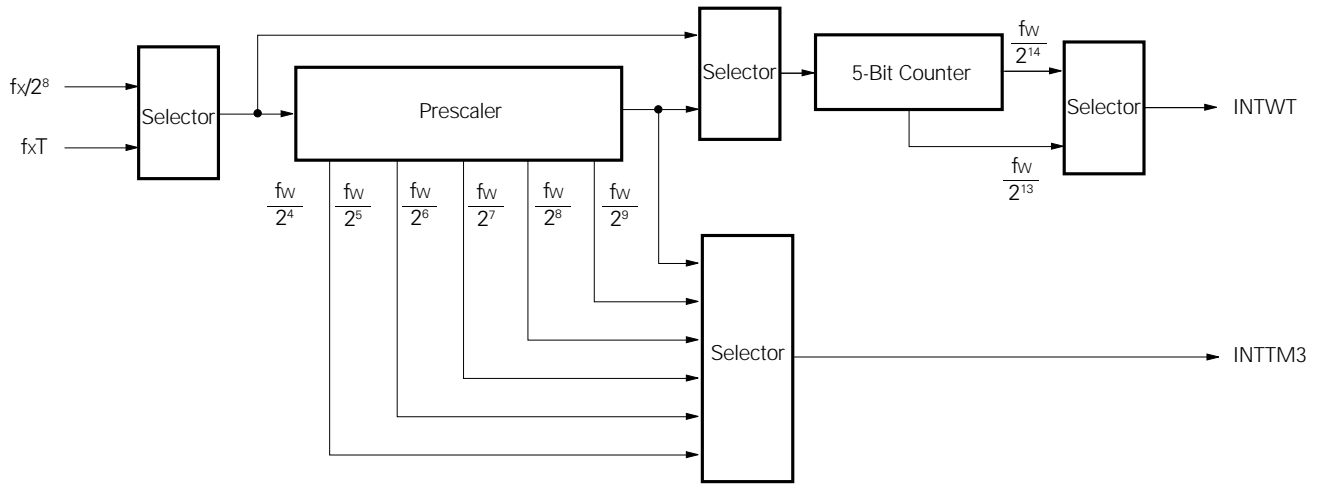
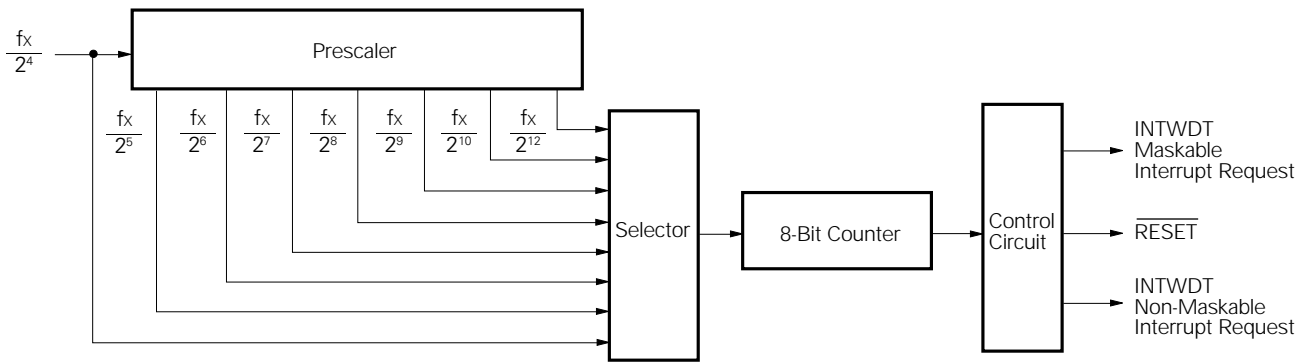


Fig. 5-5 Watchdog Timer Block Diagram

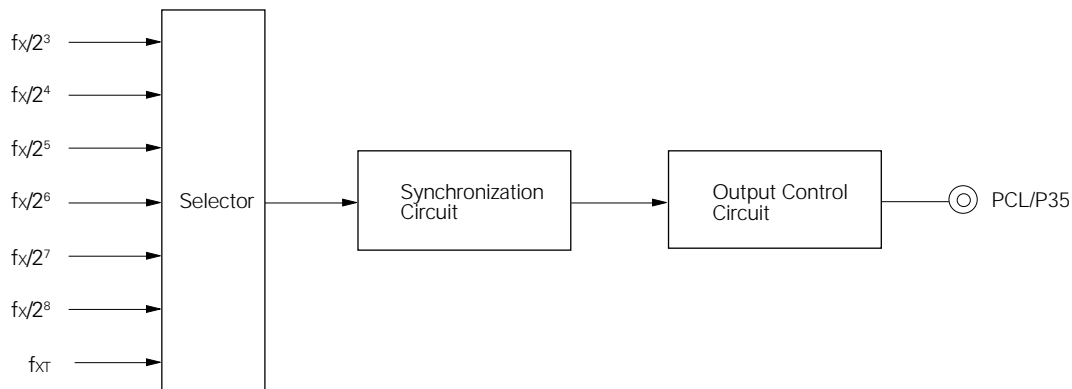


5.4 CLOCK OUTPUT CONTROL CIRCUIT

The clock with the following frequencies can be output for clock output.

- 39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz (Main system clock: at 10.0 MHz operation)
- 32.768 kHz (Subsystem clock: at 32.768 kHz operation)

Fig. 5-6 Clock Output Control Block Diagram

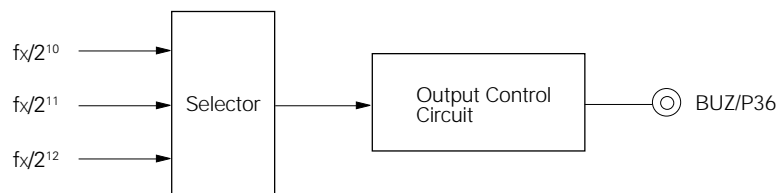


5.5 BUZZER OUTPUT CONTROL CIRCUIT

The clock with the following frequencies can be output for buzzer output.

- 2.4 kHz/4.9 kHz/9.8 kHz (Main system clock: at 10.0 MHz operation)

Fig. 5-7 Buzzer Output Control Block Diagram

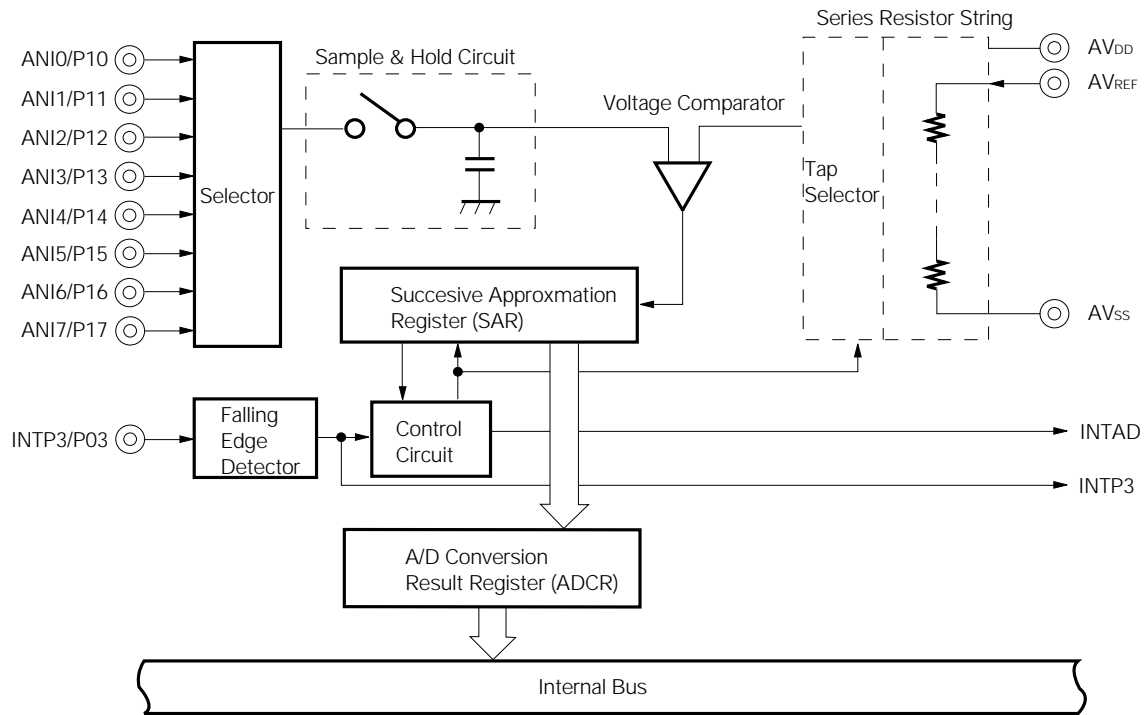


5.6 A/D CONVERTER

The A/D converter has on-chip eight 8-bit resolution channels. There are the following two method to start A/D conversion.

- Hardware starting
- Software starting

Fig. 5-8 A/D Converter Block Diagram



5.7 SERIAL INTERFACES

There are two on-chip clocked serial interfaces as follows.

- Serial Interface channel 0
- Serial Interface channel 1

Table 5-3 Type and Function of Serial Interface

Function	Serial Interface Channel 0	Serial Interface Channel 1
3-wire serial I/O mode	● (MSB/LSB-first switchable)	● (MSB/LSB-first switchable)
3-wire serial I/O mode with automatic data transmit /receive function	–	● (MSB/LSB-first switchable)
SBI (Serial Bus Interface) mode	● (MSB-first)	–
2-wire serial I/O mode● (MSB-first)	–	–

Fig. 5-9 Serial Interface Channel 0 Block Diagram

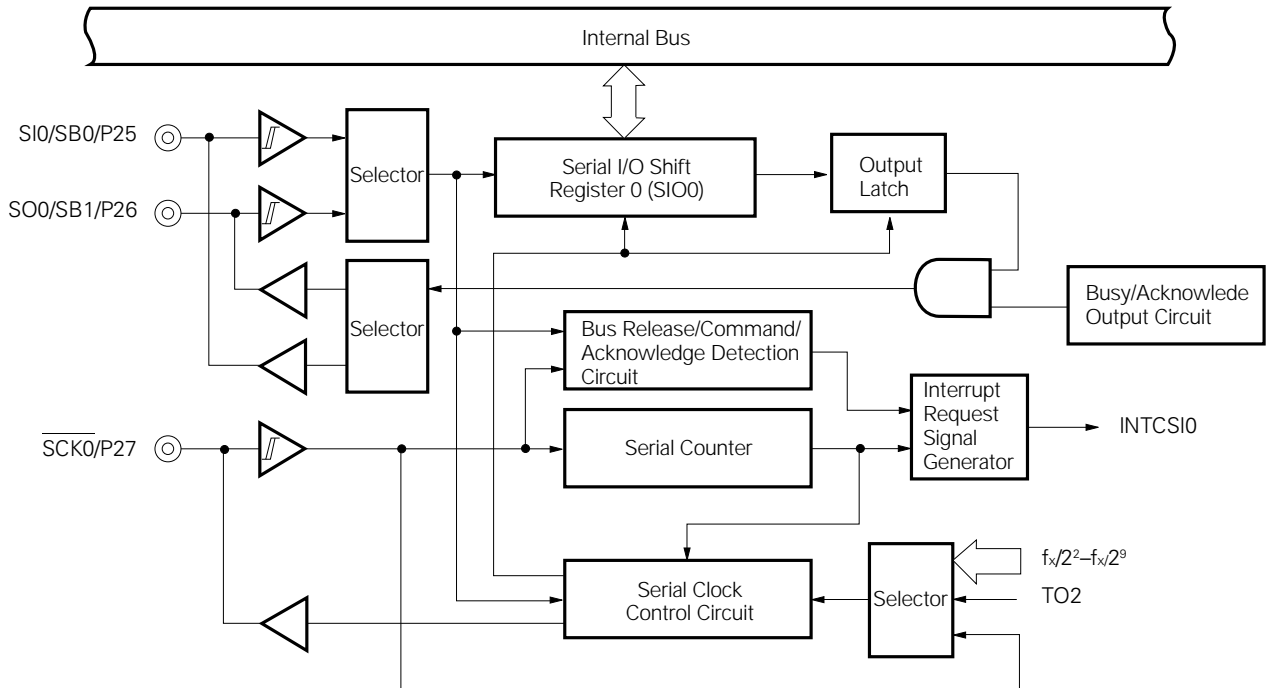
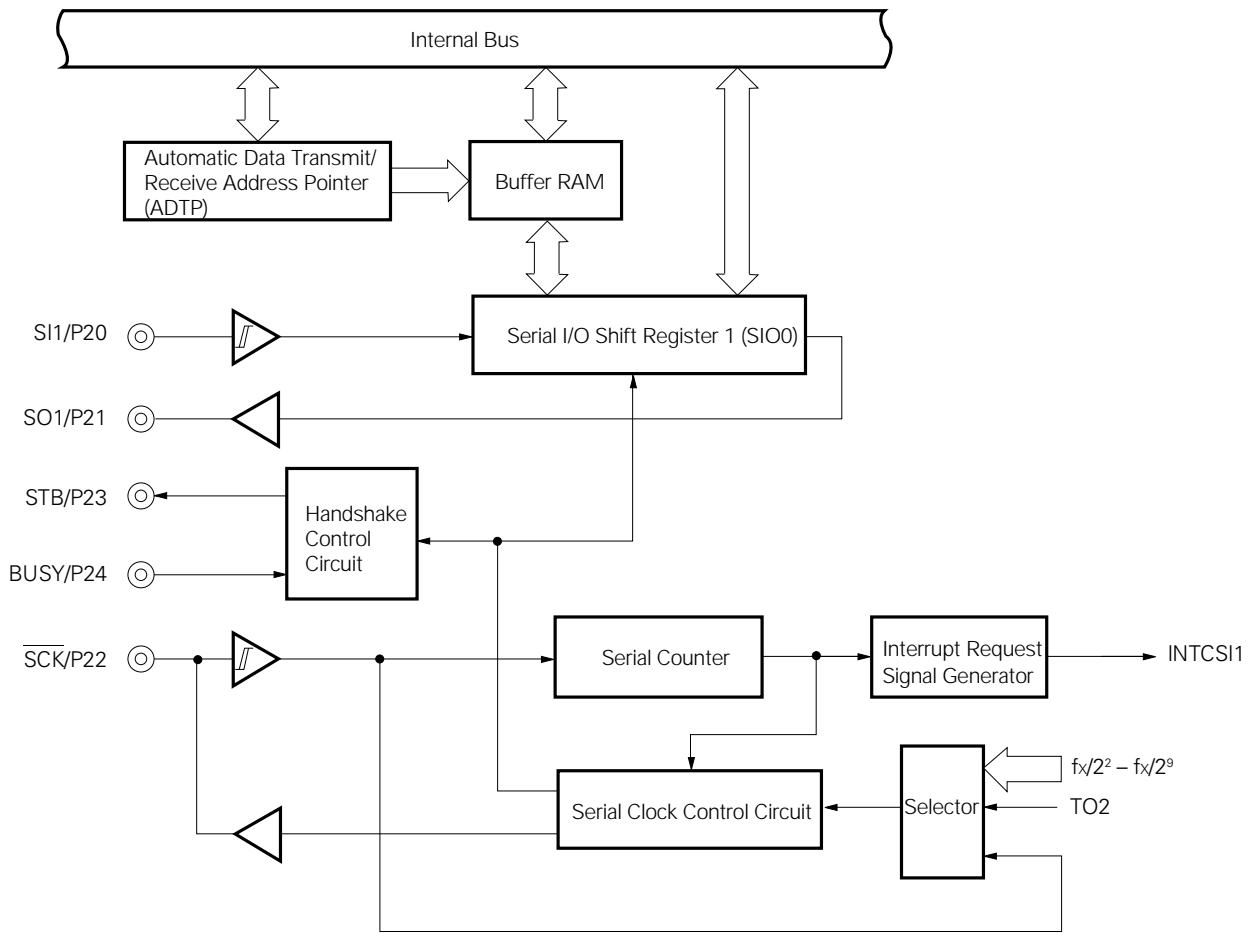


Fig. 5-10 Serial Interface Channel 1 Block Diagram



6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

6.1 INTERRUPT FUNCTIONS

There are the 14 interrupt functions of 3 different kind as shown below.

- Non-maskable interrupt : 1
- Maskable interrupt : 12
- Software interrupt : 1

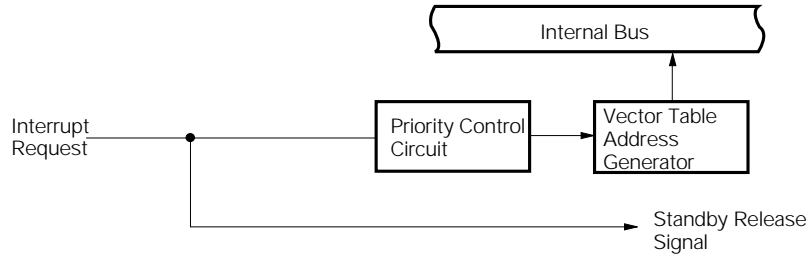
Table 6-1 Interrupt Source List

Interrupt Type	Default Priority*1	Interrupt Source		Internal /External	Vector Table Address	Basic*2 Configuratin Type		
		Name	Trigger					
Non-maskable	---	INTWDT	Watchdog timer overflow (with non-maskable interrupt selected)	Internal	0004H	A		
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer selected)			External	0006H 0008H 000AH 000CH	B
	1	INTP0	Pin input edge detection	Internal	000EH 0010H 0012H 0014H 0016H 0018H 001AH			C
	2	INTP1						D
	3	INTP2						
	4	INTP3						
	5	INTCSI0	Serial interface channel 0 transfer end					
	6	INTCSI1	Serial interface channel 1 transfer end					
	7	INTTM3	Reference time interval signal from watch timer					
	8	INTTM0	16 bit timer/event counter match signal generation					
	9	INTTM1	8-bit timer/event counter 1 match signal generation					
	10	INTTM2	8-bit timer/event counter 2 match signal generation					
11	INTAD	A/D converter conversion end						
Software	---	BRK	BRK instruction execution	Internal	003EH	E		

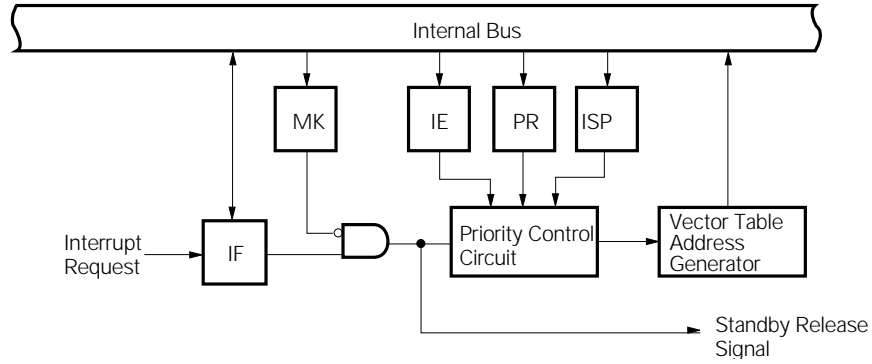
- * 1. The default pririty is the priority applicable when more than one maskable interrupt is generated. 0 is the highest priority and 11, the lowest.
2. Basic configuration types A to E correspond to A to E on the next page.

Fig. 6-1 Basic Interrupt Function Configuration (1/2)

(A) Internal Non-Maskable Interrupt



(B) Internal Maskable Interrupt



(C) External Maskable Interrupt (INTP0)

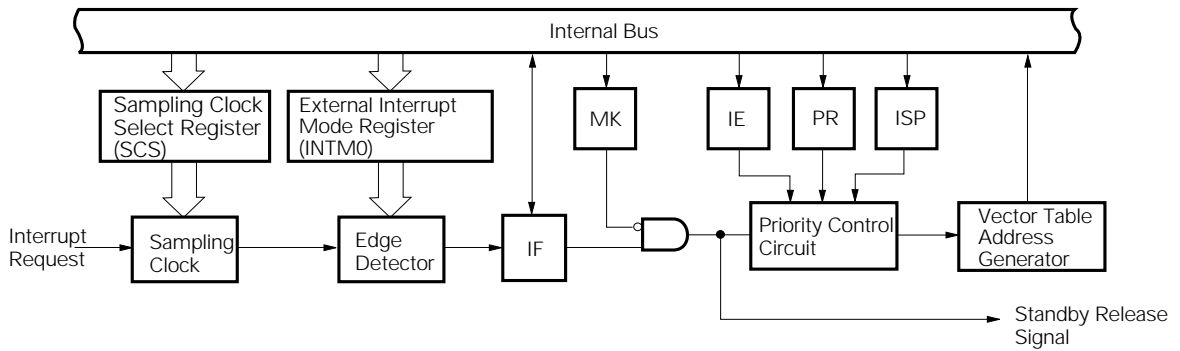
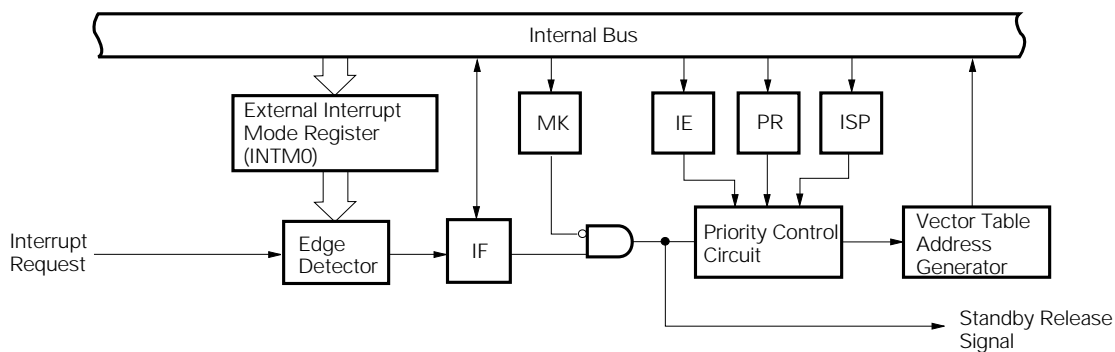
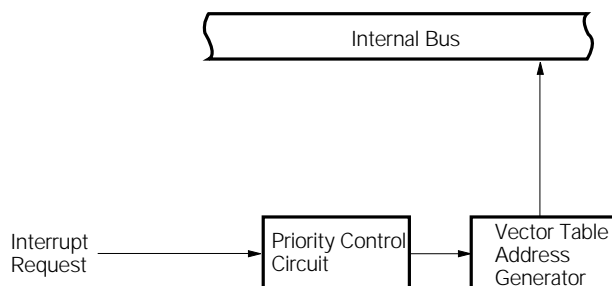


Fig. 6-1 Basic Interrupt Function Configuration (2/2)

(D) External Maskable Interrupt (Except INTP0)



(E) Software Interrupt



- Remarks**
1. IF : Interrupt request flag
 2. IE : Interrupt enable flag
 3. ISP : In-service priority flag
 4. MK : Interrupt mask flag
 5. PR : Priority specification flag

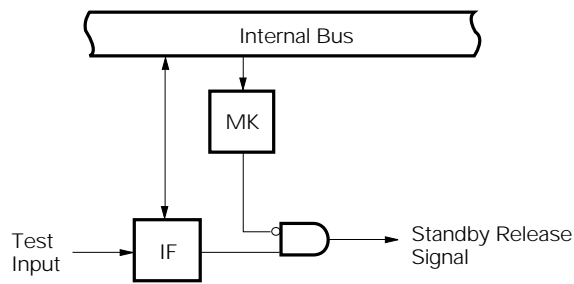
6.2 TEST FUNCTIONS

There are two test functions as shown in Table 6-2.

Table 6-2 Test Source List

Test Source		Internal/External
Name	Trigger	
INTWT	Watch timer overflow	Internal
INTPT4	Port 4 falling edge detection	External

Fig. 6-2 Test Function Basic Configuration



- Remarks
1. IF : Test input flag
 2. MK : Test mask flag

7. EXTERNAL DEVICE EXPANSION FUNCTIONS

The external device expansion function is used to connect external devices to areas other than the internal ROM, RAM and SFR.

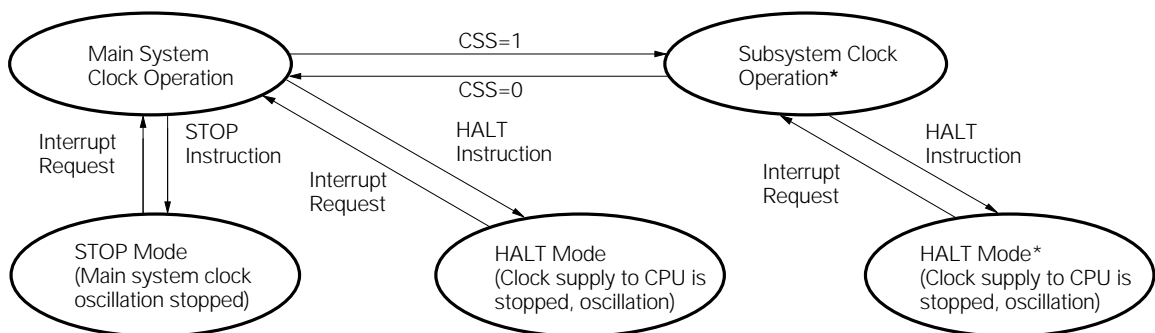
Ports 4 to 6 are used for connection with external devices.

8. STANDBY FUNCTIONS

There are the following two standby functions to reduce the current dissipation.

- **HALT mode** : The CPU operating clock is stopped. The average consumption current can be reduced by intermittent operation in combination with the normal operating mode.
- **STOP mode** : The main system clock oscillation is stopped. The whole operation by the main system clock is stopped, so that the system operates with ultra-low power consumption using only the subsystem clock.

Fig. 8-1 Standby Functions



* The power consumption can be reduced by stopping the main system clock. When the CPU is operating on the subsystem clock, set the MCC to stop the main system clock. The STOP instruction cannot be used.

Caution When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program by the program.

9. RESET FUNCTIONS

There are the following two reset methods.

- External reset input by \overline{RESET} pin.
- Internal reset by watchdog timer runaway time detection.

10. INSTRUCTION SET

(1) 8-Bit Instruction

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

2nd Operand 1st Operand	#byte	A	r*	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	\$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH XCH	MOV XCH XCH	MOV XCH XCH ADD ADDC ADD ADDC SUB SUBC SUB SUBC AND AND OR OR XOR XOR CMP	MOV XCH XCH ADD ADDC ADD ADDC SUB SUBC SUB SUBC AND AND OR OR XOR XOR CMP	MOV XCH XCH	MOV XCH XCH	MOV XCH XCH ADD ADDC ADD ADDC SUB SUBC SUB SUBC AND AND OR OR XOR XOR CMP			ROR ROL RORC ROLC	
r	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
r1											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL+B] [HL+C]		MOV											
X													MULU
C													DIVUW

* Except r=A

(2) 16-Bit Instruction

MOVW, XCHW ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

2nd Operand 1st Operand	#byte	AX	rp*	sfrp	saddrp	laddr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW*						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
laddr16		MOVW						
SP	MOVW	MOVW						

* Only when rp=BC, DE, HL.

(3) Bit Manipulation Instruction

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

2nd Operand 1st Operand	A.bit	sfr.bit	saddr.bit	PWS.bit	[HL].bit	CY	Saddr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call Instruction/Branch Instruction

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

2nd Operand 1st Operand	AX	!addr16	!addr11	[addr5]	\$addr16
Basic instruction	BR	CALL, BR	CALLF	CALLT	BR, BC, BNC, BZ, BNZ
Compound instruction					BT, BF, BTCLR, DBNZ

(5) Other Instruction

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltage	VDD			-0.3 to + 7.0	V
	AVDD			-0.3 to VDD + 0.3	V
	AVREF			-0.3 to VDD + 0.3	V
	AVSS			-0.3 to + 0.3	V
Input voltage	Vi1	P00 to P04, P10 to P17, P20 to P27, P30 to P37 P40 to P47, P50 to P57, P64 to P67, X1, X2, XT2		-0.3 to VDD + 0.3	V
	Vi2	P60 to P67	Open-drain	-0.3 to +16	V
Output voltage	Vo			-0.3 to VDD + 0.3	V
Analog input voltage	VAN	P10 to P17	Analog input pin	AVSS -0.3 to AVREF + 0.3	V
Output current high	IOH	1 pin		-10	mA
		P10 to P17, P20 to P27, P30 to P37 total		-15	mA
		P01 to P03, P40 to P47, P50 to P57, P60 to P67 total		-15	mA
Output current low	IOL*	1 pin	Peak value	30	mA
			Effective value	15	mA
		P40 to P47, P50 to P55 total	Peak value	100	mA
			Effective value	70	mA
		P01 to P03, P56, P57, P60 to P67 total	Peak value	100	mA
			Effective value	70	mA
		P01 to P03, P64 to P67 total	Peak value	50	mA
			Effective value	20	mA
		P10 to P17, P20 to P27, P30 to P37 total	Peak value	50	mA
			Effective value	20	mA
Operating temperature	Topt			-40 to +85	°C
Storage temperature	Tstg			-65 to +150	°C

* Effective value should be calculated as follows: [Effective value] = [Peak value] × √duty

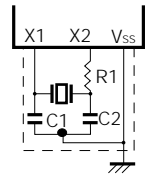
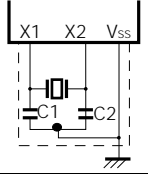
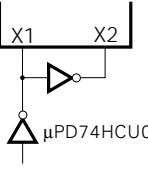
Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Capacitance ($T_a = 25\text{ }^\circ\text{C}$, $V_{DD} = V_{SS} = 0\text{ V}$)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	$f=1\text{ MHz}$ Unmeasured pins returned to 0 V				15	pF
I/O capacitance	C_{IO}	$f=1\text{ MHz}$ Unmeasured pins returned to 0 V	P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67			15	pF
			P60 to P63			20	pF

Remarks The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

Main System Clock Oscillation Circuit Characteristics ($T_a = -40\text{ to }+85\text{ }^\circ\text{C}$, $V_{DD} = 2.7\text{ to }6.0\text{ V}$)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (fx) *1	$V_{DD} = \text{Oscillator voltage range}$	1		10	MHz
		Oscillation stabilization time *2	After V_{DD} reaches oscillator voltage range MIN.			4	ms
Crystal resonator		Oscillator frequency (fx) *1		1	8.38	10	MHz
		Oscillation stabilization time *2	$V_{DD} = 4.5\text{ to }6.0\text{ V}$			10 30	ms
External clock		X1 input frequency (fx) *1		1.0		10.0	MHz
		X1 input high/low level width (txH , txL)		42.5		500	ns

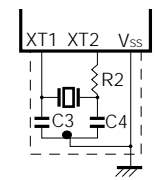
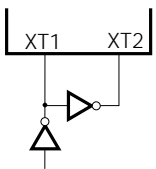
- * 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristics" for instruction execution time.
- 2. Time required to stabilize oscillation after reset or STOP mode release.

Caution 1. When using the main system clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Wiring should be as short as possible.
- Wiring should not cross other signal lines.
- Wiring should not be placed close to a varying high current.
- The potential of the oscillator capacitor ground should be the same as V_{SS} .
- Do not ground wiring to a ground pattern in which a high current flows.
- Do not fetch a signal from the oscillator.

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

Subsystem Clock Oscillation Circuit Characteristics (Ta = -40 to +85 °C, VDD = 2.7 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillator frequency (f _{XT1}) *1		32	32.768	35	kHz
		Oscillation stabilization time *2	VDD = 4.5 to 6.0 V		1.2	2	s
External clock		XT1 input frequency (f _{XT1}) *1		32		100	kHz
		XT1 input high/low level width (t _{XTH} , t _{XTL})		5		15	μs

- * 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristics" for instruction execution time.
- 2. Time required to stabilize oscillation after VDD reaches oscillator voltage MIN.

Caution 1. When using the subsystem clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Wiring should be as short as possible.
- Wiring should not cross other signal lines.
- Wiring should not be placed close to a varying high current.
- The potential of the oscillator capacitor ground should be the same as VSS.
- Do not ground wiring to a ground pattern in which a high current flows.
- Do not fetch a signal from the oscillator.

2. The subsystem clock oscillation circuit is a circuit with a low amplification level, more prone to misoperation due to noise than the main system clock.

Particular care is therefore required with the wiring method when the subsystem clock is used.

Recommended Oscillation Circuit Constant

Main system clock: Ceramic resonator (Ta = -40 to +85 °C)

μPD78011B, 78012B

Manufacture	Product Name	Frequency (MHz)	Recommended Circuit Constant			Oscillator Voltage Range	
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)
Murata Mfg. Co., Ltd.	CSB1000J	1.00	100	100	6.8	2.9	6.0
	CSBxxxxJ	1.01 to 1.25	100	100	4.7	2.7	6.0
	CSAx. xxMK	1.26 to 1.79	100	100	0	2.7	6.0
	CSAx. xxMG	1.80 to 2.44	100	100	0	2.7	6.0
	CSTx. xxMG		Built-in	Built-in	0	2.7	6.0
	CSAx. xxMG	2.45 to 4.18	30	30	0	2.7	6.0
	CSTx. xxMGW		Built-in	Built-in	0	2.7	6.0
	CSAx. xxMG	4.19 to 6.00	30	30	0	2.7	6.0
	CSTx. xxMGW		Built-in	Built-in	0	2.7	6.0
	CSAx. xxMT	6.01 to 10.0	30	30	0	2.9	6.0
	CSTx. xxMTW		Built-in	Built-in	0	2.9	6.0
Kyocera	KBR-4.19MWS	4.19	-	-	-	2.7	6.0
	KBR-4.19MKS						
	KBR-4.19MSA	4.19	33	33	-	2.7	6.0
	PBRC4.19A						
	KBR-10.0M	10.0	33	33	-	2.8	6.0
	KBR-1000F	1.00	100	100	2.2	2.7	6.0
	KBR-1000Y						

μPD78013, 78014

Manufacture	Product Name	Frequency (MHz)	Recommended Circuit Constant			Oscillator Voltage Range	
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)
Murata Mfg. Co., Ltd.	CSB1000J	1.00	100	100	6.8	2.7	6.0
	CSBxxxxJ	1.01 to 1.25	100	100	4.7	2.7	6.0
	CSAx. xxMK	1.26 to 1.79	100	100	0	2.7	6.0
	CSAx. xxMG	1.80 to 2.44	100	100	0	2.7	6.0
	CSTx. xxMG		Built-in	Built-in	0	2.7	6.0
	CSAx. xxMG	2.45 to 4.18	30	30	0	2.7	6.0
	CSTx. xxMGW		Built-in	Built-in	0	2.7	6.0
	CSAx. xxMG	4.19 to 6.00	30	30	0	2.7	6.0
	CSTx. xxMGW		Built-in	Built-in	0	2.7	6.0
	CSAx. xxMT	6.01 to 10.0	30	30	0	2.7	6.0
	CSTx. xxMTW		Built-in	Built-in	0	2.7	6.0

Remarks xxxx, x. xxx, x. xx indicate frequency.

Subsystem clock: Cristal resonator (Ta = -40 to + 60 °C)

μPD78011B, 78012B

Manufacture	Products	Frequency (MHz)	Recommended Circuit Constant			Oscillator Voltage Range	
			C3 (pF)	C4 (pF)	R2 (kΩ)	MIN. (V)	MAX. (V)
Daishinku	DT-38 (1TA632 E00, load capacitance 6.3 pF)	32.768	8	8	100	2.7	6.0

μPD78013, 78014

Manufacture	Product Name	Frequency (MHz)	Recommended Circuit Constant			Oscillator Voltage Range	
			C3 (pF)	C4 (pF)	R2 (kΩ)	MIN. (V)	MAX. (V)
Daishinku	DT-38 (1TA632 E00, load capacitance 6.3 pF)	32.768	12	12	100	2.7	6.0

DC Characteristics (Ta = -40 to +85 °C, VDD = 2.7 to 6.0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage high	VIH1	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67	0.7 VDD		VDD	V	
	VIH2	P00 to P03, P20, P22, P24 to P27, P33, P34, RESET	0.8 VDD		VDD	V	
	VIH3	P60 to P63	Open-drain	0.7 VDD	15	V	
	VIH4	X1, X2		VDD-0.5	VDD	V	
	VIH5	XT1/P04, XT2	VDD = 4.5 to 6.0 V	VDD-0.5		VDD	V
			VDD-0.3		VDD	V	
Input voltage low	VIL1	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67	0		0.3 VDD	V	
	VIL2	P00 to P03, P20, P22, P24 to P27, P33, P34, RESET	0		0.2 VDD	V	
	VIL3	P60 to P63	VDD = 4.5 to 6.0 V	0		0.3 VDD	V
				0		0.2 VDD	V
	VIL4	X1, X2		0		0.4	V
VIL5	XT1/P04, XT2	VDD = 4.5 to 6.0 V	0		0.4	V	
			0		0.3	V	
Output voltage high	VOH1	VDD = 4.5 to 6.0 V, IOH = -1 mA	VDD-1.0			V	
		IOH = -100 μA	VDD-0.5			V	
Output voltage low	VOL1	P50 to P57, P60 to P63	VDD = 4.5 to 6.0 V, IOL = 15 mA	0.4	2.0	V	
		P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67	VDD = 4.5 to 6.0 V, IOL = 1.6 mA		0.4	V	
	VOL2	SB0, SB1, SCK0	VDD = 4.5 to 6.0 V, open-drain pulled-up (R = 1 KΩ)		0.2 VDD	V	
	VOL3	IOL = 400 μA			0.5	V	
Input leakage current high	IIH1	VIN = VDD	P00 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67 RESET		3	μA	
			X1, X2, XT1/P04, XT2		20	μA	
	IIH2	VIN = 15 V	P60 to P63		80	μA	
Input leakage current low	IIL1	VIN = 0 V	P00 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67 RESET		-3	μA	
			X1, X2, XT1/P04, XT2		-20	μA	
			P60 to P63	*1		-200	μA
	Other than above			-3*2	μA		

- * 1. When memory expansion mode is used by the memory expansion mode register (MM) with no on-chip pull-up resistor by mask option.
 2. When pull-up resistors are not used (specified by mask option), the low-level input leakage current increases with -200 μA (MAX.) under either of the following conditions.

- ① When the external device expansion function is used and a low level is input to the pin.
 ② During the 3-clock period when a read instruction is executed on port 6 (P6) and the port mode register (PM6).

Remarks The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

DC Characteristics (Ta = -40 to +85 °C, VDD = 2.7 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Output leakage current high	I _{LOH1}	V _{OUT} = V _{DD}				3	μA
Output leakage current low	I _{LOL}	V _{OUT} = 0 V				-3	μA
Mask option pull-up resistor	R1	V _{IN} = 0 V, P60 to P63		20	40	90	kΩ
Software pull-up resistor	R2	V _{IN} = 0 V, P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67	4.5 V ≤ V _{DD} ≤ 6.0 V	15	40	90	kΩ
			2.7 V ≤ V _{DD} < 4.5 V	20		500	kΩ
Power supply current *5	IDD1	8.38 MHz Crystal oscillation operating mode	V _{DD} = 5.0 V ± 10 % *3		7.5	22.5	mA
			V _{DD} = 3.0 V ± 10 % *4		0.8	2.4	mA
	IDD2	8.38 MHz Crystal oscillation HALT mode	V _{DD} = 5.0 V ± 10 %		1.4	4.2	mA
			V _{DD} = 3.0 V ± 10 %		550	1650	μA
	IDD3	32.768 kHz Crystal oscillation operating mode	V _{DD} = 5.0 V ± 10 %		60	120	μA
			V _{DD} = 3.0 V ± 10 %		35	70	μA
	IDD4	32.768 kHz Crystal oscillation HALT mode	V _{DD} = 5.0 V ± 10 %		25	50	μA
			V _{DD} = 3.0 V ± 10 %		5	10	μA
	IDD5	XT1 = 0 V STOP mode When feedback resistor is used	V _{DD} = 5.0 V ± 10 %		1	20	μA
			V _{DD} = 3.0 V ± 10 %		0.5	10	μA
	IDD6	XT1 = 0 V STOP mode When feedback resistor is unused	V _{DD} = 5.0 V ± 10 %		0.1	20	μA
			V _{DD} = 3.0 V ± 10 %		0.05	10	μA

- * 3. Operating in high-speed mode (when set the processor clock control register to 00H).
- 4. Operating in low-speed mode (when set the processor clock control register to 04H).
- 5. AV_{REF} current and port current are excluded.

Remarks The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

AC Characteristics

(1) Basic Operation (Ta = -40 to +85 °C, VDD = 2.7 to 6.0 V)

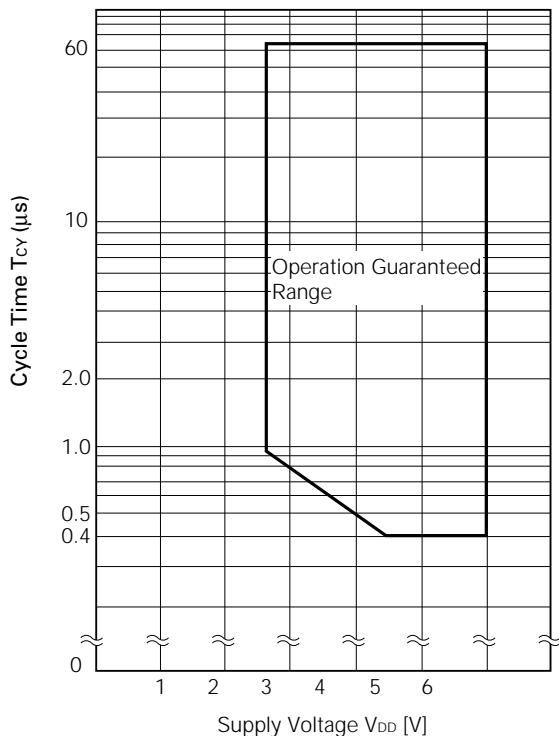
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Cycle time (Min. instruction execution time)	TCY	Operating on main system clock	VDD=4.5 to 6.0 V	0.4		64	μs
				0.96		64	μs
		Operating on subsystem clock	40	122	125	μs	
TI input frequency	fTI	VDD = 4.5 to 6.0 V	0		4	MHz	
			0		275	kHz	
TI input high/ low-level width	tTIH	VDD = 4.5 to 6.0 V	100			ns	
	tTIL		1.8			μs	
Interrupt input high/low-level width	tINTH	INTP0	8/fsam*			μs	
	tINTL	INTP1 to INTP3	10			μs	
		KR0 to KR7	10			μs	
RESET low level width	tRSL		10			μs	

* In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register, selection of fsam is possible between $f_x/2^{N+1}$, $f_x/64$ and $f_x/128$ (when N= 0 to 4).

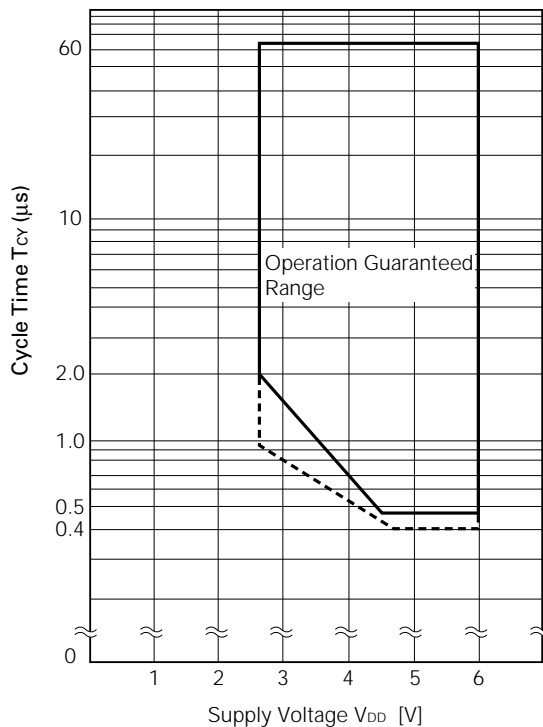
μPD78011B, 78012B, 78013, 78014

μPD78P014 (Reference)

T_{CY} vs V_{DD} (At main system clock operation)



T_{CY} vs V_{DD} (At main system clock operation)



Remarks - - - - - indicates Ta = -40 to +40 °C
 - - - - - indicates Ta = -40 to +80 °C

Caution The operation guaranteed range of the μPD78011B, 78012B, 78013 and 78014 differs from that of the μPD78P014.

(2) Read/Write Operation (Ta = -40 to +85 °C, VDD = 2.7 to 6.0 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	tASTH		0.5tcY		ns
Address setup time	tADS		0.5tcY-30		ns
Address hold time	tADH	Load resistor ∞ 5 kΩ	10		ns
Data input time from address	tADD1			(2+2n)tcY-50	ns
	tADD2		5	(3+2n)tcY-100	ns
Data input time from $\overline{RD}\downarrow$	trDD1			(1+2n)tcY-25	ns
	trDD2			(2.5+2n)tcY-100	ns
Read data hold time	trDH		0		ns
\overline{RD} low-level width	trDL1		(1.5+2n)tcY-20		ns
	trDL2		(2.5+2n)tcY-20		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	trDWT1			0.5tcY	ns
	trDWT2			1.5tcY	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	tWRWT			0.5tcY	ns
\overline{WAIT} low-level width	tWTL		(0.5+2n)tcY +10	(2+2n)tcY	ns
Write data setup time	twDS		100		ns
Write data hold time	twDH		5		ns
\overline{WR} low-level width	twRL1		(2.5+2n)tcY -20		ns
$\overline{RD}\downarrow$ delay time from $\overline{ASTB}\downarrow$	tASTRD		0.5tcY-30		ns
$\overline{WR}\downarrow$ delay time from $\overline{ASTB}\downarrow$	tASTWR		1.5tcY -30		ns
ASTB∞ delay time from $\overline{RD}\infty$ in external fetch	trDAST		tcY-10	tcY+40	ns
Address hold time from $\overline{RD}\infty$ in external fetch	trDADH		tcY	tcY+50	ns
Write data output time from $\overline{RD}\infty$	trDWD		10		ns
$\overline{WR}\downarrow$ delay time from write data	tWDWR	VDD = 4.5 to 6.0 V	0.5tcY-120	0.5tcY	ns
			0.5tcY-170	0.5tcY	ns
Address hold time from $\overline{WR}\infty$	tWRADH	VDD = 4.5 to 6.0 V	tcY	tcY+60	ns
			tcY	tcY+100	ns
$\overline{RD}\infty$ delay time from $\overline{WAIT}\infty$	twTRD		0.5tcY	2.5tcY+80	ns
$\overline{WR}\infty$ delay time from $\overline{WAIT}\infty$	tWTWR		0.5tcY	2.5tcY+80	ns

- Remarks**
1. tcY = TCY/4
 2. n indicates number of waits.
 3. CL = 100 pF (CL indicates load capacitance of P40/AD0 to P47/AD7, P50/A8 to P57/A15, P64/ \overline{RD} , P65/ \overline{WR} , P66/ \overline{WAIT} , P67/ASTB pins).

(c) SBI mode ($\overline{\text{SCK}}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	t _{KCY3}	V _{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{\text{SCK}}$ high/low-level width	t _{KH3}	V _{DD} = 4.5 to 6.0 V		t _{KCY3} /2-50			ns
	t _{KL3}			t _{KCY3} /2-150			ns
SB0, SB1 setup time (to $\overline{\text{SCK}}_{\infty}$)	t _{SIK3}	V _{DD} = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{\text{SCK}}_{\infty}$)	t _{KSI3}			t _{KCY3} /2			ns
SB0, SB1 output delay time from $\overline{\text{SCK}}_{\downarrow}$	t _{KSO3}	R = 1 kΩ , C = 100 pF*	V _{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
SB0, SB1 \downarrow from $\overline{\text{SCK}}_{\infty}$	t _{KSB}			t _{KCY3}			ns
$\overline{\text{SCK}}_{\downarrow}$ from SB0, SB1 \downarrow	t _{SBK}			t _{KCY3}			ns
SB0, SB1 high-level width	t _{SBH}			t _{KCY3}			ns
SB0, SB1 low-level width	t _{SBL}			t _{KCY3}			ns

* R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

(d) SBI mode ($\overline{\text{SCK}}$... External clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	tkCY4	VDD = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{\text{SCK}}$ high/low-level width	tkH4	VDD = 4.5 to 6.0 V		400			ns
	tkL4			1600			ns
SB0, SB1 setup time (to $\overline{\text{SCK}}_{\infty}$)	tSIK4	VDD = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{\text{SCK}}_{\infty}$)	tkSI4			tkCY4/2			ns
SB0, SB1 output delay time from $\overline{\text{SCK}}\downarrow$	tkSO4	R = 1 kΩ , C = 100 pF*	VDD = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0, SB1 \downarrow from $\overline{\text{SCK}}_{\infty}$	tkSB			tkCY4			ns
$\overline{\text{SCK}}\downarrow$ from SB0, SB1 \downarrow	tsBK			tkCY4			ns
SB0, SB1 high-level width	tsBH			tkCY4			ns
SB0, SB1 low-level width	tsBL			tkCY4			ns
★ $\overline{\text{SCK}}$ rise, fall time	tr4 tf4	When external device expansion function is used				160	ns
		When external device expansion function is used		When 16-bit timer output function is used		700	ns
		When external device expansion function is not used		When 16-bit timer output function is not used		1000	ns

* R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

(e) 2-wire serial I/O mode ($\overline{\text{SCK}}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	tkCY5	VDD = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{\text{SCK}}$ high-level width	tkH5	R = 1 kΩ, C = 100 pF*		tkCY5/2-50			ns
$\overline{\text{SCK}}$ low-level width	tkL5			tkCY5/2-50			ns
SB0, SB1 setup time (to $\overline{\text{SCK}}_{\infty}$)	tSIK5			300			ns
SB0, SB1 hold time (from $\overline{\text{SCK}}_{\infty}$)	tkSI5			600			ns
SB0, SB1 output delay time from $\overline{\text{SCK}}\downarrow$	tkSO5	R = 1 kΩ, C = 100 pF*	VDD = 4.5 to 6.0 V	0		250	ns
				0		1000	ns

* R and C are the load resistors and load capacitance of the $\overline{\text{SCK}}$ 0, SB0 and SB1 output line.

(f) 2-wire serial I/O mode ($\overline{\text{SCK}}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	tKCY6	VDD = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{\text{SCK}}$ high-level width	tKH6			650			ns
$\overline{\text{SCK}}$ low-level width	tKL6			800			ns
SB0, SB1 setup time (to $\overline{\text{SCK}}_{\infty}$)	tSIK6			100			ns
SB0, SB1 hold time (from $\overline{\text{SCK}}_{\infty}$)	tKSI6			tKCY6/2			ns
SB0, SB1 output delay time from $\overline{\text{SCK}}_{\downarrow}$	tKSO6	R = 1 kΩ, C = 100 pF*	VDD = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
$\overline{\text{SCK}}$ rise, fall time	tR6 tF6	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

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* R and C are the load resistors and load capacitance of the $\overline{\text{SCK}}_0$, SB0 and SB1 output line.

(g) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{\text{SCK}}$...Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	UNIT
$\overline{\text{SCK}}$ cycle time	tKCY7	VDD = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{\text{SCK}}$ high/low-level width	tKH7	VDD = 4.5 to 6.0 V		tKCY7/2-50			ns
	tKL7			tKCY7/2-150			ns
SI setup time (to $\overline{\text{SCK}}_{\infty}$)	tSIK7			100			ns
SI hold time (from $\overline{\text{SCK}}_{\infty}$)	tKSI7			400			ns
SO output delay time from $\overline{\text{SCK}}_{\downarrow}$	tKS07	C = 100 pF*	VDD = 4.5 to 6.0 V			300	ns
						1000	ns
STB $_{\infty}$ from $\overline{\text{SCK}}_{\infty}$	tSBD			400		tKCY7	ns
Strobe signal high-level width	tSBW			tKCY7-30		tKCY7+30	ns
Busy signal setup time (to busy signal detection timing)	tBYS			100			ns
Busy signal hold time (from busy signal detection timing)	tBYH			100			ns
$\overline{\text{SCK}}_{\downarrow}$ from busy inactive	tSPS					2tKCY7	ns

* C is the load capacitance of the SO output line.

(h) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{\text{SCK}}$...External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	UNIT
$\overline{\text{SCK}}$ cycle time	tkCY8	VDD = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{\text{SCK}}$ high/low-level width	tkH8	VDD = 4.5 to 6.0 V		400			ns
	tkL8			1600			ns
SI setup time (to $\overline{\text{SCK}}_{\infty}$)	tSIK8			100			ns
SI hold time (from $\overline{\text{SCK}}_{\infty}$)	tKSI8			400			ns
SO output delay time from $\overline{\text{SCK}}_{\downarrow}$	tkSO8	C = 100 pF*	VDD = 4.5 to 6.0 V			300	ns
						1000	ns
$\overline{\text{SCK}}$ rise, fall time	tr8	When external device expansion function function is used				160	ns
	tf8	When external device expansion function is not used				1000	ns

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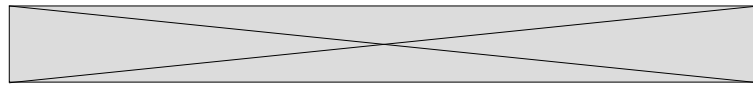
* C is the load capacitance of the SO output line.

(4) A/D converter characteristics ($T_a = -40$ to $+85$ °C, $AV_{DD} = V_{DD} = 2.7$ to 6.0 V, $AV_{SS} = V_{SS} = 0$ V)

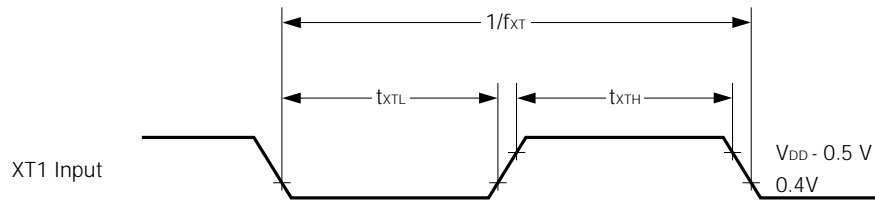
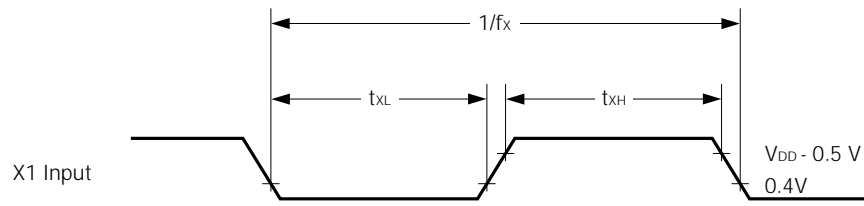
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error*					0.6	%
Conversion time	tCONV		19.1		200	μs
Sampling time	tsAMP		24/fx			μs
Analog input voltage	VIAN		AVSS		AVREF	V
Reference voltage	AVREF		2.7		AVDD	V
AVREF current	AIREF			0.5	1.5	mA

* Overall error excluding quantization error ($\pm 1/2$ LSB). It is indicated as a ratio to the full-scale value.

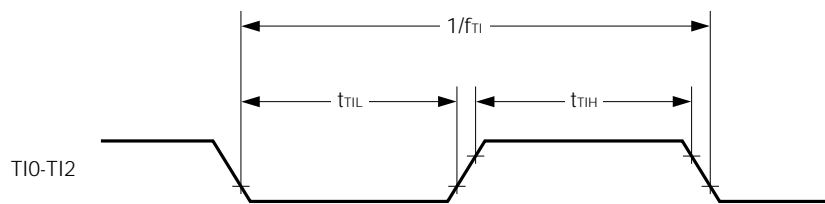
AC Timing Test Point (Excluding X1, XT1 Input)



Clock Timing

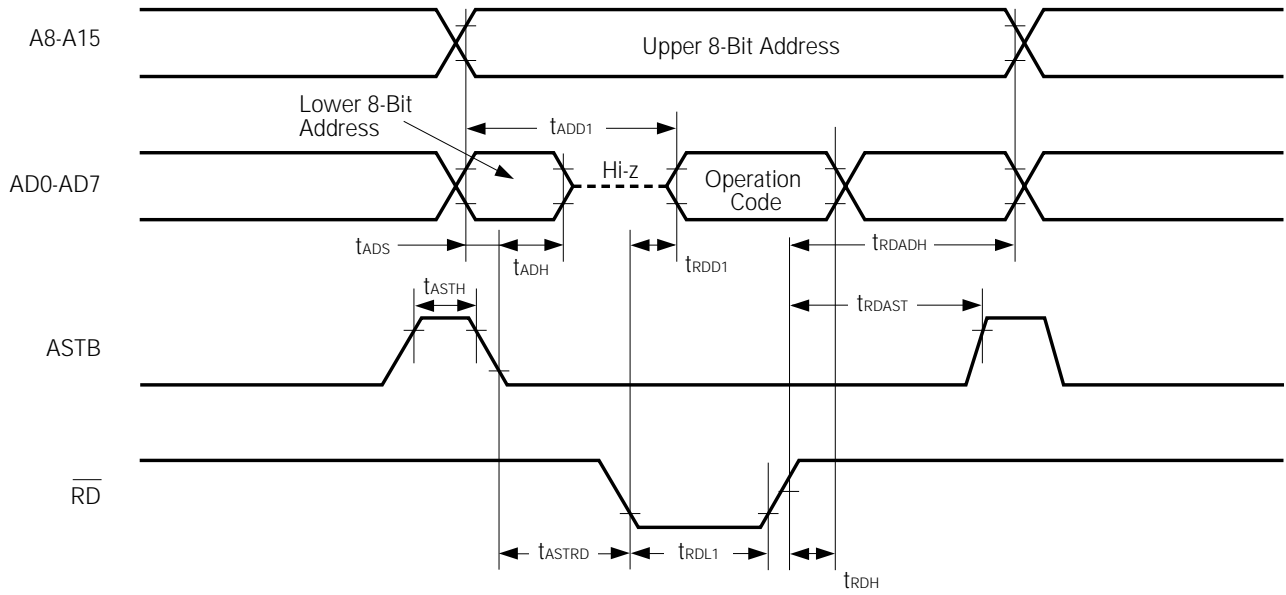


TI Timing

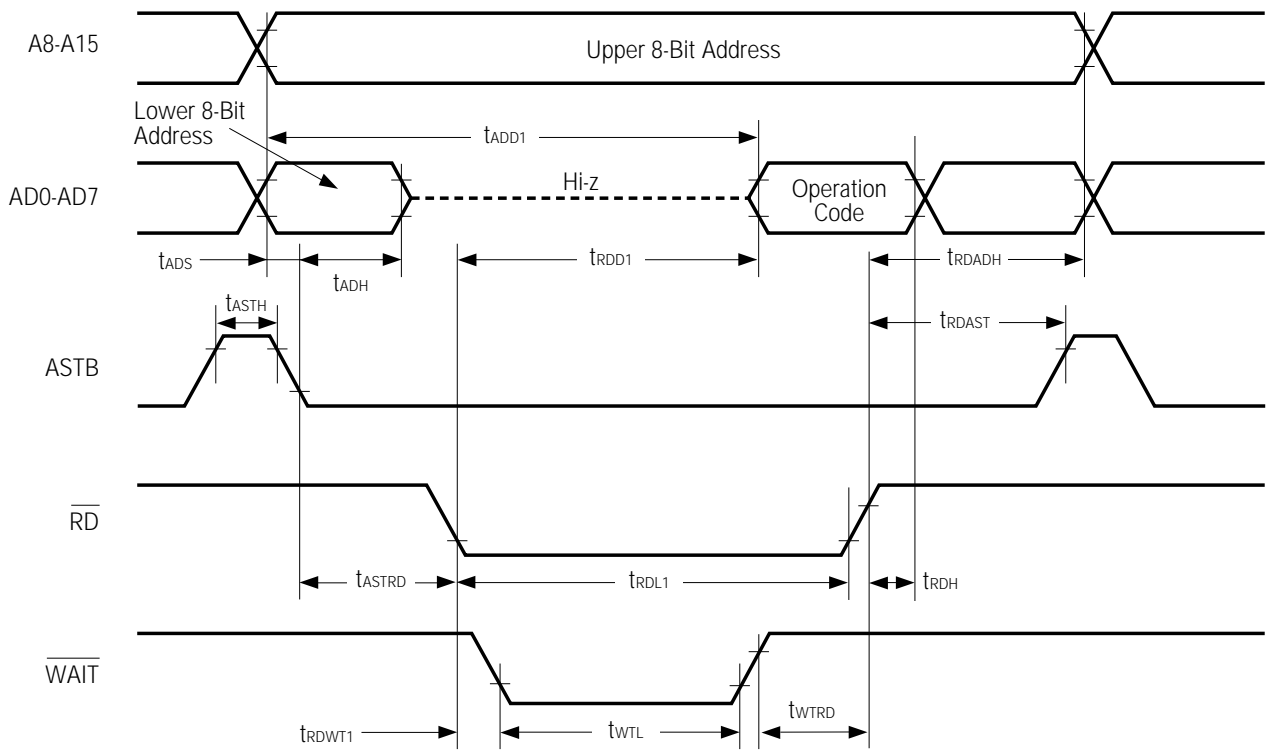


Read/Write Operation

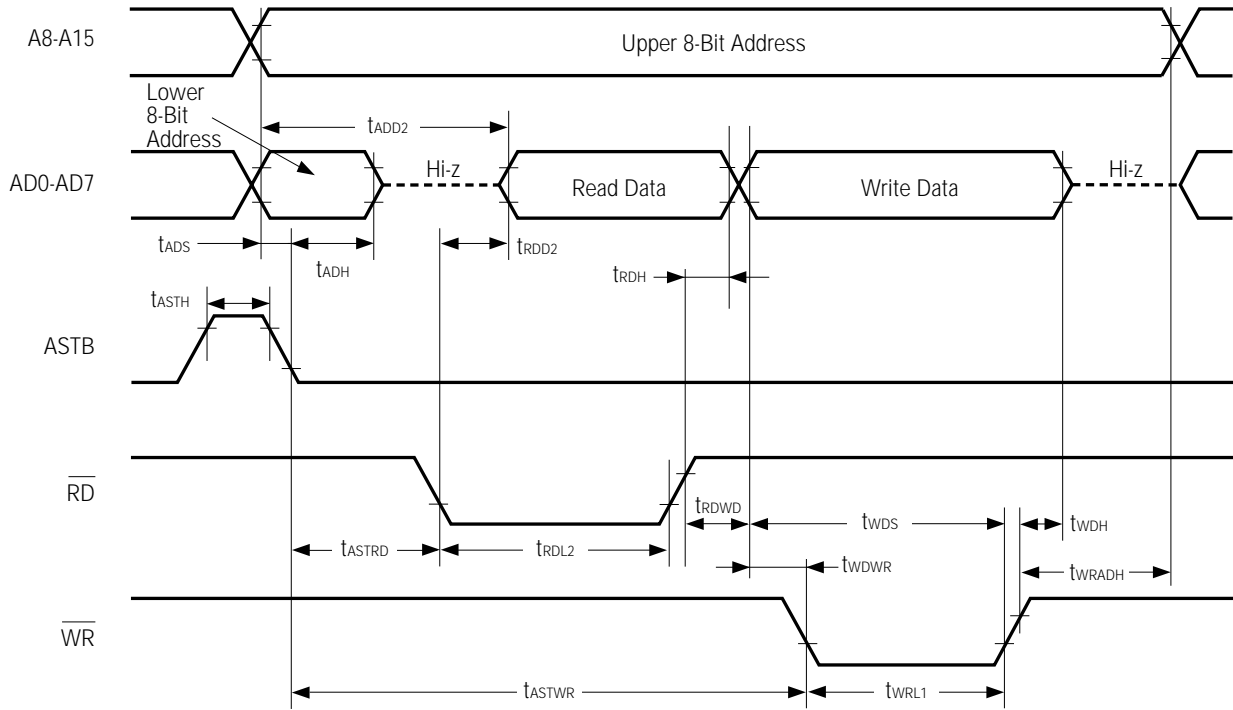
External fetch (No wait):



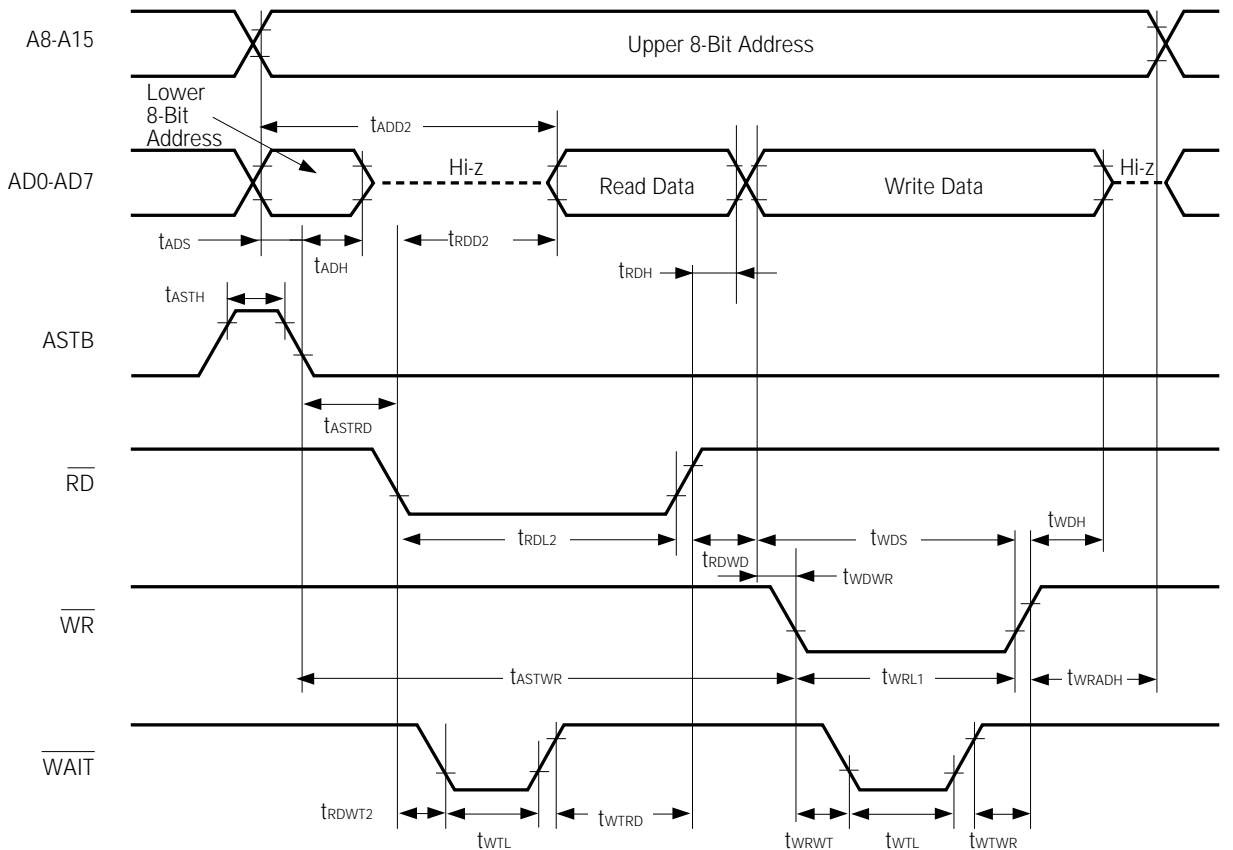
External fetch (Wait insertion):



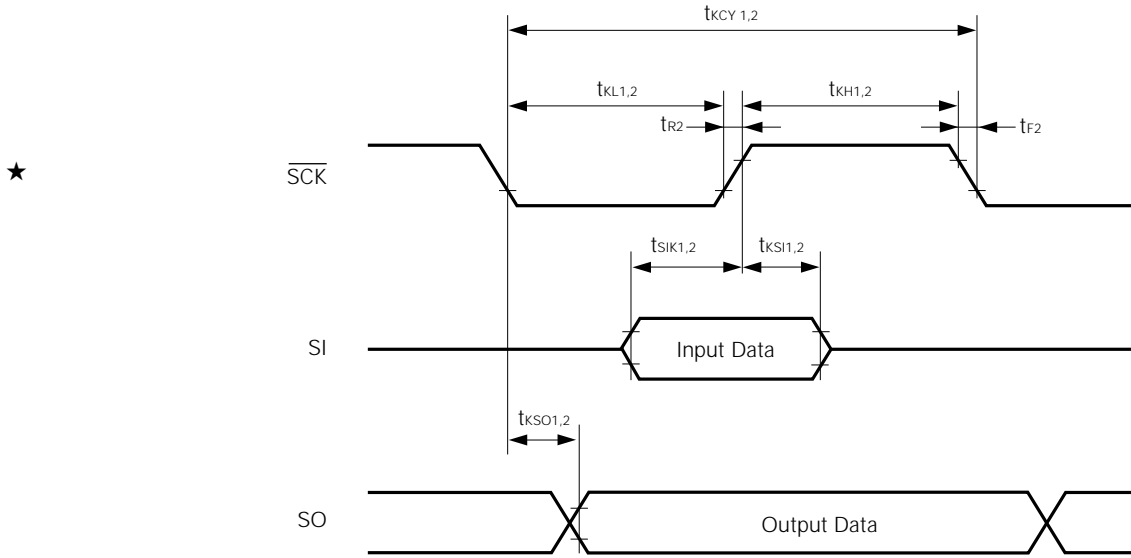
External data access (No wait):



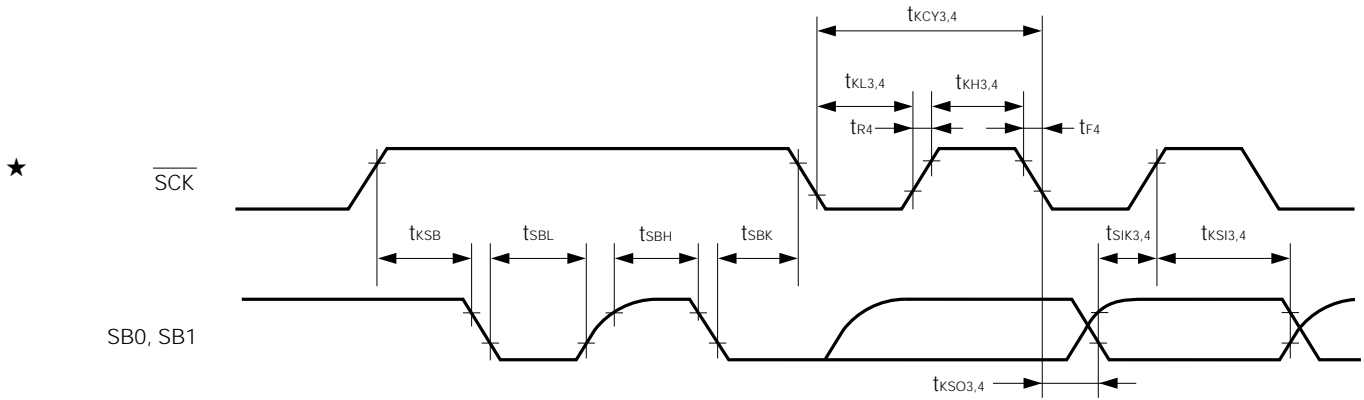
External data access (Wait insertion):



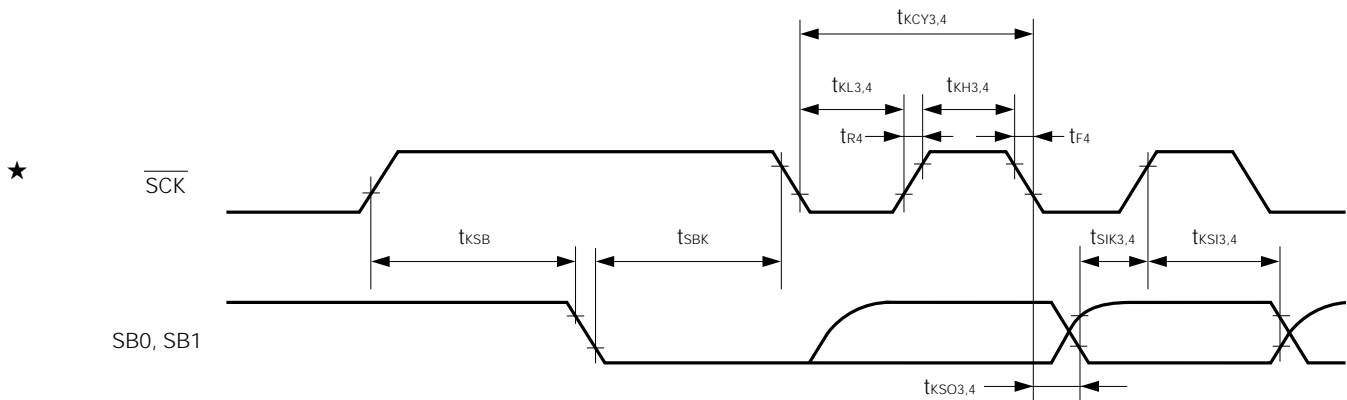
Serial Transfer Timing
3-wire serial I/O mode:



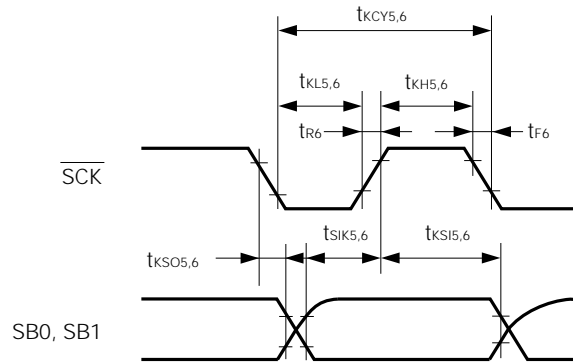
SBI mode (Bus release signal transfer):



SBI Mode (command signal transfer):

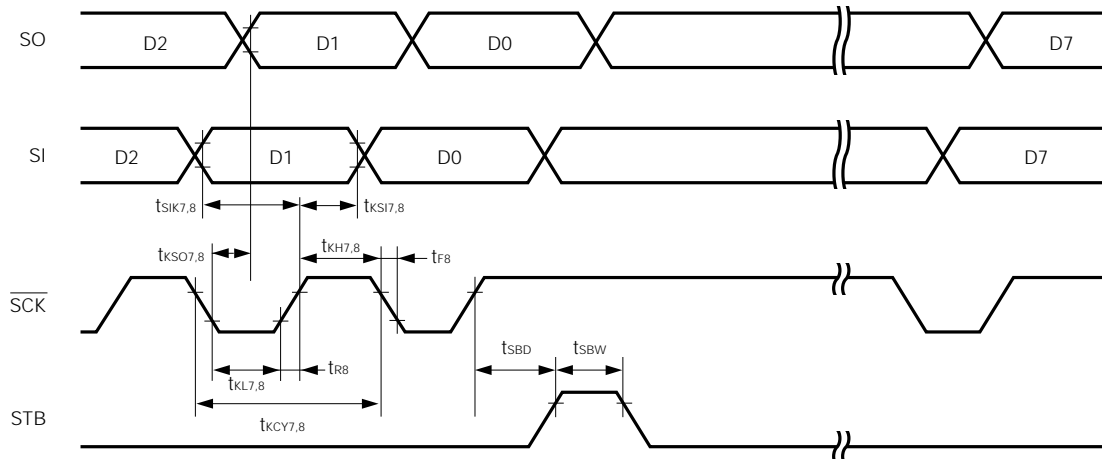


2-wire serial I/O mode:



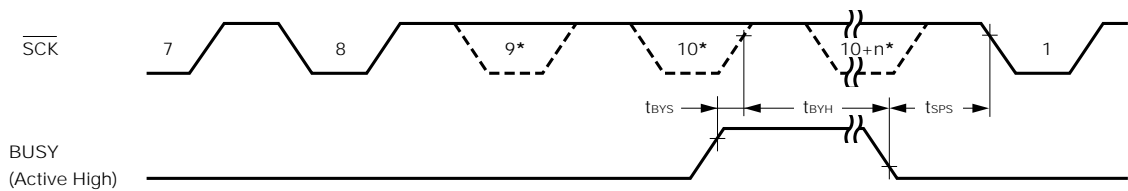
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3-wire serial I/O mode with automatic transmit/receive function:



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3-wire serial I/O mode with automatic transmit/receive function (busy processing):



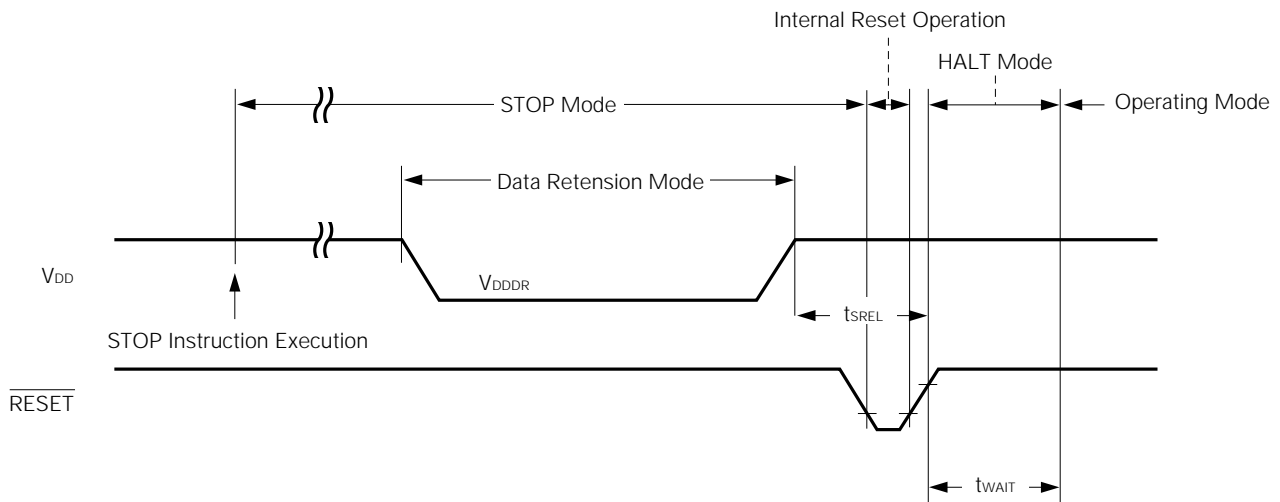
* The signal is not actually driven low here; it is shown as such to indicate the timing.

Data Memory Stop Mode Low Supply Voltage Data Retention Characteristics (Ta = -40 to +85 °C)

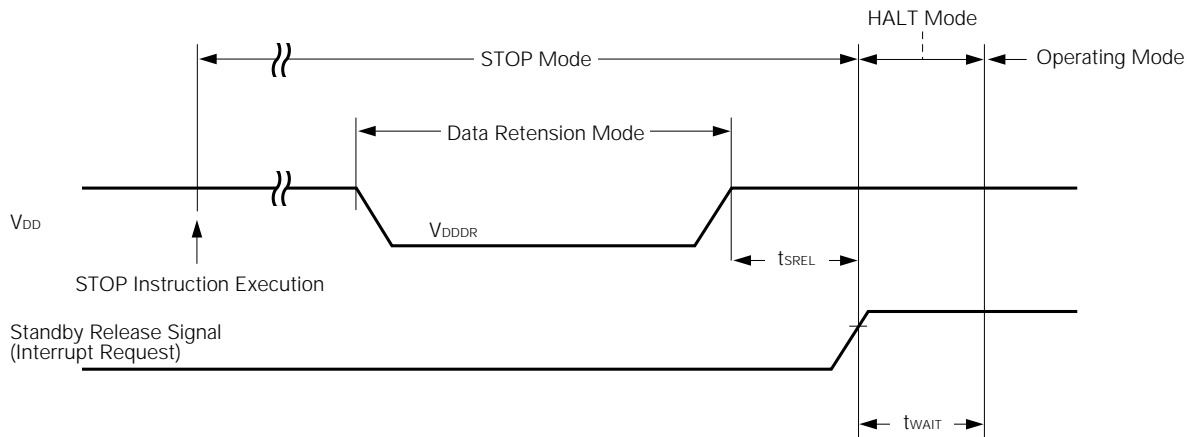
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		2.0		6.0	V
Data retention supply current	IDDDR	VDDDR = 2.0 V Subsystem clock stop and feed-back resistor disconnected		0.1	10	μA
Release signal set time	tsREL		0			μs
Oscillation stabilization wait time	tWAIT	Release by $\overline{\text{RESET}}$		$2^{18}/f_x$		ms
		Release by interrupt		*		ms

* In combination with bit 0 to bit 2 (OSTS0 to OSTS2) of oscillation stabilization time select register, selection of $2^{13}/f_x$ and $2^{15}/f_x$ to $2^{18}/f_x$ is possible.

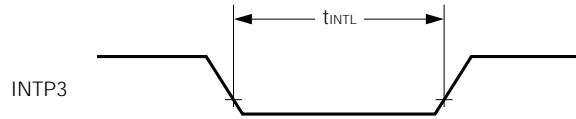
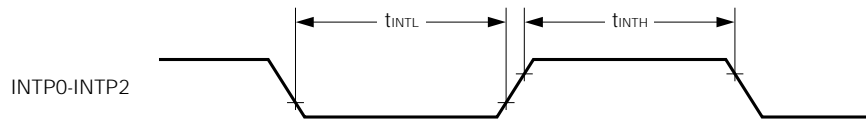
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



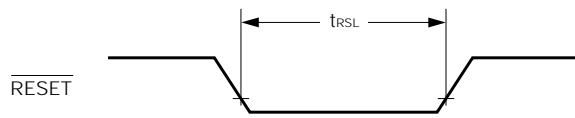
Data Retention Timing (Standby Release Signal : STOP Mode Release by Interrupt Signal)



Interrupt Input Timing

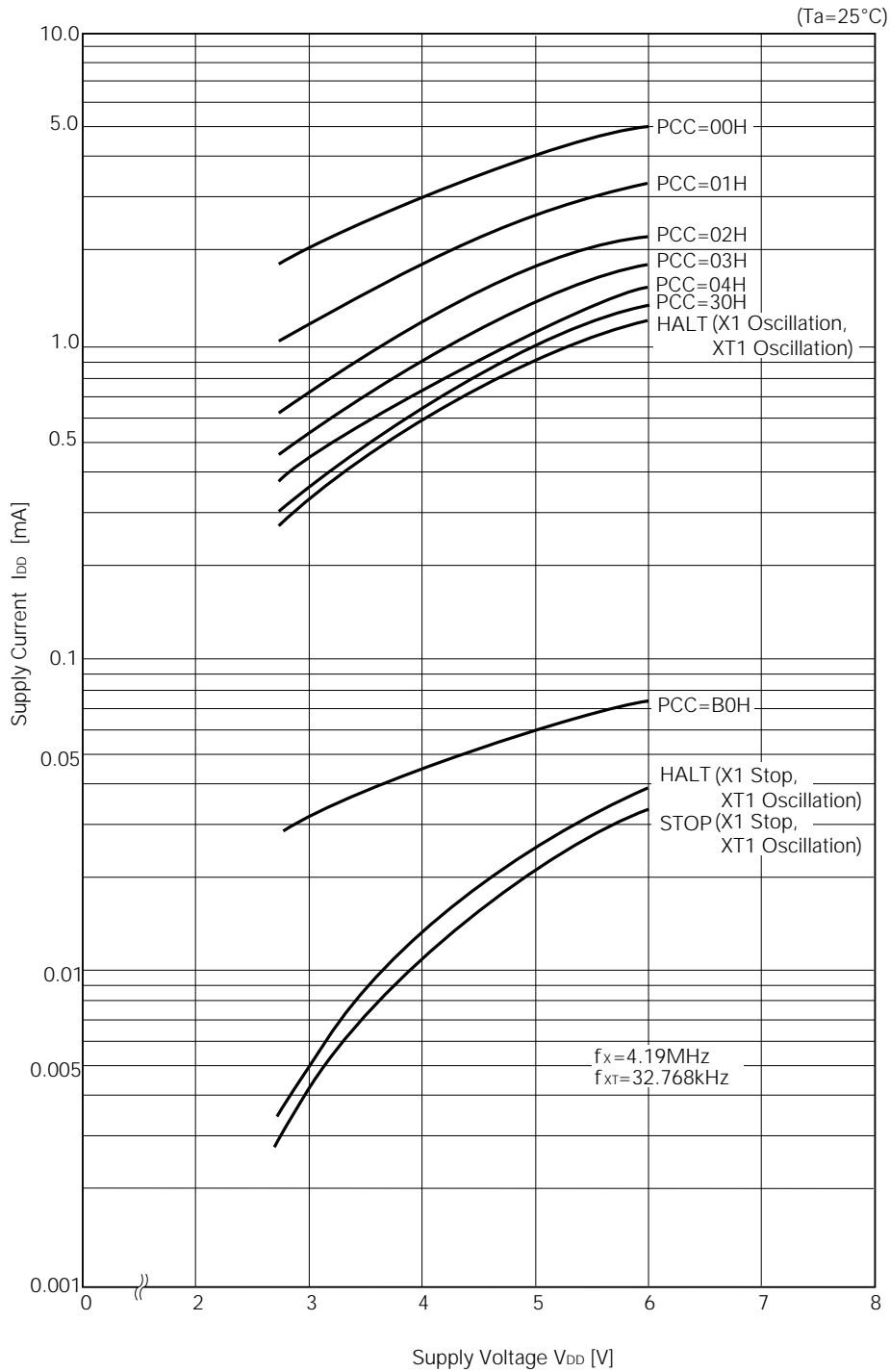


RESET Input Timing

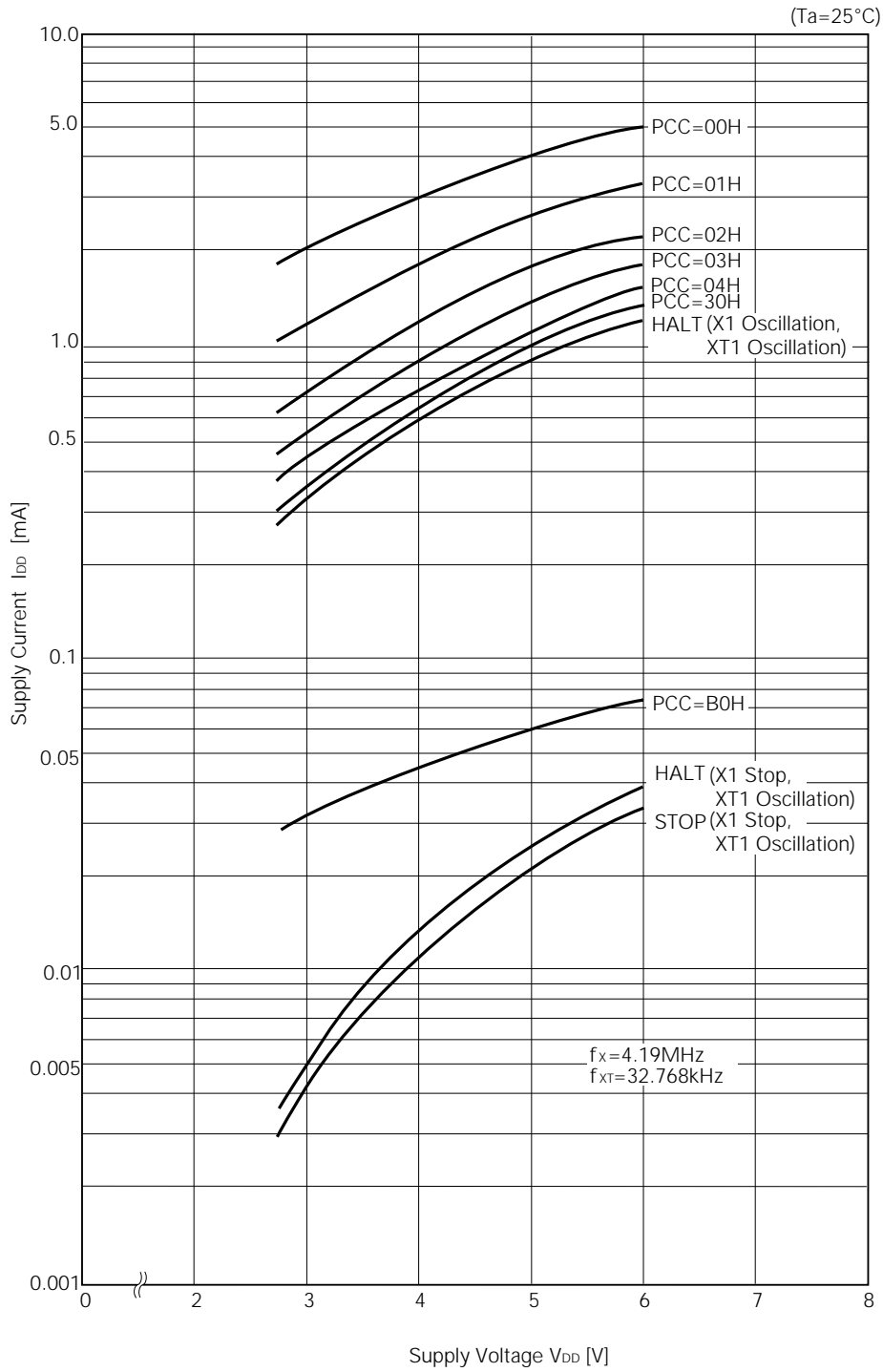


12. CHARACTERISTIC CURVE (REFERENCE VALUES)

I_{DD} vs V_{DD} (Main System Clock: 8.38 MHz)

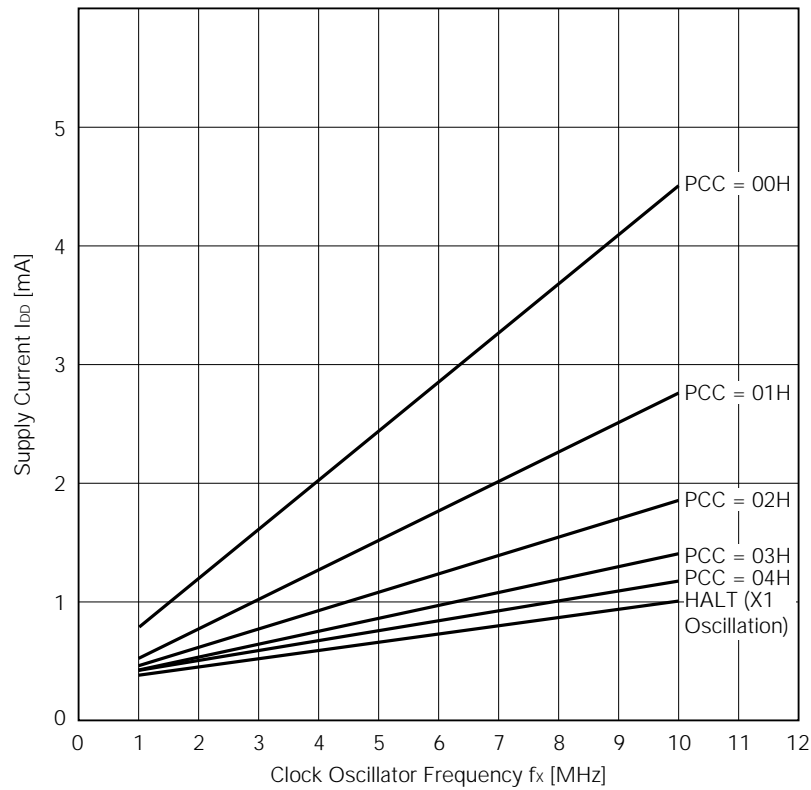


I_{DD} vs V_{DD} (Main System Clock: 4.19 MHz)



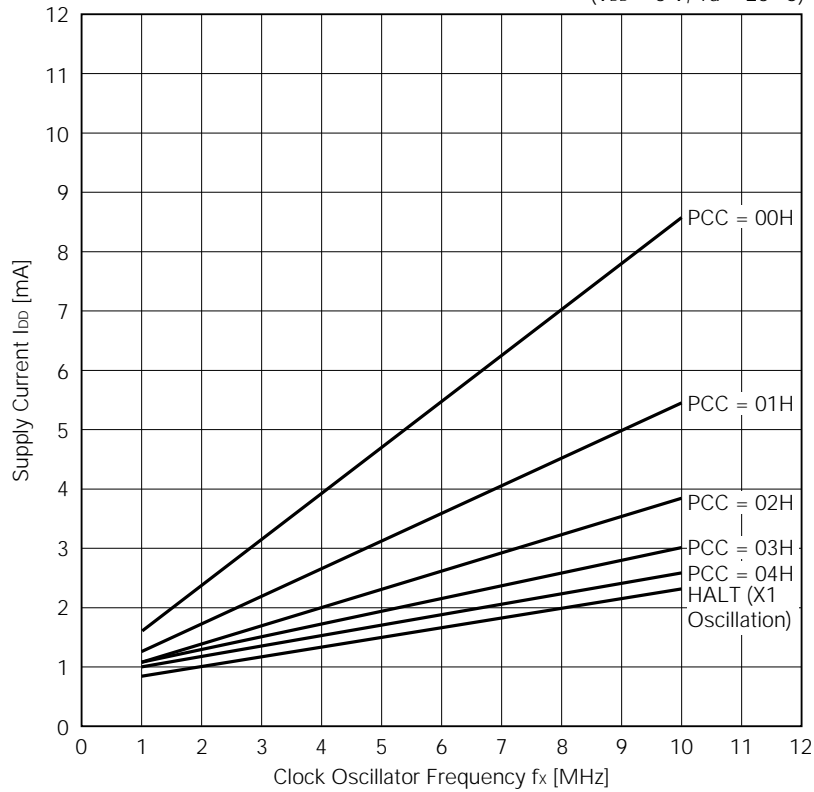
I_{DD} VS f_x

(V_{DD} = 3 V, T_a = 25 °C)

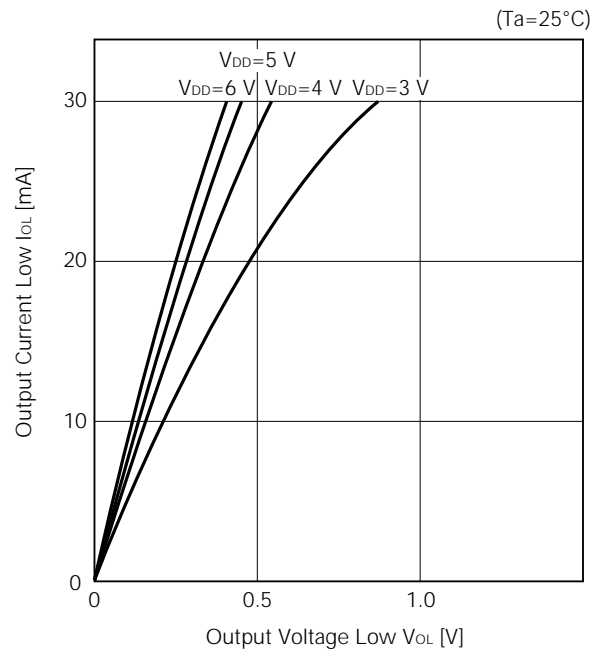


I_{DD} VS f_x

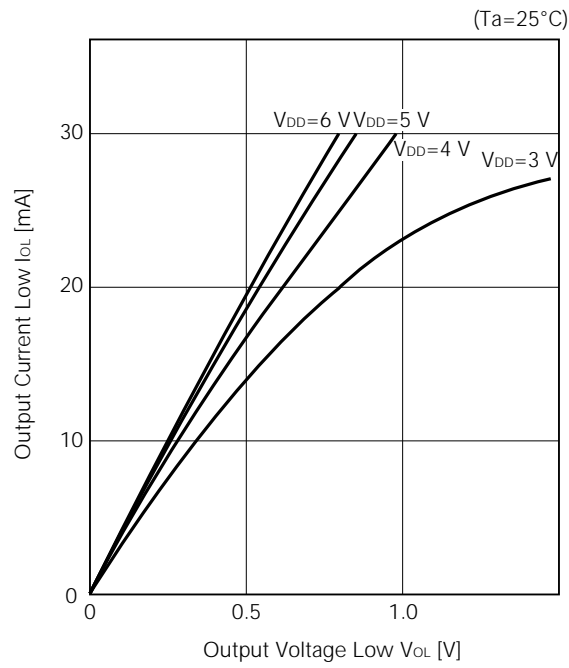
(V_{DD} = 5 V, T_a = 25 °C)



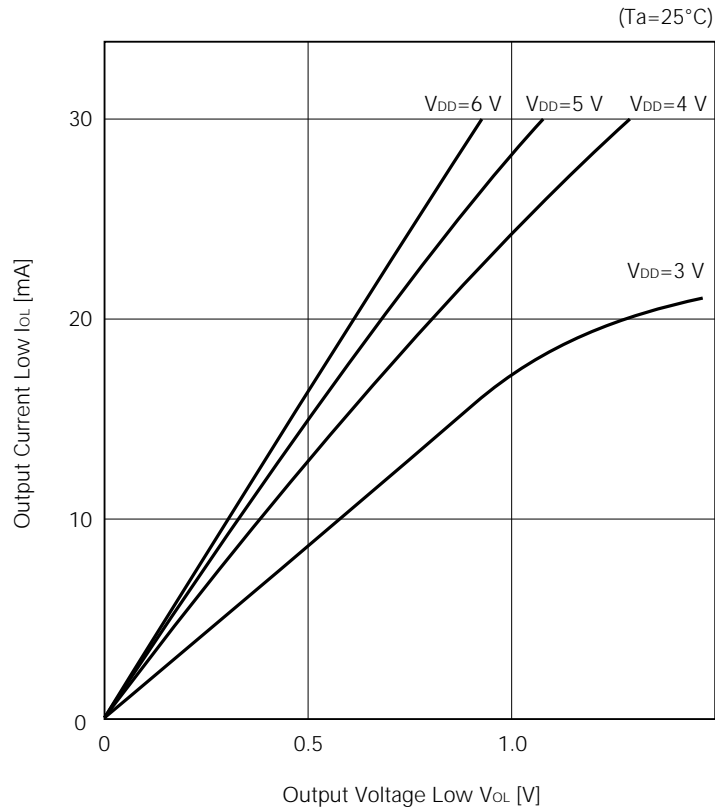
V_{OL} vs I_{OL} (Port 0, 2 to 5, P64 to P67)



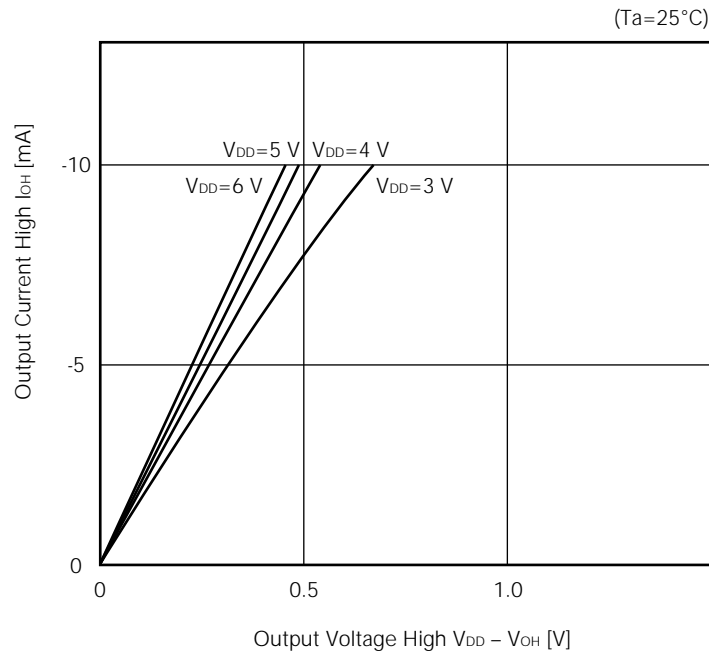
V_{OL} vs I_{OL} (Port 1)



V_{OL} vs I_{OL} (P60 to P63)



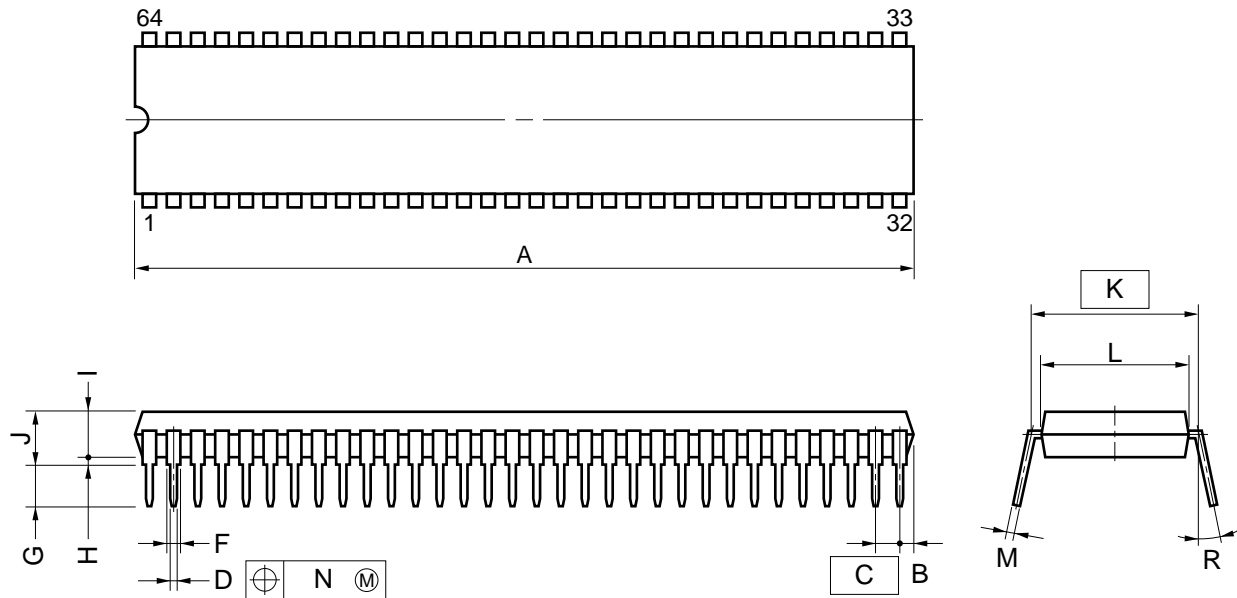
V_{OH} vs I_{OH} (Port 0 to 5, P64 to P67)



13. PACKAGE INFORMATION

DRAWINGS OF MASS-PRODUCTION PRODUCT PACKAGES (1/2)

64 PIN PLASTIC SHRINK DIP (750 mil)



NOTE

- 1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

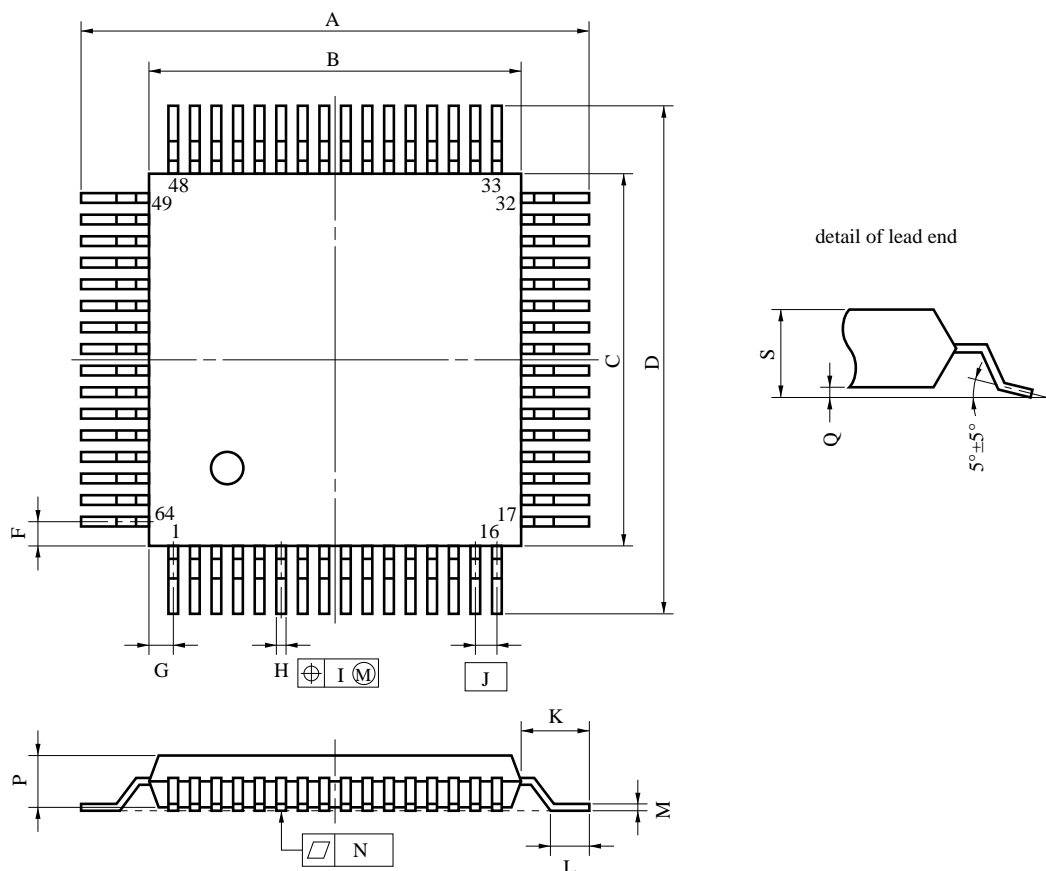
ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	0.020 ^{+0.004} _{-0.005}
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	0.25 ^{+0.10} _{-0.05}	0.010 ^{+0.004} _{-0.003}
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

Caution Dimensions and materials of ES products are different from those of mass-production products. Refer to DRAWINGS OF ES PRODUCT PACKAGES (1/2). ★

DRAWINGS OF MASS-PRODUCTION PRODUCT PACKAGES (2/2)

64 PIN PLASTIC QFP (□4)



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

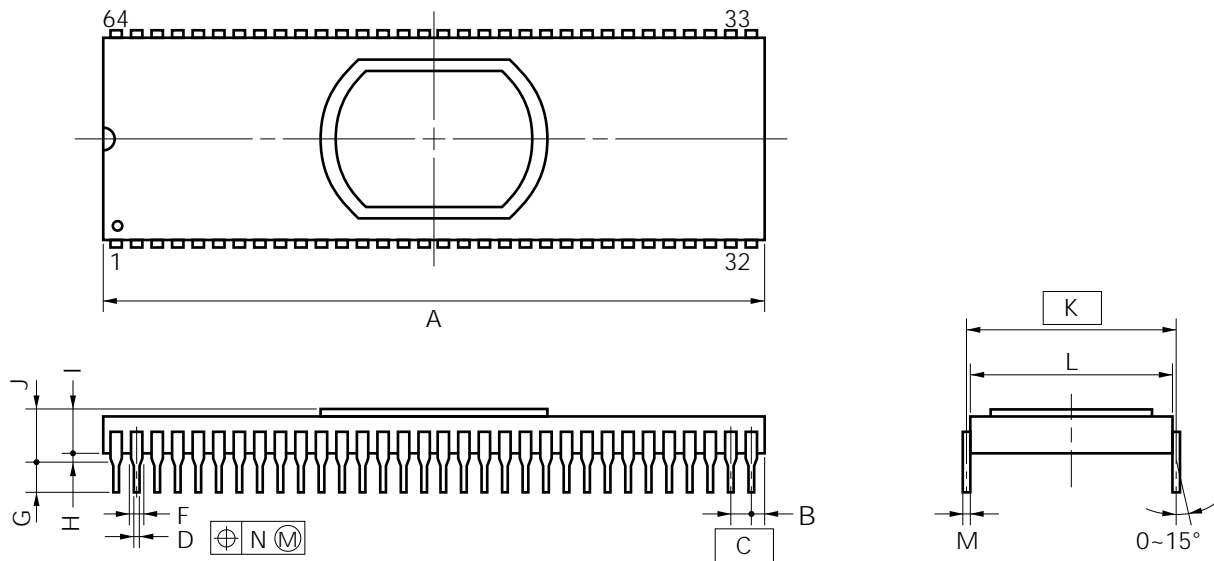
P64GC-80-AB8-3

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	0.551 ^{+0.009} / _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} / _{-0.008}
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	0.014 ^{+0.004} / _{-0.005}
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	0.031 ^{+0.009} / _{-0.008}
M	0.15 ^{+0.10} / _{-0.05}	0.006 ^{+0.004} / _{-0.003}
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

Caution Dimensions and materials of ES products are different from those of mass-production products. Refer to DRAWINGS OF ES PRODUCT PACKAGES (2/2).

DRAWINGS OF ES PRODUCT PACKAGES (1/2)

64PIN CERAMIC SHRINK DIP (SEAM WELD) (750 mil)



P64D-70-750A1

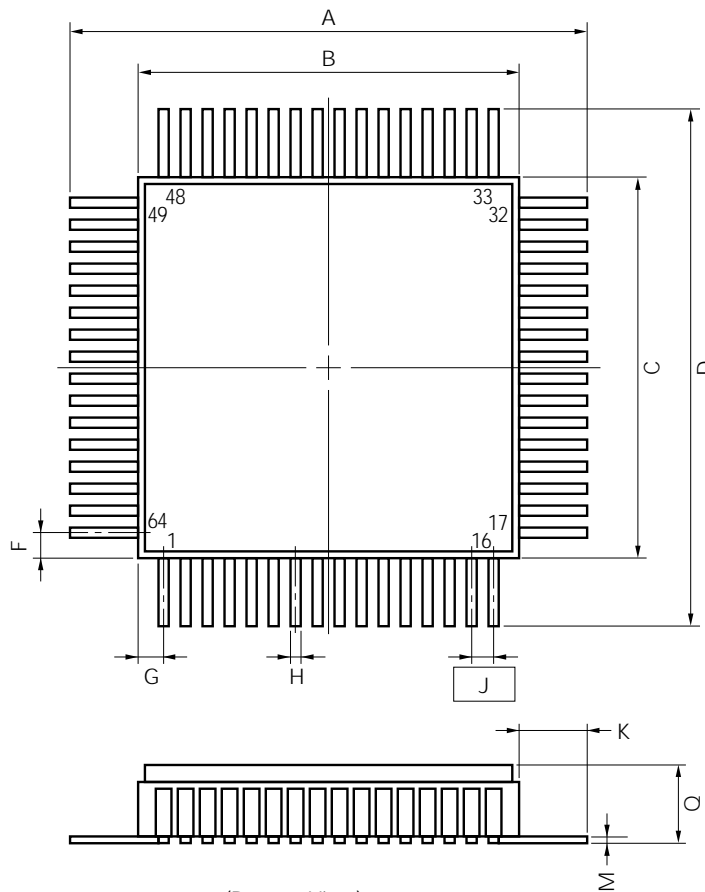
NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

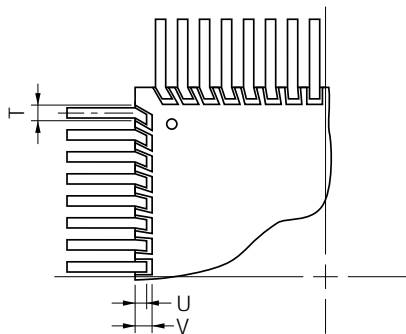
ITEM	MILLIMETERS	INCHES
A	58.16 MAX.	2.290 MAX.
B	1.521 MAX.	0.060 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.46±0.05	0.018±0.002
F	0.8 MIN.	0.031 MIN.
G	3.5±0.3	0.138±0.012
H	1.02 MIN.	0.040 MIN.
I	3.14	0.124
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	18.8	0.740
M	0.25±0.05	0.010 ^{+0.002} _{-0.003}
N	0.25	0.01

DRAWINGS OF ES PRODUCT PACKAGES (2/2)

64 PIN CERAMIC QFP (14 × 14) (FOR ES)



(Bottom View)



X64B-80A-1

ITEM	MILLIMETERS	INCHES
A	22.0±0.4	0.866±0.016
B	14.0	0.551
C	14.0	0.551
D	22.0±0.4	0.866±0.016
F	1.0	0.039
G	1.0	0.039
H	0.32	0.013
J	0.8 (T.P.)	0.031 (T.P.)
K	4.0±0.15	0.157 ^{+0.007} _{-0.006}
M	0.25	0.01
Q	3.0 MAX.	0.119 MAX.
T	0.55	0.022
U	1.0	0.039
V	1.2	0.047

14. RECOMMENDED SOLDERING CONDITIONS

The μPD78011B/78012B/78013/78014 should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document “**Semiconductor Device Mounting Technology Manual**” (IE-1207).

For soldering methods and conditions other than those recommended below, contact our salespersonnel.

Table 14-1 Surface Mounting Type Soldering Conditions

- (1) μPD78011BGC-xxx-AB8 : 64-Pin Plastic QFP (□14 mm)
- μPD78012BGC-xxx-AB8 : 64-Pin Plastic QFP (□14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: Twice max. < Points to note > (1) Start the second reflow after the device temperature by the first reflow returns to normal. (2) Flux washing by the water after the first reflow should be avoided.	IR35-00-2
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above) Number of times: Twice max. < Points to note > (1) Start the second reflow after the device temperature by the first reflow returns to normal. (2) Flux washing by the water after the first reflow should be avoided.	VP15-00-2
Pin part heating	Pin temperature: 300°C max., Duration: 3 sec. max. (per device side)	—

- (2) μPD78013GC-xxx-AB8 : 64-Pin Plastic QFP (□14 mm)
- μPD78014GC-xxx-AB8 : 64-Pin Plastic QFP (□14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: Twice < Points to note > (1) Start the second reflow after the device temperature by the first reflow returns to normal. (2) Flux washing by the water after the first reflow should be avoided.	IR35-00-2
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above), Number of times: Twice < Points to note > (1) Start the second reflow after the device temperature by the first reflow returns to normal. (2) Flux washing by the water after the first reflow should be avoided.	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max. Duration: 10 sec. max. Number of times: Once Preliminary heat temperature: 120°C max. (Package surface temperature)	WS60-00-1
Pin part heating	Pin temperature: 300°C max., Duration: 3 sec. max. (per device side)	—

Caution Use more than one soldering method should be avoided (except in the case of pin part heating).

Table 14-2 Insertion Type Soldering Conditions

μPD78011BCW-xxx : 64-Pin Plastic Shrink DIP (750 mil)

μPD78012BCW-xxx : 64-Pin Plastic Shrink DIP (750 mil)

μPD78013CW-xxx : 64-Pin Plastic Shrink DIP (750 mil)

μPD78014CW-xxx : 64-Pin Plastic Shrink DIP (750 mil)

Soldering Method	Soldering Conditions
Wave soldering (pin only)	Solder bath temperature: 260°C max., Duration: 10 sec. max.
Pin part heating	Pin temperature: 300°C max., Duration: 3 sec. max. (per pin)

Caution Wave soldering is only for the lead part in order that jet solder can not contact with the chip directly.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78011B, 78012B, 78013, 78014.

Language Processing Software

RA78K/0* ^{1,2,3}	78K/0 series common assembler package	
CC78K/0* ^{1,2,3}	78K/0 series common C compiler package	
DF78014* ^{1,2,3}	μPD78014 subseries device file	★
CC78K/0-L* ^{1,2,3}	78K/0 series common C compiler library source file	

PROM Writing Tools

PG-1500	PROM programmer	
PA-78P014CW PA-78P014GC	Programmer adapter connected to PG-1500	
PG-1500 controller* ^{1,2}	PG-1500 control program	

Debugging Tool

IE-78000-R	78K/0 series common in-circuit emulator	
IE-78000-R-BK	78K/0 series common break board	
IE-78014-R-EM	μPD78002/78014 subseries evaluation emulation board	
EP-78240CW-R EP-78240GC-R	Emulation probe common to μPD78244 subseries	
EV-9200GC-64	Socket to be mounted on user system board created for the 64-pin plastic QFP	
SD78K/0* ^{1,2}	IE-78000-R screen debugger	
SM78K/0* ^{4,5,6}	78K/0 series common system simulator	★
DF78014* ^{1,2,4,5}	μPD78014 subseries device file	

Real-Time OS

RX78K/0* ^{1,2,3}	78K/0 series common real-time OS	
MX78K/0* ^{1,2,3,6}	78K/0 series common OS	★

Fuzzy Inference Development Support System

FE9000* ¹ /FE9200* ⁵	Fuzzy knowledge data creation tool	
FT9080* ¹ /FT9085* ²	Translator	
FI78K0* ^{1,2}	Fuzzy inference module	
FD78K0* ^{1,2}	Fuzzy inference debugger	

- * 1. PC-9800 series (MS-DOS™) based
- 2. IBM PC/AT™ (PC DOS™) based
- 3. HP9000 series 300™, HP9000 series 700™ (HP-UX™) based, SPARCstation™, (SunOS™) based, EWS-4800 series (EWS-UX/V) based ★

4. PC-9800 series (MS-DOS + Windows™) based
5. IBM PC/AT (PC DOS + Windows) based
6. Under development

Remarks 1. For development tools manufactured by a third party, see the "78K/0 Series Selection Guide" (IF-1185).

- ★ 2. RA78K/0, CC78K/0, SD78K/0, and SM78K/0 are used in combination with DF78014.

APPENDIX B. RELATED DOCUMENTS



Device Related Documents

Document Name		Document No. (Japanese)	Document No. (English)
User's Manual		IEU-780	IEU-1314
78K/0 Series User's Manual - Instruction		IEU-849	IEU-1372
Application Note	Basic I	IEA-715	IEA-1288
	Basic II	IEA-740	IEA-1299
	Floating-Point Arithmetic Program	IEA-718	IEA-1289
	Electronic Notebook	IEA-744	IEA-1301

Development Tools Documents (User's Manual)

Document Name		Document No. (Japanese)	Document No. (English)
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller		EEU-704	EEU-1291
IE-78000-R		EEU-810	EEU-1398
IE-78000-R-BK		EEU-867	EEU-1427
IE-78014-R-EM		EEU-805	EEU-1400
SD78K/0 Screen Debugger	Basic	EEU-852	EEU-1414
	Reference	EEU-816	EEU-1413

Caution The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.

Embedded Software Documents (User's Manual)

Document Name	Document No. (Japanese)	Document No. (English)
Fuzzy Knowledge Data Creation Tool	EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System - Translator	EEU-862	EEU-1444

Other Documents

Document Name	Document No. (Japanese)	Document No. (English)
Package Manual	IEI-635	IEI-1213
Semiconductor Device Mounting Technology Manual	IEI-616	IEI-1207
Quality Grade on NEC Semiconductor Devices	IEI-620	IEI-1209
Semiconductor Devices Quality Guarantee Guide	MEI-603	MEI-1202

Caution The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Special: Automotive and Transportation equipment, Traffic control systems, Antidisaster systems, Anticrime systems, etc.

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