AMERICAN MICROSYSTEMS, INC.
WavePlex ™

SX061
1 Mbit/s DQPSK/DBPSK
Digital Demodulator

User's Manual

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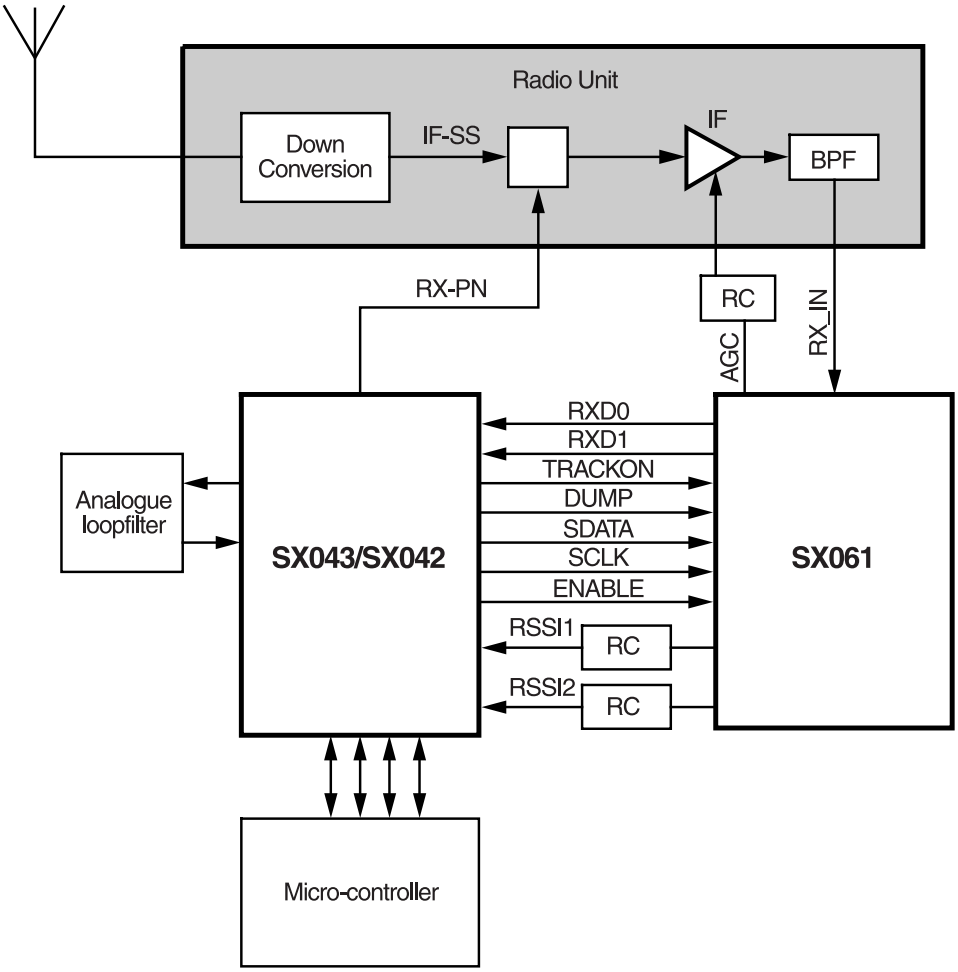
General Description

The SX061 is a digital demodulator, specially developed to work together with the AMI SX043 Spread Spectrum baseband processor. This 24 pin integrated circuit replaces many analogue components needed to work with the SX043 or SX042. This chip is only needed on the receiving radio unit (FIGURE 1). The transmitting radio unit needs no special requirements to generate the DQPSK or DBPSK signal other than the output of an SX041 or an SX043.

Figure 1: Typical SS DS Receiver Using SX043 & SX061



Features

- Up to 1 Mbit/s (D)QPSK demodulation
- Up to 500kbit/s (D)BPSK demodulation
- RSSI output for SX042/043 code tracking and synchronization
- Fully programmable using serial interface of SX042/043
- Low power consumption
- Power Down mode
- SOIC 24 package

Spread Spectrum Applications

- Wireless Local Area Networks
- Portable wireless communication
- Digital cellular telephone systems
- Wireless ISDN modems
- Other wireless systems

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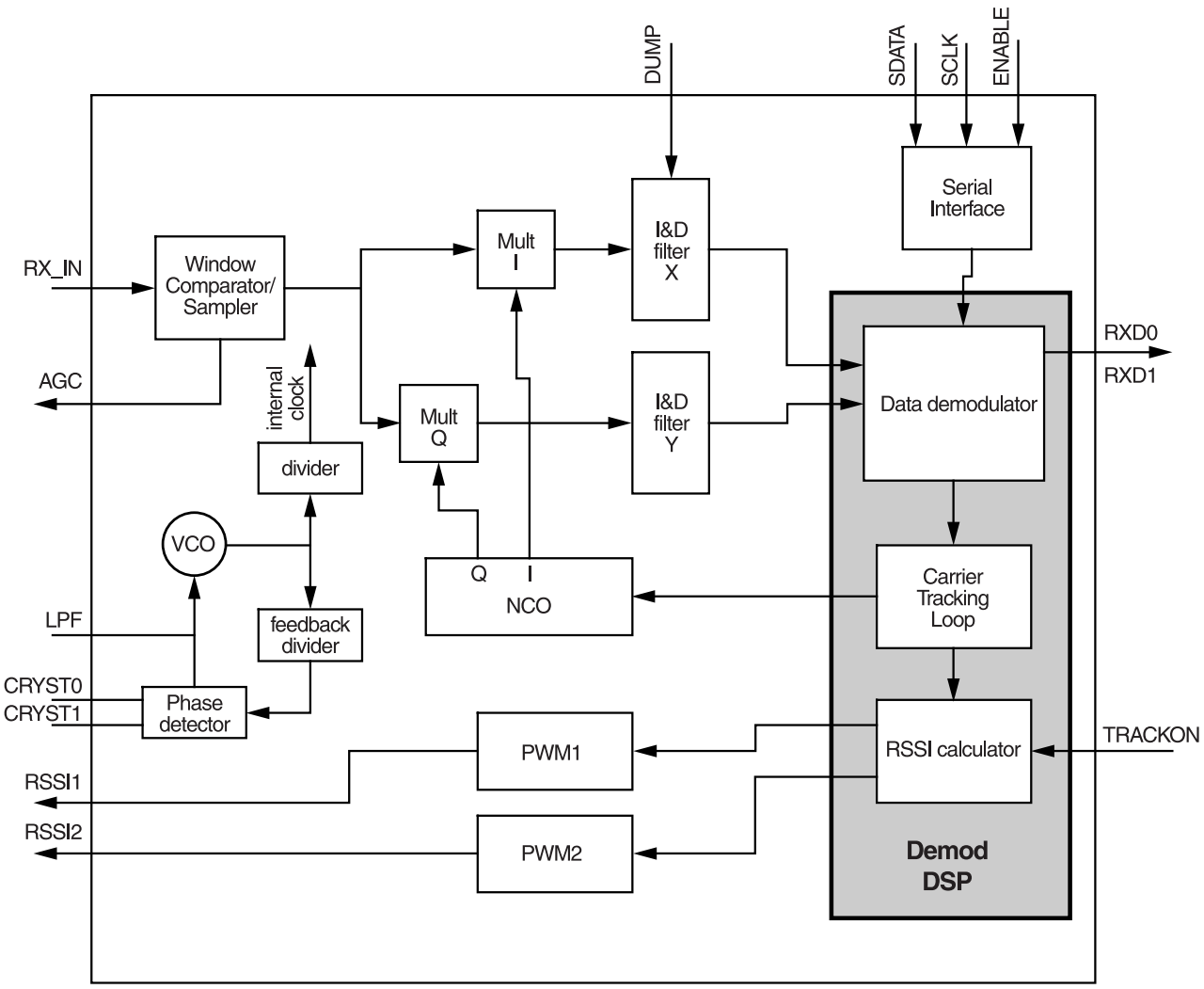
Figure 2: Block Diagram of SX061



Functional Description of the SX061

The incoming IF signal is quantized using three quantization levels. After that, the signal is multiplied with the complex LO signal, generated by a Numerical Controlled Oscillator (NCO).

The I- and Q- output signals are fed into the Integrate and Dump filters. The "Dump" signal for the filters is generated by the SX043 on the end of each symbol.

After a "DUMP" has occurred the Demodulating DSP is triggered. This DSP calculates the phase and amplitude of the signal. The phase information is filtered and subsequently used to correct the internal IF frequency of the NCO. The amplitude information is used to calculate the RSSI signals. The SX043/042 needs this RSSI signal in two different stages of the reception process:

The first stage is the "slip" mode. In this mode the SX043 needs to detect the moment that a correlation flash occurs between the transmitted and the received PN code before the codes have been synchronized. This correlation flash is generated on the RSSI output. After the two PN codes have been synchronized, the SX043 changes to the second stage: The "track" mode.

In this mode the SX043/042 needs the RSSI signal to keep the PN code in lock.

In order to distinguish these two modes the SX061 uses the TRACKON output of the SX043.

A simple RC section can obtain the analog RSSI value from the Pulse Width Modulator.

The SX061 also generates an AGC output. This AGC signal is used to control the gain of the amplifier in the Radio Unit. This guarantees an optimal quantization of the incoming signal.

The internal registers of the SX061 are programmed by a serial interface, which is controlled by the SX043.

The SX061 has a complete PLL inside for the generation of the internal clock signals. Using a reference crystal frequency of 2 MHz an internal clock signal from 1.56 MHz up to 100 MHz can be generated.

Figure 3: SX061 - SX043 Interconnections

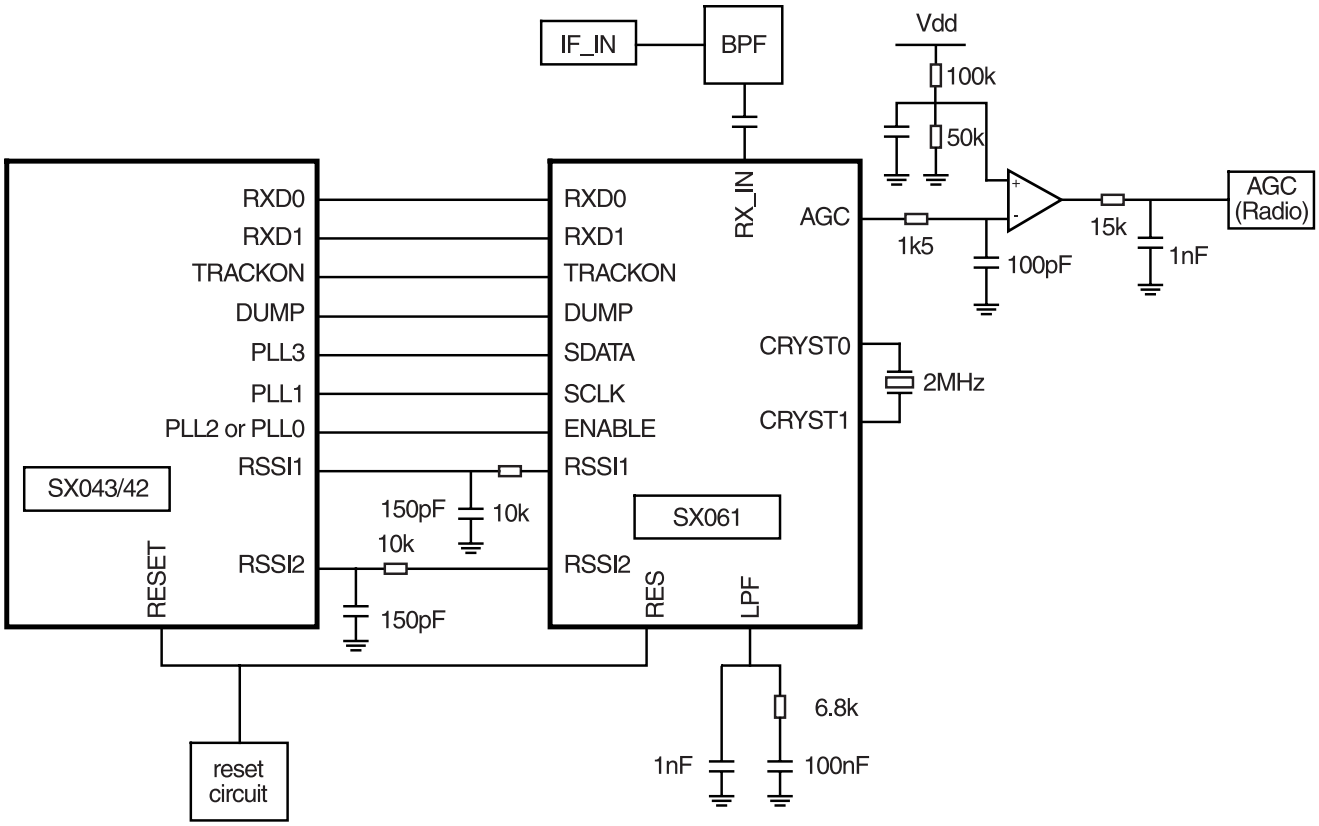


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Figure 4: Pin Layout

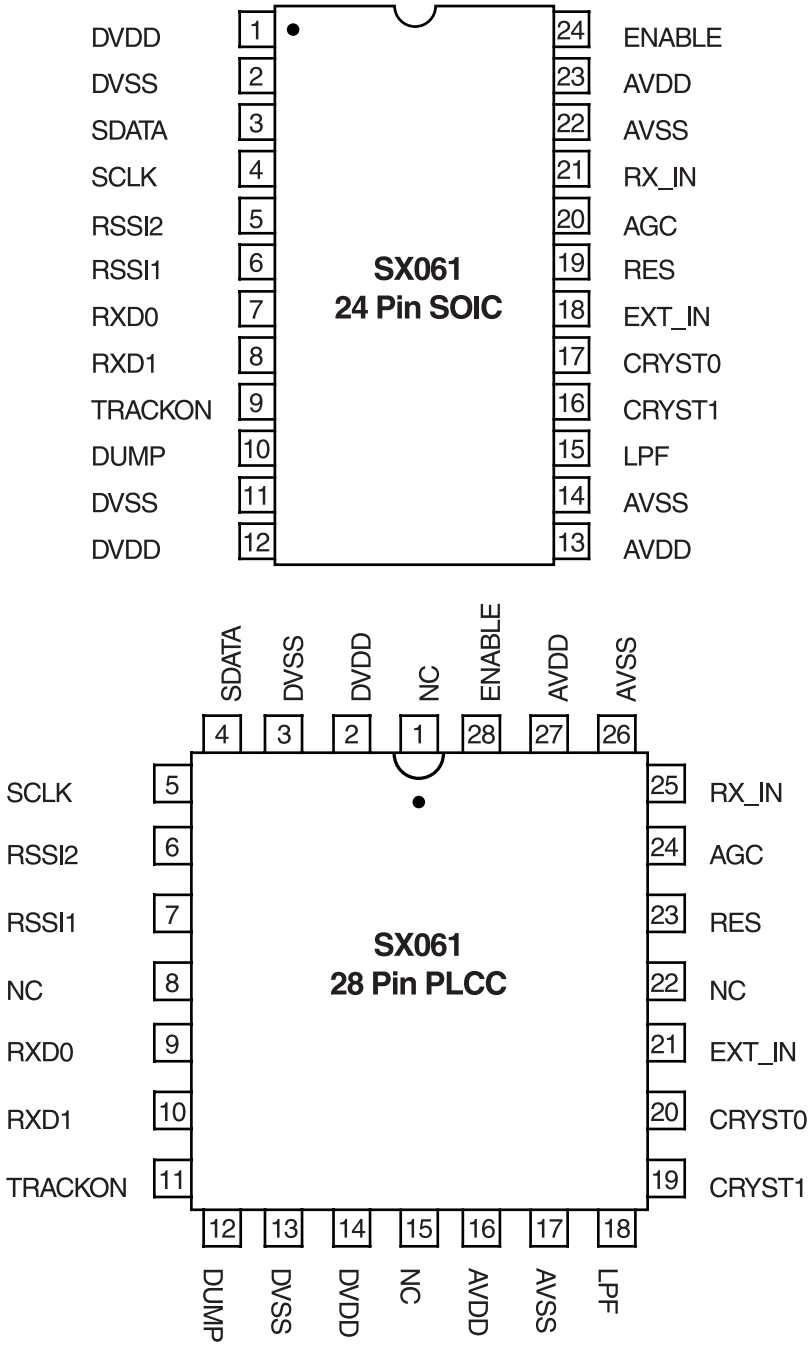

Table 1: Pin Description

PIN NAME	NUMBER ON 24 PIN SOIC	NUMBER ON 28 PIN PLCC	FUNCTION DESCRIPTION	TYPE
DVDD	1, 12	2, 14	Digital power	POWER
DVSS	2, 11	3, 13	Digital ground	GROUND
SDATA	3	4	Data for serial programming interface	INPUT
SCLK	4	5	Clock for serial programming interface, sensitive to rising edge	OUTPUT
RSSI2	5	6	RSSI2 for SX043	OUTPUT
RSSI1	6	7	RSSI1 for SX043	OUTPUT
RXD0	7	9	Received data bit 0	OUTPUT
RXD1	8	10	Received data bit 1	OUTPUT
TRACKON	9	11	Indicates that SX043 is tracking the incoming signal, active high	INPUT
DUMP	10	12	Integrate and dump control logic input	INPUT
LPF	15	18	PLL phase detector output, internal VCO input	ANALOG
CRYST1	16	19	Crystal oscillator or external reference input	CRYSTAL OSC/INPUT
CRYST0	17	20	Crystal oscillator	CRYSTAL OSC
EXT_IN	18	21	Used as digital input from external window comparator, when bypassing internal window comparator	INPUT
RES	19	23	Active low reset	INPUT
AGC	20	24	Automatic gain control	OUTPUT
RX_IN	21	25	IF signal input, can also be used as digital input from external window comparator	ANALOG/ INPUT
ENABLE	24	28	Active low enable for serial programming interface	INPUT
AVDD	13, 23	16, 27	Analog power	POWER
AVSS	14, 22	17, 26	Analog ground	GROUND
NC	-	1, 8, 15, 22		NOT CONNECTED

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Description of Individual Blocks

Serial Interface

The SX061 can be programmed using the serial interface, consistent with the SX043 PLL interface. This interface consists of three lines: SDATA, SCLK, and ENABLE. The serial data on the SDATA pin is clocked into the shift register on each rising edge of the SCLK pin when the ENABLE pin is low. At the moment the ENABLE pin goes high the new programming string replaces the current programming string. This allows programming at any moment. For the connection from the SX043 to the SX061 see the connection diagram (FIGURE 3).

The programming string consists of 51 bits. The MSB (bit 50) of the programming string is shifted in first, the LSB (bit 0) last.

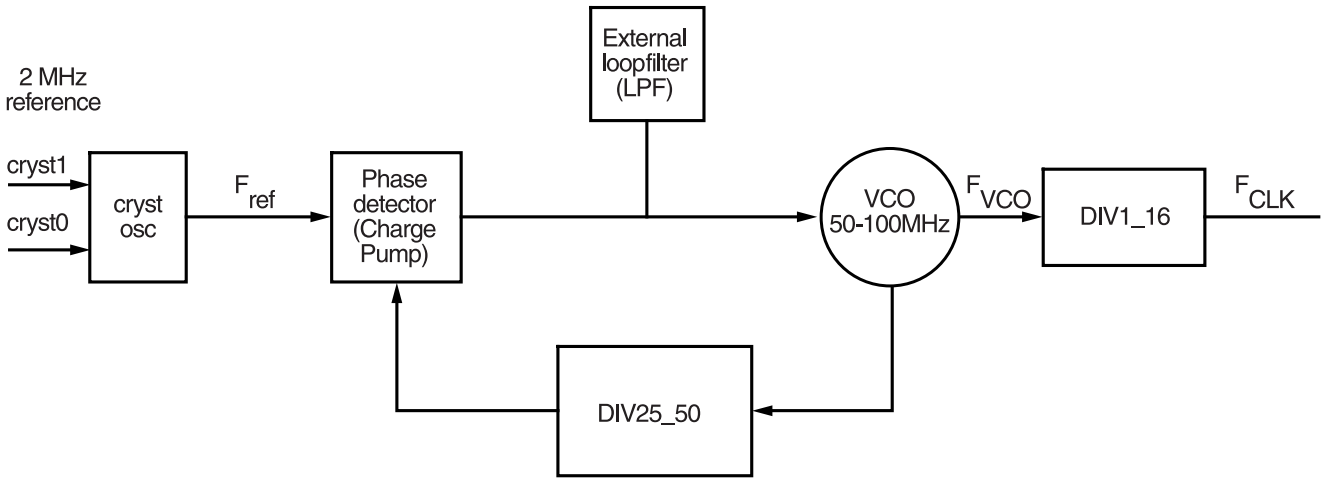
This string can be preceded by an arbitrary number of zero's or one's, which are discarded by the SX061.

Note: The programmable interface of the SX043 can only generate serial strings with a length of an integer multiple of 8 bits. So the Bitcount register of the SX043 has to be set to 56 when programming the SX061.

The programming string consists of a number of registers. An overview of the functionality of these registers is given in the last section.

The PLL

Figure 5:

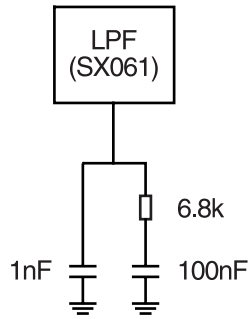


The internal PLL of the SX061 generates the clock frequency for the chip. A block diagram is given in Figure 5. The reference frequency is generated from an internal crystal oscillator.

This crystal oscillator uses the pins CRYST0 and CRYST1 to connect a 2 MHz crystal.

For correct operation of the internal PLL a capacitor of 270 pF has to be connected between CRYST1 and ground. The crystal oscillator output is internally fed into a charge pump phase detector. An external loopfilter on the LPF pin filters out the undesired ripple on the charge pump output. This external loopfilter is characterized by its transimpedance. A suitable schematic for the VCO is given in Figure 6:

Figure 6:



Note: It is very important to connect the 1 nF capacitor as close as possible to the LPF pin.

The voltage on the LPF pin controls the frequency of the VCO. This VCO has been designed to run from 50 to 100 MHz. A feedback divider regenerates the 2 MHz reference frequency on the second input of the phase detector. The feedback divider can divide by number from 25 to 50 in multiples of 5. This division ratio can be programmed using the DIV25_50 register from the programming string, as listed on the following page. Note that when a 2 MHz crystal is used, only the range from 25 to 50 should be used.

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Table 2:

DIV25_50	F_{VCO}/F_{ref}
5	25
6	30
7	35
8	40
9	45
10	50

The output of the VCO is divided again by a second divider, which can divide by 1, 2, 4, 8 or 16. This can be programmed using the div1-16 register of the programming string as listed below.

Table 3:

DIV1_16	F_{VCO}/F_{clk}
0	1
1	2
2	4
3	8
4	16

The AD Converter

The AD converter discerns three levels: 1, 0, and –1. The AD conversion is accomplished by using a window comparator.

The output of the window comparator defines the three levels. The window comparator is latched on the internal (sample) clock of the SX061. This sample clock can run at frequencies up to 100 MHz.

The input signal has to be capacatively coupled to the RX_IN pin (appr. 10nF). The input resistance of the AD-converter is 200k, the DC level is 2.1 V.

The AGC

The AD converter works optimally when the quantization error is minimized. The AGC makes sure that the quantization levels of the signal are chosen optimally. The signal is assumed to be sine shaped, and that the DC level of the signal is exactly between the two quantization levels.

In this case the input signal is always quantized the same number of times as a +1 as is it quantized as –1. When the input signal is larger the number of times that the signal is quantized as '0' is smaller than when the signal is small. The ratio between the number of +/- 1 samples and '0' samples should be about 1/3.

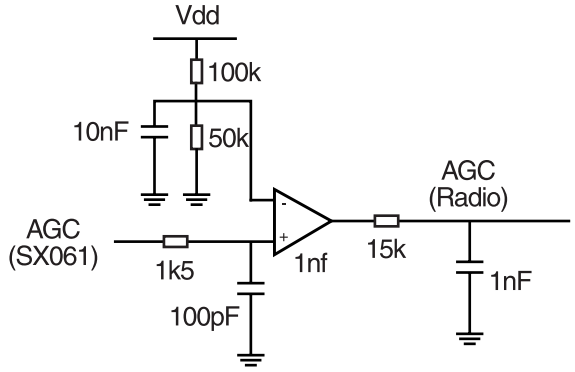
The AGC pin becomes high when a '0' is sampled and low when a '1' or '-1' is sampled. This is a measure for the above mentioned ratio. Therefore the AGC output should be compared to 1/3 of VDD. When the difference between the AGC output and the 1/3 VDD is integrated by a pure integrator, a good signal for the AGC control is obtained for almost any amplifying device.

The time constant of this integrator controls the speed of the AGC loop.

Therefore a circuit to use the AGC output of the SX061, which can control almost any AGC input of an amplifying circuit, is suggested in Figure 7.

The AGC loop has to be slower than the dither rate. Otherwise it would suppress the tau dither information. However it should be faster than the fastest variations in amplitude that the radio has to expect.

Figure 7:



The AGC in Slip Mode

When the signal is uncorrelated (in slip mode) a bandpass filter will probably make the input signal very small. This will set the AGC output to its maximum value.

When a correlation peak occurs the window comparator will act as a hard limiter. This will not influence the quality of the quantized signal severely. However, during the time that the AGC loop is not settled the performance of the SX061 is not optimal. Therefore the time needed to bring the AGC to its correct operation point should not be more than a small part of the data message (but larger than the dither rate). The speed of the AGC loop is largely determined by the external time constants.

Note: For proper operation of the AGC the AGC_comp_test bit of the COMP_SEL register has to be set to '0'.

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The NCO

The Numerical Controlled Oscillator generates the internal LO frequency at I and Q. The outputs of the NCO are 4-bit words, representing a sine and a cosine at the IF-frequency.

The frequency of the NCO, F_{NCO}, is set using a 16-bit word. This word is generated by the demodulating DSP. It consists of a frequency offset F_{offset} word plus an additional term F_{track} from the demodulating DSP to lock on the incoming signal. This term F_{track} is generated by the demodulating DSP and does not have to be set by the user (See Demodulating DSP).

So,

$$F_{NCO}=F_{offset} + F_{track.}$$

The frequency setting word FOFFSET can be programmed using the 16-bit register FOFFSET of the programming string. The offset frequency of the NCO is related to this word as shown below:

$$F_{offset}= FOFFSET * F_{clk}/2^{17}.$$

Note: The highest attainable IF frequency for a given internal clock frequency is $F_{clk}/4$. When higher IF frequencies are needed, a higher F_{clk} has to be chosen.

For the calculation of F_{clk} see the PLL section (page 9).

The I&D Filters

The internal I&D filters accumulate the output of the multiplication of the samples and the NCO I- and Q-output.

Each time a DUMP from the SX043 occurs, the content of the I&D filter is passed to the demodulating DSP. From this moment on the I&D filter outputs are referred to as X_1 and Y_1.

At the same time the internal value of the I&D is set to 0. The first operation of the DSP is dividing X_1 and Y_1 by 2^n. The number n can be set using the 4-bit I&D_gain register of the programming string.

Inter Symbol Interference (ISI) can be minimized by controlling the delay and the length of the DUMP signal. As long as the DUMP signal is high the I&D filters do not accumulate. The DUMP length and delay can be controlled using the DMP register on the SX043.

The Demodulating DSP

The demodulating DSP performs three tasks:

- Detecting the data
- Carrier tracking
- Generating the RSSI signals

Detecting Data

There are three different ways of data demodulation. These can be selected by setting the mode register, which is described in Table 4.

Table 4:

VALUE OF MODE	DESCRIPTION OF MODE
0	For demodulating a BPSK signal
1,2	For demodulating a QPSK signal
3	For tracking an unmodulated carrier

Mode 3 can be used to track an unmodulated carrier with an extra large initial frequency offset. The maximum size of this frequency offset is 0.5 * F_{symbol}. Mode 3 is also active as long as the TRACKON input pin is low. When connected to the SX043 the TRACKON pin indicates whether the SX043 is in dither mode or not.

The DIF_DATA bit of the programming string allows the user to convert a differential transmitting coding scheme (DQPSK or DBPSK) into a non-differential coding scheme (QPSK or BPSK) for reception. This is explained in Table 5.

Table 5:

TRANSMISSION	DIF_DAT A	RECEPTION
BPSK	'1'	BPSK
QPSK	'1'	QPSK
DBPSK	'1'	DBPSK
DQPSK	'1'	DQPSK
DBPSK	'0'	BPSK
DQPSK	'0'	QPSK

Carrier Tracking

From the inner and outer products from (X_1,Y_1) and (X_2,Y_2) the demodulating DSP extracts a measure for the phase error. This phase error is used in a digital loopfilter, which adds a tracking term F_{track} to the frequency setting word of the NCO.

The gain of the loopfilter can be set by the 4 bit PHASE_GAIN register. The content of this register is used to perform a Shift Right operation on the detected phase error from the inner and outer products. Therefore a larger value of the PHASE_GAIN register results in a smaller loop gain. Usually the value of PHASE_GAIN should be between 4 and 8.

The SX061 only generates the F_{track} term under two conditions:

The LOCK bit of the programming string should be set to 1 and the TRACKON input pin should be high. If one of these conditions is not fulfilled the NCO frequency is only determined by the offset frequency.

Generating RSSI1 and RSSI2

From the inner and outer products from (X_1,Y_1) and (X_2,Y_2) the demodulating DSP also derives a measure for the energy of the detected symbol. This energy is used to generate the RSSI1 and RSSI2 output. A pulse width modulator generates these RSSI outputs from two 16-bit words calculated by the demodulating DSP. These words are called PWM1 and PWM2 for the RSSI1 and the RSSI2 pulse width modulator.

The RSSI2 output is used to monitor the received signal strength during reception. The output of RSSI2 corresponds to the energy of the current symbol. So PWM2 = X_1*X_1+Y_1*Y_1. If the signal is lost during reception, this can be monitored by a micro controller when it reads the RSSI2 register of the SX043.

The RSSI1 serves two purposes: Detecting the correlation peak when the SX043 is in slip mode and generating the tau-dither information when the SX043 is in track mode. The SX061 knows whether the SX043 is in track or in slip mode by monitoring the TRACKON signal. When the receiver is in slip mode the PWM1 value is the same as the output of RSSI2. So PWM1 = X1*X1+Y1*Y1.

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Generating RSSI1 and RSSI2 *Continued*

When the SX043 detects this as a true correlation peak it changes to track mode.

In track mode the PWM1 value corresponds to the difference between the energy of the current symbol and the energy of the symbol one dither period ago. In order to store the energy values of the last symbols, the demodulating DSP contains an internal FIFO with a programmable depth (Max depth =15).

The depth of the FIFO can be programmed with the 4-bit DELAY register. The value in the DELAY register has to be the same as the RNT register of the SX043. The maximum dither rate is therefore 15 symbols.

In slip mode the PWM1 value is always positive. In track mode the PWM1 value can be positive as well as negative. Therefore an offset is added to the PWM1 value, which sets the output voltage of RSSI1 at _ VDD. This can be done because the SX043 only looks at the difference between the current RSSI1 value and the RSSI1 value one dither period ago.

In order to match the output of the RSSI1 and RSSI2 to the input range of the SX043 the PWM_GAIN register is used. The larger the value of the PWM_GAIN register, the smaller the RSSI1 output. Increasing PWM_GAIN by 1 decreases the output of the RSSI1 by a factor 2. Usual values of PWM_GAIN are between 1 and 3.

Note: The value of the PWM_GAIN register does not influence the value of the DC offset of the RSSI1 output in track mode.

The output range of the DC value of the RSSI outputs is from 0 to _ VDD. The reason for this is that this is also the input range of the ADCs on the SX043 on its RSSI inputs. So a simple RC section, filtering the ripple on the RSSI output at _ * F_{clk} frequency and passing any change at the symbol rate, is sufficient.

Triggering the Demodulating DSP

The Demodulating DSP uses its own clock. The frequency of this clock F_{clk_DSP} is derived from the main clock, using a programmable divider. The DIV_DSP register controls the division ratio, which is to be used as listed below:

Table 6:

VALUE OF DIV_DSP (2 BITS)	F_{Clk}/F_{clk_dsp}
0	8
1	16
2	32
3	64

The demodulating DSP is triggered at the moment a DUMP signal occurs. One complete DSP calculation takes 10 clock cycles on the DSP.

The DSP has to finish operation before the next DUMP signal occurs. The demodulating DSP is not allowed to trigger two times on the same DUMP. If this happens the division ratio of the DIV_DSP has to be increased.

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Designing a Link Using the SX061 and the SX043/42

In order to setup the SX061 correctly the following steps have to be taken:

1. Specify link parameters
2. Setup the SX043
3. Setup the internal clocks on the SX061
4. Setup the AGC loop
5. Setup the internal IF frequency
6. Setup the RSSI outputs
7. Synchronizing the Receiver: Slip Mode
8. Synchronizing the Receiver: Track Mode
9. Setup the carrier tracking loop
10. Setup the data transmission
11. Optimization

Most of these steps involve setting a specific part of the programming string. When all the values have been set correctly, this will result in the final programming string for the application. A basic understanding of the functionality of the SX043/SX042 is assumed. This part should be regarded as an addition to the SX043 User's Manual. Whenever the SX043 is mentioned and used as a receiver, the very same information is also applicable on the SX042. In this section it is assumed that there is one SX043 which is used as a transmitter and receiver at the same time. Other configurations, using two SX043's or a combination of SX041, SX042/SX043 are also possible.

1. Specify Link Parameters

First, a consistent set of parameters has to be defined for the spread spectrum link. These include:

- Data rate
- Modulation type, defining symbol rate
- Q Processing Gain, defining chip rate

Note: The IF input frequency puts certain demands on the internal clock frequency of the SX061. Therefore obey the demands as mentioned in section 3: Setup the internal clocks on the SX061.

2. Setup the SX043

The PN codes have to be programmed correctly on the SX043 (see the SX043 User's Manual). After these values have been set the DUMP signal of the SX043 should be stable. This can be accomplished by writing 0x01 to the TRK register. This will also make the TRACKON signal low. This should not change until closing the tau-dither loop.

Note: The complete IF/RF circuit has to operate correctly.

3. Setup the Internal Clocks on the SX061

Program the PLL of the SX061. Choose the internal clock frequency at between 150 and 300 times the symbol rate. A higher clock frequency makes the SX061 consume more current without performance increase, a lower frequency makes the effects of the quantization error significant.

The maximum LO frequency is _ of F_{clk}. As the carrier tracking loop should be able to increase the internal LO frequency a little, the IF frequency has to be at least a few percent less than this limit.

Note: The TEST_MODE bit of the register has to always be 0, and the VCO_EXT bit has to be set to 1.

Designing a Link Using the SX061 and the SX043/42 *Continued*

4. Setup the AGC Loop

The AGC loop can be closed and tested now. This has to be tested using an unmodulated (no spreading/ despreading) carrier.

Note: COMP_SEL register has to be set to 0.

5. Setup the Internal IF Frequency

The IF frequency is selected by programming the FOFFSET register. This will make the NCO run at the IF frequency. For a description on how to choose a value for this register see the NCO section.

To check if there is correlation between the incoming signal and the internal IF, the RSSI outputs can be monitored.

6. Setup the RSSI Outputs

By choosing the values of ID_GAIN and PWM_GAIN the RSSI signal can be scaled. This has to be done in such a way that the output of the RSSI signal is about half the output scale (_ * Vdd). The effect on the RSSI outputs caused by changing the values of ID_GAIN and PWM_GAIN is as follows: Increasing the PWM_GAIN register by one, will decrease the RSSI outputs by a factor two. Increasing the ID_GAIN register by one, will decrease the RSSI outputs by a factor four. This is because the I&D outputs are squared, to deduce an energy level from them. So dividing them by two results in an energy level divided by 4. Do not increase the I&D gain value too much when increasing the PWM_GAIN value is also possible. This is because increasing the I&D gain value is like throwing away information (the LSB bits of X and Y). These bits will also be lost for data demodulation and carrier tracking.

Note: While the TRACKON signal is low, there is no difference between RSSI1 and RSSI2.

Choosing another FOFFSET value should result in a significant decrease in the RSSI output, as indicated by the I&D transfer graph. This graph shows that when the frequency of the input signal is equal to F_{offset}, the RSSI output is maximal. When the difference between the input signal and F_{offset} is 0.5 * F_{symbol}, then the output is minimal. On the top of the first side lobe, where F_{IF}-F_{offset}= _ * F_{Symbol} the output is about 5% of the nominal output.

This is also a check for a correct setup of the internal NCO.

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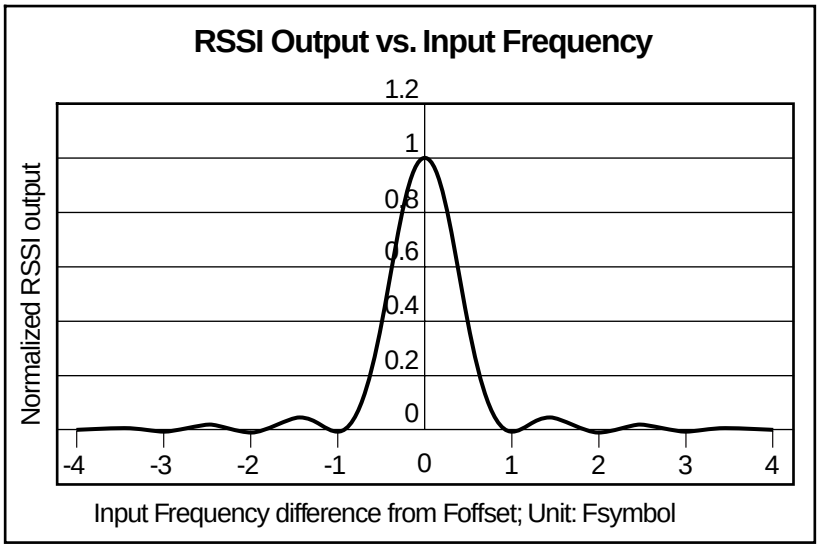
Designing a Link Using the SX061 and the SX043/42 *Continued*

Figure 8:



7. Synchronizing the Receiver: Slip Mode

When the previous steps have been taken, the spreading and despreading should be activated by selecting the spread mode on the CMDR register on the SX043.

It is suggested to start with a slow slip rate. A good starting point for the slip rate is to choose the SX043 register RNS = 4.

By writing a 0x04 to the TRK register of the SX043 the SX043 gets into slip mode. On the RSSI outputs of the SX061 correlation peaks should be visible. The height of the correlation peaks should be comparable to the height of the RSSI signal when no spreading/ despreading was applied. This means a value of about _ * Vdd.

The next step is to set the correlation thresholds of the SX043. A good starting value is about 3 or 4 by writing this value to the lower 4 bits of the RFO register on the SX043. In order to avoid false signal detects, the threshold value should be as high as possible.

To see if the SX043 recognizes the correlation peak, the reception sequence of the SX043 is started by writing a '1' to bit 7 of the RCTL0 register of the SX043. If the threshold was exceeded the TRACKON signal will go high.

8. Synchronizing the Receiver: Track Mode

It is recommended to start with a slow slip rate and a large dither depth.

A good starting point is to choose the SX043 register RNS = 4 for the slip rate and to choose the dither depth at least 10%. This means setting RN4C at 90% of RN4A and RN4D at 110% of RN4A.

Choose the dither rate as 10 (RNT = 10). The same value has to be written to the DELAY register of the programming string. Set the LOCK bit of the programming string to '0'.

After the SX043 now detects a correlation peak, it goes to track-mode. Set the MODE register of the SX061 to 0 to receive a BPSK signal.

Looking at the RSSI2 output monitors the quality of the link. The RSSI2 output is slowly modulated by the frequency difference of the incoming signal and the internal IF. The RSSI2 level should be about _ Vdd. When no data is transmitted the RXD0 and RXD1 should have a constant value. Each transition on this line indicates an error. By setting the mode register to 1 the SX061 interprets the incoming signal as a (D)QPSK signal. Also in this situation there should not be any errors on the RXD0 and RXD1 output. (Even when the system will be used for BPSK data transmission).

Designing a Link Using the SX061 and the SX043/42 *Continued*

9. Setup the Carrier Tracking Loop

The carrier tracking loop is closed by setting the LOCK bit to '1'. The PHASE_GAIN register controls the gain in the carrier tracking loop. The amplitude modulation of the RSSI signal will become much slower when the loop is closed. A value between 5 and 7 should be chosen.

10. Setup the Data Transmission

Once a complete link has been established, data can be transmitted. For correct operation of the data FIFO's of the SX043 write a '1' to the reset FIFO RX/TX of the FCR register. When using the same SX043 for both transmission and reception, the DIF_DATA bit of the SX061 has to be set to '1'.

11. Optimization

For optimal performance the following parameters can be changed.

In order to minimize the power consumption of the SX061 the sample rate has to be chosen as low as possible, without loss of reception quality. 80 samples per symbol is about the minimum attainable value. Changing the sample rate, and therefore the internal clock frequency, also affects the internal IF frequency. This has to be corrected by choosing the appropriate value for the FOFFSET register. It also affects the output of the I&D filters. Therefore new values for the gain registers (ID_GAIN, PWM_GAIN and PHASE_GAIN) can be necessary.

For faster acquisition the slip rate can be increased. The RC section on the RSSI outputs has to be fast enough to detect the correlation peaks and slow enough to suppress the ripple.

General Remarks

A reset of 10ns length needs to be applied on the reset pin using a High-Low-High transition (the same as for the SX043).

All output pads have 4mA CMOS driving capabilities.

The VSS pads need to be connected to a single ground node. They are **not connected** internally (only through substrate).

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Overview of Registers

Table 7:

REGISTER NAME	BIT RANGE	NUMBER OF BITS
PHASE_GAIN	0..3	4
DIV_DSP	4, 5	2
LOCK	6	1
Mode	7, 8	2
DELAY	9..12	4
PWM_GAIN	13..16	4
ID_GAIN	17..20	4
FOFFSET	21..36	16
DIF_DATA	37	1
DIV1_16	38..40	3
DIV25_50	41..44	4
COMP_SEL	45..48	4(for test only)
TEST_MODE	49	1(for test only)
VCO_EXT	50	1(for test only)

Description of Each Register

PHASE_GAIN, 4 bits

PHASE_GAIN defines the gain in the carrier tracking loop. The lower the number, the larger the gain.

DIV_DSP, 2 bits

DIV_DSP divides the internal clock by the following number, which results in the clk_dsp. This clk_dsp is the clock signal for the demodulating DSP.

Table 8:

VALUE OF DIV_DSP	F_{Clk}/F_{clk_dsp}
0	8
1	16
2	32
3	64

LOCK, 1 bit

When LOCK='1' the carrier tracking loop is activated. When LOCK='0' the carrier tracking loop is not used.

Description of Each Register *Continued*

Mode, 2 bits

Mode defines three different modes.

Table 9:

VALUE OF MODE	DESCRIPTION OF MODE
0	For demodulating a BPSK signal
1,2	For demodulating a QPSK signal
3	For tracking an unmodulated carrier

DELAY, 4 bits

This number should be equal to the dither rate register of the SX043. It defines the depth of the FIFO for the generation of the RSSI1 signal in track mode.

PWM_GAIN, 4 bits

This number defines the gain in the RSSI outputs. The smaller the number, the larger the gain in the loop.

ID_GAIN, 4 bits

Gain in the output of the I&D filters. The smaller the number, the larger the gain in the I&D output. The number should be as small as possible, without generating overflows in the I&D output.

FOFFSET, 16 bits

This number defines the IF frequency, generated by the internal numerical oscillator. This number can be calculated as follows:

$$F_{offset} = FOFFSET * F_{clk}/2^{17}.$$

See the description of DIV1_16 and DIV25_50 for the generation of the sample clock.

DIF_DATA, 1 bit

The DIF_DATA bit allows the user to convert a differential transmitting coding scheme (DQPSK or DBPSK) into a non-differential coding scheme (QPSK or BPSK) for reception. This is explained in Table 10.

Table 10:

TRANSMISSION	DIF_DAT A	RECEPTION
BPSK	'1'	BPSK
QPSK	'1'	QPSK
DBPSK	'1'	DBPSK
DQPSK	'1'	DQPSK
DBPSK	'0'	BPSK
DQPSK	'0'	QPSK

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Description of Each Register *Continued*

DIV1_16, 3 bits

This divider relates the output of the VCO to the sample clock (see Table 11).

Table 11:

DIV1_16	F_{VCO}/F_{clk}
0	1
1	2
2	4
3	8
4	16

DIV25_50, 4 bits

This divider relates the output frequency of the reference crystal to the VCO output. This divider is part of the internal PLL.

Table 12:

DIV25_50	F_{VCO}/F_{ref}
5	25
6	30
7	35
8	40
9	45
10	50

COMP_SEL, 4 bits

Each of the 4 bits of the COMP_SEL register has a different function for test purposes. For normal operation the register has to be set up according to Table 13.

Table 13:

BIT#	
0	always set to '1'
1	always set to '0'
2	always set to '0'
3	always set to '0'

TEST_MODE, 1 bit

If TEST_MODE='1' the SX061 is in test mode. For normal operation, TEST_MODE has to be set to '0'.

VCO_EXT, 1 bit

Set to '1' for normal operation.