PEX 8311

ExpressLane PCI Express-to-Generic Local Bus Bridge

Data Book

Version 0.90

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Revision History

Version	Date	Description of Changes
0.10	October, 2005	Initial data book content for Silicon Revision AA.
0.50	November, 2005	Yellow Book release Silicon Revision AA.
0.75	December, 2005	Yellow Book update Silicon Revision AA.
0.85	December, 2005	Initial Blue Book release, Silicon Revision AA.
0.90	April, 2006	Blue Book update. • Corrected device description, to "PCI Express-to-Generic Local Bus Bridge." • Rewrote Chapters 1, 2, 3, and 13. • Chapter 2 – Added missing PMEIN# signal at C16 (was marked as N/C). • Chapter 5 – Clarified 64-bit addressing limitations. • Section 12.1.2 – Changed PME references to PME_IN# and PME_OUT#. Added PCI Express and Local Configuration Space register clarification. • Chapter 18 – split into two chapters, 18 and 19, and renumbered subsequent chapters. Other changes include: – Clarified primary and secondary interface references. – Table 18-5 – Added "MAININDEX/MAINDATA" information to "Main Control Register" row. – Corrected Endpoint mode **Bridge Control** register (**BRIDGECTL**) bit 6 description to indicate Local Bus Reset. – Added missing, blank and corrupted serial EEPROM-handling information to the **Serial EEPROM Control** register *Serial EEPROM Address Width* field (**EECTL**[24:23]) description, • Chapter 22 (was Chapter 21) – Rewrote Section 22.1 and added new Table 22-3 (renumbered all subsequent tables). – Removed VDDQ references. – Removed second paragraph of Section 22.3. – Removed "(PCI)" references from Tables 22-2 and 22-3 (were Tables 21-1 and 21-2, respectively). – Table 22-2 (was Table 21-1) – Changed V_{OUT} and Maximum Power Consumption values. – Table 22-3 (was Table 21-2) – Changed VDD2.5 and V_{IH} values. – Removed Table 21-3. – Removed Table 21-5, and moved its new $Theta_{j-a}$ text and value to the beginning of Section 22.5. – Table 22-5 (was Table 21-6) – Changed V_{IH} maximum value. • Applied miscellaneous changes and corrections.

Preface

The information contained in this document is subject to change without notice. This preliminary document will be updated periodically as new information is made available.

Scope

This document is the primary source of technical documentation describing the features, functions and operations of the PLX Technology ExpressLane™ PEX 8311 PCI Express-to-Generic Local Bus bridge.

Intended Audience

This data book is intended for hardware and software engineers developing systems hardware and software for the PEX 8311 device, as well as engineering managers evaluating the PEX 8311 for use in their designs.

Supplemental Documentation

This data book assumes that the reader is familiar with the following documents:

- PCI Special Interest Group (PCI-SIG)

  3855 SW 153rd Drive, Beaverton, OR 97006 USA

  Tel: 503 619-0569, Fax: 503 644-6708, http://www.pcisig.com
  - *PCI Local Bus Specification, Revision 3.0*
  - *PCI Local Bus Specification, Revision 2.2*
  - *PCI to PCI Bridge Architecture Specification, Revision 1.1*
  - *PCI Bus Power Management Interface Specification, Revision 1.1*
  - *PCI Express Base Specification, Revision 1.0a*
  - *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0*
  - *PCI Standard Hot Plug Controller and Subsystem Specification, Revision 1.0*
- The Institute of Electrical and Electronics Engineers, Inc.

  445 Hoes Lane, PO Box 1331, Piscataway, NJ 08855-1331, USA

  Tel: 800 678-4333 (domestic only) or 732 981-0060, Fax: 732 981-1721, http://www.ieee.org
  - *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture, 1990*
  - *IEEE 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*
  - *IEEE Standard 1149.1b-1994, Specifications for Vendor-Specific Extensions*
- *Intelligent I/O (I_2O) Architecture Specification, Revision 1.5*, 1997

  I_2O Special Interest Group (I_2O SIG®),

  http://www.developer.osdl.org/dev/opendoc/Online/Local/I20/index.html

Supplemental Documentation Abbreviations

Note: *In this data book, shortened titles are provided to the previously listed documents. The following table lists these abbreviations.*

Abbreviation	Document
PCI r3.0	*PCI Local Bus Specification, Revision 3.0*
PCI r2.2	*PCI Local Bus Specification, Revision 2.2*
PCI-to-PCI Bridge r1.1	*PCI to PCI Bridge Architecture Specification, Revision 1.1*
PCI Power Mgmt. r1.1	*PCI Bus Power Management Interface Specification, Revision 1.1*
PCI Express Base 1.0a	*PCI Express Base Specification, Revision 1.0a*
PCI Express-to-PCI/ PCI-X Bridge r1.0	*PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0*
PCI Standard Hot Plug r1.0	*PCI Standard Hot Plug Controller and Subsystem Specification, Revision 1.0*
I_2O r1.5	*Intelligent I/O (I_2O) Architecture Specification, Revision 1.5*
IEEE Standard 1149.1-1990	*IEEE Standard Test Access Port and Boundary-Scan Architecture*

Data Assignment Conventions

Data Width	PEX 8311 Convention
Half byte (4 bits)	Nybble
1 byte (8 bits)	Byte
2 bytes (16 bits)	Word
4 bytes (32-bits)	DWORD/DWord/Dword
8 bytes (64-bits)	QWORD/QWord/Qword

Terms and Abbreviations

The following table lists common terms and abbreviations used in this document. Terms and abbreviations defined in the *PCI Express r1.0a* are not included in this table.

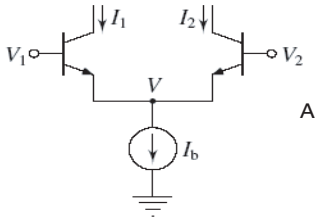
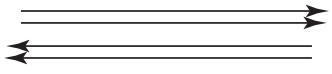
Terms and Abbreviations

Terms and Abbreviations	Definition
#	Indicates an Active-Low signal.
ACK	Acknowledge Control Packet. A control packet used by a destination to acknowledge data packet receipt. A signal that acknowledges the signal receipt.
ADB	Allowable Disconnect Boundary.
ADQ	Allowable Disconnect Quantity. In PCI Express, the ADQ is a buffer size. Used to indicate memory requirements or reserves.
Asynchronous	Inputs and Outputs can be asynchronous to a clock. Level sensitive signals.
BAR	Base Address Register.
C Mode	Non-Multiplexed Local Bus interface based on 80960CX RISK Processor Protocol.
CA	Completion with Completer Abort status.
CFG	Access initiated by PCI Configuration transactions on the primary interface.
Clock cycle	One period of the clock.
Completer	Device addressed by a *requester.*
CRS	Configuration Retry Status.
CSR	Configuration Status register; Control and Status register; Command and Status register.
DAC	Dual Address cycle. A PCI transaction wherein a 64-bit address is transferred across a 32-bit data path in two Clock cycles.
Destination Bus	Target of a transaction that crosses a bridge is said to reside on the destination bus.
DLLP	Data Link Layer Packet (originates at the Data Link Layer); can contain Flow Control (FCx DLLPs) acknowledge packets (ACK and NAK DLLPs); and power management (PMx DLLPs).
DM	Direct Master. A type of transfer that originates from an external Local Bus master and addresses a device in PCI Express Space.
DMA	Direct Memory Access. Method of transferring data between a device and main memory, without intervention by the CPU.
Downstream	Transactions that are forwarded from the primary interface to the secondary interface of a bridge are said to be *flowing downstream*.
DS	Direct Slave. A type of transfer that originates from PCI Express Space and addresses a device on the Local Bus.
ECRC	End-to-end Cyclic Redundancy Check (CRC)
EE	Access initiated by the Serial EEPROM Controller during initialization.
Endpoint mode	The primary interface is the PCI Express interface. The secondary interface is the Local Bus interface.
Endpoints	Devices, other than the Root Complex and switches, that are requesters or completers of PCI Express transactions, as follows: • Endpoints can be PCI Express endpoints or ***legacy*** endpoints. • ***Legacy*** endpoints can support I/O and Locked transaction semantics. PCI Express endpoints do ***not support*** I/O nor Locked transaction semantics.

Terms and Abbreviations *(Cont.)*

Terms and Abbreviations	Definition
FCP	Flow Control Packet devices on each link exchange FCPs, which carry *header* and *data payload* credit information for one of three packet types – Posted requests, Non-Posted requests, and Completions.
Host	Computer that provides services to computers that connect to it on a network. Considered in charge of the other devices connected to the bus.
HwInit	Hardware initialized register or register bit. The register bits are initialized by a PEX 8311 hardware initialization mechanism or PEX 8311 Serial EEPROM register initialization feature. Register bits are Read-Only after initialization and can only be reset with "Fundamental Reset."
I	CMOS Input.
I/O	CMOS Bi-Directional Input/Output.
J mode	Multiplexed Local Bus interface based on 80960JX RISK Processor Protocol.
JTAG	Joint Test Action Group
Lane	A PCI Express physical data link consisting of a differential signal pair in each direction.
Layers	PCI Express defines three layers: • ***Transaction Layer*** – The primary function of the Transaction Layer is TLP assembly and disassembly. The major components of a transaction layer packet (TLP) are *Header*, *Data Payload*, and an optional *Digest* field. • ***Data Link Layer*** – The primary task of the Data Link Layer is to provide link management and data integrity, including error detection and correction. This layer defines the data control for PCI Express. • ***Physical Layer*** – The primary value to users is that this layer appears to the upper layers as PCI. It connects the lower protocols to the upper layers.
LCPU	Local Bus Central Processing Unit (Local Bus Intelligent Device).
LCS	Local Configuration Space.
Local Bus	Interface that provides an interconnect of other components to a PLX device.
Local Bus Master	Local Bus device that initiates transfers.
Local Bus Slave (Target)	Bus device that responses to Local Bus Master-initiated transactions.
Local Configuration Space (**LCS**)	The set of registers used to configure and control operations on the PEX 8311 Local Bus.
LTSSM	Link Training and Status State Machine.
MM	PCI Express Configuration Space (**PECS**) Register access initiated by PCI Memory transactions on the primary or secondary interface, using the address range defined by **PCI Base Address 0**.
MSI	Message Signaled Interrupt.
MWI	Memory Write and Invalidate.
NAK	Negative Acknowledge.
NMI	Non-Maskable Interrupt – the highest-priority interrupt recognized.
Non-Posted Transaction	Memory Read, I/O Read or Write, or Configuration Read or Write that returns a completion to the master.
NS	No Snoop.
O	CMOS Output.
OD	Open Drain.

Terms and Abbreviations *(Cont.)*

Terms and Abbreviations	Definition
Originating Bus	Master of a transaction that crosses a bridge is said to reside on the *originating bus*.
Packet Types	There are three packet types: • ***TLP***, Transaction Layer Packet • ***DLLP***, Data Link Layer Packet • ***PLP***, Physical Layer Packet
PCI	Peripheral Component Interconnect. The Original 32/64 bit parallel interconnect standard, defined in the *PCI r2.2*. When listed in the signal tables, indicates PCI-compliance.
PCI Express Configuration Space (**PECS**)	The set of PEX 8311 registers used to initialize, enumerate, and operate the PEX 8311's PCI Express interface.
PCI Express Requester	Generates a "Request" packet, thereby initiating a transaction on the PCI Express interface.
PCI Express Target	Returns data and/or completions on the PCI Express interface, to the Requester.
PCI Express Transaction	Read, write, read burst, or write burst operation on the PCI Express interface. Includes an Address phase, followed by one or more data phases.
PCI Express Transfer	During a transfer, data is moved from the source to the destination on the PCI Express interface. TRDY# and IRDY# assertion indicates a Data transfer.
PECS	PCI Express Configuration Space.
Port	Interface between a PCI Express component and the ***link***. Consists of transmitters and receivers, as follows: • An ***ingress*** port receives a packet. • An ***egress*** port transmits a packet. • A ***link*** is a physical connection between two devices that consists of x*N* ***lanes***. • An x1 link consists of one Transmit and one Receive signal, wherein each signal is a differential pair. This is one lane. There are four lines or signals in an x1 link.  A Differential Pair  A Differential Pair in each direction = one *Lane* This is an *x1 Link* *There are four signals*
Posted Transaction	Memory Write that does not return a completion to the master.
Preempt	Ongoing transaction is interrupted to perform another transaction.
Primary Interface	Interface closest to the PCI Express Root Complex (Endpoint mode) or the Local host CPU (Root Complex mode).
PU	Signal is internally pulled up.

Terms and Abbreviations *(Cont.)*

Terms and Abbreviations	Definition
QoS	Quality of Service.
RC	Root Complex.
RCB	Read Boundary Completion.
Request packet	A *Non-Posted Request packet* transmitted by a requester contains a completion packet returned by the associated completer. A *Posted Request packet* transmitted by a requester does not contain a completion packet returned by the completer.
Requester	Device that originates a transaction or places a transaction sequence into the PCI Express fabric.
RO	Read-Only register or register bit. Register bits are Read-Only and cannot be altered by software. Register bits are initialized by a PEX 8311 hardware initialization mechanism or PEX 8311 Serial EEPROM register initialization feature.
RO	Relaxed Ordering.
Root Complex	Denotes the device that connects the CPU and memory subsystem to the PCI Express fabric. It can support one or more PCI Express ports.
Root Complex Mode	The primary interface is the Local Bus interface. The secondary interface is the PCI Express interface.
RsvdP	***Reserved*** and Preserved. ***Reserved*** for future RW implementations. Registers are Read-Only and must return 0 when read. Software must preserve value read for writes to bits.
RsvdZ	***Reserved*** and Zero. ***Reserved*** for future RW1C implementations. Registers are Read-Only and must return 0 when read. Software must use 0 for writes to bits.
RW	Read-Write register. Register bits are Read-Write and set or cleared by software to the needed state.
RW1C	Read-Only Status. Write 1 to clear status register. Register bits indicate status when read; a set bit indicating a status event is cleared by writing 1. Writing 0 to RW1C bits has no effect.
RX	Received Packet.
SC	Successful Completion.
Secondary Interface	The interface farthest from the PCI Express Root Complex (Endpoint mode) or the Local host CPU (Root Complex mode).
SPI	Serial Peripheral Interface
STRAP	Strapping pads (*such as*, BAR0ENB#, IDDQN#, MODE[1:0], and USERi) must be connected to H or L on the board.
STS	Sustained Three-State Output, Driven High for One CLK before Float.
Switch	Device that appears to software as two or more logical bridges.
TAP	Test Access Port.
TC	Traffic Class.
TLP	Translation Layer Packet.
TP	Totem Pole.
TS	Three-State Bi-Directional.
TX	Transmitted Packet.

Terms and Abbreviations *(Cont.)*

Terms and Abbreviations	Definition
Upstream	Transactions that are forwarded from the secondary interface to the primary interface of a bridge are said to be *flowing upstream*.
UR	Unsupported request.
VC	Virtual Channel.
WO	Write-Only register. Used to indicate that a register is written by the Serial EEPROM Controller.

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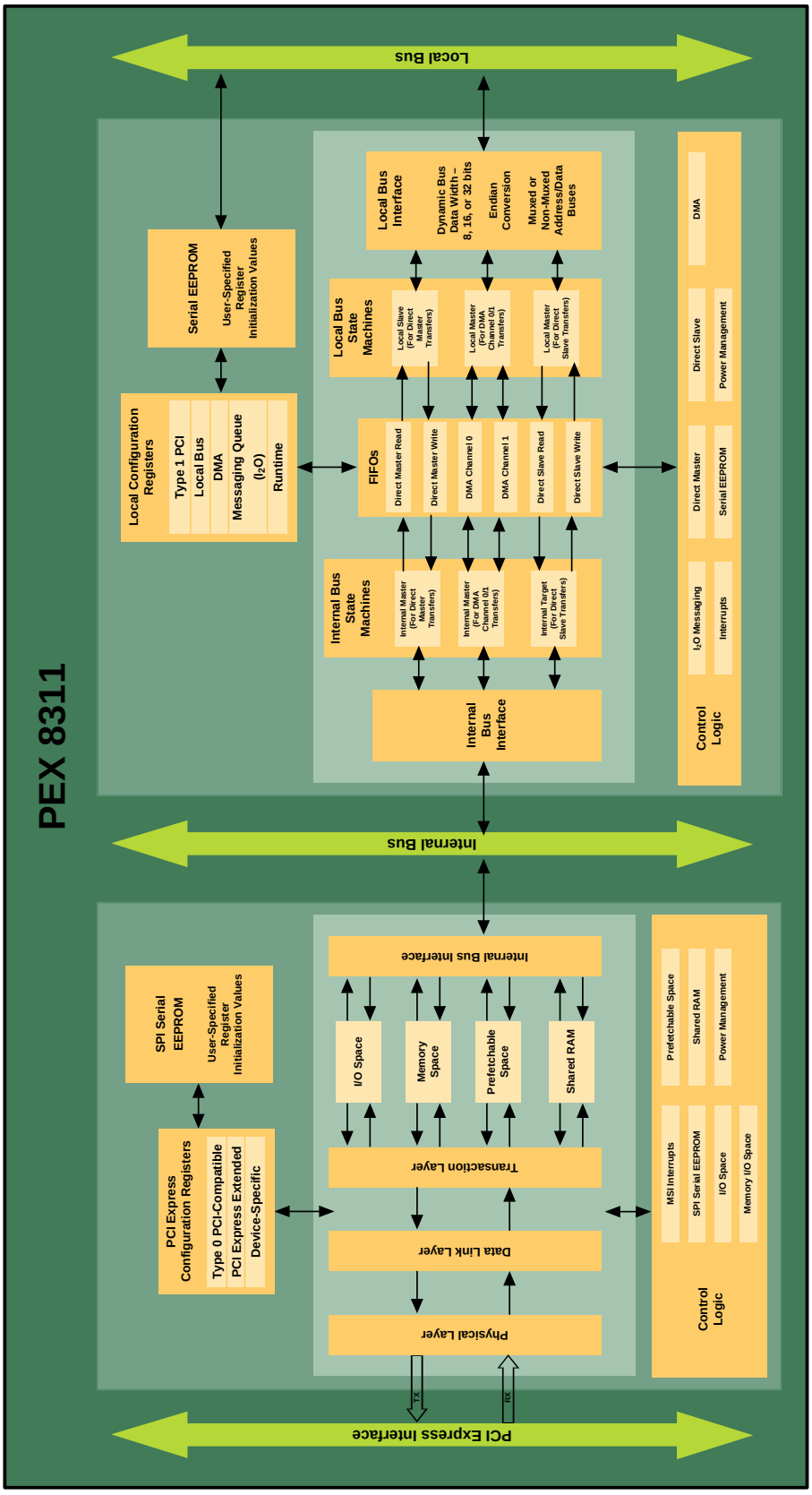
Chapter 1 Introduction

1.1 Features

- Standards compliant
  - *PCI Local Bus Specification, Revision 3.0 (PCI r3.0)*
  - *PCI Local Bus Specification, Revision 2. 2 (PCI r2.2)*
  - *PCI to PCI Bridge Architecture Specification, Revision 1.1 (PCI-to-PCI Bridge r1.1)*
  - *PCI Bus Power Management Interface Specification, Revision 1.1 (PCI Power Mgmt. r1.1)*
  - *PCI Express Base Specification, Revision 1.0a (PCI Express r1.0a)*
  - *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0 (PCI Express-to-PCI/ PCI-X Bridge r1.0)*
  - *PCI Standard Hot Plug Controller and Subsystem Specification, Revision 1.0 (PCI Standard Hot Plug r1.0)*
  - *Intelligent I/O (I_2O) Architecture Specification, Revision 1.5 (I_2O r1.5)*
- Forward and reverse bridging between the PCI Express interface and Local Bus
- Root Complex and Endpoint PCI Express mode support
- PCI Express single-lane (x1) port (one Virtual Channel)
- PCI Express 2.5 Gbps per direction
- PCI Express full Split Completion protocol
- SPI (Serial Peripheral Interface) Serial EEPROM port
- Internal 8-KB shared RAM available to PCI Express and Local Bus
- General-purpose I/O balls – Four GPIO balls, one GPI ball, and one GPO ball
- Low-power CMOS in 337-ball PBGA Package
- 1.5V and 2.5V core operating voltage, 3.3V I/O
- Bus Mastering interface between a PCI Express port and 32-bit, 66-MHz processor Local Bus
  - *Hot-Plug r1.1*-compatible in Endpoint mode
  - Direct connection to two types of Local Bus processor interface
    - **C Mode (non-multiplexed address/data)** – Intel i960, DSPs, custom ASICs and FPGAs, and others
    - **J Mode (multiplexed address/data)** – Intel i960, IBM PowerPC 401, DSPs, FPGAs, and others
  - Asynchronous clock input for Local Bus
  - Commercial Temperature Range operation
  - *IEEE 1149.1* JTAG boundary scan

- Three Data Transfer modes – *Direct Master*, *Direct Slave*, and *DMA*
  - **Direct Master** – Upstream traffic data transfer generation originating from a Master on the Local Bus and is addressed to a PCI Express device
    - Two Local Bus Address spaces to the PCI Express Space – one to PCI Express memory and one to PCI Express I/O
    - Generates PCI Memory and I/O transaction types, including Memory Write/Read, I/O Write/Read, and Type 0 and Type 1 configuration in Root Complex Mode
    - Read Ahead, Programmable Read Prefetch Counter(s) (all modes)
  - **Direct Slave** – Downstream traffic data transfer between a Master on the PCI Express port and a 32-, 16-, or 8-bit Local Bus device
    - Two general-purpose Address spaces to the Local Bus and one Expansion ROM Address space
    - Delayed Write, Read Ahead, Posted Write, Programmable Read Prefetch Counter
    - Programmable Local Bus Ready timeout and recovery
  - **DMA** – PEX 8311 services data transfer descriptors, mastering on the PCI Express interface and Local Bus during transfer
    - Two independent channels
    - **Block mode** – Single descriptor execution
    - **Scatter/Gather mode** – Descriptors in PCI Express or Local Bus memory; Linear descriptor list execution; Dynamic descriptor DMA Ring Management mode with Valid bit semaphore control; Burst descriptor loading
    - Hardware EOT/Demand controls to stop/pause DMA in any mode
    - Programmable Local Bus burst lengths, including infinite burst
  - Six independent, programmable FIFOs – Direct Master Read and Write, Direct Slave Read and Write, DMA Channel 0 and Channel 1
  - Advanced features common to Direct Master, Direct Slave, and DMA
    - Zero wait state burst operation
    - 264-Mbps bursts on the Local Bus
    - Deep FIFOs, which prolong maximum PCI Express package generation
    - Unaligned transfers on the PCI Express interface and Local Bus
    - On-the-fly Local Bus Endian conversion
    - Programmable Local Bus wait states
    - Parity checking on the PCI Express interface and Local Bus
- *I_2O r1.5*-Ready Messaging Unit
- Twelve 32-bit Mailbox (eight on the Local and four on the PCI Express end of the logic) and two 32-bit Doorbell registers enable general-purpose messaging
- Reset and interrupt signal directions configurable for Root Complex and Endpoint applications
- Programmable Interrupt Generator
- Microwire serial EEPROM interface
  - Stores user-specified power-on/reset configuration register values
- **LCS** register-compatible with the PCI 9054, PCI 9056, and PCI 9656

Figure 1-1. PEX 8311 Block Diagram



1.2 Overview

The ExpressLane™ PEX 8311 is a PCI Express-to-Generic Local Bus bridge. This device features PLX proprietary Data Pipe Architecture® technology. This technology consists of powerful, flexible engines for high-speed Data transfers, as well as intelligent Messaging Units for managing distributed I/O functions.

1.2.1 PCI Express Endpoint Interface

The PEX 8311 includes the following PCI Express Endpoint Interface features:

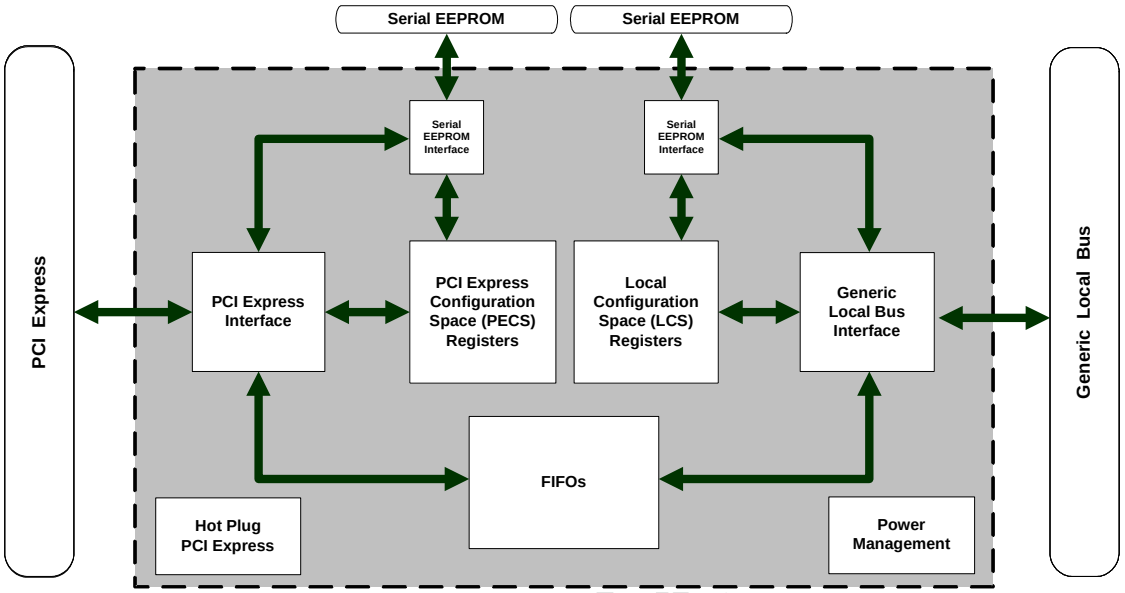
- Full 2.5 Gbps per direction
- Single lane and Single virtual channel operation
- Compatible with multi-lane and multi-virtual channel PCI Express devices
- Packetized serial traffic with PCI Express Split Completion protocol
- Data Link Layer CRC generator and checker
- Automatic Retry of bad packets
- Integrated low-voltage differential drivers
- 8b/10b signal encoding
- In-band interrupts and messages
- Message Signaled Interrupt (MSI) support

1.2.2 High-Speed Data Transfers

Data Pipe Architecture technology provides independent Direct Transfer and DMA methods for moving data. Data Pipe Architecture technology data transfer supports the following:

- PCI Express-to-Local Bus Burst transfers at the maximum bus rates (Direct Slave)
- PCI Express Memory-Mapped Single access to internal configuration registers
- PCI Express Type 0 Single access to internal **LCS** registers
- PCI Express Memory-Mapped Single/Burst access to internal shared RAM
- PCI Express Configuration access to PCI configuration registers (Endpoint mode only)
- Local Bus access to PCI Express (Direct Master)
- Local Bus Single access to Local Bus internal configuration registers
- Local Bus Configuration access to PCI Express configuration registers (Root Complex mode only)
- Local Bus Memory-Mapped Single/Burst access to internal shared RAM
- Unaligned transfers on Local Bus
- On-the-fly Local Bus Endian conversion
- Programmable Local Bus wait states
- Parity checking on both sides

Figure 1-2. High-Speed Data Transfers



1.2.2.1 Direct Transfers

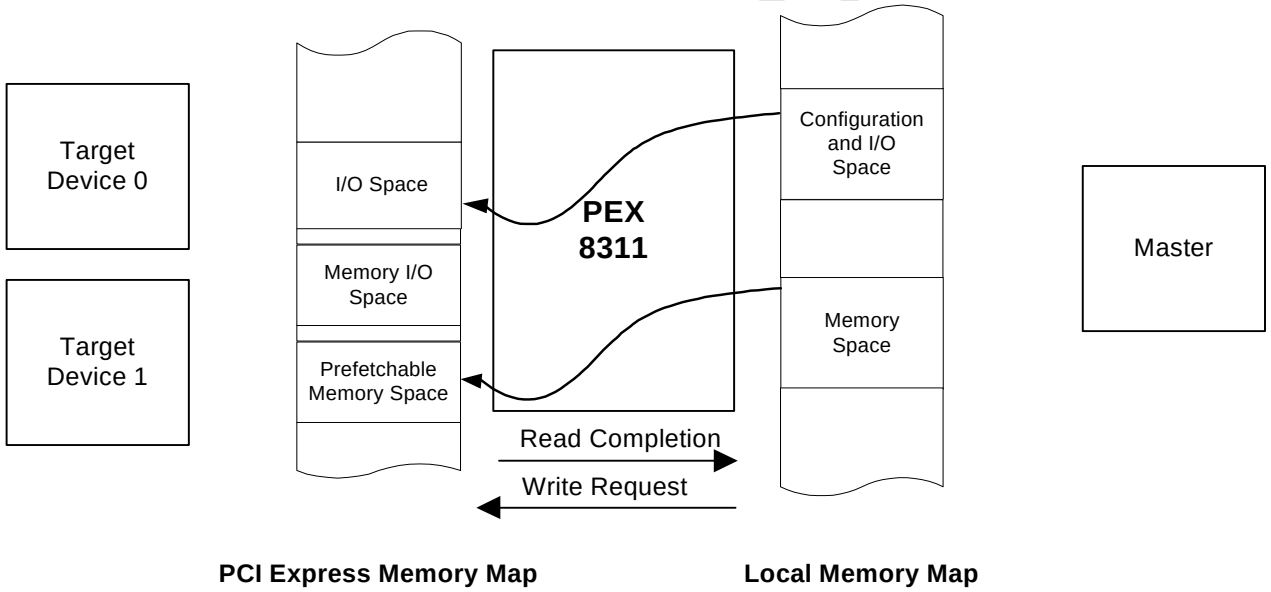
Data Pipe Architecture technology Direct Transfers are used by a Transfer Initiator on the PCI Express or Local Bus interface to move data through the PEX 8311 to a device on the other bus. The Transfer Initiator takes responsibility for moving the data into the PEX 8311 on a Write, or out of the PEX 8311 on a Read. The PEX 8311 is responsible for moving the data out to the target device on a write, or in from the target device on a read.

Direct Master

When a master on the Local processor bus uses Direct Transfer, this is termed a *Direct Master transfer*. The PEX 8311 becomes an upstream traffic generator on the PCI Express interface. Data Pipe Architecture technology provides independent FIFOs for Direct Master Read and Write transfers. It also supports mapping of one or more independent Direct Master Local Bus Address spaces to PCI Express addresses, as illustrated in Figure 1-3.

Direct Master transfers support generation of PCI Memory and I/O transaction types, including Type 0 and Type 1 cycles for system configuration in Root Complex mode only.

Figure 1-3. Direct Master Address Mapping

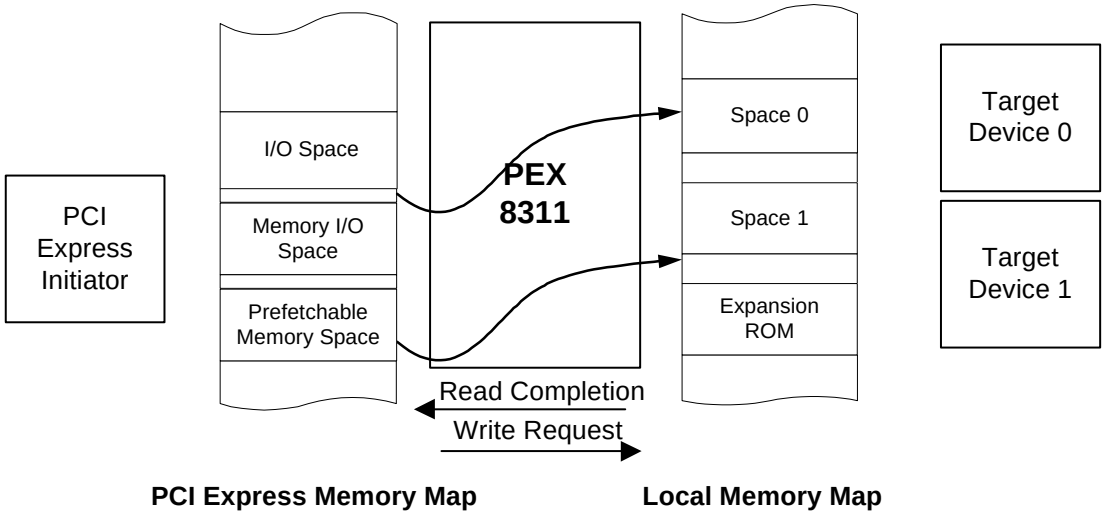


Direct Slave

When downstream traffic is initiated to the PEX 8311 by another PCI Express device on the PCI Express interface, this is termed a *Direct Slave transfer*. The PEX 8311 is a slave (technically, a target) on the PCI Express link. Data Pipe Architecture technology provides independent FIFOs for Direct Slave Read and Write transfers. It also supports mapping of one or more independent Direct Slave PCI Express Address spaces to Local Bus addresses, as illustrated in Figure 1-4.

With software, Direct Slave transfers support Local Bus Data transfers of various widths (*for example*, on a 32-bit Local Bus, data widths of 8, 16, and 32 bits are supported).

Figure 1-4. Direct Slave Address Mapping



1.2.2.2 DMA

When a device initiates data traffic on either bus utilizing Data Pipe Architecture technology DMA transfers, instead of the Master moving data, it places a description of the entire transfer in the PEX 8311 registers and allows the PEX 8311 to perform the entire Data transfer with its DMA engine. This offers two main benefits:

- Data movement responsibilities are off-loaded from the Master. A transfer descriptor is short and takes little effort on the part of the Master to load. Once the descriptor is loaded into the PEX 8311, the Master is free to spend its time and resources elsewhere.
- Because the PEX 8311 supports multiple DMA channels, each with its own FIFO, it can simultaneously service multiple PCI Express and processor Local Bus masters. During DMA transfers, the PEX 8311 masters each bus. Consequently, during DMA transfers, there are no external masters to Retry. During DMA transfers, when the PEX 8311 is Retried or Data Transfer is preempted on either bus, it can simply change context to another transfer and continue. Furthermore, DMA transfers can simultaneously run with Direct Master and Direct Slave transfers, providing support for several simultaneous Data transfers. Direct Master and Direct Slave transfers retain higher priority than DMA.

Data Pipe Architecture technology supports two DMA transfer modes – *Block* and *Scatter/Gather.*

DMA Block Mode

DMA Block mode is the simplest DMA mode. A Local Bus Master or PCI Express upstream programs the description of a single transfer in the PEX 8311 and sets the Start bit(s) (DMACSR*x*[1]=1). The PEX 8311 indicates DMA completion to the Master, by setting a Done bit in one of its registers that the Master polls (DMACSRx[4]) or by asserting an interrupt.

DMA Scatter/Gather Mode

In most cases, however, one descriptor is not sufficient. A Local Bus Master or PCI Express upstream typically generates a list of several descriptors in its memory before submitting them to the PEX 8311. In these cases, DMA Scatter/Gather mode is used to enable the PEX 8311 list processing with minimal master intervention.

With DMA Scatter/Gather mode, the Local Bus Master or PCI Express upstream device tells the PEX 8311 the location of the first descriptor in its list, sets the Start bit(s) (DMACSR*x*[1]=1), then waits for the PEX 8311 to service the entire list. This offloads both data and DMA descriptor transfer responsibilities from the Master.

Data Pipe Architecture technology supports DMA Scatter/Gather mode descriptor lists in PCI or Local Bus memory. It also supports linear and circular descriptor lists, the latter being termed *DMA Ring Management mode*.

DMA Ring Management mode uses a Valid bit in each descriptor to enable dynamic list management. In this case, the Local Bus Master or PCI Express upstream device and the PEX 8311 continuously "walk" the descriptor list, the Master in the lead filling invalid descriptors, setting the Ring Management Valid bit(s) when done (DMASIZ*x*[31]=1), and the PEX 8311 following behind servicing valid descriptors, resetting the Valid bit when done. The PEX 8311 supports write back to serviced descriptors, allowing status and actual transfer counts to post prior to resetting the Valid bit(s).

Hardware DMA Controls – EOT and Demand Mode

To optimize DMA transfers in datacom/telecom and other applications, Data Pipe Architecture technology supports hardware controls of the Data transfer.

With End of Transfer (EOT), an EOT# signal is asserted to the PEX 8311 to end the transfer. When EOT# is asserted, the PEX 8311 immediately terminates the current DMA transfer and writes back to the current DMA descriptor the actual number of bytes transferred. Data Pipe Architecture technology also supports unlimited bursting. EOT and unlimited bursting are especially useful in applications *such as* Ethernet adapter boards, wherein the lengths of read packets are not known until the packets are read.

In DMA Demand mode, a hardware DREQ*x*#/DACK*x*# signal pair is used to pause and resume the DMA transfer. Data Pipe Architecture technology provides one **DREQ*x*#/DACK*x*#** signal pair for each DMA channel. Demand mode provides a means for a peripheral device with its own FIFO to control DMA transfers. The peripheral device uses Demand mode both to pause the transfer when the FIFO is full on a write or empty on a read and to resume the transfer when the FIFO condition changes to allow the Data transfer to continue. Demand mode can also be used for many non-FIFO-based applications.

1.2.3 Intelligent Messaging Unit

Data Pipe Architecture technology provides two methods for managing system I/O through messaging.

The first method is provided through general-purpose Mailbox and Doorbell registers. When all PCI Express-based components are under direct control of the system designer (*for example*, an embedded system, *such as* a set-top box), it is often desirable to implement an application-specific Messaging Unit through the general-purpose Mailbox and Doorbell registers.

The second method is provided through Intelligent I/O (I_2O) support. As the device-independent, industry-standard method for I/O control, I_2O is the easiest way to obtain interoperability of all PCI-based components in the system.

1.2.4 PEX 8311 I/O Accelerators

The PEX 8311 *PCI Express r1.0a*-compliant device extends the PLX family of PEX 8000 series devices to provide compatibility to the new PCI Express interface.

The PCI Express Configuration Space (**PECS**) register set is backward-compatible with the PEX 8111 PCI Express-to-PCI Bus Bridge. The Local Configuration Space (**LCS**) register set is backward-compatible with the previous generation PCI 9054, PCI 9056, and PCI 9656 I/O Accelerators.

The PEX 8311 incorporates the industry-leading PLX Data Pipe Architecture technology, including programmable Direct Master and Direct Slave transfer modes, intelligent DMA engines, and PCI messaging functions.

1.2.5 Applications

The PEX 8311 continues the PLX tradition of extending its product capabilities to meet the leading edge requirements of I/O intensive embedded-processor applications. The PEX 8311 builds upon the industry-leading PLX PCI 9054, PCI 9056, and PCI 9656 products, providing an easy upgrade path to PCI Express Interface and Local Bus operation. The PEX 8311 supports all legacy processors and designs, using the C and J Local Bus interfaces. Additionally, the PEX 8311 offers several important new features that expand its applicability and performance.

1.2.5.1 High-Performance PCI Express Endpoint Boards

The PEX 8311 is also designed for traditional PCI Express Endpoint board applications to provide an easy migration of existing designs based on internal PCI Bus interconnect to PCI Express interface to achieve higher bandwidth. Specific applications include high-performance communications, networking, disk control, and data encryption adapters.

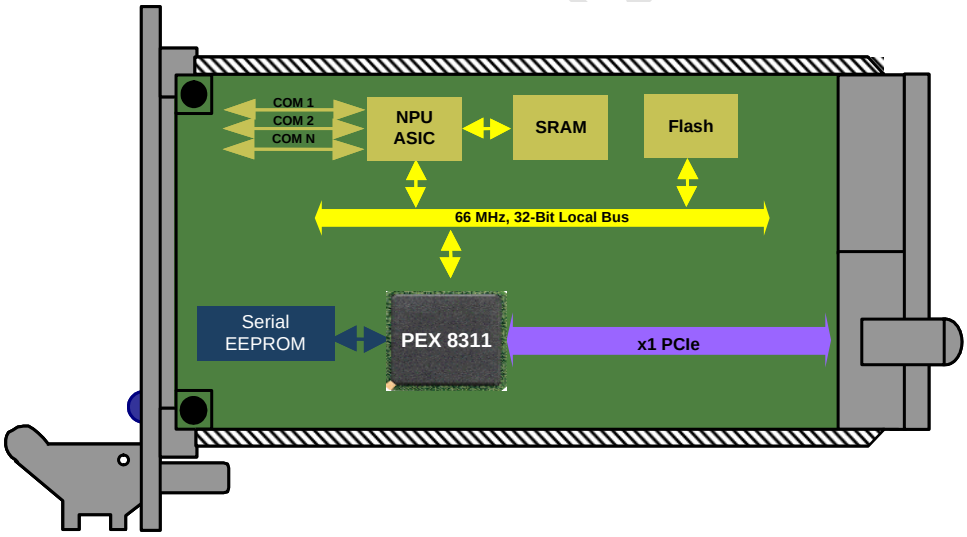
Today, Power Management and Green PCs are major initiatives in traditional PCI applications. The PEX 8311 supports Active and Device State Power Management.

Figure 1-5 illustrates the PEX 8311 in a PCI Express Endpoint board application with a CPU, with C or J Local Bus modes.

The C and J Local Bus modes, in addition to supporting Intel i960 processors, are being adopted by designers of a wide variety of devices, ranging from DSPs to custom ASICs, because of their high-speed, low overhead, and relative simplicity.

For applications using I/O types not supported directly by the processor, *such as* SCSI for storage applications, the PEX 8311 provides a high-speed interface between the processor and PCI Express-based I/O devices. Furthermore, the Local Bus interface supports processors that do not include integrated I/O.

Figure 1-5. PEX 8311 PCI Express Adapter Board with C or J Mode Processor



1.2.5.2 High-Performance Embedded Root Complex Designs

I/O intensive embedded Root Complex designs are another major PEX 8311 application, which include network switches and routers, printer engines, and set-top boxes, CompactPCI system boards, and industrial equipment.

While the support requirements of these embedded Root Complex designs share many similarities with Endpoint board designs, *such as* their requirement for intelligent management of Local Bus I/O, PCI Express Board Electromechanical guidelines, there are three significant differences.

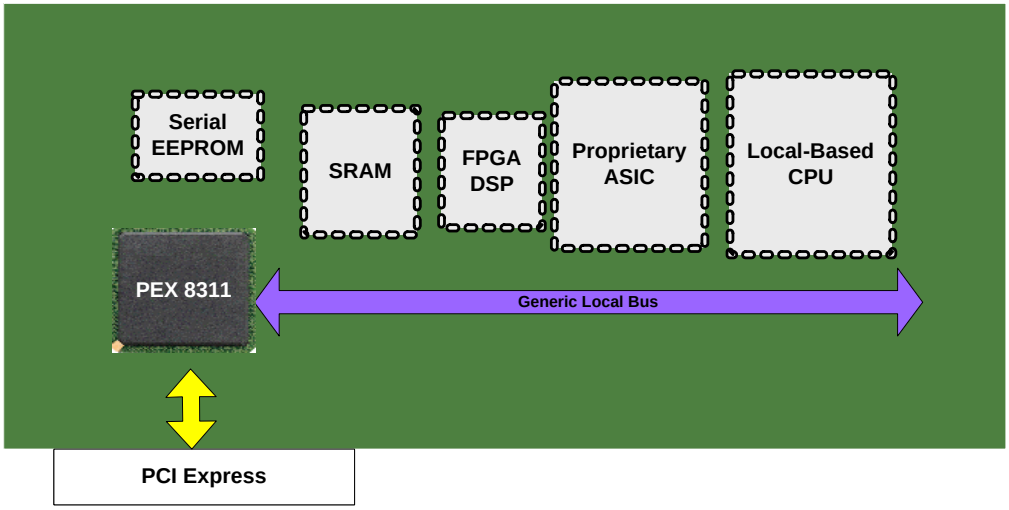
First, the Root Complex is responsible for configuring the PCI Express System hierarchy. The PEX 8311 supports PCI Type 0 and Type 1 Configuration cycles to accomplish this.

Second, the Root Complex is responsible for accepting MSI from PCI Express downstream devices, as well as providing Root Complex specific Configuration Registers to control the overall system. The PEX 8311 provides MSI acceptance that is routed to the Local Bus as a Local Bus Interrupt or Local System Error signal.

Third, for Root Complex, the directions of the reset signal reverse. The PEX 8311 includes a strapping option for reversing the directions of the PCI Express and Local Bus reset signals. In one setting, the direction is appropriate for an Endpoint; in the other setting, it is appropriate for a Root Complex.

Figure 1-6 illustrates the PEX 8311 in an embedded Root Complex system.

Figure 1-6. PEX 8311 in Embedded Root Complex System



1.2.6 Data Transfer

The PEX 8311 allows for Local Burst Transfers up to 264 Mbps and six Programmable FIFOs for Zero Wait State Burst operation. Table 1-1 delineates FIFO depth.

Table 1-1. FIFO Depth

FIFO	Depth
Direct Master Write	64 Dwords
Direct Master Read	32 Dwords
Direct Slave Write	64 Dwords
Direct Slave Read	32 Dwords
DMA Channel 0	64 Dwords
DMA Channel 1	64 Dwords

The PEX 8311 includes the following data transfer features:

- **Unaligned Transfer Support** – Allows transferring data on any byte-boundary combination of the Local Address spaces. Only the last and first data of the PCI Express packet can be unaligned.
- **Big/Little Endian Conversion** – Supports dynamic switching between Big Endian (Address Invariance) and Little Endian (Data Invariance) operations for Direct Master, Direct Slave, DMA, and internal Register accesses on the Local Bus.
- **On-the-Fly Endian Conversion of Local Bus Data Transfers** – Supports on-the-fly Endian conversion of Local Bus Data transfers. The Local Bus can be applied as Big/Little Endian by using the BIGEND# input ball or programmable internal register configuration. When BIGEND# is asserted, it overrides the internal register configuration during Direct Master, and internal Register accesses on the Local Bus.
- **C and J Mode Data Transfers** – Provided to communicate with i960, PPC401, DSPs, ASICs, and FPGA processors, using three possible Data Transfer modes:
  - Direct Master Operation
  - Direct Slave Operation
  - DMA Operation
- **Direct Master** – A dedicated data path within the PEX 8311 that allows a master device on the Local Bus to initiate Memory, I/O, or Configuration accesses to devices in the PCI Express Space. Dedicated FIFOs provide support for single-cycle bursts on the Local Bus. For DM reads, the FIFOs can be used in conjunction with PCI Express Read Ahead functions to significantly reduce latency times for sequential reads.
- **Direct Slave** – A dedicated data path within the PEX 8311 that allows PCI Express Requesters to access devices on the PEX 8311 Local Bus by way of Memory- or I/O-Mapped accesses. FIFOs enable bursting on the Local Bus. Local Prefetch functions are provided to reduce latency of follow-on sequential reads.
- **Three PCI Express-to-Local Address Spaces** – The PEX 8311 supports three PCI Express-to-Local Address spaces in Direct Slave mode – Space 0, Space 1, and Expansion ROM. These spaces allow any PCI Express upstream device to access the Local Bus Memory spaces with programmable wait states, bus data width, burst capabilities, and so forth.

- **Direct Master and Direct Slave Read Ahead Mode** – Allows prefetched data to be read from the internal Read FIFO instead of the external bus. The address must be subsequent to the previous address and Dword-aligned. This feature allows for increased bandwidth utilization through reduced data latency.
  - **PCI Express Read Ahead for Direct Master Reads** – The DM Read FIFO works in conjunction with Read Ahead capability in the PCI Express interface, to greatly reduce completion time for follow-on sequential Reads from the host. *For example*, when the Local CPU reads one DWord mapped as PCI Express Space, up to 4 KB of sequential data can be requested in anticipation of a sequential Read from the Local Master.
  - **Local Bus Read Ahead for Direct Slave Reads** – The PEX 8311 includes programmable control to prefetch data during Direct Slave and Direct Master prefetches (known or unknown size). To perform Burst reads, prefetching must be enabled. The prefetch size can be programmed to match the Master burst length, or can be used as Direct Master or Direct Slave Read Ahead mode data. Reads single data (8, 16, or 32 bit) when the Master initiates a single cycle; otherwise, the PEX 8311 prefetches the programmed size.
- **Posted Memory Writes** – Supports Posted Memory Writes for maximum performance and to avoid potential deadlock situations.
- **Two DMA Channels with Independent FIFOs** – Provides two independently programmable DMA Controllers with independently programmable FIFOs. Each channel supports DMA Block and Scatter/Gather modes, including DMA Ring Management (Valid mode), as well as EOT and DMA Demand modes.
- **PCI Express Support (64-Bit Address Space)** – Supports generation of 64-bit PCI Express Address TLPs beyond the low 4-GB Address Boundary space. The 64-bit PCI Express Address TLPs can be used during PEX 8311 upstream traffic generation (Direct Master and DMA).

1.2.7 Messaging Unit

The PEX 8311 includes the following message unit features:

- **I_2O-Ready Messaging Unit** – Incorporates the I_2O-Ready Messaging Unit, which enables the adapter or embedded system to communicate with other I_2O-supported devices. The I_2O Messaging Unit is fully compatible with the *I_2O r1.5* PCI Extension.
- **Mailbox Registers** – Includes twelve 32-bit Mailbox registers that can be accessed from the PCI Express interface or Local Bus. Only the eight Mailboxes on the Local Bus can be utilized for I_2O Messaging Unit.
- **Doorbell Registers** – Includes two 32-bit doorbell registers. One asserts interrupts from the PCI Express interface to the Local Bus. The other generates message interrupts from the Local Bus to the PCI Express interface.

1.2.8 Root Complex Features

The PEX 8311 includes the following Root Complex features:

- **Type 0 and Type 1 Configuration** – In Direct Master mode, supports Type 0 and Type 1 PCI Express Configuration TLP generation.
- **Reset Signal Direction** – Includes a strapping option (ROOT_COMPLEX#) to reverse the direction of the PCI Express interface and Local Bus Reset signals.

1.2.9 Electrical/Mechanical

The PEX 8311 includes the following electrical/mechanical features:

- **Packaging** – Available in a 337-ball, 21 x 21 mm PBGA package.
- **1.5V and 2.5V Core, 3.3V I/O** – Low-power CMOS 1.5V and 2.5V core with 3.3V I/O. Typically consumes less than 500 mW total, when operating full-speed at room temperature.
- **5V Tolerant Operation** – Provides 3.3V signaling with 5V I/O tolerance on Local Bus.
- **Commercial Temperature Range Operation** – The PEX 8311 works in a 0 to +70°C temperature range.
- **JTAG** – Supports *IEEE 1149.1* JTAG boundary-scan.

1.2.10 Miscellaneous

Other features provided in the PEX 8311 are as follows:

Serial EEPROM Interface – Includes two optional serial EEPROM interfaces, Microwire and SPI, used to load configuration information for Local Bus and PCI Express Configuration Registers, respectively. This is useful for loading information unique to a particular adapter, *such as* the Device or Vendor ID, especially in designs that do not include a Local processor.

Interrupt Generator – Can assert Local and generate PCI Express interrupts from external and internal sources.

1.3 Compatibility with Other PLX Devices

1.3.1 Ball Compatibility

The PEX 8311 is ***not*** ball compatible with other PLX Bus Master Accelerators, Target I/O Accelerators, PCI Express Bridges, nor Switches.

1.3.2 Register Compatibility

All registers implemented in the PCI 9056 and PCI 9656 are implemented in the PEX 8311. However, only Local Bus-specific registers implemented in the PCI 9054 are implemented in the PEX 8311.

The PEX 8311 is ***not*** register-compatible with the following PLX Target I/O Accelerators – PCI 9030, PCI 9050, nor PCI 9052.

The PEX 8311 includes many new bit definitions and several new registers. (Refer to Chapter 18, "PCI Express Configuration Registers.")

- All internal registers are accessible from the PCI Express interface or Local Bus
- Most internal registers can be set up through an external serial EEPROM
  - **PECS** register set includes all PEX 8111 registers
  - **LCS** register set includes all PCI 9056-device registers
- Internal registers allow Writes to and Reads from an external serial EEPROM
- Internal registers allow control of GPIO, GPI, and GPO balls

Chapter 2 Ball Descriptions

2.1 Introduction

This chapter provides descriptions of the PEX 8311 signal balls. The signals are divided into the following groups:

- PCI Express Signals
  - PCI Express Interface Signals
  - PCI Express Configuration Space Serial EEPROM Support Signals
- Local Bus Interface Signals
  - Local Bus Interface C Bus Mode Signals (Non-Multiplexed)
  - Local Bus Interface J Bus Mode Signals (Multiplexed)
  - Local Configuration Space Serial EEPROM Interface Signals
- Miscellaneous Signals
- JTAG Signals
- Test Signals
- No Connect Signals
- Power and Ground Signals

2.2 Ball Description Abbreviations

Table 2-1. Ball Description Abbreviations

Abbreviation	Description
#	Active low
DIFF	PCI Express Differential buffer
DTS	Driven Three-State, driven high for one-half CLK before float
I	Input
I/O	Bi-Directional
O	Output
OD	Open Drain
PD	100K-Ohm Pull-Down resistor
PU	100K-Ohm Pull-Up resistor
S	Schmitt Trigger
STS	Sustained Three-State, driven inactive one Clock cycle before float
TP	Totem Pole
TS	Three-State

2.3 PCI Express Signals

This section provides descriptions of the PEX 8311 PCI Express signal balls. The signals are divided into the following groups:

- PCI Express Interface Signals
- PCI Express Configuration Space Serial EEPROM Support Signals

2.3.1 PCI Express Interface Signals

Table 2-2. PCI Express Interface Signals (9 Balls)

Signal	Type	Balls	Description
PERn0	I DIFF	F2	**Receive Minus** PCI Express Differential Receive signal
PERp0	I DIFF	G1	**Receive Plus** PCI Express Differential Receive signal
PERST#	I/O 6 mA 3.3V	C3	**PCI Express Reset** In Endpoint mode, PERST# is an input. It resets the entire bridge when asserted. In Root Complex mode, PERST# is an output. It is asserted when a PCI reset is detected.
PETn0	O DIFF	K2	**Transmit Minus** PCI Express Differential Transmit signal
PETp0	O DIFF	J1	**Transmit Plus** PCI Express Differential Transmit signal
REFCLK-	I DIFF	H2	**PCI Express Clock Input Minus** PCI Express differential, 100-MHz spread-spectrum reference clock. REFCLK- is connected to the PCI Express REFCLK- signal in Endpoint mode, and to an external differential clock source in Root Complex mode.
REFCLK+	I DIFF	H1	**PCI Express Clock Input Plus** PCI Express differential, 100-MHz spread spectrum reference clock. Connected to the PCI Express REFCLK+ signal in Endpoint mode, and to an external differential clock source in Root Complex mode.
WAKEIN#	I 3.3V	B2	**Wake In Signal** In Root Complex mode, WAKEIN# is an input, and indicates that the PCI Express device requested a wakeup while the link is in the L2 state.
WAKEOUT#	OD 6 mA 3.3V	D1	**Wake Out Signal** In Endpoint mode, WAKEOUT# is an output, and asserted when the link is in the L2 state.

2.3.2 PCI Express Configuration Space Serial EEPROM Support Signals

Table 2-3. PCI Express Configuration Space Serial EEPROM Support Signals (4 Balls)

Signal	Type	Balls	Description
EECLK	O TP 3 mA 3.3V	L4	**Serial EEPROM Clock** Provides the serial bit clock to the serial EEPROM. Connects directly to the serial EEPROM's Serial Clock input (SCK) pin. EECLK frequency is programmable by the **PECS Serial EEPROM Clock Frequency** (**EECLKFREQ**) register, and varies from 2 to 25 MHz.
EECS#	O TP 3 mA 3.3V	K3	**Serial EEPROM Chip Select** Active-Low serial EEPROM Chip Select. Connects directly to the serial EEPROM's CS# input pin.
EERDDATA	I 3.3V	M3	**Serial EEPROM Read Data** Inputs Serial Read data from the serial EEPROM. Connect to the serial EEPROM's Serial Data Out (SO) pin, and pull to 3.3V through a 10K-Ohm or lower resistor.
EEWRDATA	O TP 3 mA 3.3V	L3	**Serial EEPROM Write Data** Outputs Serial data to be written to the serial EEPROM. Connects directly to the serial EEPROM Serial Data Input (SI) pin.

2.4 Local Bus Interface Signals

This section provides descriptions of the PEX 8311 Local Bus-specific signal balls. The signals are divided into the following groups:

- Local Bus Interface C Bus Mode Signals (Non-Multiplexed)
- Local Bus Interface J Bus Mode Signals (Multiplexed)
- Local Configuration Space Serial EEPROM Interface Signals

Note: *Certain balls change type when in Reset/BDSEL mode. This is indicated in the Ball Type column for the associated balls. Balls with a type that makes no mention of Reset/BDSEL mode maintain only the one type, which is indicated in the Type column entry for that ball, regardless of the silicon mode. For balls that include a Reset/BDSEL mode type, the other specified type is used in all other silicon modes.*

Reset/BDSEL mode is defined as:

- *ROOT_COMPLEX# de-asserted and PERST# asserted (PCI Express Reset input in Endpoint mode), or*
- *ROOT_COMPLEX# asserted and LRESET# asserted (Local Bus Reset input in Root Complex mode), or*
- *BD_SEL# de-asserted (Bridge is in Test mode, all I/Os are three-stated)*

2.4.1 Pull-Up and Pull-Down Resistors

For designs that do not implement JTAG:

- Ground the TRST# ball
- Drive, pull, or tie the TCK, TDI, and TMS inputs to a known value
- Pull the TDO output up with an external pull-up resistor

IEEE Standard 1149.1-1990 requires pull-up resistors on the TDI, TMS, and TRST# balls. To remain *PCI r2.2*-compliant, no internal pull-up resistors are provided on JTAG balls in the PEX 8311; therefore, the pull-up resistors must be externally added to the PEX 8311 when implementing JTAG.

IDDQEN# (V10) has an internal 100K-Ohm pull-down resistor. For normal operation, pull IDDQEN# to 3.3V through a resistor of 10K Ohms or less.

PMEIN# (C16) has an internal 10K-Ohm pull-up resistor to VDD3.3. If PMEIN# is not used, this ball can be remain unconnected.

The balls listed in Table 2-4 have an internal 100K-Ohm pull-up resistor to VDD3.3. Due to the weak value of the internal pull-up resistors for the balls listed in Table 2-4, it is strongly recommended that external pull-up to 3.3V or pull-down resistors (3K to 10K Ohms) be used on those signal balls when implementing them in a design. However, depending upon the application, certain signal balls listed in Table 2-4 can remain unconnected, driven or tied high or low. External pull-up or pull-down resistors on the Address and/or Data Buses are recommended, but optional.

Although the EEDI/EEDO ball has an internal pull-up resistor, it can become necessary to add an external pull-up or pull-down resistor. (Refer to Table 4-3, "Serial EEPROM Guidelines," for further details.)

The balls listed in Table 2-5 do not have internal resistors.

Table 2-4. Balls with Internal 100K-Ohm Pull-Up Resistors (to VDD3.3)

Mode	Ball
C and J only	ADS#, BAR0ENB#, BIGEND#, BLAST#, BTERM#, CCS#, DACK[1:0]#, DMPAF/EOT#, DP[3:0], DREQ[1:0]#, EEDI/EEDO, LA[28:2], LBE[3:0]#, LINTi#, LINTo#, LRESET#, LSERR#, LW/R#, PMEIN#, READY#, ROOT_COMPLEX#, WAIT#
C only	LA[31:30], LD[31:0]
J only	DEN#, DT/R#, LAD[31:0]

Table 2-5. Balls with No Internal Resistors

Mode	Ball
C and J only	BREQi, BREQo, LHOLD, LHOLDA, BD_SEL#, EECS, EESK, LCLK, MODE[1:0], TCK, TDI, TDO, TRST#, TMS, USERi/LLOCKi#, USERo/LLOCKo#
C only	LA29
J only	ALE

Because the Open Drain (OD) balls (*for example*, BREQo) are created using I/O buffers, they must be pulled-up to ensure their input buffer is at a known state, which are three-stated when not driven (STS). Recommended resistor pull-up value is 4.7 to 10K Ohms.

Table 2-6 delineates recommendations for multiplexed balls listed in Table 2-5.

Table 2-7 delineates recommendations for non-multiplexed balls listed in Table 2-5.

Table 2-6. Recommendations for Multiplexed Balls Listed in Table 2-5

Ball(s)	Signal	Recommendation
G18	BREQi	Pulled, tied, or driven low.
G17	BREQo	Requires an external pull-down resistor.
Y8	LA29 (C mode) ALE (J mode)	LA29 requires an external pull-up resistor to 3.3V (recommend 10K ohms), ALE requires an external pull-down resistor.
G20	LHOLD	Output ball, floats during reset or BD_SEL# assertion; therefore, an external pull-up or pull-down resistor is ***not*** required.
G19	LHOLDA	Input ball, pull low or drive high or low.
D20	USERi/LLOCKi#	Use a pull-up resistor. (Refer to Section 4.3.2, "Local Initialization and PCI Express Interface Behavior.")
D19	USERo/LLOCKo#	External pull-up or pull-down resistor is ***not*** required.

Table 2-7. Recommendations for Non-Multiplexed Balls Listed in Table 2-5

Ball(s)	Signal	Recommendation
H20, H19	MODE[1:0]	Tie high or low.
E1	BAR0ENB#	Input select. Requires an external pull-up or pull-down for standard operation. Functionality dependent.
B19	BD_SEL#	Must be tied to ground during standard operation.
A20	EECS	Outputs that are always driven by the PEX 8311 and can be connected or remain unconnected (floating).
A19	EESK	
C15	ITDO	Internal Test Data signal. Requires an external pull-up resistor for standard operation.
J20	LCLK	Does ***not*** require an external pull-up nor pull-down resistor.
A15	PCLK_IN	Does ***not*** require an external pull-up nor pull-down resistor.
A3	PLXT1	PLX Test #1 defined signal. Requires an external pull-up resistor for standard operation.
A10	PLXT2	PLX Test #2 defined signal. Requires an external pull-down resistor for standard operation.
B10	PMEOUT#	Power Management Event in Root Complex mode. Requires an external pull-up resistor for standard operation.
A18	ROOT_COMPLEX#	Root Complex or Endpoint Select signal. Due to a weak pull-up value, requires an external pull-up resistor for standard operation in Endpoint mode. Requires an external pull-down resistor for standard operation in Root Complex mode.

2.4.2 Local Bus Interface C Bus Mode Signals (Non-Multiplexed)

Table 2-8. Local Bus Interface C Mode Signals (96 Balls)

Signal	Type	Balls	Description
ADS#	I/O TS 24 mA PU	F19	**Address Strobe** Indicates the valid address and start of a new Bus access. ADS# is asserted for the first clock of the Bus access.
BIGEND#	I PU	D18	**Big Endian Select** Can be asserted during the Local Bus Address phase of a Direct Master transfer or Configuration register access to specify use of Big Endian Byte ordering. Uses an AL_BTT24_U buffer (which includes a pull-up resistor).
BLAST#	I/O TS 24 mA PU	F20	**Burst Last** As an input, the Local Bus Master asserts BLAST# to indicate the last Data transfer of a Bus access. As an output, the PEX 8311 asserts BLAST# to indicate the last Data transfer of the Bus access.
BREQi	I	G18	**Bus Request In** Asserted to indicate a Local Bus Master requires the bus. When enabled through the Configuration registers, the PEX 8311 releases the bus during a Direct Slave or DMA transfer when BREQi is asserted.
BREQo	O DTS 24 mA	G17	**Bus Request Out** When the Backoff Timer expires, the PEX 8311 asserts BREQo until it is granted the Local Bus.
BTERM#	I/O DTS 24 mA PU	J19	**Burst Terminate** As an input, BTERM# assertion causes the PEX 8311 (as the Local Master) to break the transfer (typically a burst). When the transfer is not completed, the PEX 8311 generates a new Address cycle and continues the transfer. As an output, the PEX 8311 (as a Local target) only asserts BTERM# to request the Master to break the transfer when a PCI Abort condition is detected.
CCS#	I PU	D17	**Configuration Register Select** Internal PEX 8311 **LCS** registers are selected when CCS# is asserted low during Local Bus accesses to the PEX 8311.

Table 2-8. Local Bus Interface C Mode Signals (96 Balls) *(Cont.)*

Signal	Type	Balls	Description
DACK[1:0]#	O TP 24 mA PU *When [(ROOT_COMPLEX# is not asserted and PERST# is asserted) or (ROOT_COMPLEX# and LRESET# are asserted) or BD_SEL# is not asserted)], balls go Hi-Z.*	B18, C20	**DMA Channel *x* Demand Mode Acknowledge** When DMA Channel *x* is programmed through the **LCS DMA** registers to operate in Demand mode, this output indicates a DMA transfer is in process. DACK0# is associated with Channel 0. DACK1# is associated with Channel 1.
DMPAF EOT#	When DMAMODE0[14]=1 and/or DMAMODE1[14]=1) I PU otherwise O TP 24 mA PU *When [(ROOT_COMPLEX# is not asserted and PERST# is asserted) or (ROOT_COMPLEX# and LRESET# are asserted) or BD_SEL# is not asserted)], ball goes Hi-Z.*	C18	Multiplexed I/O ball. Default functionality is DMPAF output (**LCS DMAMODE0**[14] and **DMAMODE1**[14]=00b). **Direct Master Programmable Almost Full** DMPAF (Output). Direct Master Write FIFO Almost Full status output. Programmable through **LCS DMPBAM**[10, 8:5]. **End of Transfer for Current DMA Channel** EOT# (Input): Terminates the current DMA transfer. EOT# serves as a general-purpose EOT. Before asserting EOT#, be aware of DMA channel activity.
DP[3:0]	I/O TS 24 mA PU	M15, M16, L15, L16	**Data Parity** Parity is even for each of up to four byte lanes on the Local Bus. Parity is checked for writes to or reads by the PEX 8311. Parity is asserted for reads from or writes by the PEX 8311.
DREQ[1:0]#	I PU	B17, C19	**DMA Channel *x* Demand Mode Request** When DMA Channel 0 is programmed through the Configuration registers to operate in Demand mode, this input serves as a DMA request. DREQ0# is associated with Channel 0. DREQ1# is associated with Channel 1.

Table 2-8. Local Bus Interface C Mode Signals (96 Balls) *(Cont.)*

Signal	Type	Balls	Description
LA[31:2]	I/O TS 24 mA PU (LA[31:30, 28:2] only)	Y7, W8, Y8, W9, Y9, W10, Y10, V11, W11, Y11, W12, Y12, W13, Y13, W14, Y14, V15, W15, Y15, U16, V16, W16, Y16, U17, V17, W17, Y17, V18, W18, Y18	**Local Address Bus** Carries the upper 30 bits of the physical Address Bus. Incremented during bursts to indicate successive Data cycles.
LBE[3:0]#	I/O TS 24 mA PU	Y19, Y20, W20, W19	**Local Byte Enables** Encoded, based on the bus data-width configuration, as follows: **32-Bit Bus** The four Byte Enables indicate which of the four bytes are valid during a Data cycle: LBE3# Byte Enable 3 – LD[31:24] LBE2# Byte Enable 2 – LD[23:16] LBE1# Byte Enable 1 – LD[15:8] LBE0# Byte Enable 0 – LD[7:0] **16-Bit Bus** LBE[3, 1:0]# are encoded to provide BHE#, LA1, and BLE#, respectively: LBE3# Byte High Enable (BHE#) – LD[15:8] LBE2# ***not used*** LBE1# Address bit 1 (LA1) LBE0# Byte Low Enable (BLE#) – LD[7:0] **8-Bit Bus** LBE[1:0]# are encoded to provide LA[1:0], respectively: LBE3# ***not used*** LBE2# ***not used*** LBE1# Address bit 1 (LA1) LBE0# Address bit 0 (LA0)
LCLK	I	J20	**Local Processor Clock** Local Bus clock input. ***Note:*** *LCLK must be driven at all times during normal operation.*
LD[31:0]	I/O TS 24 mA PU	V19, V20, U19, U20, T17, T18, T19, T20, R17, R18, R19, R20, P17, P18, P19, P20, N17, N18, N19, N20, M17, M18, M19, M20, L17, L18, L19, L20, K17, K18, K19, K20	**Local Data Bus** When the PEX 8311 is the Local Bus Master, it carries 8-, 16-, or 32-bit data quantities, depending upon bus data-width configuration. Direct Master accesses to the PEX 8311 are 32 bits only.

Table 2-8. Local Bus Interface C Mode Signals (96 Balls) *(Cont.)*

Signal	Type	Balls	Description
LHOLD	O TP 24 mA *When [(ROOT_COMPLEX# is not asserted and PERST# is asserted) or (ROOT_COMPLEX# and LRESET# are asserted) or BD_SEL# is not asserted)], ball goes Hi-Z.*	G20	**Local Hold Request** Asserted to request use of the Local Bus.
LHOLDA	I	G19	**Local Hold Acknowledge** The external Local Bus Arbiter asserts LHOLDA when bus ownership is granted in response to LHOLD. Do not grant the Local Bus to the PEX 8311, unless requested by LHOLD.
LINTi#	I PU	E20	**Local Interrupt Input** When enabled by the **LCS Interrupt Control/Status** register (**INTCSR**[11, 8] = 11b), PCI Express Assert_INTA and Deassert_INTA messages are transmitted to PCI Express Space following LINTi# signal assertions (High-Low) and de-assertions (Low-High), respectively.
LINTo#	O OD 24 mA PU	E19	**Local Interrupt Output** Synchronous output that remains asserted when the interrupt is enabled [by way of the **LCS Interrupt Control/Status** register (**INTCSR**)] and the interrupt condition exists.
LRESET#	When ROOT_COMPLEX# is asserted I PU otherwise O TP 24 mA PU	E18	**Local Bus Reset** As an input, in Root Complex mode, PERST# is generated as long as LRESET# is asserted. Resets the PEX 8311. As an output, in Endpoint mode, LRESET# is asserted when the PEX 8311 is in reset (PERST#=0). Can be used to reset the backend logic on the board. When ROOT_COMPLEX# is low (asserted), LRESET# is an input. When asserted, all internal logic and registers are forced to their initial states, and PERST# is asserted to PCI Express Space. When ROOT_COMPLEX# is high (de-asserted), LRESET# is an output that asserts in response all PCI Express resets, Soft resets, and Local Bus device resets. (Refer to Chapter 3, "Reset Operation and Initialization Summary," for further details.)
LSERR#	O OD 24 mA PU	J18	**Local System Error Interrupt Output** Synchronous output that remains asserted when the interrupt is enabled (by way of the **LCS INTCSR** register) and the interrupt condition exists.

Table 2-8. Local Bus Interface C Mode Signals (96 Balls) *(Cont.)*

Signal	Type	Balls	Description
LW/R#	I/O TS 24 mA PU	U18	**Local Write/Read** Asserted low for reads and high for writes.
PMEIN#	I PU (10K)	C16	**Power Management Event Input (Endpoint Mode Only)** When the PEX 8311 is operating in Endpoint mode (ROOT_COMPLEX# is de-asserted), asserting PMEIN# low generates a PM_PME message to PCI Express Space. (Refer to Section 12.1.3, "Endpoint Mode Power Management Signaling," for details.) PMEIN# has an internal 10K-Ohm pull-up resistor to VDD3.3.
PMEOUT#	OD 24 mA	B10	**Power Management Event Out** Valid only in Root Complex mode (ROOT_COMPLEX# is asserted). Open Drain output used to signal to a Local Host that a PM_PME message was received from a device in PCI Express Space. PMEOUT# is ***not*** 5V tolerant. (Refer to Section 12.2.4, "Root Complex Mode Local Bus PMEOUT# Signal," for details.)
READY#	I/O DTS 24 mA PU	F18	**Ready I/O** Direct Slave or DMA accesses: A Local slave asserts READY# to indicate that Read data on the bus is valid or when Write data is to be sampled on the next rising edge of LCLK. READY# input is not sampled until the internal Wait State Counter(s) expires (WAIT# output de-asserted). Direct Master accesses from external Local Master: READY# is an output, driven low when Read data on the bus is valid or when write data is to be sampled on the next rising edge of LCLK.
USERi LLOCKi#	I	D20	Multiplexed input ball. Default functionality is USERi (CNTRL[18]=1). **User Input** USERi: General-purpose input that can be read in the PEX 8311 Configuration registers. Also used to select the PEX 8311 behavior in response to PCI accesses during initialization. (Refer to Section 4.3.2, "Local Initialization and PCI Express Interface Behavior.") **Local Lock Input** LLOCKi#: Indicates an atomic operation that can require multiple transactions to complete. Used by the PEX 8311 for direct Local access to the internal PCI Bus.

Table 2-8. Local Bus Interface C Mode Signals (96 Balls) *(Cont.)*

Signal	Type	Balls	Description
USERo LLOCKo#	O TP 24 mA *When [(ROOT_COMPLEX# is not asserted and PERST# is asserted) or (ROOT_COMPLEX# and LRESET# are asserted) or BD_SEL# is not asserted)], ball goes Hi-Z.*	D19	Multiplexed output ball. Default functionality is USERo (CNTRL[19]=1). **User Output** USERo: General-purpose output controlled from the PEX 8311 Configuration registers. Driven low during software reset. [Refer to Section 3.1.2.2, "Local Bridge Local Bus Reset," (Endpoint mode) or Section 3.2.1, "Local Bus Reset," (Root Complex mode) for details.] **Local Lock Output** LLOCKo#: Indicates an atomic operation for a Direct Slave PCI-to-Local Bus access can require multiple transactions to complete.
WAIT#	I/O TS 24 mA PU	H17	**Wait I/O** As an input, the Local Bus Master can assert WAIT# to pause the PEX 8311 (insert wait states) during a Direct Master access Data phase. As an output, the PEX 8311 can be programmed to insert wait states (to pause the Local Slave) by asserting WAIT# for a predefined number of Local Bus Clock cycles during Direct Slave transfers.

2.4.3 Local Bus Interface J Bus Mode Signals (Multiplexed)

Table 2-9. Local Bus Interface J Mode Signals (96 Balls)

Signal	Type	Balls	Description
ADS#	I/O TS 24 mA PU	F19	**Address Strobe** Indicates a valid address and start of a new Bus access. ADS# asserts for the first clock of the Bus access.
ALE	I/O TS 24 mA	Y8	**Address Latch Enable** Indicates the valid address and start of a new Bus access. ALE asserts for the first clock of the Bus access. As an input, the PEX 8311 latches the incoming address on the positive edge of LCLK, following ALE assertion. Verify that the ALE pulse is similar to the example provided in Figure 22-3: PEX 8311 ALE Output Delay to Local Clock. As an output, refer to Figure 22-3.
BIGEND#	I PU	D18	**Big Endian Select** Can be asserted during the Local Bus Address phase of a Direct Master transfer or Configuration register access to specify use of Big Endian Byte ordering. Uses an AL_BTT24_U buffer (which includes a pull-up resistor).
BLAST#	I/O TS 24 mA PU	F20	**Burst Last** As an input, the Local Bus Master asserts BLAST# to indicate the last Data transfer of a Bus access. As an output, the PEX 8311 asserts BLAST# to indicate the last Data transfer of the Bus access.
BREQi	I	G18	**Bus Request In** Asserted to indicate a Local Bus Master requires the bus. When enabled through the Configuration registers, the PEX 8311 releases the bus during a Direct Slave or DMA transfer when BREQi is asserted.
BREQo	O DTS 24 mA	G17	**Bus Request Out** When the Backoff Timer expires, the PEX 8311 asserts BREQo until it is granted the Local Bus.
BTERM#	I/O DTS 24 mA PU	J19	**Burst Terminate** As an input, assertion causes the PEX 8311 (as the Local Master) to break the transfer (typically a burst). When the transfer is not completed, the PEX 8311 generates a new Address cycle and continues the transfer. As an output, the PEX 8311 (as a Local target) only asserts BTERM# to request the Master to break the transfer when a PCI Abort condition is detected.
CCS#	I PU	D17	**Configuration Register Select** When asserted low, CCS# Reads or Writes by external Local Masters are directed to the PEX 8311 **LCS** registers.

Table 2-9. Local Bus Interface J Mode Signals (96 Balls) *(Cont.)*

Signal	Type	Balls	Description
DACK[1:0]#	O TP 24 mA PU *When [(ROOT_COMPLEX# is not asserted and PERST# is asserted) or (ROOT_COMPLEX# and LRESET# are asserted) or BD_SEL# is not asserted)], balls go Hi-Z.*	B18, C20	**DMA Channel *x* Demand Mode Acknowledge** When DMA Channel *x* is programmed through the Configuration registers to operate in Demand mode, this output indicates a DMA transfer is in process. DACK0# is associated with Channel 0. DACK1# is associated with Channel 1.
DEN#	O TS 24 mA PU	W8	**Data Enable** When asserted low, the Local Bus device can drive the Local Data Bus. Used in conjunction with DT/R# to provide control for data transceivers attached to the Local Bus.
DMPAF	When DMAMODE0[14]=1 and/or DMAMODE1[14]=1 I PU otherwise O TP 24 mA PU	C18	Multiplexed I/O ball. Default functionality is DMPAF output (DMAMODE0[14] and DMAMODE1[14]=00b). **Direct Master Programmable Almost Full** DMPAF (Output): Direct Master Write FIFO Almost Full status output. Programmable through DMPBAM[10, 8:5].
EOT#	*When [(ROOT_COMPLEX# is not asserted and PERST# is asserted) or (ROOT_COMPLEX# and LRESET# are asserted) or BD_SEL# is not asserted)], ball goes Hi-Z.*		**End of Transfer for Current DMA Channel** EOT# (Input): Terminates the current DMA transfer. EOT# serves as a general-purpose EOT. Before asserting EOT#, therefore, be aware of DMA channel activity.
DP[3:0]	I/O TS 24 mA PU	M15, M16, L15, L16	**Data Parity** Parity is even for each of up to four byte lanes on the Local Bus. Parity is checked for writes to or on reads by the PEX 8311. Parity is asserted for reads from or writes by the PEX 8311.

Table 2-9. Local Bus Interface J Mode Signals (96 Balls) *(Cont.)*

Signal	Type	Balls	Description
DREQ[1:0]#	I PU	B17, C19	**DMA Channel *x* Demand Mode Request** When DMA Channel 0 is programmed through the Configuration registers to operate in Demand mode, this input serves as a DMA request. DREQ0# is associated with Channel 0. DREQ1# is associated with Channel 1.
DT/R#	O TS 24 mA PU	Y7	**Data Transmit/Receive** When asserted low, indicates the PEX 8311 is driving data onto the Local Data Bus. Used in conjunction with DEN# to provide control for data transceivers attached to the Local Bus. When asserted high, indicates that the PEX 8311 receives data.
LA[28:2]	I/O TS 24 mA PU	W9, Y9, W10, Y10, V11, W11, Y11, W12, Y12, W13, Y13, W14, Y14, V15, W15, Y15, U16, V16, W16, Y16, U17, V17, W17, Y17, V18, W18, Y18	**Local Address Bus** Provides the current Dword address (except the upper three bits [31:29]) during any phase of an access. Incremented on successive Data cycles during Burst cycles. LA[1:0] can also be obtained by using the LBE[1:0]# balls.
LAD[31:0]	I/O TS 24 mA PU	V19, V20, U19, U20, T17, T18, T19, T20, R17, R18, R19, R20, P17, P18, P19, P20, N17, N18, N19, N20, M17, M18, M19, M20, L17, L18, L19, L20, K17, K18, K19, K20	**Local Address/Data Bus** During an Address phase: As a Local Bus master, the PEX 8311 provides a 32-bit address for 8-bit data quantities, and LAD[31:0] provide byte addressing. For 16-bit data quantities, LAD[31:1] provide word addressing and LAD[0] is driven to 0. For 32-bit data quantities, LAD[31:2] provide Dword addressing and LAD[1:0] are driven to 00b. As a Local Bus slave, Master accesses to the PEX 8311 can only be 32-bit quantities (LAD[1:0] are ignored). The input address is latched into the PEX 8311, on the positive edge of LCLK during ADS# assertion or following ALE assertion. During a Data phase: As a Local Bus master, the PEX 8311 provides an 8-bit data quantity on LAD byte lanes, 16-bit data quantities on LAD word lanes, and 32-bit data quantities on LAD[31:0], depending on the bus data-width access. As a Local Bus slave, 32-bit Data Bus for reading from or writing to the PEX 8311.

Table 2-9. Local Bus Interface J Mode Signals (96 Balls) *(Cont.)*

Signal	Type	Balls	Description
LBE[3:0]#	I/O TS 24 mA PU	Y19, Y20, W20, W19	**Local Byte Enable** Encoded, based on the bus data-width configuration, as follows: **32-Bit Bus** The four Byte Enables indicate which of the four bytes are valid during a Data cycle: LBE3# Byte Enable 3 – LAD[31:24] LBE2# Byte Enable 2 – LAD[23:16] LBE1# Byte Enable 1 – LAD[15:8] LBE0# Byte Enable 0 – LAD[7:0] **16-Bit Bus** LBE[3, 1:0]# are encoded to provide BHE#, LA1, and BLE#, respectively: LBE3# Byte High Enable (BHE#) – LAD[15:8] LBE2# ***not used*** LBE1# Address bit 1 (LA1) LBE0# Byte Low Enable (BLE#) – LAD[7:0] **8-Bit Bus** LBE[1:0]# are encoded to provide LA[1:0], respectively: LBE3# ***not used*** LBE2# ***not used*** LBE1# Address bit 1 (LA1) LBE0# Address bit 0 (LA0)
LCLK	I	J20	**Local Processor Clock** Local Bus clock input. ***Note:*** *LCLK must be driven at all times during normal operation.*
LHOLD	O TP 24 mA *When [(ROOT_COMPLEX# is not asserted and PERST# is asserted) or (ROOT_COMPLEX# and LRESET# are asserted) or BD_SEL# is not asserted)], ball goes Hi-Z.*	G20	**Local Hold Request** Asserted to request use of the Local Bus.
LHOLDA	I	G19	**Local Hold Acknowledge** The external Local Bus Arbiter asserts LHOLDA when bus ownership is granted in response to LHOLD. Do not grant the Local Bus to the PEX 8311, unless requested by LHOLD.

Table 2-9. Local Bus Interface J Mode Signals (96 Balls) *(Cont.)*

Signal	Type	Balls	Description
LINTi#	I PU	E20	**Local Interrupt Input (Endpoint Mode Only)** In Endpoint Mode only (ROOT_COMPLEX# is de-asserted), when enabled by way of the **LCS Interrupt Control/Status** register (**INTCSR**[11,8] = 11b), high-low and low-high transitions on LINTi# cause Assert_INTA and Deassert_INTA messages to be sent to PCI Express space.
LINTo#	O OD 24 mA PU	E19	**Local Interrupt Output** Synchronous output that remains asserted when the interrupt is enabled and the interrupt condition exists.
LRESET#	When ROOT_COMPLEX# is asserted I PU otherwise O TP 24 mA PU	E18	**Local Bus Reset** As an input, in Root Complex mode, PERST# is generated when LRESET# is asserted. Resets the PEX 8311. As an output, in Endpoint mode, LRESET# is asserted when the PEX 8311 is in reset (PERST#=0). Can be used to reset the backend logic on the board.
LSERR#	O OD 24 mA PU	J18	**Local System Error Interrupt Output** Synchronous output that remains asserted when the interrupt is enabled and the interrupt condition exists.
LW/R#	I/O TS 24 mA PU	U18	**Local Write/Read** Asserted low for reads and high for writes.
PMEIN#	I PU (10K)	C16	**Power Management Event Input (Endpoint Mode Only)** When the PEX 8311 is operating in Endpoint mode (ROOT_COMPLEX# is de-asserted), asserting PMEIN# low generates a PM_PME message to PCI Express Space. (Refer to Section 12.1.3, "Endpoint Mode Power Management Signaling," for details.) PMEIN# has an internal 10K-Ohm pull-up resistor to VDD3.3.
PMEOUT#	OD 24 mA	B10	**Power Management Event Out** Valid only in Root Complex mode (ROOT_COMPLEX# is asserted). Open Drain output used to request a change in the power state. PMEOUT# is ***not*** 5V tolerant.

Table 2-9. Local Bus Interface J Mode Signals (96 Balls) *(Cont.)*

Signal	Type	Balls	Description
READY#	I/O DTS 24 mA PU	F18	**Ready I/O** Direct Slave or DMA accesses: A Local slave asserts READY# to indicate that Read data on the bus is valid or that Write data will be sampled on the next rising edge of LCLK. READY# input is not sampled until the internal Wait State Counter(s) expires (WAIT# output is de-asserted). Direct Master accesses from external Local Master: READY# is an output, driven low when Read data is valid or when Write data is to be sampled on the next LCLK rising edge.
USERi LLOCKi#	I	D20	Multiplexed input ball. Default functionality is USERi (CNTRL[18]=1). **User Input** USERi: General-purpose input that can be read in the PEX 8311 Configuration registers. Also used to select the PEX 8311 behavior in response to PCI accesses during initialization. (Refer to Section 4.3.2, "Local Initialization and PCI Express Interface Behavior.") **Local Lock Input** LLOCKi#: Indicates an atomic operation that can require multiple transactions to complete. Used by the PEX 8311 for direct Local access to the internal PCI Bus.
USERo LLOCKo#	O TP 24 mA *When [(ROOT_COMPLEX# is not asserted and PERST# is asserted) or (ROOT_COMPLEX# and LRESET# are asserted) or BD_SEL# is not asserted)], ball goes Hi-Z.*	D19	Multiplexed output ball. Default functionality is USERo (CNTRL[19]=1). **User Output** USERo: General-purpose output controlled from the PEX 8311 Configuration registers. Driven low during software reset. [Refer to Section 3.1.2.2, "Local Bridge Local Bus Reset," (Endpoint mode) or Section 3.2.1, "Local Bus Reset," (Root Complex mode) for details.] **Local Lock Output** LLOCKo#: Indicates an atomic operation for a Direct Slave PCI-to-Local Bus access that can require multiple transactions to complete.
WAIT#	I/O TS 24 mA PU	H17	**Wait I/O** As an input, the Local Bus Master can assert WAIT# to pause the PEX 8311 (insert wait states) during a Direct Master access Data phase. As an output, the PEX 8311 can be programmed to insert wait states (to pause the Local Slave) by asserting WAIT# for a predefined number of Local Bus Clock cycles during Direct Slave transfers.

2.4.4 Local Configuration Space Serial EEPROM Interface Signals

Table 2-10. Local Configuration Space Serial EEPROM Interface Signals (3 Balls)

Signal	Type	Balls	Description
EECS	O TP 12 mA *When BD_SEL# is not asserted, ball goes Hi-Z.*	A20	**Serial EEPROM Chip Select**
EEDI/EEDO	I/O TS 12 mA *When **CNTRL**[31]=1, ball goes Hi-Z.*	B20	**Serial EEPROM Data In/Serial EEPROM Data Out** Multiplexed Write and Read data to the serial EEPROM.
EESK	O TP 12 mA *When BD_SEL# is not asserted, ball goes Hi-Z.*	A19	**Serial EEPROM Clock** Serial bit clock for the serial EEPROM.

2.5 Miscellaneous Signals

Table 2-11. Miscellaneous Signals (11 Balls)

Signal	Type	Balls	Description
BAR0ENB#	I 3.3V PU	E1	**PCI Base Address 0 Register Enable** When low, the **PECS PCI Base Address 0** register is enabled. When high, the **PCI Base Address 0** register is enabled by the **PECS Device-Specific Control (DEVSPECCTL)** register *PCI Base Address 0 Enable* bit.
GPIO[3:0]	I/O 12 mA 3.3V PU	A1, D3, B1, C1	**General Purpose I/O** Program as an Input or Output general-purpose ball. Internal device status is also an output on GPIO[3:0]. Interrupts are generated on balls that are programmed as inputs. The **General-Purpose I/O Control** register is used to configure these I/O. GPIO0 defaults to a Link Status output. GPIO1 defaults to an input. When GPIO2 is low at the trailing edge of RESET#, the **TLPCFG0** register *Limit Completion Flow Control Credit* bit is set. When GPIO3 is low at the trailing edge of RESET#, the **TLPCFG0** register *Delay Link Training* bit is set.
MODE[1:0]	I	H20, H19	**Local Bus Mode** MODE0 selects the PEX 8311 Local Bus operation mode: **MODE0 MODE1 Local Bus Mode** 1 1 ***Reserved*** 0 0 C 1 0 J 0 1 ***Reserved*** The MODE input level must be stable at power-on. Connect MODE1 to ground for standard operation
PCLK_IN	I 3.3V	A15	**Internal Clock Input** A 66-MHz clock input to the internal PEX 8311 interface. PCLK_IN can be directly connected as a source to PCLKO through an external damping resistor (33 Ohms recommended value) when the ROOT_COMPLEX# signal is de-asserted (Endpoint mode). An external 66-MHz clock source (oscillator) is required when the ROOT_COMPLEX# signal is asserted (Root Complex mode). Use internal clock requirement guidelines. When an external source is used, follow the *PCI r2.2* guidelines.
PCLKO	O TP 26 mA PCI	A8	**Internal Clock Output** A buffered clock output from the internal reference clock, with the frequency is programmable, depending on the **PECS DEVINIT** register *PCLKO Clock Frequency* field value. Default signal frequency is 66 MHz.
PWR_OK	O 6 mA 3.3V	D2	**Power OK** Valid only in Endpoint mode. When the available power indicated in the PCI Express Set Slot Power Limit message is greater than or equal to the power requirement indicated in the POWER register, PWR_OK is asserted.
ROOT_COMPLEX#	I 3.3V PU	A18	**ROOT_COMPLEX# Mode Select** When low (asserted), the PEX 8311 acts as a PCI Express Root Complex device (North bridge). When high (de-asserted), the PEX 8311 acts as a PCI Express Endpoint device (peripheral board).

2.6 JTAG Signals

Table 2-12. JTAG Signals (5 Balls)

Signal	Type	Balls	Description
TCK	I	A13	**Test Clock** JTAG test clock. Sequences the Test Access Port (TAP) Controller as well as all PEX 8311 JTAG registers. Ground when JTAG is not used.
TDI	I PU	A14	**Test Data Input** Serial data input to JTAG instruction and data registers. TAP Controller state and particular instruction held in the instruction register determines which register is fed by TDI for a specific operation. TDI is sampled into the JTAG registers on the rising edge of TCK. Hold open when JTAG is not used.
TDO	O TS 12 mA 3.3V	C14	**Test Data Output** Serial data output for JTAG instruction and data registers. The TAP Controller state and particular instruction held in the instruction register determines which register feeds TDO for a specific operation. Only one register (instruction or data) is allowed as the active connection between TDI and TDO for any given operation. TDO changes state on the falling edge of TCK and is only active during the shifting of data through the device. TDO is placed into a high-impedance state at all other times. Hold open when JTAG is not used.
TMS	I PU	A11	**Test Mode Select** Mode input signal to the TAP Controller. The TAP Controller is a 16-state FSM that provides the control logic for JTAG. The state of TMS at the rising edge of TCK determines the sequence of states for the TAP Controller. Hold open when JTAG is not used.
TRST#	I PU	B14	**Test Reset** Resets the JTAG TAP Controller when driven to ground. Ground when JTAG is not used.

2.7 Test Signals

Table 2-13. Test Signals (12 Balls)

Signal	Type	Balls	Description
BD_SEL#	I PCI	B19	**Board Select** Selects a device to operate in standard mode. When asserted low, standard operation is selected. When asserted high, test operation is selected.
BTON	I	D10	**Test Enable** Connect to ground for standard operation.
BUNRI	I	F3	**Test Mode Select** Connect to ground for standard operation.
IDDQEN#	I	V10	**IDDQ Enable** Places the PEX 8311 Local Bus output buffers into a quiescent state. Asserting IDDQEN# to logic low (0) along with BD_SEL# to logic high (1) forces the PEX 8311 into a quiescent state. All analog power is disabled and I/Os are three-stated. For normal operation, pull IDDQEN# to 3.3V through a resistor of 10K Ohms or less.
ITDO	I/O	C15	**Internal Test Data** External pull-up resistor required for standard operation.
PLXT1	I	A3	**PLX-Defined Test 1** Connect to power through a pull-up resistor for standard operation.
PLXT2	I	A10	**PLX-Defined Test 2** Must be connected to ground for standard operation.
SMC	I	V4	**Scan Path Mode Control** Connect to ground for standard operation.
TEST	I	N1	**Test Mode Select** Connect to ground for standard operation.
TMC	I	E2	**Test Mode Control** Connect to ground for standard operation.
TMC1	I	V3	**IDDQ Test Control Input** Connect to ground for standard operation.
TMC2	I	E3	**I/O Buffer Control** Connect to ground for standard operation.

2.8 No Connect Signals

Table 2-14. No Connect Signals (59 Balls)

Signal	Type	Balls	Description
N/C	I/O Manufacturer Test Balls	A4, A5, A6, A7, A9, A12, B3, B4, B5, B6, B7, B8, B9, B11, B12, B13, C4, C5, C6, C7, C8, C10, C11, C12, D4, D5, D11, D16, E4, E6, M2, N2, N3, N4, P1, P2, P3, P4, R1, R2, R3, R4, T1, T2, T3, T4, U1, U2, U3, U4, U7, V2, V5, V6, V7, V8, W6, W7, Y6	**No Connect** Signals designated *N/C* are true no connects and cannot be used to route other functional signals across the board. Must remain floating for standard operation. Quantity – 59

2.9 Power and Ground Signals

Table 2-15. Power and Ground Signals (138 Balls)

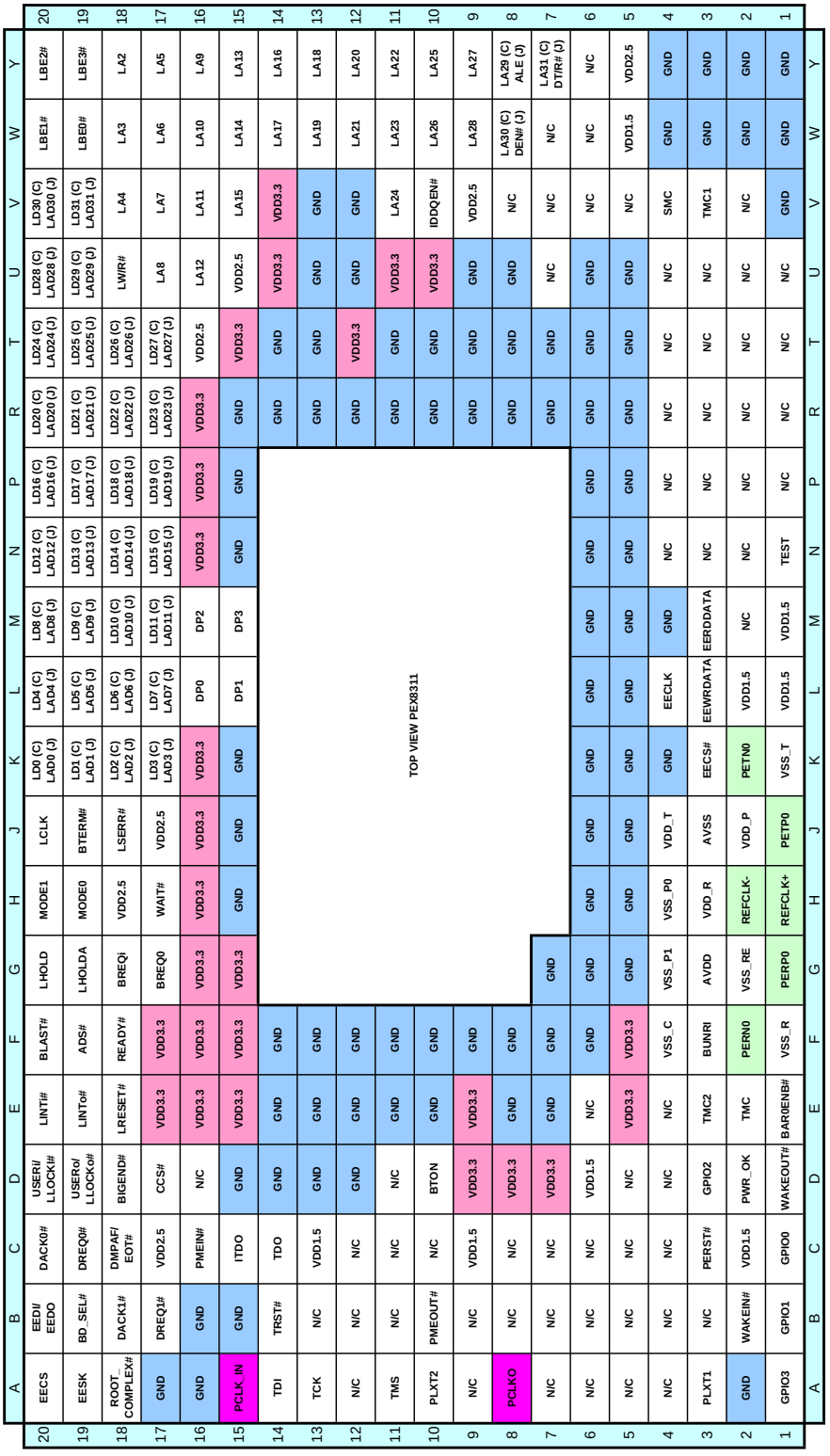
Signal	Type	Balls	Description
AVDD	Power	G3	**Analog Supply Voltage** Connect to the +1.5V power supply.
AVSS	Ground	J3	**Analog Ground** Connect to ground.
GND	Ground	A2, A16, A17, B15, B16, D12, D13, D14, D15, E7, E8, E10, E11, E12, E13, E14, F6, F7, F8, F9, F10, F11, F12, F13, F14, G5, G6, G7, H5, H6, H15, J5, J6, J15, K4, K5, K6, K15, L5, L6, M4, M5, M6, N5, N6, N15, P5, P6, P15, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, T5, T6, T7, T8, T9, T10, T11, T13, T14, U5, U6, U8, U9, U12, U13, V1, V12, V13, W1, W2, W3, W4, Y1, Y2, Y3, Y4	**Ground** Connect to ground. Quantity – 86
VDD_P	Power	J2	**PLL Supply Voltage** Connect to the +1.5V filtered PLL power supply.
VDD_R	Power	H3	**Receiver Supply Voltage** Connect to the +1.5V power supply.
VDD_T	Power	J4	**Transmitter Supply Voltage** Connect to the +1.5V power supply.

Table 2-15. Power and Ground Signals (138 Balls) *(Cont.)*

Signal	Type	Balls	Description
VDD1.5	Power	C2, C9, C13, D6, L1, L2, M1, W5	**Core Supply Voltage** Connect to the +1.5V power supply. Quantity – 8
VDD3.3	Power	D7, D8, D9, E5, E9, E15, E16, E17, F5, F15, F16, F17, G15, G16, H16, J16, K16, N16, P16, R16, T12, T15, U10, U11, U14, V14	**I/O Supply Voltage** Connect to the +3.3V power supply. Quantity – 26
VDD2.5	Power	C17, H18, J17, T16, U15, V9, Y5	**Local Core Supply Voltage** Connect to the +2.5V power supply. Quantity – 7
VSS_C	Ground	F4	**Common Ground** Connect to ground.
VSS_P0	Ground	H4	**PLL Ground** Connect to ground.
VSS_P1	Ground	G4	**PLL Ground** Connect to ground.
VSS_R	Ground	F1	**Receiver Ground** Connect to ground.
VSS_RE	Ground	G2	**Receiver Ground** Connect to ground.
VSS_T	Ground	K1	**Transmitter Ground** Connect to ground.

2.10 Physical Ball Assignment

Figure 2-1. PEX 8311 Physical Ball Assignment (Top View)



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	
20	EECS	EEDI/ EEDO	DACK0#	USER0/ LLOCKi#	LINTi#	BLAST#	LHOLD	MODE1	LCLK	LD0 (C) LAD0 (J)	LD4 (C) LAD4 (J)	LD8 (C) LAD8 (J)	LD12 (C) LAD12 (J)	LD16 (C) LAD16 (J)	LD20 (C) LAD20 (J)	LD24 (C) LAD24 (J)	LD28 (C) LAD28 (J)	LD30 (C) LAD30 (J)	LBE1#	LBE2#	20
19	EESK	BD_SEL#	DREQ0#	USER0/ LLOCKo#	LINTo#	ADS#	LHOLDA	MODE0	BTERM#	LD1 (C) LAD1 (J)	LD5 (C) LAD5 (J)	LD9 (C) LAD9 (J)	LD13 (C) LAD13 (J)	LD17 (C) LAD17 (J)	LD21 (C) LAD21 (J)	LD25 (C) LAD25 (J)	LD29 (C) LAD29 (J)	LD31 (C) LAD31 (J)	LBE0#	LBE3#	19
18	ROOT_ COMPLEX#	DACK1#	DMPAF/ EOT#	BIGEND#	LRESET#	READY#	BREQi	VDD2.5	LSERR#	LD2 (C) LAD2 (J)	LD6 (C) LAD6 (J)	LD10 (C) LAD10 (J)	LD14 (C) LAD14 (J)	LD18 (C) LAD18 (J)	LD22 (C) LAD22 (J)	LD26 (C) LAD26 (J)	LWR#	LA4	LA3	LA2	18
17	GND	DREQ1#	VDD2.5	CCS#	VDD3.3	VDD3.3	BREQ0	WAIT#	VDD2.5	LD3 (C) LAD3 (J)	LD7 (C) LAD7 (J)	LD11 (C) LAD11 (J)	LD15 (C) LAD15 (J)	LD19 (C) LAD19 (J)	LD23 (C) LAD23 (J)	LD27 (C) LAD27 (J)	LA8	LA7	LA6	LA5	17
16	GND	GND	PMEIN#	N/C	VDD3.3	VDD3.3	VDD3.3	VDD3.3	VDD3.3	VDD3.3	DP0	DP2	VDD3.3	VDD3.3	VDD3.3	VDD2.5	LA12	LA11	LA10	LA9	16
15	PCLK_IN	GND	ITDO	GND	VDD3.3	VDD3.3	VDD3.3	GND	GND	GND	DP1	DP3	GND	GND	GND	VDD3.3	VDD2.5	LA15	LA14	LA13	15
14	TDI	TRST#	TDO	GND	GND	GND									GND	GND	VDD3.3	VDD3.3	LA17	LA16	14
13	TCK	N/C	VDD1.5	GND	GND	GND									GND	GND	GND	GND	LA19	LA18	13
12	N/C	N/C	N/C	GND	GND	GND									GND	VDD3.3	GND	GND	LA21	LA20	12
11	TMS	N/C	N/C	N/C	GND	GND									GND	GND	VDD3.3	LA24	LA23	LA22	11
10	PLXT2	PMEOUT#	N/C	BTON	GND	GND									GND	GND	VDD3.3	IDDQEN#	LA26	LA25	10
9	N/C	N/C	VDD1.5	VDD3.3	VDD3.3	GND									GND	GND	GND	VDD2.5	LA28	LA27	9
8	PCLKO	N/C	N/C	VDD3.3	GND	GND									GND	GND	GND	N/C	LA30 (C) DEN# (J)	LA29 (C) ALE (J)	8
7	N/C	N/C	N/C	VDD3.3	GND	GND	GND								GND	GND	N/C	N/C	N/C	LA31 (C) DTR# (J)	7
6	N/C	N/C	N/C	VDD1.5	N/C	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	N/C	N/C	N/C	6
5	N/C	N/C	N/C	N/C	VDD3.3	VDD3.3	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	N/C	VDD1.5	VDD2.5	5
4	N/C	N/C	N/C	N/C	N/C	VSS_C	VSS_P1	VSS_P0	VDD_T	GND	EECLK	GND	N/C	N/C	N/C	N/C	N/C	SMC	GND	GND	4
3	PLXT1	N/C	PERST#	GPIO2	TMC2	BUNRI	AVDD	VDD_R	AVSS	EECS#	EEWRDATA	EERDDATA	N/C	N/C	N/C	N/C	N/C	TMC1	GND	GND	3
2	GND	WAKEIN#	VDD1.5	PWR_OK	TMC	PERN0	VSS_RE	REFCLK-	VDD_P	PETN0	VDD1.5	N/C	N/C	N/C	N/C	N/C	N/C	N/C	GND	GND	2
1	GPIO3	GPIO1	GPIO0	WAKEOUT#	BARDENB#	VSS_R	PERP0	REFCLK+	PETP0	VSS_T	VDD1.5	VDD1.5	TEST	N/C	N/C	N/C	N/C	GND	GND	GND	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	

Chapter 3 Reset Operation and Initialization Summary

3.1 Endpoint Mode Reset Operation

The PEX 8311 operates in Endpoint mode when the ROOT_COMPLEX# ball is strapped high.

The actions that the PEX 8311 takes upon receipt of various reset events and interface initialization requirements are described in the following sections.

3.1.1 Full Device Resets

The PEX 8311 receives four types of reset over the PCI Express interface:

- Physical layer resets that are platform specific and referred to as *Fundamental Resets* (Cold/Warm Reset; PCI Express PERST# signal asserted (refer to *PCI Express Base 1.0a*, Section 6.6)
- PCI Express Physical Layer mechanism (Hot Reset)
- PCI Express Data Link transitioning to the PCI Express interface DL_Down state
- PCI Express Power Management Reset (D3→D0 state)

These four PCI Express interface reset sources are described in the sections that follow. PCI Express Reset events initiate a Local Bus Reset, which resets PEX 8311 registers and Local Bus backend logic.

Table 3-1 delineates which device resources are reset when each of the PCI Express reset sources are asserted.

Table 3-1. Full Device Reset Behavior

Reset Sources	Device Resources			
	PCI Express Interface Logic	Local Interface Logic	LRESET# Asserted	Configuration Registers
PCI Express PERST# signal asserted	X[a]	X	X	X
PCI Express Hot Reset	X	X	X	X[b]
PCI Express Link Down	X	X	X	X[b]
D3→D0 Power Management Reset	X	X	X	X

a. "X" represents "Don't Care."

b. **PECS General Purpose I/O Control (GPIOC)** register is not reset for Link Down nor Hot Reset.

3.1.1.1 PCI Express Reset PERST# Input (Hard Reset)

The PCI Express Reset PERST# input ball is a PCI Express System reset. It is asserted by the Root Complex and causes all PCI Express downstream devices to reset. The PEX 8311 is reset upon receiving PERST# asserted and causes Local LRESET# to assert. Most Local Bus output signals are set to float while LRESET# remains asserted, with the exceptions listed in Table 3-2.

The PEX 8311 uses the PCI Express PERST# signal as a fundamental reset input. When PERST# assertion follows the power-on event, it is referred to as a *Cold Reset*. The PCI Express system also generates this signal without removing power; which is referred to as a *Warm Reset*. The PEX 8311 treats Cold and Warm Resets without distinction. When the PERST# input is asserted low, all PEX 8311 internal logic is asynchronously reset, and all Configuration registers are initialized to their default values when PERST# is asserted. The PEX 8311 also places its Local Bus outputs into a high-impedance state, unless stated otherwise in Table 3-2 and Section 2.4, "Local Bus Interface Signals."

The PEX 8311 propagates the Cold/Warm Reset from the PCI Express interface to the Local reset interface. The LRESET# signal is asserted while PERST# is asserted. During a Cold Reset, LRESET# is asserted for at least 100 ms after the power levels are valid. During other types of resets, LRESET# is asserted for at least 1 ms. Local Bus Masters must allow sufficient time for the **LCS** Configuration Serial EEPROM load to complete before attempting accesses to PEX 8311 registers or PCI Express Space (this time depends upon the serial EEPROM load length).

Table 3-2. Local Bus Output Signals that Do Not Float when PERST# Is Asserted

Signal	Value when PERST# Is Asserted
EECS	0
EESK	0
LRESET#	0
USERo	0

3.1.1.2 Link Training and Status State Machine (LTSSM) Hot Reset

PCI Express supports the Link Training Control Reset (a training sequence with the *Hot Reset* bit asserted), or Hot Reset (as described in *PCI Express Base 1.0a*, Section 4.2.5.11), for propagating Reset requests downstream. When the PEX 8311 receives a Hot Reset on the PCI Express interface, it propagates that reset to the Local LRESET# signal. In addition, the PEX 8311 discards all transactions being processed and returns registers, state machines and externally observable state internal logic to the state-specified default or initial conditions. Software is responsible for ensuring that the Link Reset assertion and de-assertion messages are timed such that the bridge adheres to proper reset assertion and de-assertion durations on the Local LRESET# signal.

3.1.1.3 Primary Reset Due to Data Link Down

When the PEX 8311 PCI Express interface is in standard operation and the link is down, the Transaction and Data Link Layers enter the DL_Down state. The PEX 8311 discards all transactions being processed and returns registers, state machines and externally observable state internal logic to the state-specified default or initial conditions. In addition, the entry of the PEX 8311 PCI Express interface into DL_Down status initiates a Local Bus reset, using the Local LRESET# signal.

3.1.1.4 PCI Express Configuration Space Power Management Reset

When the **PECS Power Management Control/Status** register *Power State* field (**PWRMNGCSR**[1:0] transitions from 11b (D3) to 00b (D0), a full device reset is initiated. The effects of this reset are identical to a PERST# Hard Reset, as described in Section 3.1.1.1, "PCI Express Reset PERST# Input (Hard Reset)." This sequence includes:

1. All logic is reset.
2. All PECS and LCS registers is reset.
3. Local LRESET# is asserted.
4. PECS and LCS serial EEPROM loads.

3.1.2 Local Bridge Resets

In addition to PCI Express interface reset sources, the PEX 8311 supports the following Partial Device Resets:

- Local Bridge Full Reset, by way of the **PECS Bridge Control** register *Local Bridge Full Reset* bit (**BRIDGECTL**[6])
- Local Bridge Local Bus Reset, by way of the **LCS Control** register *Local Bus Reset* bit (**CNTRL**[30])

When attempting a Configuration access to the PEX 8311 on the Local Bus, the Local Bus Master device must allow sufficient time for the **LCS** Configuration Serial EEPROM load to complete before attempting accesses to the PEX 8311 (this time depends upon the serial EEPROM load length).

3.1.2.1 Local Bridge Full Reset by way of PECS Bridge Control Register

A Local Bus interface reset is initiated by software, by setting the **PECS Bridge Control** register *Local Bridge Full Reset* bit (**BRIDGECTL**[6]). This targeted reset is used for various reasons, including recovery from error conditions on the Local Bus, or to initiate re-enumeration. Writing 1 to the *Local Bridge Full Reset* bit resets all **Local Space Configuration** registers and Local Bus logic, and forces the Local Bus Reset (LRESET#) signal to assert.

The Local Bridge and backend logic remain held in reset while the *Local Bridge Full Reset* bit remains set. Software is responsible for ensuring that the PEX 8311 does not receive transactions that require forwarding to the **LCS** registers or Local Bus while the *Local Bridge Full Reset* bit is set. When the *Local Bridge Full Reset* bit is cleared, the **LCS** registers are initialized from the **LCS** Configuration Serial EEPROM, or set to hardwired defaults if no serial EEPROM is present. Designers must allow sufficient time for this operation to complete before attempting accesses to **LCS** registers or devices on the opposite bus. In addition, the **LCS PCI Configuration** registers (such as, **PCICR** and **BAR*n***) must be re-initialized by system software before attempting accesses from PCI Express Space to the **LCS Memory-Mapped** registers or Local Bus.

3.1.2.2 Local Bridge Local Bus Reset

A Local bridge Local Bus reset is initiated by the **LCS Control** register *Local Bus Reset* bit. When the *Local Bus Reset* bit is set (**CNTRL**[30]=1), the following functional blocks are reset:

- Local Bus logic
- DMA logic
- Local Space FIFOs
- **LCS Local Configuration** and **Messaging Queue** registers

The internal bus logic, **LCS PCI Configuration**, **DMA**, and **Runtime** registers, and *Local Init Status* bit (**LMISC1**[2]) are not reset.

When the *Local Bus Reset* bit is set (**CNTRL**[30]=1), the PEX 8311 responds to Type 0/Type 1, Memory-Mapped Configuration access to **LCS PCI Configuration**, **Local, Runtime,** and **DMA** registers, initiated from the PCI Express interface. Because the Local Bus is in reset, **LCS Local Configuration** and **Messaging Queue** registers are not accessible from PCI Express Space, and accesses are ***not*** allowed on the Local Bus. The PEX 8311 remains in this condition until the PCI Express Root Complex clears the bit (**CNTRL**[30]=0). The Local Bus serial EEPROM is reloaded when the *Reload Configuration Registers* bit is set (**CNTRL**[29]=1).

During a software reset, USERo is driven low. USERo (and PERST#) behavior is as follows:

- During a hard reset (PERST#=0), USERo is three-stated. On the second rising edge of LCLK after PERST# is de-asserted, LRESET# de-asserts. On the next falling edge of LCLK, USERo is driven to 0 (from three-state). On the next rising edge of LCLK, USERo is driven to the value specified in CNTRL[16] (default value = 1).
- When the *Local Bus Reset* bit is set (**CNTRL**[30]=1), the LRESET# and USERo signals are asserted low (0). When the *Local Bus Reset* bit is cleared (**CNTRL**[30]=0), USERo reverts to the value specified in **CNTRL**[16], one LCLK after the LRESET# signal is de-asserted (driven to 1).

Note: *The Local Bus cannot clear CNTRL[30] because the Local Bus is in a reset state, although the Local processor does not use LRESET# to reset.*

3.1.2.3 Local Configuration Space Power Management Reset

An **LCS** Power Management Reset occurs when the **LCS Power Management Control/Status** register *Power State* field (**PMCSR**[1:0]) transitions from D3hot to D0. This action results in a Local Bridge Full Reset, as described in Section 3.1.2, "Local Bridge Resets."

3.2 Root Complex Mode Reset Operation

The PEX 8311 operates in Root Complex mode when its ROOT_COMPLEX# signal is strapped low. Table 3-3 delineates the four Root Complex mode Reset mechanisms.

Table 3-4 delineates which device resources are reset when each of the Local Bus reset sources are asserted or set.

Table 3-3. Root Complex Mode Reset Mechanisms

Reset Mechanism	Reset Type	Description
Local LRESET# signal	Hard Reset	Upon LRESET# assertion, all internal logic and registers are reset, and a Fundamental Reset is output to PCI Express space through PERST# assertion. When LRESET# is de-asserted, the Local and PCI Express Configuration serial EEPROMS are loaded.
LCS Control register *Local Bus Reset* bit (**CNTRL**[30])	PCI Express Bridge Reset	Causes a Partial Reset of the Local Bridge and Full Reset of the PCI Express Bridge. When cleared, the Local and PCI Express Configuration serial EEPROMS are loaded.
PECS Bridge Control register *PCI Express Hot Reset* bit (**BRIDGECTL**[6])	PCI Express Interface Reset	Resets the **PECS PCI** Configuration registers, and generates an LTSSM Hot Reset to PCI Express space. When cleared, **PECS** registers are loaded from serial EEPROM. **LCS** registers are not affected by this reset.
PECS Power Management Control/Status register *Power State* bit transition from D3→D0 state (**PMCSR**[1:0])	PCI Express Power Management Reset	Resets the **PECS PCI** Configuration registers, and generates an LTSSM Hot Reset to PCI Express space.

Table 3-4. Root Complex Mode Reset Behavior

Reset Source	LCS Registers		PECS Registers	PCI Express Reset Out	
	LOCAL, RTIME, MSG	PCI, DMA, EEPROM_RD	ALL_REGS, EEPROM_RD	Hot Reset (LTSSM)	Fundamental Reset (PERST#)
LRESET# Signal	X[a]	X	X	X	X
LCS **CNTRL**[30]=1	–[b]	X	X	X	X
PECS **BRIDGECTL**[6]=1	–	–	–	X	–
PECS (**PMCSR**[1:0]) D3hot→D0	–	–	X	X	–

a. "X" represents "Don't Care."

b. "–" represents "Not Applicable."

3.2.1 Local Bus Reset

In Root Complex mode (ROOT_COMPLEX# strapped low), the Local LRESET# signal is the primary hardware Reset input. LRESET# assertion results in a complete reset of all PEX 8311internal logic and all **PECS** and **LCS** registers. LRESET# assertion also causes PERST# assertion, which resets downstream devices as well. The **PECS** and **LCS** register serial EEPROM load begins after LRESET# is de-asserted.

Table 3-5 delineates the Local Bus Output signals that do not float when LRESET# is asserted.

Table 3-5. Local Bus Output Signals that Do Not Float when LRESET# Is Asserted

Signal	Value when LRESET# Is Asserted
EECS	0
EESK	0
USERo	0

3.2.2 PCI Express Bridge Reset

A PCI Express interface reset, PCI Express logic, and localized Local Bus logic within the PEX 8311 is initiated by the **LCS Control** register *PCI Express Bridge Reset* bit. When the *PCI Express Bridge Reset* bit is set (CNTRL[30]=1), the following functional blocks are reset:

- Internal Master logic on the Local Bus
- Internal Slave logic on the Local Bus
- DMA logic
- **Type 1 Configuration**, **Mailbox**, **DMA**, and **PECS** registers
- PCI Express logic
- Local Space FIFOs
- Internal interrupts/lock
- Power Management interrupts
- PERST# Asserted to PCI Express interface

The Local Bus logic, **Local Configuration**, **Runtime**, and **Messaging Queue** registers are ***not*** reset. A PCI Express Bridge Reset is cleared only by a Local Bus Master on the Local Bus. The PEX 8311 remains in this reset condition for the duration that the *PCI Express Bridge Reset* bit is set (**CNTRL**[30]=1). During this time, the PEX 8311 responds only to Local Bus-initiated **Local Configuration**, **Runtime**, and **DMA** registers' accesses.

Note: *The PCI Express Bridge Reset bit cannot be cleared from the PCI Express interface because the PCI Express is in a reset state and Configuration accesses to Root Complex by the downstream devices are illegal.*

3.2.3 PCI Express Hot Reset by way of PECS Bridge Control Register

A PCI Express interface reset is initiated by software, by setting the **Bridge Control** register *PCI Express Hot Reset* bit. This targeted reset is used for various reasons, including recovery from error conditions on the PCI Express interface, or to initiate re-enumeration.

A Write to the *PCI Express Hot Reset* bit causes a PCI Express Link Training and Status State Machine (LTSSM) Hot Reset sequence to transmit, without affecting the **LCS** registers. In addition, the logic associated with the PCI Express interface is re-initialized and transaction buffers associated with the PCI Express interface are cleared.

3.2.4 PCI Express Configuration Space Power Management Reset

When the **PECS Power Management Control/Status** register *Power State* field (**PWRMNGCSR**[1:0]) changes from 11b (D3) to 00b (D0), a Fundamental Reset of the PCI Express bridge is initiated. This sequence includes:

1. All PECS registers is reset.
2. All PCI Express logic is reset.
3. LTSSM Hot Reset is transmitted to PCI Express space.
4. PECS serial EEPROM loads.

LCS registers are ***not*** affected. Register values loaded by the Local Host processor, after the **PECS** Serial EEPROM loads, must be restored before resuming operation.

3.3 Initialization Summary

3.3.1 PCI Express Interface

The PEX 8311 supports the following initialization sequences on the PCI Express interface:

- No serial EEPROM, blank serial EEPROM, or invalid serial EEPROM
  - If the first byte read from the serial EEPROM is not a valid signature byte (5Ah), then an invalid serial EEPROM is detected. In this case, the default PCI Express Device ID (8111h) is selected. Use a 10K-Ohm pull-up resistor to ensure that EERDDATA is high when no serial EEPROM is installed.
  - Enable the PCI Express and internal interfaces, using default register values.
- Valid serial EEPROM with Configuration register data
  - Enable the PCI Express and internal interfaces using register values loaded from the serial EEPROM. The **DEVINIT** register interface enable bits are the last set by the serial EEPROM.

3.3.2 Local Bus Interface

The PEX 8311 supports the following initialization sequences on the Local Bus interface:

- No serial EEPROM, blank serial EEPROM, or Local Bus Processor
  - If the EEDI/EEDO ball is always high (1K-Ohm pull-up resistor is recommended), then no physical serial EEPROM is detected. In this case, the Local Processor must be present to configure the PEX 8311 Local Bus and set Local Init Status bit LMISC1[2]=1.
  - If the EEDI/EEDO ball is always low (1K-Ohm pull-down resistor is recommended), then no physical serial EEPROM is detected. In this case, the PEX 8311 Local Bus is reverted to its default values and sets the *Local Init Status* bit **LMISC1**[2]=1 by itself, regardless of whether the Local Processor is present. Local Bus Device ID (9056h) is selected.
- Valid serial EEPROM with configuration register data
  - The PEX 8311 Local Bus is configured by the serial EEPROM and designer, to define whether to set the *Local Init Status* bit by serial EEPROM or Local Processor, when present.

Chapter 4 Serial EEPROM Controllers

4.1 Overview

For initializing its internal registers following power-on or exit from reset, the PEX 8311 provides two serial EEPROM interfaces:

- **SPI-compatible interface** – Used for loading of registers in the PCI Express Configuration Space (**PECS**)
- **Micro-Wire-compatible interface** – Used to load registers in the Local Configuration Space (**LCS**)

These serial EEPROMs are required only when default values are not suitable for the application in use.

4.2 PCI Express Configuration Space Serial EEPROM Interface (SPI-Compatible Interface)

The PEX 8311 provides an interface to SPI-compatible serial EEPROMs. This interface consists of a Chip Select, Clock, Write Data, and Read Data balls, and operates at up to 25 MHz. Compatible 128-byte serial EEPROMs include the Atmel AT25010A, Catalyst CAT25C01, and ST Microelectronics M95010W. The PEX 8311 supports up to a 16-MB serial EEPROM, utilizing 1-, 2-, or 3-byte addressing. ThePEX 8311 automatically determines the appropriate addressing mode.

4.2.1 Serial EEPROM Data Format

The serial EEPROM data is stored in the following format as delineated in Table 4-1.

Table 4-1. Serial EEPROM Data

Location	Value	Description
0h	5Ah	Validation Signature
1h	Refer to Table 4-2	Serial EEPROM Format Byte
2h	REG BYTE COUNT (LSB)	Configuration register Byte Count (LSB)
3h	REG BYTE COUNT (MSB)	Configuration register Byte Count (MSB)
4h	REGADDR (LSB)	1st Configuration Register Address (LSB)
5h	REGADDR (MSB)	1st Configuration Register Address (MSB)
6h	REGDATA (Byte 0)	1st Configuration Register Data (Byte 0)
7h	REGDATA (Byte 1)	1st Configuration Register Data (Byte 1)
8h	REGDATA (Byte 2)	1st Configuration Register Data (Byte 2)
9h	REGDATA (Byte 3)	1st Configuration Register Data (Byte 3)
Ah	REGADDR (LSB)	2nd Configuration Register Address (LSB)
Bh	REGADDR (MSB)	2nd Configuration Register Address (MSB)
Ch	REGDATA (Byte 0)	2nd Configuration Register Data (Byte 0)
Dh	REGDATA (Byte 1)	2nd Configuration Register Data (Byte 1)

Table 4-1. Serial EEPROM Data *(Cont.)*

Location	Value	Description
Eh	REGDATA (Byte 2)	2nd Configuration Register Data (Byte 2)
Fh	REGDATA (Byte 3)	2nd Configuration Register Data (Byte 3)
……		
REG BYTE COUNT + 4	MEM BYTE COUNT (LSB)	Shared memory Byte Count (LSB)
REG BYTE COUNT + 5	MEM BYTE COUNT (MSB)	Shared memory Byte Count (MSB)
REG BYTE COUNT + 6	SHARED MEM (Byte 0)	1st byte Shared memory
REG BYTE COUNT + 7	SHARED MEM (Byte 1)	2nd byte of Shared Memory
……		
FFFFh	SHARED MEM (Byte *n*)	Last byte of Shared Memory

Table 4-2 delineates the serial EEPROM Format Byte organization.

Table 4-2. Serial EEPROM Format Byte

Bits	Description
0	**Configuration Register Load.** When set, configuration registers are loaded from the EEPROM. The address of the first configuration register is located at bytes 3 and 4 in the EEPROM. When cleared, but REG BYTE COUNT is non-zero, the configuration data is read from the EEPROM and discarded.
1	**Shared Memory Load.** When set, shared memory is loaded from the serial EEPROM starting at location REG BYTE COUNT + 6. The byte number to load is determined by the value in serial EEPROM locations REG BYTE COUNT + 4 and REG BYTE COUNT + 5.
7:2	***Reserved***

4.2.2 Initialization

After the device reset is de-asserted, the serial EEPROM internal status register is read to determine whether a serial EEPROM is installed. A pull-up resistor on the EERDDATA ball produces a value of FFh when there is no serial EEPROM installed. If a serial EEPROM is detected, the first byte (validation signature) is read. If a value of 5Ah is read, it is assumed that the serial EEPROM is programmed for the PEX 8311. The serial EEPROM address width is determined while this first byte is read. If the first byte is not 5Ah, the serial EEPROM is blank, or programmed with invalid data. In this case, the PCI Express and PCI interfaces are enabled for a default enumeration. Also, the **Serial EEPROM Control (EECTL)** register *serial EEPROM Address Width* field reports a value of 0 (undetermined width).

When the serial EEPROM contains valid data, the second byte (Serial EEPROM Format Byte) is read to determine which sections of the serial EEPROM are loaded into the PEX 8311 configuration registers and memory.

Bytes 2 and 3 determine the amount of serial EEPROM locations containing configuration register addresses and data. Each configuration register entry consists of two bytes of register address (bit 12 low selects the PCI configuration registers, and bit 12 high selects the Memory-Mapped Configuration registers) and four bytes of register write data. If bit 1 of the serial EEPROM Format Byte is set, locations REG BYTE COUNT + 4 and REG BYTE COUNT + 5 are read to determine the number of bytes to transfer from the serial EEPROM into shared memory.

The REG BYTE COUNT must be a multiple of 6 and MEM BYTE COUNT must be a multiple of 4.

The EECLK ball frequency is determined by the **Serial EEPROM Clock Frequency** (**EECLKFREQ)** register *EE Clock Frequency* field. The default clock frequency is 2 MHz. At this clock rate, it takes about 24 µs per DWORD during configuration register or shared memory initialization. For faster loading of large serial EEPROMs that support a faster clock, the first configuration register load from the serial EEPROM is to the **Serial EEPROM Clock Frequency** (**EECLKFREQ**) register.

Note: *When operating in Root Complex mode, ensure that the serial EEPROM sets the* ***DEVINIT*** *register PCI Enable bit. When operating in Endpoint mode, ensure the serial EEPROM sets the* ***DEVINIT*** *register PCI Express Enable bit.*

4.2.3 Serial EEPROM Random Read/Write Access

A PCI Express or internal PCI Bus master can use the **Serial EEPROM Control (EECTL)** register to access the serial EEPROM. This register contains 8-bit read and write data fields, read and write start signals, and related status bits.

The following "C" routines demonstrate the firmware protocol required to access the serial EEPROM through the **Serial EEPROM Control (EECTL)** register. An interrupt is generated when the **Serial EEPROM Control (EECTL)** register *Serial EEPROM BUSY* bit moves from true to false.

4.2.3.1 Serial EEPROM Opcodes

```
READ_STATUS_EE_OPCODE = 5
WREN_EE_OPCODE = 6
WRITE_EE_OPCODE = 2
READ_EE_OPCODE = 3
```

4.2.3.2 Serial EEPROM Low-Level Access Routines

```
int EE_WaitIdle()
{
    int eeCtl, ii;
    for (ii = 0; ii < 100; ii++)
     {
        PEX 8311Read(EECTL, eeCtl);      /* read current value in EECTL */
        if ((eeCtl & (1 << EEPROM_BUSY)) == 0) /* loop until idle */
            return(eeCtl);
    }
    PANIC("EEPROM Busy timeout!\n");
}
void EE_Off()
{
    EE_WaitIdle();                       /* make sure EEPROM is idle */
    PEX 8311Write(EECTL, 0);             /* turn off everything (especially
EEPROM_CS_ENABLE)*/
}
int EE_ReadByte()
{
    int eeCtl = EE_WaitIdle();           /* make sure EEPROM is idle */
    eeCtl |= (1 << EEPROM_CS_ENABLE) |
             (1 << EEPROM_BYTE_READ_START);
    PEX 8311Write(EECTL, eeCtl);         /* start reading */
    eeCtl = EE_WaitIdle();               /* wait until read is done */
    return((eeCtl >> EEPROM_READ_DATA) & FFh); /* extract read data from
EECTL */
}
void EE_WriteByte(int val)
{
    int eeCtl = EE_WaitIdle();           /* make sure EEPROM is idle */
    eeCtl &= ~(FFh << EEPROM_WRITE_DATA);/* clear current WRITE value */
    eeCtl |= (1 << EEPROM_CS_ENABLE) |
             (1 << EEPROM_BYTE_WRITE_START) |
             ((val & FFh) << EEPROM_WRITE_DATA);
    PEX 8311Write(EECTL, eeCtl);
}
```

4.2.3.3 Serial EEPROM Read Status Routine

```
...
EE_WriteByte(READ_STATUS_EE_OPCODE);  /* read status opcode */
status = EE_ReadByte();               /* get EEPROM status */
EE_Off();                             /* turn off EEPROM */
...
```

4.2.3.4 Serial EEPROM Write Data Routine

```
...
EE_WriteByte(WREN_EE_OPCODE);         /* must first write-enable */
EE_Off();                             /* turn off EEPROM */
EE_WriteByte(WRITE_EE_OPCODE);        /* opcode to write bytes */
#ifdef THREE_BYTE_ADDRESS_EEPROM      /* three-byte addressing EEPROM? */
    EE_WriteByte(addr >> 16);         /* send high byte of address */
#endif
EE_WriteByte(addr >> 8);              /* send next byte of address */
EE_WriteByte(addr);                   /* send low byte of address */
for (ii = 0; ii < n; ii++)
{
    EE_WriteByte(buffer[ii]);         /* send data to be written */
}
EE_Off();                             /* turn off EEPROM */
...
```

4.2.3.5 Serial EEPROM Read Data Routine

```
...
EE_WriteByte(READ_EE_OPCODE);         /* opcode to write bytes */
#ifdef THREE_BYTE_ADDRESS_EEPROM      /* three-byte addressing EEPROM? */
    EE_WriteByte(addr >> 16);         /* send high byte of address */
#endif
EE_WriteByte(addr >> 8);              /* send next byte of address */
EE_WriteByte(addr);                   /* send low byte of address */
for (ii = 0; ii < n; ii++)
{
   buffer[ii] = EE_ReadByte(buffer[ii]);   /* store read data in buffer */
}
EE_Off();                             /* turn off EEPROM */
```

4.3 Local Configuration Space Serial EEPROM Interface (Micro-Wire-Compatible Interface)

This section describes **LCS** serial EEPROM use within the PEX 8311. The PEX 8311 Local Bus supports 2K- or 4K-bit serial EEPROMs. The PEX 8311 requires serial EEPROMs that support sequential reads. (Visit http://www.plxtech.com/products/io_accelerators/default.asp for the latest information on supported serial EEPROMs.)

The PEX 8311 supports two serial EEPROM load lengths – long serial EEPROM and extra long serial EEPROM (refer to Figure 4-1):

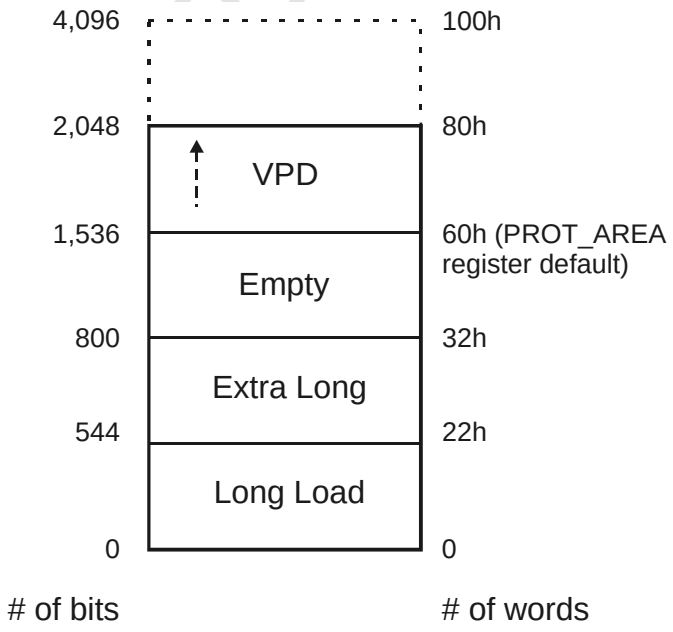
- **Long Load Mode** – Default. The PEX 8311 Local Bus loads 34, 16-bit words from the serial EEPROM when the Extra Long Load from Serial EEPROM bit is clear (LBRD0[25]=0)
- **Extra Long Load Mode** – The PEX 8311 Local Bus loads 50, 16-bit words from the serial EEPROM when the Extra Long Load from Serial EEPROM bit is set (LBRD0[25]=1)

The serial EEPROM is read or written from the PCI Express interface or Local Bus, through the Serial EEPROM Control register bits (CNTRL[31, 27:24]) or VPD capability on the Local Configuration space.

The 3.3V serial EEPROM clock (EESK) is internally derived. The PEX 8311 generates the serial EEPROM clock by internally dividing the 66.6 MHz clock by 268. For internal 66.6 MHz running clock, EESK is 248.7 kHz.

During Local Bus serial EEPROM loading, the PEX 8311 accepts Direct Slave accesses but can take longer (in the case of a Read access) to respond with Completions until the Local Init Status bit is set. Local Processor accesses are delayed by holding READY# de-asserted.

Figure 4-1. Serial EEPROM Memory Map



4.3.1 PEX 8311 Initialization from Serial EEPROM

After reset, the PEX 8311 attempts to read the serial EEPROM to determine its presence. A first-returned bit cleared to 0 indicates a serial EEPROM is present. The first word is then checked to verify that the serial EEPROM is programmed. If the first word (16 bits) is all ones (1), a blank serial EEPROM is present. If the first word (16 bits) is all zeros (0), no serial EEPROM is present. For both conditions, the PEX 8311 reverts to the default values. (Refer to Table 4-3.) The Serial EEPROM Present bit is set (CNTRL[28]=1) when the serial EEPROM is detected as present and is programmed or blank.

The PEX 8311 **LCS** registers is programmed by an optional serial EEPROM and/or by a Local processor, as delineated in Table 4-3. The serial EEPROM is reloaded by setting the *Reload Configuration Registers* bit (CNTRL[29]=1).

The PEX 8311 internally Retries all PCI Express-initiated accesses, or allows Master Aborts until the *Local Init Status* bit is set to "done" (LMISC1[2]=1).

Note: *All PCI Express accesses are granted after the Local Init Status bit is set.*

Table 4-3. Serial EEPROM Guidelines

Local Processor	Local Bus Serial EEPROM	System Boot Condition	Device which Sets LMISC1[2]
None	None	The PEX 8311 Local Bus uses default values. The EEDI/EEDO ball must be pulled low – a 1K-Ohm resistor is required (rather than pulled high, which is typically executed for this ball). If the PEX 8311 Local Bus detects all zeros (0), it reverts to default values and sets the Local Init Status bit (**LMISC1**[2]=1) by itself.	PEX 8311
None	Programmed	Boot with serial EEPROM values. The Local Init Status bit must be set (**LMISC1**[2]=1) by the serial EEPROM.	Serial EEPROM
None	Blank	The PEX 8311 Local Bus detects a blank device, reverts to default values, and sets the Local Init Status bit (**LMISC1**[2]=1) by itself.	PEX 8311
Present	None	The Local processor programs the PEX 8311 registers, then sets the Local Init Status bit (**LMISC1**[2]=1). A 1K-Ohm or greater value pull-up resistor or EEDI/EEDO is recommended, but not required. The EEDI/EEDO ball has an internal pull-up resistor. (Refer to Table 2-4."Balls with Internal 100K-Ohm Pull-Up Resistors (to VDD3.3),") ***Note:*** *Certain systems can avoid configuring devices that do not respond with successful completion or completion with CRS set. In this case, the Root Complex times out after completion. In addition, certain systems can hang when Direct Slave reads and writes take overly long (during initialization, the Root Complex also performs Direct Slave accesses). The value of the Direct Slave Retry Delay Clocks in the Local Configuration space (**LBRD0**[31:28]) can resolve this.*	Local CPU
Present	Programmed	Load serial EEPROM, but the Local processor cannot reprogram the PEX 8311. Either the Local processor or the serial EEPROM must set the Local Init Status bit (**LMISC1**[2]=1).	Serial EEPROM or Local CPU
Present	Blank	The PEX 8311 detects a blank serial EEPROM and reverts to default values. ***Notes:*** *In certain systems, the Local processor can be overly late to reconfigure the PEX 8311 registers before the BIOS configures them.* *The serial EEPROM is programmed through the PEX 8311 after the system boots in this condition.*	PEX 8311

Note: *When the serial EEPROM is missing and a Local processor is present with blank Flash, the condition None/None (as listed in Table 4-3) applies, until the processor's Flash is programmed.*

4.3.2 Local Initialization and PCI Express Interface Behavior

The PEX 8311 issues an internal Retry or allows an internal Master Abort to generate to the internal PCI Express interface block, depending on the USERi strapping option during the PEX 8311 RESET condition until the Local Init Status bit is set (**LMISC1**[2]=1). This bit is programmed in three ways:

1. By the Local processor, through the Local Configuration register.
2. By the serial EEPROM, during a serial EEPROM load, when the Local processor does not set this bit.
3. If the Local processor and the serial EEPROM are missing, or the serial EEPROM is blank (with or without a Local processor), the PEX 8311 uses defaults and sets this bit. (Refer to Table 4-3.)

To avoid the PEX 8311 generating Unsupported Request (UR) to the Root Complex Configuration Register accesses to the Local Configuration space during serial EEPROM loading, the USERi ball must be pulled high. The PEX 8311 determines the behavior, as follows:

- The USERi ball is sampled at the rising edge of PERST# to determine the selected response mode during Local Bus initialization.
- If USERi is low (through an external 1K-Ohm pull-down resistor), the PEX 8311 responds with UR Completions to the PCI Express Type 1 accesses to the PEX 8311 Local Configuration space until Local Bus initialization is complete.
- If USERi is high (through an external 1K- to 4.7K-Ohm pull-up resistor), the PEX 8311 responds to PCI Express Type 1 accesses to the Local Configuration space, with either Completion with CRS set or Successful Completion with data after Local Bus initialization is complete. This depends on the **PECS PCI Express Device Control** register *Bridge Configuration Retry Enable* bit being set (**DEVCTL**[15]=1). Local Bus initialization is complete when the **LCS** *Local Init Status* bit is set (**LMISC1**[2]=1).

During run time, USERi is used as a general-purpose input. [Refer to Table 2-8 (C mode) and Table 2-9 (J mode).]

4.3.2.1 Long Serial EEPROM Load

If the Extra Long Load from Serial EEPROM bit is ***not*** set (**LBRD0**[25]=0), the registers listed in Table 4-4 are loaded from the serial EEPROM after a reset is de-asserted. The serial EEPROM is organized in words (16 bits). The PEX 8311 first loads the Most Significant Word bits (MSW[31:16]), starting from the Most Significant Bit (MSB[31]). The PEX 8311 then loads the Least Significant Word bits (LSW[15:0]), starting again from the Most Significant Bit (MSB[15]). Therefore, the PEX 8311 loads the Device ID, Vendor ID, Class Code, and so forth.

The serial EEPROM values is programmed using a serial EEPROM programmer. The values can also be programmed using the PEX 8311 VPD function. [Refer to Chapter 16, "Vital Product Data (VPD)," or through the Serial EEPROM Control register (**CNTRL**).]

Using the **CNTRL** register or VPD, the designer can perform reads and writes from/to the serial EEPROM, 32 bits at a time. Program serial EEPROM values in the order listed in Table 4-4. The 34, 16-bit words listed in the table are stored sequentially in the serial EEPROM.

4.3.2.2 Extra Long Serial EEPROM Load

If the Extra Long Load from Serial EEPROM bit is set (LBRD0[25]=1), the registers listed in Table 4-4 and Table 4-5 are loaded from the serial EEPROM, with the Table 4-4 values loaded first.

Program serial EEPROM values in the order listed in Table 4-5. Store the 50 16-bit words listed in Table 4-4 and Table 4-5 sequentially in the serial EEPROM, with the Table 4-4 values loaded first.

Table 4-4. Long Serial EEPROM Load Registers

Serial EEPROM Byte Offset	Description	Register Bits Affected
0h	PCI Device ID	PCIIDR[31:16]
2h	PCI Vendor ID	PCIIDR[15:0]
4h	PCI Class Code	PCICCR[23:8]
6h	PCI Class Code / Revision ID	PCICCR[7:0] / PCIREV[7:0]
8h	PCI Maximum Latency / PCI Minimum Grant	PCIMLR[7:0] / PCIMGR[7:0]
Ah	Internal PCI Wire Interrupt / Internal PCI Interrupt Line	PCIIPR[7:0] / PCIILR[7:0]
Ch	MSW of Mailbox 0 (User-Defined)	MBOX0[31:16]
Eh	LSW of Mailbox 0 (User-Defined)	MBOX0[15:0]
10h	MSW of Mailbox 1 (User-Defined)	MBOX1[31:16]
12h	LSW of Mailbox 1 (User-Defined)	MBOX1[15:0]
14h	MSW of Direct Slave Local Address Space 0 Range	LAS0RR[31:16]
16h	LSW of Direct Slave Local Address Space 0 Range	LAS0RR[15:0]
18h	MSW of Direct Slave Local Address Space 0 Local Base Address (Remap)	LAS0BA[31:16]
1Ah	LSW of Direct Slave Local Address Space 0 Local Base Address (Remap)	LAS0BA[15:2, 0], ***Reserved*** [1]
1Ch	MSW of Mode/DMA Arbitration	MARBR[31,29:16] or DMAARB[31, 29:16], ***Reserved*** [30]
1Eh	LSW of Mode/DMA Arbitration	MARBR[15:0] or DMAARB[15:0]
20h	Local Miscellaneous Control 2 / Serial EEPROM Write-Protected Address Boundary	LMISC2[5:0], ***Reserved*** [7:6] / PROT_AREA[6:0], ***Reserved*** [7]
22h	Local Miscellaneous Control 1 / Local Bus Big/Little Endian Descriptor	LMISC1[7:0] / BIGEND[7:0]
24h	MSW of Direct Slave Expansion ROM Range	EROMRR[31:16]
26h	LSW of Direct Slave Expansion ROM Range	EROMRR[15:11, 0], ***Reserved*** [10:1]
28h	MSW of Direct Slave Expansion ROM Local Base Address (Remap) and BREQo Control	EROMBA[31:16]
2Ah	LSW of Direct Slave Expansion ROM Local Base Address (Remap) and BREQo Control	EROMBA[15:11, 5:0], ***Reserved*** [10:6]
2Ch	MSW of Local Address Space 0/Expansion ROM Bus Region Descriptor	LBRD0[31:16]
2Eh	LSW of Local Address Space 0/Expansion ROM Bus Region Descriptor	LBRD0[15:0]
30h	MSW of Local Range for Direct Master-to-PCI	DMRR[31:16]
32h	LSW of Local Range for Direct Master-to-PCI ***(Reserved)***	DMRR[15:0]
34h	MSW of Local Base Address for Direct Master-to-PCI Memory	DMLBAM[31:16]
36h	LSW of Local Base Address for Direct Master-to-PCI Memory ***(Reserved)***	DMLBAM[15:0]
38h	MSW of Local Bus Address for Direct Master-to-PCI I/O Configuration	DMLBAI[31:16]

Table 4-4. Long Serial EEPROM Load Registers *(Cont.)*

Serial EEPROM Byte Offset	Description	Register Bits Affected
3Ah	LSW of Local Bus Address for Direct Master-to-PCI I/O Configuration ***(Reserved)***	DMLBAI[15:0]
3Ch	MSW of PCI Base Address (Remap) for Direct Master-to-PCI Memory	DMPBAM[31:16]
3Eh	LSW of PCI Base Address (Remap) for Direct Master-to-PCI Memory	DMPBAM[15:0]
40h	MSW of PCI Configuration Address for Direct Master-to-PCI I/O Configuration	DMCFGA[31, 23:16], ***Reserved*** [30:24]
42h	LSW of PCI Configuration Address for Direct Master-to-PCI I/O Configuration	DMCFGA[15:0]

Table 4-5. Extra Long Serial EEPROM Load Registers

Serial EEPROM Byte Offset	Description	Register Bits Affected
44h	PCI Subsystem ID	PCISID[15:0]
46h	PCI Subsystem Vendor ID	PCISVID[15:0]
48h	MSW of Direct Slave Local Address Space 1 Range (1 MB)	LAS1RR[31:16]
4Ah	LSW of Direct Slave Local Address Space 1 Range (1 MB)	LAS1RR[15:0]
4Ch	MSW of Direct Slave Local Address Space 1 Local Base Address (Remap)	LAS1BA[31:16]
4Eh	LSW of Direct Slave Local Address Space 1 Local Base Address (Remap)	LAS1BA[15:2, 0], ***Reserved*** [1]
50h	MSW of Local Address Space 1 Bus Region Descriptor	LBRD1[31:16]
52h	LSW of Local Address Space 1 Bus Region Descriptor ***(Reserved)***	LBRD1[15:0]
54h	Hot Swap Control/Status ***(Reserved)***	***Reserved***
56h	Hot Swap Next Capability Pointer / Hot Swap Control ***(Reserved)***	HS_NEXT[7:0] / HS_CNTL[7:0]
58h	***Reserved***	Reserved
5Ah	Internal Arbiter Control	PCIARB[3:0], ***Reserved*** [15:4]
5Ch	Power Management Capabilities	PMC[15:9, 2:0]
5Eh	Power Management Next Capability Pointer ***(Reserved)*** / Power Management Capability ID ***(Reserved)***	Reserved
60h	Power Management Data / PMCSR Bridge Support Extension ***(Reserved)***	PMDATA[7:0] / ***Reserved***
62h	Power Management Control/Status	PMCSR[14:8]

4.3.3 Serial EEPROM Access

The CNTRL[31, 27:24] register bits are programmed to control the EESK, EECS, and EEDI/EEDO settings. Bit 24 is used to generate EESK (clock), bit 25 controls the Chip Select, bit 26 controls the EEDI output logic level, and bit 31 enables the EEDO Input buffer. Bit 27, when read, returns the value of EEDI.

Setting bits [31, 25:24] to 1 causes the output to go high. A pull-up resistor is required on the EEDI/EEDO ball for the ball to go high when bit 31 is set. When reading the EEPROM, bit 31 must be set to 1 (CNTRL[31]=1).

To perform the read, the basic approach is to set the EECS and EEDO bits (bits [25, 31]=11b, respectively) to the desired level and then toggle EESK high and low until completed. *For example*, reading the serial EEPROM at location 0 involves the following steps:

1. Clear the EECS, EEDI, EEDO, and EESK Input Enable bits.
2. Set EECS high.
3. Toggle EESK high, then low.
4. Set the EEDI bit high (Start bit).
5. Toggle EESK high, then low.
6. Repeat step 5.
7. Clear EEDI.
8. Toggle EESK high, then low.
9. Toggle EESK high, then low 8 times (clock in Serial EEPROM Address 0).
10. Set EEDO Input Enable to 1 (CNTRL[31]=1) to float the EEDO input for reading.
11. Toggle EESK high, then low 16 times (clock in 1 word from serial EEPROM).
12. After each clock pulse, read bit 27 and save.
13. Clear the EECS bit.
14. Toggle EESK high, then low. The read is complete.

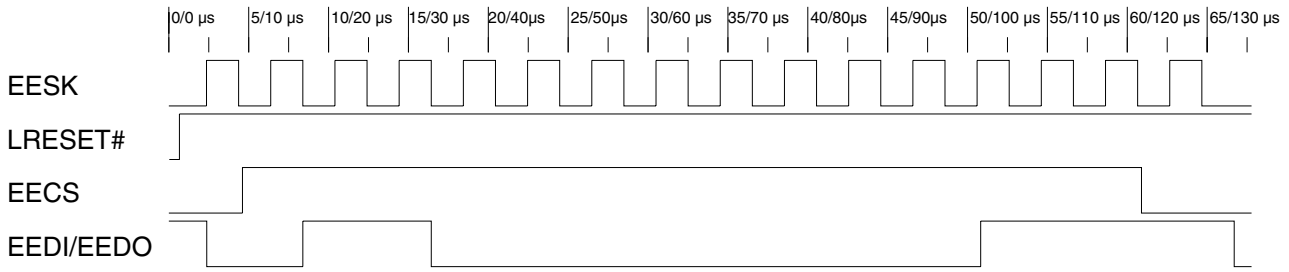
The serial EEPROM uses word addressing with 8-bit sequential address values. Due to PEX 8311 Local Bus EEPROM interface EEDI/EEDO signal multiplexing and to avoid contention between the least-significant Address bit and the serial EEPROM's Start bit, Read access to an odd-numbered word address (bit 0 set) must be performed by using the even-numbered word address (bit 0 clear), along with the serial EEPROM's sequential read functionality, clocking in 32 (or more) data bits while keeping EECS continually asserted during the Read access.

During a serial EEPROM Write operation, the serial EEPROM's programming cycle is triggered by EECS de-assertion. When EECS is re-asserted, the serial EEPROM drives its Ready status on its DO ball connected to the PEX 8311 EEDI/EEDO ball. (Refer to manufacturer's data sheet for Ready functionality.) Ready status (DO=1) indicates internal write completion. If the PEX 8311 is driving the EEDI (EEDI/EEDO ball) signal to a logic low when EECS is reasserted after a Write operation, contention exists on the multiplexed EEDI/EEDO bus. The contention is released when Ready functionality is cleared by clocking in a Start bit (causing the serial EEPROM to float its DO output). To remove contention following a Write cycle, re-assert EECS after waiting the Minimum CS Low Time, and, after Ready status is high or the Write Cycle Time expires (typically 10 to 15 µs), set the EEDI output to logic high, then clock the Start bit into the serial EEPROM by toggling EESK high, then low. This Start bit is used as part of the next serial EEPROM instruction, or, the cycle is terminated by de-asserting EECS. Contention can also be avoided by setting the EEDI output high after clocking out the LSB of the data after each Write sequence.

The serial EEPROM can also be read or written, using the VPD function. [Refer to Chapter 16, "Vital Product Data (VPD)."]

4.3.4 Serial EEPROM Initialization Timing Diagram

Figure 4-2. Serial EEPROM Initialization Timing Diagram



Notes: *Time scales provided are based on a 66-MHz internal clock.*

The EEDI/EEDO signal is not sampled by the serial EEPROM until after EECS is asserted.

Upon LRESET# de-assertion, the PEX 8311 issues a Read command of Serial EEPROM Address 0.

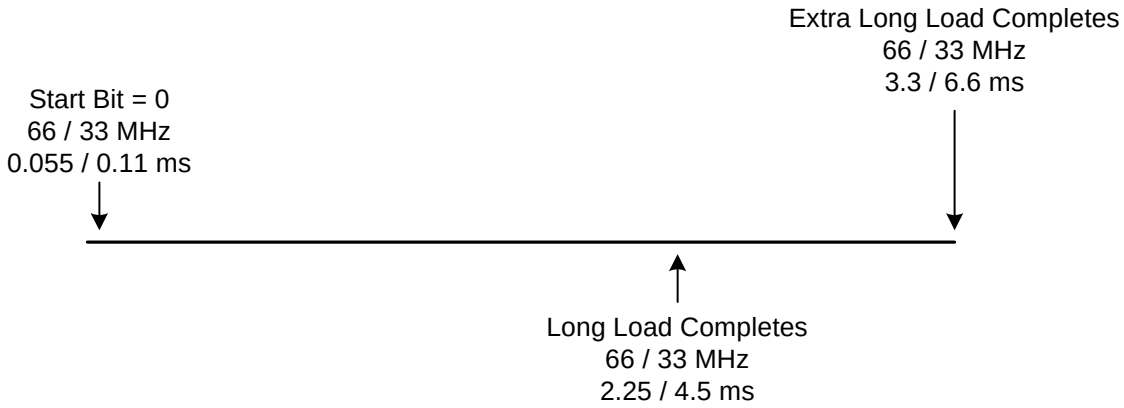
For this timing diagram, no serial EEPROM is present; however, the Local processor is present to perform initialization. Therefore, the PEX 8311 does not detect a serial EEPROM Start bit because the EEDI/EEDO signal is sampled high (due to the internal pull-up resistor). Thereafter, the EESK, EECS and EEDI/EEDO signal balls are driven to 0.

When the PEX 8311 detects a serial EEPROM Start bit and the first 16 bits (which correspond to PCIIDR[31:16]) are not all zeros (0) or all ones (1), the PEX 8311 continues to assert EECS and generate the serial EEPROM clock (EESK) to load its registers with the programmed serial EEPROM values.

The first bit downloaded after the Start bit is PCIIDR[31].

Figure 4-3 illustrates the approximate length of time required to detect the Start bit, and length of time required for Long or Extra Long Serial EEPROM Load. While the PEX 8311 is downloading serial EEPROM data, PCI accesses to the PEX 8311 are Retried and Local Master accesses are accepted, but do not complete (READY# de-asserted) until the serial EEPROM download completes.

Figure 4-3. Serial EEPROM Timeline



Chapter 5 Address Spaces

5.1 Introduction

The PEX 8311 supports the following PCI Express-to-Local Bus and Local Bus-to-PCI Express Address spaces:

- PCI-compatible Configuration (00h to FFh; 256 bytes)
- PCI Express Extended Configuration (100h to FFFh; Endpoint mode only)
- I/O (32-bit)
- Memory (32-bit Non-Prefetchable)
- Prefetchable Memory (64-bit)

The first two spaces are strictly for PCI Express to Internal Local Bus accesses, used for accessing the Local Configuration registers, and are described in Chapter 9, "Configuration Transactions."

The other three Address spaces determine which transactions to forward downstream or upstream. The Memory Base, Remap, and I/O ranges are defined by a set of Base, Remapped, and Limit registers in the Configuration header. The Local Bus has dedicated Address space for each direction of the transfer that is mapped using any of the three spaces from the PCI Express interface. Direct Slave accesses, PCI Express-initiated accesses going across one of the three PCI Express Spaces, are mapped to Direct Slave Space 0, Space 1, or Expansion ROM Space that is used as another Memory space on the Local Bus. Direct Master accesses, Local Bus-initiated accesses, are going across Direct Master Space and are mapped to one of the three PCI Express Spaces. The DMA accesses have their standalone bi-directional space for each Channel. Depending on the direction, transactions falling within the ranges defined by the Base and Limit registers are forwarded from one bus to another. Transactions falling outside these ranges are ignored and errors might be generated.

The PEX 8311 performs Address Translation as transactions cross the bridge.

Table 5-1 lists which interface is primary (upstream) or secondary (downstream) for the two PEX 8311 bridge modes.

Table 5-1. Primary and Secondary Interface Definitions for Endpoint and Root Complex Modes

Bridge Mode	Primary Interface (Upstream)	Secondary Interface (Downstream)
Endpoint	PCI Express	Local
Root Complex	Local	PCI Express

5.2 I/O Space

The I/O Address space determines whether to forward I/O Read or I/O Write transactions across the PEX 8311. PCI Express uses the 32-bit Short Address Format (DWORD-aligned) for I/O transactions.

5.2.1 Enable Bits

The PEX 8311 response to I/O transactions is controlled by two Configuration register bits:

- **PCI Command** register *I/O Access Enable* bit
- **PCI Command** register *Bus Master Enable* bit

The *I/O Enable* bit must be set for I/O space to be used for downstream traffic, wherein any I/O transaction to be forwarded by the PEX 8311 downstream to Local Bus remap Spaces. If this bit is not set, the I/O space is used for upstream traffic, wherein all I/O transactions initiated by Local Remap spaces are forwarded upstream by the PEX 8311, to I/O space and then to the PCI Express interface. If this bit is not set in Endpoint mode, PCI Express I/O requests are completed with Unsupported Request status. If this bit is not set in Root Complex mode, I/O transactions are ignored (no upstream traffic generation) and a Local System Error (LSERR#) is generated, when enabled.

The PEX 8311 response to re-map the I/O transactions forwarded from PCI Express I/O space to Local Bus Spaces onto the Local Bus is controlled by the following Local Configuration register bits:

- **Local PCI Command** register *I/O Access Enable* bit
- **Direct Slave Local Address Space 0** *Local Address Space 0 Enable*
- **Direct Slave Local Address Space 0 Range** *Memory Space 0 Indicator*
- **Direct Slave Local Address Space 1** *Local Address Space 0 Enable*
- **Direct Slave Local Address Space 1 Range** *Memory Space 1 Indicator*
- **Direct Slave Expansion ROM Range** *Local Address Expansion ROM Enable*

The PEX 8311 response to re-map Local Bus-initiated transactions to be forwarded from Local Bus Spaces to PCI Express I/O space is controlled by the following Local Configuration register bits:

- **Local PCI Command** register *Bus Master Enable* bit
- **CNTRL** PCI Command Codes Control for Direct Master and DMA accesses

The bridge *I/O Access Enable, Local Address Space 0 Enable, Local Address Space 1 Enable, Local Address Expansion ROM Enable, Memory Space 0 Indicator, and Memory Space 1 Indicator* bits must be set for any I/O transaction to be forwarded from PCI Express I/O space to Local Bus (Direct Slave) or from Local Bus to PCI Express I/O space (Direct Master and DMA Local-to-PCI Express). If any of these bits are not set, PCI Express I/O-initiated transactions that are mapped to disabled space are completed with Unsupported Request status.

The *Bus Master Enable and Local Register Bus Master Enable* bits must be set for any I/O transaction to be forwarded upstream.

- **Endpoint mode** – If these bits are not set, the Local Bus-initiated transactions to PCI Express (upstream) as an I/O transaction are stalled and a Local Bus error condition might occur.
- **Root Complex mode** – If these bits are not set, the Local Bus-initiated transactions to PCI Express (downstream) as an I/O transaction are stalled and a Local Bus error condition might occur.

5.2.2 I/O Base, Space Base, Range, and Limit Registers

The following I/O Base, Space Base, Range, and Limit Configuration registers are used to determine whether to forward I/O transactions across the PEX 8311:

- **I/O Base** (upper 4 bits of 8-bit register correspond to Address bits [15:12])
- **I/O Base Upper** (16-bit register corresponds to Address bits [31:16])
- **I/O Limit** (upper 4 bits of 8-bit register correspond to Address bits [15:12])
- **I/O Limit Upper** (16-bit register corresponds to Address bits [31:16])
- **PCIBAR2** PCI Base Address for Accesses to Local Address Space 0
- **Direct Slave Local Address Space 0 Range** Space 0 Range
- **Direct Slave Local Address Space 0 Local Base Address (Remap)** Space 0 Remap Address
- **PCIBAR3** PCI Base Address for Accesses to Local Address Space 1
- **Direct Slave Local Address Space 1 Range** Space 1 Range
- **Direct Slave Local Address Space 1 Local Base Address (Remap)** Space 1 Remap Address
- **PCIERBAR** PCI Base Address for Local Expansion ROM
- **Direct Slave Expansion ROM Range** Expansion ROM Range
- **Direct Slave Expansion ROM Local Base Address (Remap)** Expansion ROM Remap Address
- **Local Base Address for Direct Master-to-PCI I/O Configuration** Local Base Address for Accesses to PCI I/O Address
- **Local Range for Direct Master-to-PCI** Direct Master I/O Range
- **PCI Base Address for Direct Master-to-PCI Memory** Direct Master I/O Remap Address
- **PCI Dual Address Cycle Base Address for Direct Master Accesses** PCI DAC Base Address for Direct Master Accesses (must be set to zero)

The PEX 8311 PCI Express interface I/O Base consists of one 8-bit register and one 16-bit register. The upper four bits of the 8-bit register define bits [15:12] of the I/O Base address. The lower four bits of the 8-bit register determine the PEX 8311's I/O address capability. The 16 bits of the **I/O Base Upper** register define bits [31:16] of the I/O Base address.

The I/O limit consists of one 8-bit register and one 16-bit register. The upper four bits of the 8-bit register define bits [15:12] of the I/O limit. The lower four bits of the 8-bit register determine the PEX 8311's I/O address capability, and reflect the value of the same field in the **I/O Base** register. The 16 bits of the **I/O Limit Upper** register define bits [31:16] of the I/O Limit address.

Because Address bits [11:0] are not included in the Address space decoding, the I/O address range retains a granularity of 4 KB, and is always aligned to a 4 KB boundary. The maximum I/O range is 4 GB.

The Direct Slave spaces (Space 0 and Space 1 only), when configured for I/O transactions, consist of a 32-bit PCI Base Address register for each Space in which bit 1 is always cleared to 0 and upper bits [31:2] are used as a PCI Base Address for access to Local Address.

Each Direct Slave space provides a dedicated 32-bit Direct Slave Local Address Range register. For I/O accesses, bit 1 is always cleared to 0 and upper bits [31:2] are used to define the range of each Direct Slave space.

Each Direct Slave space provides a dedicated 32-bit Direct Slave Local Base Address Remap register that maps all incoming traffic from PCI Express (I/O space) to Local Bus. The upper bits [31:2] are used to map downstream traffic to the Local Bus.

The Local Bus, by default, is a Memory-Mapped bus. For the PEX 8311 to generate I/O-Mapped transactions by way of Direct Master or DMA, the **LCS Control** register (**CNTRL**[15:0]) must be programmed to PCI I/O Command Codes before transactions begin.

The Direct Master space (Local-to-PCI Memory space), when configured for I/O transactions, (**CNTRL**[15:8]) consists of a 32-bit Local Base Address register, in which the upper 15 bits [31:16] are used for decoding Local Bus accesses. The Direct Master Base Address value must be multiple of the 64-KB Range value.

The Direct Master space provides a 32-bit Direct Master Range register, in which the upper 15 bits [31:16] are used to define a range of the Direct Master space.

The Direct Master space provides a dedicated 32-bit PCI Base Address Remap register. The upper 15 bits [31:16] are used to remap decoded Local Bus accesses to PCI Express I/O space and then to the PCI Express interface.

The PEX 8311 does not perform Address Translation for DMA transactions. Source and destination addresses are used to map DMA transactions from the PEX 8311 Configuration registers. The **LCS Control** register (**CNTRL**[7:0]) is used to configure PEX 8311 DMA transactions, to drive PCI I/O Command codes during DMA transactions.

PCI Express-initiated I/O transactions that fall within the range defined by the Base and Limit are forwarded downstream to the downstream bus. Local Bus-initiated I/O transactions that are within the range are ignored. I/O transactions on the PEX 8311 upstream bus that do not fall within the range defined by the Base and Limit are ignored. I/O transactions on the PEX 8311 downstream bus that do not fall within the range are forwarded upstream.

For 16-bit I/O addressing, when the **I/O Base** has a value greater than the **I/O Limit**, the I/O range is disabled. For 32-bit I/O addressing, when the I/O base specified by the **I/O Base** and **I/O Base Upper** registers has a value greater than the I/O limit specified by the **I/O Limit** and **I/O Limit Upper** registers, the I/O range is disabled. In these cases, I/O transactions are forwarded upstream, and no I/O transactions are forwarded downstream.

Figure 5-1 illustrates I/O forwarding in Endpoint mode. Figure 5-2 illustrates I/O forwarding in Root Complex mode.

Figure 5-1. I/O Forwarding in Endpoint Mode

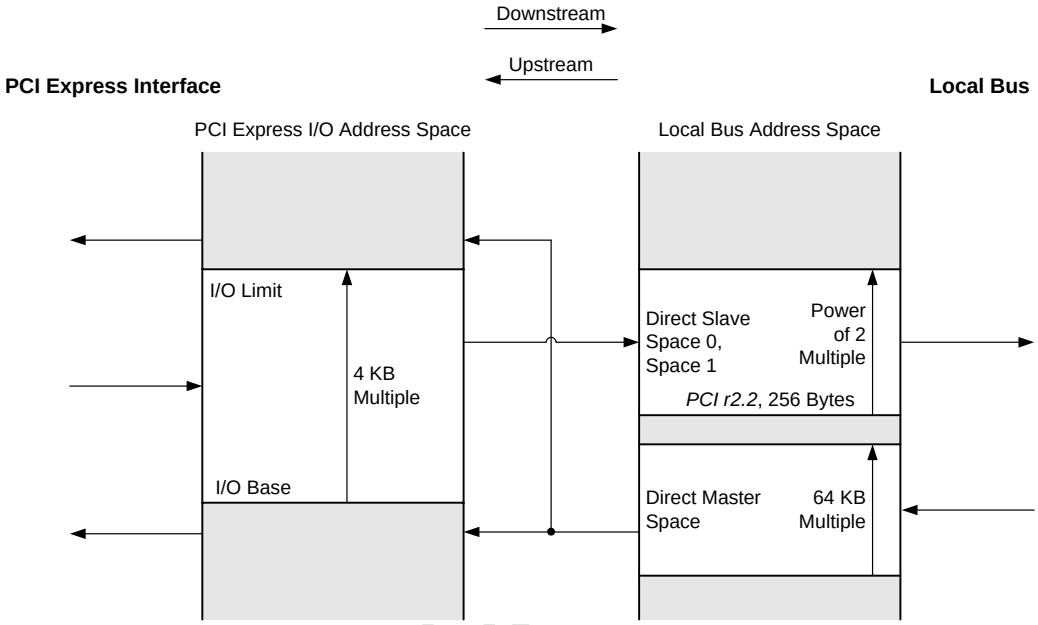
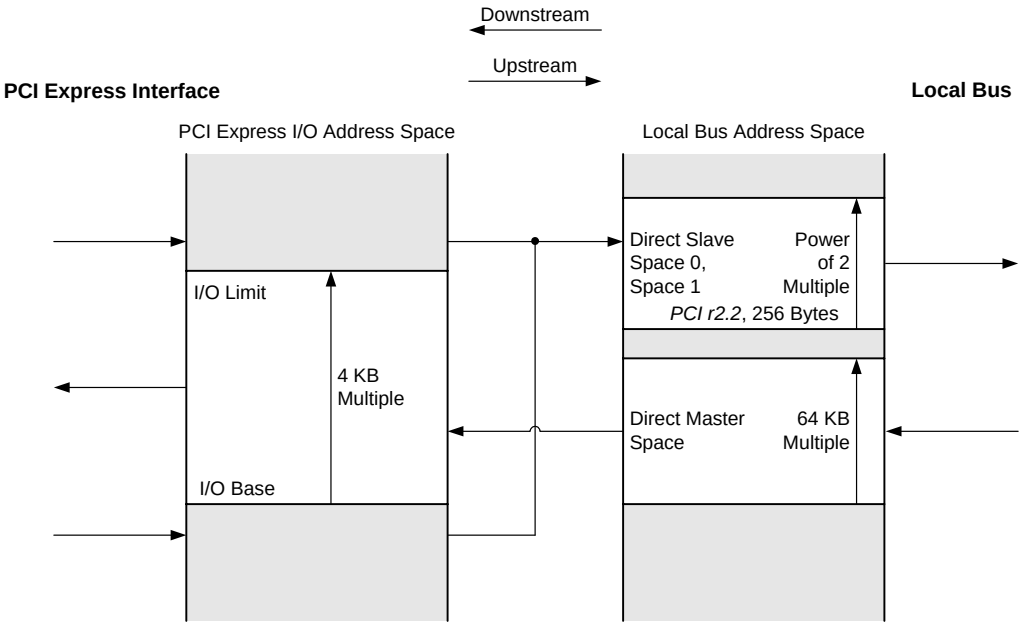


Figure 5-2. I/O Forwarding in Root Complex Mode



5.3 Memory-Mapped I/O Space

The Memory-Mapped I/O Address space determines whether to forward Non-Prefetchable Memory Read or Write transactions across the PEX 8311. For Local Bus-to-PCI Express reads, prefetching occurs in this space only when the Memory Read Line or Memory Read Multiple commands are issued by the Direct Master Space and/or DMA Controller on the internal bus as the transfer is mapped to Memory-Mapped I/O space on the PEX 8311 PCI Express. For PCI Express-to-Local Bus reads, the Memory-Mapped I/O space is mapped to one of the Direct Slave spaces and the number of bytes to read is determined by the Memory Read Request TLP. Transactions that are forwarded using this Address space are limited to a 32-bit range.

5.3.1 Enable Bits

The PEX 8311 response to Memory-Mapped I/O transactions is controlled by three Configuration register bits:

- **PCI Command** register *Memory Space Enable* bit
- **PCI Command** register *Bus Master Enable* bit
- **Bridge Control** register *VGA Enable* bit

The *Memory Space Enable* bit must be set for a memory transaction to be forwarded downstream. If this bit is not set, Memory transactions are forwarded upstream.

The PEX 8311 response to re-map the Memory-Mapped I/O transactions forwarded from PCI Express-to-Local Bus Spaces and onto the Local Bus is controlled by six Local Configuration register bits:

- **Local PCI Command** register *Memory Space Enable* bit
- **Direct Slave Local Address Space 0** *Local Address Space 0 Enable*
- **Direct Slave Local Address Space 0 Range** *Memory Space 0 Indicator*
- **Direct Slave Local Address Space 1** *Local Address Space 1 Enable*
- **Direct Slave Local Address Space 1 Range** *Memory Space 1 Indicator*
- **Direct Slave Expansion ROM Range** *Local Address Expansion ROM Enable*

The PEX 8311 response to re-map Local Bus-initiated transactions forwarded from Local Bus-to-PCI Express Memory-Mapped I/O space is controlled by the following Local Configuration register bits:

- **Local PCI Command** register *Bus Master Enable* bit
- **CNTRL** PCI Command Codes Control for Direct Master and DMA accesses
  - **Endpoint mode** – If these bits are not set, Non-Posted Memory requests to the Local Bus (downstream) are completed with an Unsupported Request status. Posted Write data is discarded.
  - **Root Complex mode** – If these bits are not set, Local Bus-initiated transactions to PCI Express Memory-Mapped I/O space (upstream) is stalled and Local Bus error conditions might occur.

The *Bus Master Enable* and Local register *Bus Master Enable* bits must be set for Memory transactions to be forwarded upstream (Endpoint mode) or downstream (Root Complex mode).

- **Endpoint mode** – If these bits are not set, Memory transactions initiated from the Local Bus-to-PCI Express (upstream) are stalled and Local Bus error conditions can occur.
- **Root Complex mode** – If these bits are not set, Non-Posted Memory requests on the PCI Express interface are completed with an Unsupported Request status. Posted Write data is discarded.

5.3.2 Memory-Mapped I/O Base, Range, and Limit Registers

The following Memory Base, Range, and Limit Configuration registers are used to determine whether to forward Memory-Mapped I/O transactions across the PEX 8311:

- **Memory Base** (bits [15:4] of 16-bit register correspond to Address bits [31:20])
- **Memory Limit** (bits [15:4] of 16-bit register correspond to Address bits [31:20])
- **PCIBAR2** PCI Base Address for Accesses to Local Address Space 0
- **Direct Slave Local Address Space 0 Range** Space 0 Range
- **Direct Slave Local Address Space 0 Local Base Address (Remap)** Space 0 Remap Address
- **PCIBAR3** PCI Base Address for Accesses to Local Address Space 1
- **Direct Slave Local Address Space 1 Range** Space 1 Range
- **Direct Slave Local Address Space 1 Local Base Address (Remap)** Space 1 Remap Address
- **PCIERBAR** PCI Base Address for Local Expansion ROM
- **Direct Slave Expansion ROM Range** Expansion ROM Range
- **Direct Slave Expansion ROM Local Base Address (Remap)** Expansion ROM Remap Address
- **Local Base Address for Direct Master-to-PCI Memory Configuration** Local Base Address for Accesses to PCI Memory Address
- **Local Range for Direct Master-to-PCI** Direct Master Memory Range
- **PCI Base Address for Direct Master-to-PCI Memory** Direct Master Memory Remap Address
- **PCI Dual Address Cycle Base Address for Direct Master Accesses** PCI DAC Base Address for Direct Master Accesses (must be cleared to 0)

Memory Base register bits [15:4] define bits [31:20] of the Memory-Mapped I/O Base address. **Memory Limit** register bits [15:4] define bits [31:20] of the Memory-Mapped I/O limit. Bits [3:0] of each register are hardwired to 0h.

Because Address bits [19:0] are not included in the Address space decoding, the Memory-Mapped I/O Address range retains a granularity of 1 MB, and is always aligned to a 1-MB boundary. The maximum Memory-Mapped I/O range is 4 GB.

The Direct Slave spaces (Space 0, Space 1, and Expansion ROM) when configured for Memory Transaction consist of 32-bit PCI Base Address register for each Space in which bits [2:1] are always cleared to 00b, bit 3 defines whether space is prefetchable, and upper bits [31:4] are used as a PCI Base Address for access to Local Address.

Each Direct Slave space provides a dedicated 32-bit Direct Slave Local Address Range register. For Memory-Mapped accesses, bits [2:1] are always cleared to 00b, bit 3 defines whether space is prefetchable, and upper bits [31:4] are used to define the range of each Direct Slave space.

Each Direct Slave space provides a dedicated 32-bit Direct Slave Local Base Address Remap register that maps all incoming traffic from PCI Express (Memory-Mapped I/O space)-to-Local Bus. Upper bits [31:4] are used to map downstream traffic to the Local Bus.

By default, the Local Bus is a Memory-Mapped bus. For the PEX 8311 to generate Memory-Mapped transactions by way of Direct Master or DMA, the **LCS Control** register (**CNTRL**[15:0]) must be programmed to PCI Memory Command Codes before transactions begin.

The Direct Master space (Local-to-PCI Memory space), when configured to Memory transactions (**CNTRL**[15:8]), consists of a 32-bit Local Base Address register, in which the upper 15 bits [31:16] are used for decoding Local Bus accesses. The Direct Master Base Address value must be multiple of the 64 KB Range value.

The Direct Master space provides a 32-bit Direct Master Range register, in which the upper 15 bits [31:16] are used to define a range of the Direct Master space.

The Direct Master space provides a dedicated 32-bit PCI Base Address Remap register. The upper 15 bits [31:16] are used to remap decoded Local Bus accesses to PCI Express Memory-Mapped I/O space and then to the PCI Express interface.

The PEX 8311 does not perform Address Translation for DMA Transactions. Source and destination addresses are used to map DMA transactions from the PEX 8311 Configuration registers. The **LCS Control** register (**CNTRL**[7:0]) is used to configure PEX 8311 DMA transactions, to drive PCI Memory Command codes during DMA transactions.

Memory transactions that fall within the range defined by the Base and Limit are forwarded downstream (PCI Express-to-Local Bus in Endpoint mode, Local Bus-to-PCI Express in Root Complex mode), and Memory transactions forwarded upstream that are within the range are ignored. Downstream Memory transactions that do not fall within the range defined by the Base and Limit are ignored on the upstream bus, and are forwarded upstream from the downstream bus.

Memory transactions that fall within the range defined by the Base and Limit are forwarded downstream from the primary interface to the secondary interface, and Memory transactions on the secondary interface that are within the range are ignored. Memory transactions that do not fall within the range defined by the Base and Limit are ignored on the primary interface and are forwarded upstream from the secondary interface (provided they are not in the Address range defined by the set of Prefetchable Memory Address registers or are not forwarded downstream by the VGA mechanism).

If the Memory Base is programmed to maintain a value greater than the Memory Limit, the Memory-Mapped I/O range is disabled. In this case, Memory transaction forwarding is determined by the Prefetchable Base and Limit registers.

Figure 5-3 illustrates Memory-Mapped I/O forwarding in Endpoint mode. Figure 5-4 illustrates Memory-Mapped I/O forwarding in Root Complex mode.

Figure 5-3. Memory-Mapped I/O Forwarding in Endpoint Mode

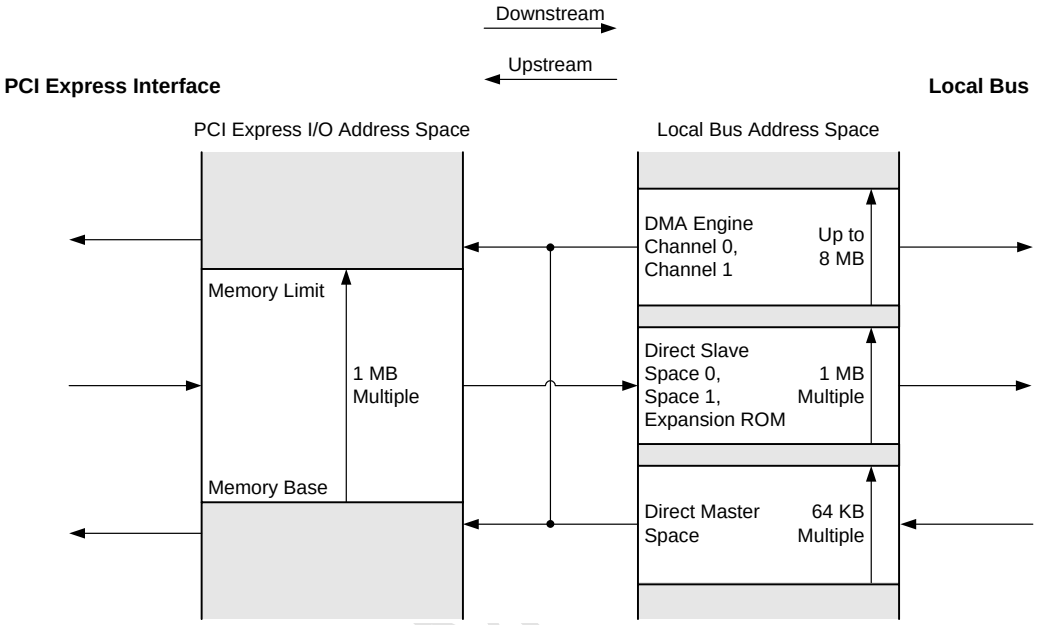
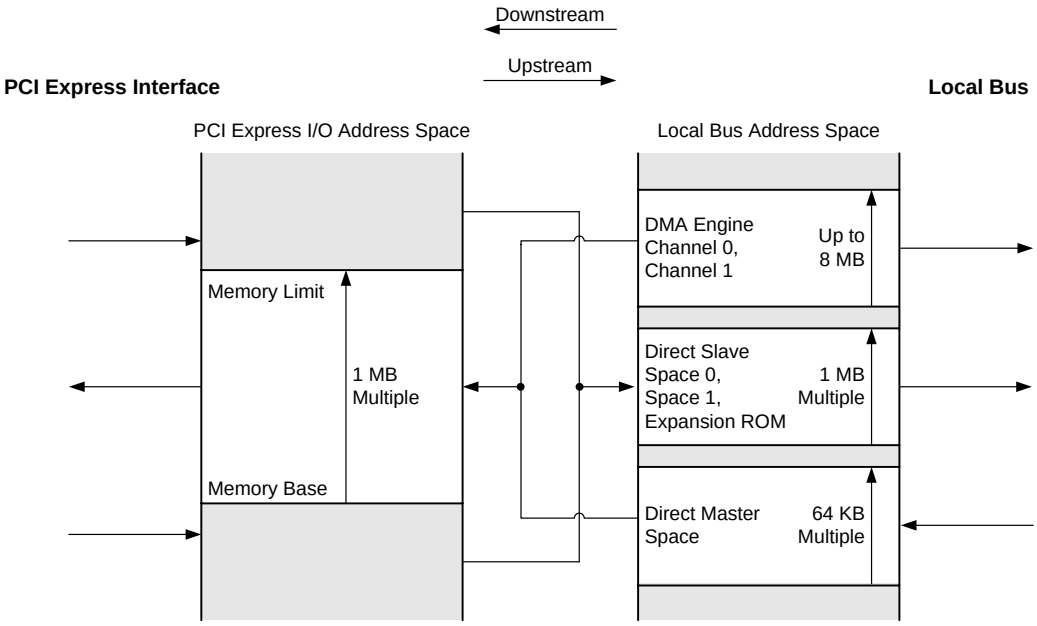


Figure 5-4. Memory-Mapped I/O Forwarding in Root Complex Mode



5.4 Prefetchable Space

The Prefetchable Address space determines whether to forward Prefetchable Memory Read or Write transactions across the PEX 8311.

- For Local-to-PCI Express reads, prefetching occurs for Direct Master and DMA PCI Express-to-Local transactions in this space for Memory Read commands (Memory Read, Memory Read Line, and Memory Read Multiple) configured in the **LCS Control** register (**CNTRL**[11:8, 3:0]).
- For Memory Read commands, the **PECS Device Specific Control** register *Blind Prefetch Enable* bit **(DEVSPECCTL**[0]) must be set for prefetching to occur.
- For PCI Express-to-Local reads, the number of bytes to read is determined by the Memory Read request; therefore, internal prefetching between Prefetchable Space on the PCI Express and Direct Slave Spaces on the Local Bus does not occur. The prefetch occurs on the Local Bus when the respective Direct Slave space and/or DMA Channel *Local-to-PCI Express Prefetch Enable* bit is set to enable.

5.4.1 Enable Bits

The prefetchable space responds to the enable bits as described in Section 5.3.1.

5.4.2 Prefetchable Base and Limit Registers

The following Prefetchable Memory Base and Limit Configuration registers are used to determine whether to forward Prefetchable Memory transactions across the bridge:

- **Prefetchable Memory Base** (bits [15:4] of 16-bit register correspond to Address bits [31:20])
- **Prefetchable Memory Base Upper** (32-bit register corresponds to Address bits [63:32])
- **Prefetchable Memory Limit** (bits [15:4] of 16-bit register correspond to Address bits [31:20])
- **Prefetchable Memory Limit Upper** (32-bit register corresponds to Address bits [63:32])
- **PCIBAR2** PCI Base Address for Accesses to Local Address Space 0
- **Direct Slave Local Address Space 0 Range** Space 0 Range
- **Direct Slave Local Address Space 0 Local Base Address (Remap)** Space 0 Remap Address
- **PCIBAR3** PCI Base Address for Accesses to Local Address Space 1
- **Direct Slave Local Address Space 1 Range** Space 1 Range
- **Direct Slave Local Address Space 1 Local Base Address (Remap)** Space 1 Remap Address
- **PCIERBAR** PCI Base Address for Local Expansion ROM
- **Direct Slave Expansion ROM Range** Expansion ROM Range
- **Direct Slave Expansion ROM Local Base Address (Remap)** Expansion ROM Remap Address
- **Local Base Address for Direct Master-to-PCI Memory Configuration** Local Base Address for Accesses to PCI Memory Address
- **Local Range for Direct Master-to-PCI** Direct Master Memory Range
- **PCI Base Address for Direct Master-to-PCI Memory** Direct Master Memory Remap Address
- **PCI Dual Address Cycle Base Address for Direct Master Accesses** PCI DAC Base Address for Direct Master Accesses (cleared to 0 for SAC and non-zero for DAC accesses)

Bits [15:4] of the **Prefetchable Memory Base** register define bits [31:20] of the Prefetchable Memory Base address. Bits [15:4] of the **Prefetchable Memory Limit** register define bits [31:20] of the prefetchable memory limit. Bits [3:0] of each register are hardwired to 0h. For 64-bit addressing, the **Prefetchable Memory Base Upper** and **Prefetchable Memory Limit Upper** registers are also used to define the space.

Because Address bits [19:0] are not included in the Address space decoding, the Prefetchable Memory Address range retains a granularity of 1 MB, and is always aligned to a 1-MB boundary. The maximum Prefetchable Memory range is 4 GB with 32-bit addressing, and 2^{61} with 64-bit addressing.

The Direct Slave spaces (Space 0, Space 1, and Expansion ROM), when configured for Memory transactions, consist of a 32-bit PCI Base Address register for each space, in which bits [2:1] are always cleared to 00b, bit 3 defines whether space is prefetchable, and upper bits [31:4] are used as a PCI Base Address for access to Local Address.

Each Direct Slave space provides a dedicated 32-bit Direct Slave Local Address Range register. For Memory-Mapped accesses, bits [2:1] are always cleared to 00b, bit 3 defines whether space is prefetchable, and upper bits [31:4] are used to define the range of each Direct Slave space.

Each Direct Slave space provides a dedicated 32-bit Direct Slave Local Base Address Remap register that maps all incoming traffic from PCI Express (Prefetchable Memory-Mapped space)-to-Local Bus. The upper bits [31:4] are used to map downstream traffic to the Local Bus.

By default, the Local Bus is a Memory-Mapped bus. For the PEX 8311 to generate Memory-Mapped transactions by way of Direct Master or DMA, the **LCS Control** register (**CNTRL**[15:0]) must be programmed to PCI Memory Command codes before transactions begin.

The Direct Master space (Local-to-PCI Memory space), when configured to Memory transactions (**CNTRL**[15:8]), consists of a 32-bit Local Base Address register, in which the upper 15 bits [31:16] are used for decoding Local Bus accesses. The Direct Master Base Address value must be multiple of the 64-KB Range value.

The Direct Master space provides a 32-bit Direct Master Range register, in which the upper 15 bits [31:16] are used to define a range of the Direct Master space.

The Direct Master space provides a dedicated 32-bit PCI Base Address Remap register. The upper 15 bits [31:16] are used to remap decoded Local Bus accesses to PCI Express Prefetchable Memory-Mapped space and then to the PCI Express interface.

The PEX 8311 does not perform Address Translation for DMA Transactions. Source and destination addresses are used to map DMA transactions from the PEX 8311 Configuration registers. The **LCS Control** register (**CNTRL**[7:0]) is used to configure PEX 8311 DMA transactions, to drive PCI Memory Command codes during DMA transactions.

Memory transactions that fall within the range defined by the Base, Range, and Limit are forwarded downstream from the upstream to downstream bus. Memory transactions on the downstream bus that are within the range are ignored.

Memory transactions that do not fall within the range defined by the Base, Range, and Limit are ignored on the upstream bus, and are forwarded upstream from the downstream-to-upstream bus (provided they are not within the address range defined by the set of Memory-Mapped I/O Address registers or are not forwarded downstream by another mechanism).

If the **Prefetchable Memory Base** is programmed to maintain a value greater than the **Prefetchable Memory Limit**, the Prefetchable Memory range is disabled. In this case, Memory transaction forwarding is determined by the Memory-Mapped I/O Base and Limit registers.

The four Prefetchable Base and Limit registers of the PCI Express Prefetchable space must be considered when disabling the Prefetchable range.

Figure 5-5 illustrates Memory-Mapped I/O and Prefetchable Memory forwarding in Endpoint mode. Figure 5-6 illustrates Memory-Mapped I/O and Prefetchable Memory forwarding in Endpoint mode.

Figure 5-5. Memory-Mapped I/O and Prefetchable Memory Forwarding in Endpoint Mode

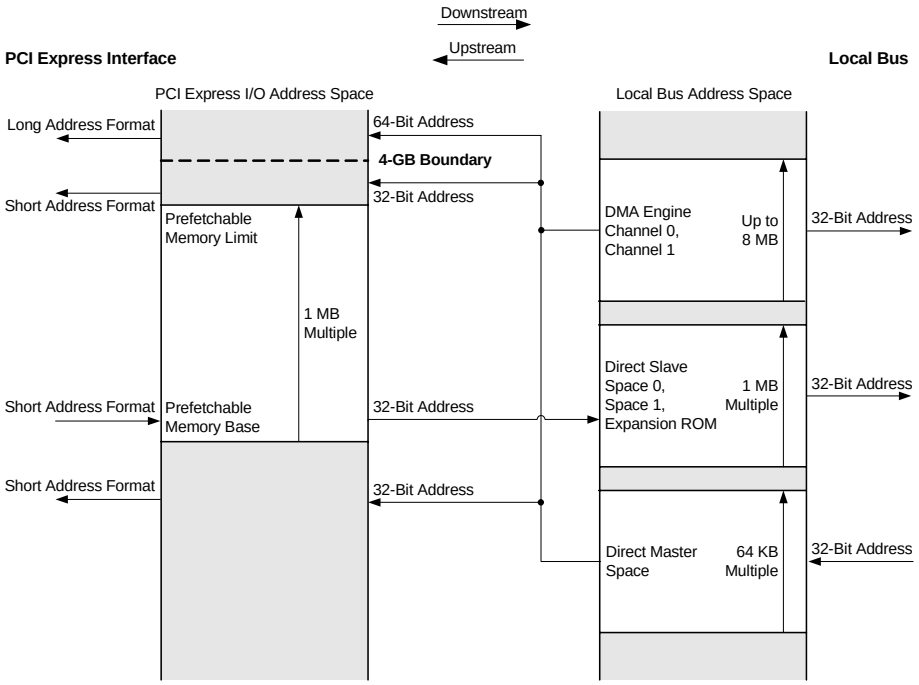
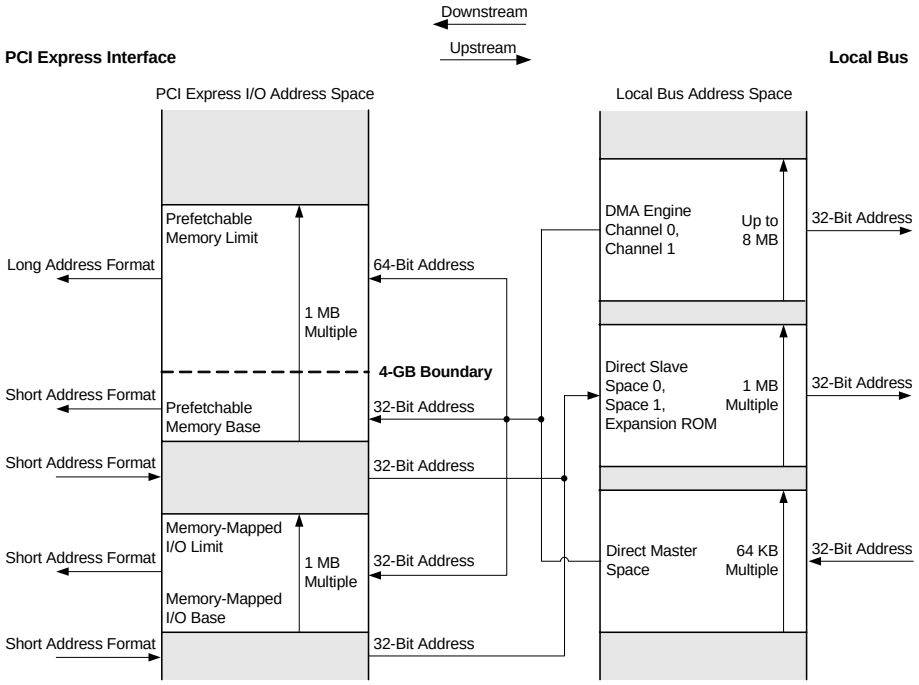


Figure 5-6. Memory-Mapped I/O and Prefetchable Memory Forwarding in Root Complex Mode



5.4.3 64-Bit Addressing

The PEX 8311 supports generation of 64-bit Long Address format for Direct Master and DMA transactions, as illustrated in Figure 5-5 and Figure 5-6. This allows the PEX 8311 and Local Processors to access devices in PCI Express space that reside above the 4-GB Address Boundary space.

64-addressing is ***not supported*** for Direct Slave accesses to Local Bus space. For this reason, the PEX 8311 must always be mapped to Memory or I/O addresses below the 4-GB Address Boundary space. Additional limitations for Endpoint and Root Complex modes are described in Section 5.4.3.1 and Section 5.4.3.2.

5.4.3.1 Endpoint Mode Configuration

The PEX 8311 supports generation of PCI Express TLP with Long Address format to upstream devices. The **Prefetchable Memory Base Upper** and **Prefetchable Memory Limit Upper** registers must be cleared to 0h, and the Direct Master Dual Address Cycle and DMA*x* Dual Address Cycle registers must be set to non-zero value. A zero (0h) value in Direct Master Dual Address Cycle and/or DMA*x* Dual Address Cycle registers prevents the PEX 8311 from responding to Local Bus transactions by internally generating Dual Address Cycle to Prefetchable Memory. Internal accesses are Single Address Cycle. The internal Dual Address Cycle accesses, TLP with Long Address format, is used to address devices located above the 4-GB Address Boundary space.

When the PEX 8311 detects a downstream access, PCI Express Memory transaction with an address above the 4-GB Address Boundary space, the transaction is completed with Unsupported Request status. The PEX 8311 generates an upstream traffic, TLP with Long Address format, in response to Local Bus accesses to address devices located above the 4-GB Address Boundary space only when Direct Master and/or DMA accesses internally fall within the range of Prefetchable memory.

Upstream traffic from the Local Bus, Direct Master, and/or DMA that internally falls outside both the Prefetchable Memory space and Memory-Mapped I/O space must be Single Address Cycle, DMDAC and/or DMADAC*x* cleared to 0h for PEX 8311 to address devices located below the 4-GB Address Boundary space, TLP with Short Address format.

5.4.3.2 Root Complex Mode Configuration

If both the Prefetchable **Memory Base Upper** and **Prefetchable Memory Limit Upper** registers are cleared to 0h, the PEX 8311 generation of addresses above the 4-GB Address Boundary space, TLP with Long Address format, are ***not supported***.

Local Bus-initiated transactions by way of Direct Master and DMA Dual Address Cycle accesses are internally ignored by the Prefetchable Memory space. Local Bus System errors (LSERR#) are generated, when enabled.

If the PEX 8311 PCI Express Prefetchable Memory space is located entirely above the 4-GB Address Boundary space, both the **Prefetchable Memory Base Upper** and **Prefetchable Memory Limit Upper** registers are set to non-zero values. The PEX 8311 ignores Single Address Cycle Memory transactions internally generated by Direct Master or DMA, and forwards PCI Express Memory transactions with addresses below the 4-GB Address Boundary space upstream to the Local Bus Spaces (Direct Slave) (unless they fall within the Memory-Mapped I/O range).

Local Bus accesses by way of Direct Master and/or DMA Dual Address Cycle transaction that internally fall within the range defined by the **Prefetchable Base**, **Prefetchable Memory Base Upper**, **Prefetchable Memory Limit**, and **Prefetchable Memory Limit Upper** registers are forwarded downstream to the PCI Express interface.

Dual Address Cycle transactions that internally do not fall within the range defined by these registers are ignored.

If the PEX 8311 detects an upstream access, PCI Express memory transaction above the 4-GB Address Boundary space that falls within the range defined by these registers, it is completed with Unsupported Request status.

If the PEX 8311 PCI Express Prefetchable Memory space spans the 4-GB Address Boundary space, the **Prefetchable Memory Base Upper** register is cleared to 0h, and the **Prefetchable Memory Limit Upper** register is set to a non-zero value.

If the Local Bus accesses, Direct Master and/or DMA Single Address Cycle that internally are greater than or equal to the prefetchable memory base address, the transaction is forwarded downstream to the PCI Express interface.

If an upstream, PCI Express Memory transaction is detected with an address below the 4-GB Address Boundary space, and is less than the Prefetchable Memory Base address, the transaction is forwarded upstream to the Local Bus Spaces (Direct Slave). If the Local Bus accesses, Direct Master and/or DMA Dual Address Cycle internally mapped to be less than or equal to the **Prefetchable Memory Limit** register, the transaction is forwarded downstream to the PCI Express interface.

When the PEX 8311 detects an upstream access, the PCI Express memory transaction above the 4-GB Address Boundary space is less than or equal to the **Prefetchable Memory Limit** register, it is completed with Unsupported Request status.

Local Bus-initiated transactions by way of Direct Master and DMA Dual Address Cycle accesses that are greater than the **Prefetchable Memory Limit** register are internally ignored by the Prefetchable Memory space. Local Bus System errors (LSERR#) are generated, when enabled.

Chapter 6 C and J Modes Bus Operation

6.1 Local Bus Cycles

The PEX 8311 interfaces the PCI Express interface to two Local Bus types, as listed in Table 6-1. It operates in one of two modes – C and J, selected through the MODE0 ball – corresponding to the two bus types. Connect the MODE1 ball to ground for standard operation.

Table 6-1. MODE0 Ball-to-Bus Mode Cross-Reference

MODE0	Bus Mode	Bus Type
0	C	Intel/Generic, 32-bit non-multiplexed
1	J	Intel/Generic, 32-bit multiplexed

6.2 Local Bus Arbitration and BREQi

The PEX 8311 asserts LHOLD to request the Local Bus for a Direct Slave or DMA transfer. The PEX 8311 owns and becomes the Local Bus Master when LHOLD and LHOLDA are both asserted. As the Local Bus Master, the PEX 8311 responds to BREQi assertion to relinquish Local Bus ownership during Direct Slave or DMA transfers when either of the following conditions are true:

- BREQi is asserted and enabled (MARBR[18]=1)
- Gating is enabled and the Local Bus Latency Timer is enabled and expires (**MARBR**[27, 16, 7:0])

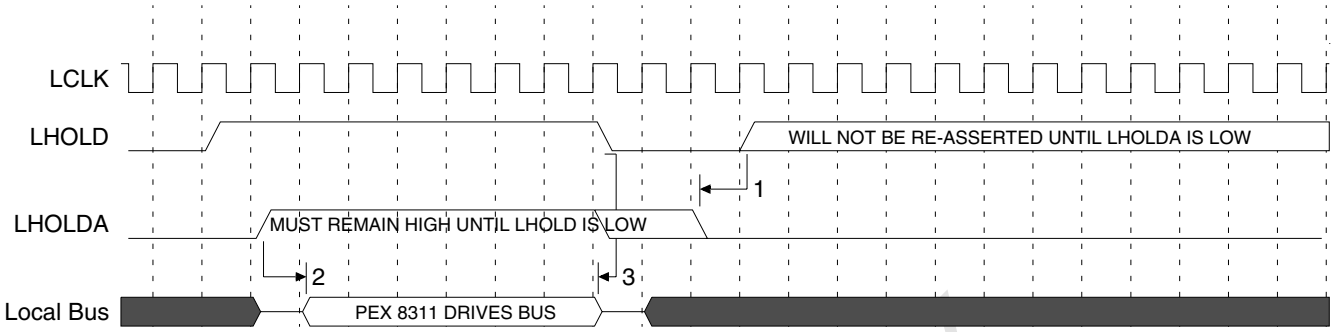
Before releasing the Local Bus, the PEX 8311 attempts to transfer up to a total of three additional Dwords of data. This includes the last transfer with BLAST# asserted. The actual number of additional transfers depends upon the Local Bus data width and address when BREQi is asserted. The minimum assertion duration of the BREQi signal is one Local Bus Clock cycle. Typically, Local Bus logic asserts BREQi and holds it asserted until either BLAST# is asserted (BLAST#=0) or LHOLD is de-asserted (LHOLD=0).

When the PEX 8311 releases the Local Bus, the external Local Bus Arbiter can grant the Local Bus to another Master. If the PEX 8311 needs to complete the disconnected transfer, it requests the Local Bus by re-asserting LHOLD upon detection of LHOLDA de-assertion and the Local Bus Pause Timer being zero (0), when enabled.

Note: *The Local Bus Pause Timer applies only to DMA operation. It does not apply to Direct Slave operations.*

6.2.1 Local Bus Arbitration Timing Diagram

Figure 6-1. Local Bus Arbitration (LHOLD and LHOLDA) Timing Diagram



Notes: *In response to the PEX 8311 assertion of LHOLD, the external Local Bus Arbiter asserts LHOLDA to grant the Local Bus to the PEX 8311. In Figure 6-1, the Local Bus Arbiter asserts LHOLDA immediately upon detection of LHOLD assertion; however, the Local Bus Arbiter has the option, when necessary, to assert LHOLDA significantly later.*

Figure 6-1 was created using the Timing Designer tool. It is accurate and adheres to its specified protocol(s). This diagram illustrates transfers and signal transitions, but should not be relied upon to exactly indicate, on a clock-for-clock basis, wherein PEX 8311-driven signal transitions will occur.

6.3 Big Endian/Little Endian

6.3.1 PCI Express Data Bits Mapping onto Local Bus

PCI Express is a serial interface; therefore, for clarity, the description is provided from the perspective of data being de-packetized and assembled into a Dword of payload data. Table 6-2 through Table 6-5 clarify PEX 8311 signal mapping between the data from the PCI Express interface and Local Bus during Big/Little Endian conversion.

Notes:

*1) In each Local Bus ball entry, **n-m** denotes that that row's PCI ball maps to Local Bus ball **m** during Local Bus cycle **n** that results from the PCI Express cycle (PCI Express-to-Local Bus transfers) or in the PCI Express cycle (Local-to-PCI Express transfers). Examples follow.*

C Mode:

In Table 6-2 (refer to shaded entry), a Local Bus ball of "2-LD5" for PCI ball AD21 during 16-bit Little Endian Local Bus transfers denotes that during a PCI Express-to-Local Bus transfer, the value of PCI Express Dword format data ball AD21 during each PCI Express transfer occurs on Local Bus ball LD5 of the second resulting 16-bit Local Bus transfer. During a Local-to-PCI Express transfer, it denotes that the value of PCI Express Dword format data ball AD21 results from the value of Local Bus ball LD5 during the second 16-bit Local Bus transfer.

In Table 6-3 (refer to shaded entry), a Local Bus ball of "2-LD21" for PCI Express Dword format data ball AD21 during 16-bit Little Endian Local Bus transfers denotes that during a PCI Express-to-Local Bus transfer, the value of PCI Express Dword format data ball AD21 during each PCI Express transfer occurs on Local Bus ball LD21 of the second resulting 16-bit Local Bus transfer. During a Local-to-PCI Express transfer, it denotes that the value of PCI Express Dword format data ball AD21 results from the value of Local Bus ball LD21 during the second 16-bit Local Bus transfer.

J Mode:

In Table 6-4 (refer to shaded entry), a Local Bus ball of "2-LAD5" for PCI ball AD21 during 16-bit Little Endian Local Bus transfers denotes that during a PCI Express-to-Local Bus transfer, the value of PCI Express Dword format data ball AD21 during each PCI Express transfer occurs on Local Bus ball LAD5 of the second resulting 16-bit Local Bus transfer. During a Local-to-PCI Express transfer, it denotes that the value of PCI Express Dword format data ball AD21 results from the value of Local Bus ball LAD5 during the second 16-bit Local Bus transfer.

In Table 6-5 (refer to shaded entry), a Local Bus ball of "2-LAD21" for PCI Express Dword format data ball AD21 during 16-bit Little Endian Local Bus transfers denotes that during a PCI Express-to-Local Bus transfer, the value of PCI Express Dword format data ball AD21 during each PCI Express transfer occurs on Local Bus ball LAD21 of the second resulting 16-bit Local Bus transfer. During a Local-to-PCI Express transfer, it denotes that the value of PCI Express Dword format data ball AD21 results from the value of Local Bus ball LAD21 during the second 16-bit Local Bus transfer.

2) Mappings occur only during Data phases. Addresses always map directly, as indicated in the 32-bit Little Endian column after the Address Translation specified in the Configuration registers is performed.

*3) Big/Little Endian modes are selected by register bits and ball signals, depending on the Data phase type (Direct Master read/write, Direct Slave read/write, DMA PCI Express-to-Local Bus/ Local-to-PCI Express, and Configuration register read/write). (For further details, refer to the **BIGEND** register, and the BIGEND# ball description in Table 2-8, "Local Bus Interface C Mode Signals (96 Balls)," and Table 2-9,"Local Bus Interface J Mode Signals (96 Balls)."*

Table 6-2. PCI Express Dword Format Bus Data Bits Mapping onto Local Bus C Mode – Low Byte Lane

PCI Express Dword Format Bus	C Mode Local Bus Ball Byte Lane Mode = 0 (BIGEND[4]=0)					
	Little Endian			Big Endian		
	32-Bit	16-Bit	8-Bit	32-Bit	16-Bit	8-Bit
AD0	1-LD0	1-LD0	1-LD0	1-LD24	1-LD8	1-LD0
AD1	1-LD1	1-LD1	1-LD1	1-LD25	1-LD9	1-LD1
AD2	1-LD2	1-LD2	1-LD2	1-LD26	1-LD10	1-LD2
AD3	1-LD3	1-LD3	1-LD3	1-LD27	1-LD11	1-LD3
AD4	1-LD4	1-LD4	1-LD4	1-LD28	1-LD12	1-LD4
AD5	1-LD5	1-LD5	1-LD5	1-LD29	1-LD13	1-LD5
AD6	1-LD6	1-LD6	1-LD6	1-LD30	1-LD14	1-LD6
AD7	1-LD7	1-LD7	1-LD7	1-LD31	1-LD15	1-LD7
AD8	1-LD8	1-LD8	2-LD0	1-LD16	1-LD0	2-LD0
AD9	1-LD9	1-LD9	2-LD1	1-LD17	1-LD1	2-LD1
AD10	1-LD10	1-LD10	2-LD2	1-LD18	1-LD2	2-LD2
AD11	1-LD11	1-LD11	2-LD3	1-LD19	1-LD3	2-LD3
AD12	1-LD12	1-LD12	2-LD4	1-LD20	1-LD4	2-LD4
AD13	1-LD13	1-LD13	2-LD5	1-LD21	1-LD5	2-LD5
AD14	1-LD14	1-LD14	2-LD6	1-LD22	1-LD6	2-LD6
AD15	1-LD15	1-LD15	2-LD7	1-LD23	1-LD7	2-LD7
AD16	1-LD16	2-LD0	3-LD0	1-LD8	2-LD8	3-LD0
AD17	1-LD17	2-LD1	3-LD1	1-LD9	2-LD9	3-LD1
AD18	1-LD18	2-LD2	3-LD2	1-LD10	2-LD10	3-LD2
AD19	1-LD19	2-LD3	3-LD3	1-LD11	2-LD11	3-LD3
AD20	1-LD20	2-LD4	3-LD4	1-LD12	2-LD12	3-LD4
AD21	1-LD21	2-LD5	3-LD5	1-LD13	2-LD13	3-LD5
AD22	1-LD22	2-LD6	3-LD6	1-LD14	2-LD14	3-LD6
AD23	1-LD23	2-LD7	3-LD7	1-LD15	2-LD15	3-LD7
AD24	1-LD24	2-LD8	4-LD0	1-LD0	2-LD0	4-LD0
AD25	1-LD25	2-LD9	4-LD1	1-LD1	2-LD1	4-LD1
AD26	1-LD26	2-LD10	4-LD2	1-LD2	2-LD2	4-LD2
AD27	1-LD27	2-LD11	4-LD3	1-LD3	2-LD3	4-LD3
AD28	1-LD28	2-LD12	4-LD4	1-LD4	2-LD4	4-LD4
AD29	1-LD29	2-LD13	4-LD5	1-LD5	2-LD5	4-LD5
AD30	1-LD30	2-LD14	4-LD6	1-LD6	2-LD6	4-LD6
AD31	1-LD31	2-LD15	4-LD7	1-LD7	2-LD7	4-LD7

Table 6-3. PCI Express Dword Format Bus Data Bits Mapping onto Local Bus C Mode – High Byte Lane

PCI Express Dword Format Bus	C Mode Local Bus Ball Byte Lane Mode = 1 (BIGEND[4]=1)					
	Little Endian			Big Endian		
	32-Bit	16-Bit	8-Bit	32-Bit	16-Bit	8-Bit
AD0	1-LD0	1-LD16	1-LD24	1-LD24	1-LD24	1-LD24
AD1	1-LD1	1-LD17	1-LD25	1-LD25	1-LD25	1-LD25
AD2	1-LD2	1-LD18	1-LD26	1-LD26	1-LD26	1-LD26
AD3	1-LD3	1-LD19	1-LD27	1-LD27	1-LD27	1-LD27
AD4	1-LD4	1-LD20	1-LD28	1-LD28	1-LD28	1-LD28
AD5	1-LD5	1-LD21	1-LD29	1-LD29	1-LD29	1-LD29
AD6	1-LD6	1-LD22	1-LD30	1-LD30	1-LD30	1-LD30
AD7	1-LD7	1-LD23	1-LD31	1-LD31	1-LD31	1-LD31
AD8	1-LD8	1-LD24	2-LD24	1-LD16	1-LD16	2-LD24
AD9	1-LD9	1-LD25	2-LD25	1-LD17	1-LD17	2-LD25
AD10	1-LD10	1-LD26	2-LD26	1-LD18	1-LD18	2-LD26
AD11	1-LD11	1-LD27	2-LD27	1-LD19	1-LD19	2-LD27
AD12	1-LD12	1-LD28	2-LD28	1-LD20	1-LD20	2-LD28
AD13	1-LD13	1-LD29	2-LD29	1-LD21	1-LD21	2-LD29
AD14	1-LD14	1-LD30	2-LD30	1-LD22	1-LD22	2-LD30
AD15	1-LD15	1-LD31	2-LD31	1-LD23	1-LD23	2-LD31
AD16	1-LD16	2-LD16	3-LD24	1-LD8	2-LD24	3-LD24
AD17	1-LD17	2-LD17	3-LD25	1-LD9	2-LD25	3-LD25
AD18	1-LD18	2-LD18	3-LD26	1-LD10	2-LD26	3-LD26
AD19	1-LD19	2-LD19	3-LD27	1-LD11	2-LD27	3-LD27
AD20	1-LD20	2-LD20	3-LD28	1-LD12	2-LD28	3-LD28
AD21	1-LD21	2-LD21	3-LD29	1-LD13	2-LD29	3-LD29
AD22	1-LD22	2-LD22	3-LD30	1-LD14	2-LD30	3-LD30
AD23	1-LD23	2-LD23	3-LD31	1-LD15	2-LD31	3-LD31
AD24	1-LD24	2-LD24	4-LD24	1-LD0	2-LD16	4-LD24
AD25	1-LD25	2-LD25	4-LD25	1-LD1	2-LD17	4-LD25
AD26	1-LD26	2-LD26	4-LD26	1-LD2	2-LD18	4-LD26
AD27	1-LD27	2-LD27	4-LD27	1-LD3	2-LD19	4-LD27
AD28	1-LD28	2-LD28	4-LD28	1-LD4	2-LD20	4-LD28
AD29	1-LD29	2-LD29	4-LD29	1-LD5	2-LD21	4-LD29
AD30	1-LD30	2-LD30	4-LD30	1-LD6	2-LD22	4-LD30
AD31	1-LD31	2-LD31	4-LD31	1-LD7	2-LD23	4-LD31

Table 6-4. PCI Express word Format Bus Data Bits Mapping onto Local Bus J Mode – Low Byte Lane

PCI Express Dword Format Bus	J Mode Local Bus Ball Byte Lane Mode = 0 (BIGEND[4]=0)					
	Little Endian			Big Endian		
	32-Bit	16-Bit	8-Bit	32-Bit	16-Bit	8-Bit
AD0	1-LAD0	1-LAD0	1-LAD0	1-LAD24	1-LAD8	1-LAD0
AD1	1-LAD1	1-LAD1	1-LAD1	1-LAD25	1-LAD9	1-LAD1
AD2	1-LAD2	1-LAD2	1-LAD2	1-LAD26	1-LAD10	1-LAD2
AD3	1-LAD3	1-LAD3	1-LAD3	1-LAD27	1-LAD11	1-LAD3
AD4	1-LAD4	1-LAD4	1-LAD4	1-LAD28	1-LAD12	1-LAD4
AD5	1-LAD5	1-LAD5	1-LAD5	1-LAD29	1-LAD13	1-LAD5
AD6	1-LAD6	1-LAD6	1-LAD6	1-LAD30	1-LAD14	1-LAD6
AD7	1-LAD7	1-LAD7	1-LAD7	1-LAD31	1-LAD15	1-LAD7
AD8	1-LAD8	1-LAD8	2-LAD0	1-LAD16	1-LAD0	2-LAD0
AD9	1-LAD9	1-LAD9	2-LAD1	1-LAD17	1-LAD1	2-LAD1
AD10	1-LAD10	1-LAD10	2-LAD2	1-LAD18	1-LAD2	2-LAD2
AD11	1-LAD11	1-LAD11	2-LAD3	1-LAD19	1-LAD3	2-LAD3
AD12	1-LAD12	1-LAD12	2-LAD4	1-LAD20	1-LAD4	2-LAD4
AD13	1-LAD13	1-LAD13	2-LAD5	1-LAD21	1-LAD5	2-LAD5
AD14	1-LAD14	1-LAD14	2-LAD6	1-LAD22	1-LAD6	2-LAD6
AD15	1-LAD15	1-LAD15	2-LAD7	1-LAD23	1-LAD7	2-LAD7
AD16	1-LAD16	2-LAD0	3-LAD0	1-LAD8	2-LAD8	3-LAD0
AD17	1-LAD17	2-LAD1	3-LAD1	1-LAD9	2-LAD9	3-LAD1
AD18	1-LAD18	2-LAD2	3-LAD2	1-LAD10	2-LAD10	3-LAD2
AD19	1-LAD19	2-LAD3	3-LAD3	1-LAD11	2-LAD11	3-LAD3
AD20	1-LAD20	2-LAD4	3-LAD4	1-LAD12	2-LAD12	3-LAD4
AD21	1-LAD21	2-LAD5	3-LAD5	1-LAD13	2-LAD13	3-LAD5
AD22	1-LAD22	2-LAD6	3-LAD6	1-LAD14	2-LAD14	3-LAD6
AD23	1-LAD23	2-LAD7	3-LAD7	1-LAD15	2-LAD15	3-LAD7
AD24	1-LAD24	2-LAD8	4-LAD0	1-LAD0	2-LAD0	4-LAD0
AD25	1-LAD25	2-LAD9	4-LAD1	1-LAD1	2-LAD1	4-LAD1
AD26	1-LAD26	2-LAD10	4-LAD2	1-LAD2	2-LAD2	4-LAD2
AD27	1-LAD27	2-LAD11	4-LAD3	1-LAD3	2-LAD3	4-LAD3
AD28	1-LAD28	2-LAD12	4-LAD4	1-LAD4	2-LAD4	4-LAD4
AD29	1-LAD29	2-LAD13	4-LAD5	1-LAD5	2-LAD5	4-LAD5
AD30	1-LAD30	2-LAD14	4-LAD6	1-LAD6	2-LAD6	4-LAD6
AD31	1-LAD31	2-LAD15	4-LAD7	1-LAD7	2-LAD7	4-LAD7

Table 6-5. PCI Express word Format Bus Data Bits Mapping onto Local Bus J Mode – High Byte Lane

PCI Express Dword Format Bus	J Mode Local Bus Ball Byte Lane Mode = 1 (BIGEND[4]=1)					
	Little Endian			Big Endian		
	32-Bit	16-Bit	8-Bit	32-Bit	16-Bit	8-Bit
AD0	1-LAD0	1-LAD16	1-LAD24	1-LAD24	1-LAD24	1-LAD24
AD1	1-LAD1	1-LAD17	1-LAD25	1-LAD25	1-LAD25	1-LAD25
AD2	1-LAD2	1-LAD18	1-LAD26	1-LAD26	1-LAD26	1-LAD26
AD3	1-LAD3	1-LAD19	1-LAD27	1-LAD27	1-LAD27	1-LAD27
AD4	1-LAD4	1-LAD20	1-LAD28	1-LAD28	1-LAD28	1-LAD28
AD5	1-LAD5	1-LAD21	1-LAD29	1-LAD29	1-LAD29	1-LAD29
AD6	1-LAD6	1-LAD22	1-LAD30	1-LAD30	1-LAD30	1-LAD30
AD7	1-LAD7	1-LAD23	1-LAD31	1-LAD31	1-LAD31	1-LAD31
AD8	1-LAD8	1-LAD24	2-LAD24	1-LAD16	1-LAD16	2-LAD24
AD9	1-LAD9	1-LAD25	2-LAD25	1-LAD17	1-LAD17	2-LAD25
AD10	1-LAD10	1-LAD26	2-LAD26	1-LAD18	1-LAD18	2-LAD26
AD11	1-LAD11	1-LAD27	2-LAD27	1-LAD19	1-LAD19	2-LAD27
AD12	1-LAD12	1-LAD28	2-LAD28	1-LAD20	1-LAD20	2-LAD28
AD13	1-LAD13	1-LAD29	2-LAD29	1-LAD21	1-LAD21	2-LAD29
AD14	1-LAD14	1-LAD30	2-LAD30	1-LAD22	1-LAD22	2-LAD30
AD15	1-LAD15	1-LAD31	2-LAD31	1-LAD23	1-LAD23	2-LAD31
AD16	1-LAD16	2-LAD16	3-LAD24	1-LAD8	2-LAD24	3-LAD24
AD17	1-LAD17	2-LAD17	3-LAD25	1-LAD9	2-LAD25	3-LAD25
AD18	1-LAD18	2-LAD18	3-LAD26	1-LAD10	2-LAD26	3-LAD26
AD19	1-LAD19	2-LAD19	3-LAD27	1-LAD11	2-LAD27	3-LAD27
AD20	1-LAD20	2-LAD20	3-LAD28	1-LAD12	2-LAD28	3-LAD28
AD21	1-LAD21	2-LAD21	3-LAD29	1-LAD13	2-LAD29	3-LAD29
AD22	1-LAD22	2-LAD22	3-LAD30	1-LAD14	2-LAD30	3-LAD30
AD23	1-LAD23	2-LAD23	3-LAD31	1-LAD15	2-LAD31	3-LAD31
AD24	1-LAD24	2-LAD24	4-LAD24	1-LAD0	2-LAD16	4-LAD24
AD25	1-LAD25	2-LAD25	4-LAD25	1-LAD1	2-LAD17	4-LAD25
AD26	1-LAD26	2-LAD26	4-LAD26	1-LAD2	2-LAD18	4-LAD26
AD27	1-LAD27	2-LAD27	4-LAD27	1-LAD3	2-LAD19	4-LAD27
AD28	1-LAD28	2-LAD28	4-LAD28	1-LAD4	2-LAD20	4-LAD28
AD29	1-LAD29	2-LAD29	4-LAD29	1-LAD5	2-LAD21	4-LAD29
AD30	1-LAD30	2-LAD30	4-LAD30	1-LAD6	2-LAD22	4-LAD30
AD31	1-LAD31	2-LAD31	4-LAD31	1-LAD7	2-LAD23	4-LAD31

6.3.2 Local Bus Big/Little Endian Mode Accesses

For each of the following transfer types, the PEX 8311 Local Bus is independently programmed, by way of the BIGEND register, to operate in Little or Big Endian mode:

- Local Bus accesses to the PEX 8311 Configuration registers
- Direct Slave PCI accesses to Local Address Space 0, Space 1, and Expansion ROM
- DMA Channel *x* accesses to the Local Bus
- Direct Master accesses to the internal PCI Bus

For Local Bus accesses to the internal Configuration registers and Direct Master accesses, use BIGEND# to dynamically change the Endian mode.

Note: *The PCI Express interface is serial and always Little Endian. For Little Endian to Big Endian conversion, only byte lanes are swapped, not individual bits.*

Chapter 7 C and J Modes Functional Description

7.1 Introduction

The functional operation described in this section is modified or programmed through the PEX 8311 programmable internal registers.

7.2 Recovery States (J Mode Only)

In J mode, the PEX 8311 inserts one recovery state on the Local Bus between the last Data transfer and the next Address cycle.

Note: *The PEX 8311 does **not** support the i960J function that uses READY# input to add recovery states. No additional recovery states are added when READY# input remains asserted during the last Data cycle.*

7.3 Wait State Control

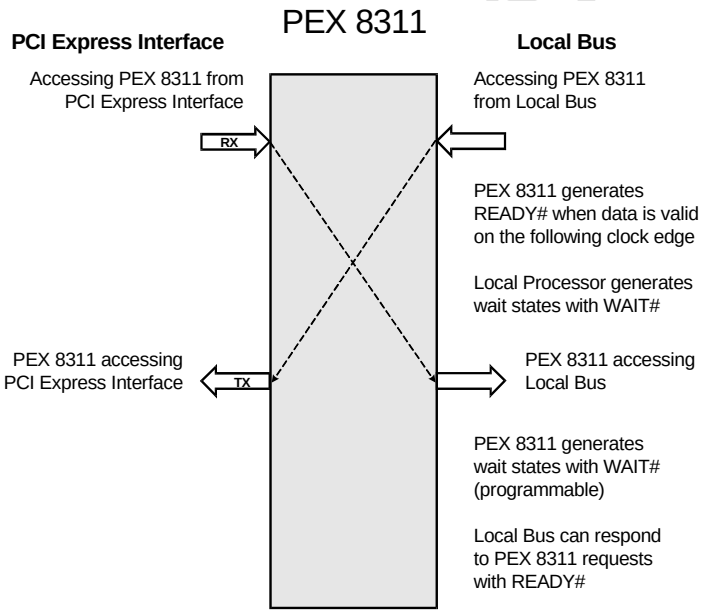
If the PEX 8311 Local Bus READY# mode is disabled (**LBRD0**[6]=0 for Space 0, **LBRD1**[6]=0 for Space 1, **LBRD0**[22]=0 for Expansion ROM, and/or **DMAMODE*x***[6]=0 for Channel *x*, where *x* is the DMA Channel number), the external READY# input signal does not affect wait states for a Local access. Wait states between Data cycles are asserted internally by Wait State Counter(s) (**LBRD0**[5:2] for Space 0, **LBRD1**[5:2] for Space 1, **LBRD0**[21:18] for Expansion ROM, and/or **DMAMODE*x***[5:2] for Channel *x*). The Wait State Counter(s) is initialized with its Configuration register value at the start of each data access.

If READY# mode is enabled (**LBRD0**[6]=1 for Space 0, **LBRD1**[6]=1 for Space 1, **LBRD0**[22]=1 for Expansion ROM, and/or **DMAMODE*x***[6]=1 for Channel *x*), it has no effect until the Wait State Counter(s) reaches 0. READY# then controls the number of additional wait states.

BTERM# input is not sampled until the Wait State Counter(s) reaches 0. BTERM# assertion overrides READY# when BTERM# is enabled (**LBRD0**[7]=1 for Space 0, **LBRD1**[7]=1 for Space 1, **LBRD0**[23]=1 for Expansion ROM, and/or **DMAMODE*x***[7]=1 for Channel *x*) and asserted.

Figure 7-1 illustrates the PEX 8311 wait states for C and J modes.

Figure 7-1. Wait States



Note: *Figure 7-1 represents a sequence of Bus cycles.*

7.3.1 Local Bus Wait States

In Direct Master mode when accessing the PEX 8311 registers, the PEX 8311 acts as a Local Bus slave. The PEX 8311 asserts wait states by delaying the READY# signal. The Local Bus Master inserts wait states with the WAIT# signal. For writes to PEX 8311 registers, assert WAIT# until data is valid.

In Direct Slave and DMA modes, the PEX 8311 acts as a Local Bus master. The PEX 8311 inserts Local Bus Slave wait states with the WAIT# signal. The Local Bus Target asserts external wait states by delaying the READY# signal. The Internal Wait State Counter(s) is programmed to insert wait states between the address and first data states, with the same number of wait states between subsequent data within bursts. (Refer to Table 7-1.)

For Direct Master writes, to insert wait states between the Address phase and the first data, the WAIT# signal must be asserted during the Address phase [ADS# (C mode) or ALE# (J mode) assertion]. Thereafter, WAIT# is toggled, as necessary, to insert wait states.

During Direct Master accesses, when the WAIT# signal is asserted during the Address phase (ADS# assertion) or after the ADS# assertion for a Direct Master read, the PEX 8311 latches the address but does not begin an internal request on the PCI Express interface, no TLP Read request is generated until WAIT# is de-asserted. This results in the PEX 8311 not having the data available on the Local Bus. In this case, WAIT# de-assertion by the Local Bus Master enables the PEX 8311 to become the Direct Master Read access on the Local Bus. WAIT# assertion by the Local Bus Master on the second Local Bus Clock cycle after the Address phase (ADS# de-assertion) allows the Direct Master Read access to generate a TLP Read request on the PCI Express interface.

Note: *Do not use READY# as a gating signal for WAIT# de-assertion. Otherwise, the PEX 8311 does not complete the transfer.*

Table 7-1. Internal Wait State Counters

Bits	Description
LBRD0[5:2]	Local Address Space 0 Internal Wait State Counter (address-to-data; data-to-data; 0 to 15 wait states)
LBRD1[5:2]	Local Address Space 1 Internal Wait State Counter (address-to-data; data-to-data; 0 to 15 wait states)
LBRD0[21:18]	Expansion ROM Internal Wait State Counter (address-to-data; data-to-data; 0 to 15 wait states)
DMAMODE0[5:2]	DMA Channel 0 Internal Wait State Counter (address-to-data; data-to-data; 0 to 15 wait states)
DMAMODE1[5:2]	DMA Channel 1 Internal Wait State Counter (address-to-data; data-to-data; 0 to 15 wait states)

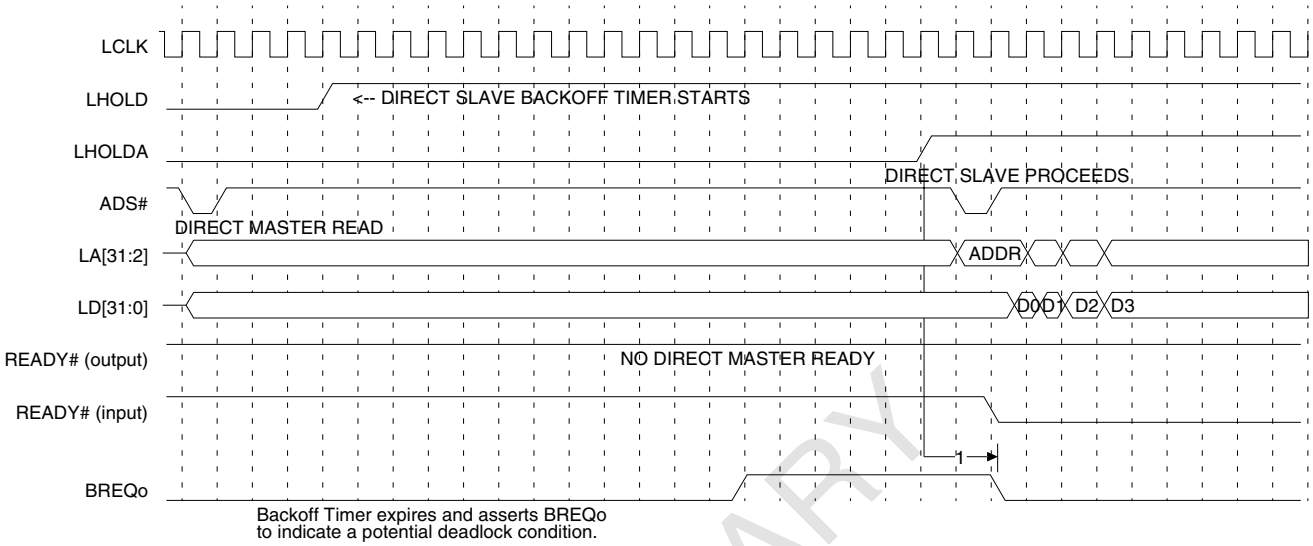
7.4 C and J Modes Functional Timing Diagrams

General notes about timing designer (graphical) waveforms:
The graphical Timing Diagrams were created using the Timing Designer tool. They are accurate and adhere to their specified protocol(s). These diagrams show transfers and signal transitions, but should not be relied upon to show exactly, on a clock-for-clock basis, in which PEX 8311-driven signal transitions will occur.

General notes about captured waveforms:
The captured Timing Diagrams were captured from a simulation signal display tool that displays the results of stimulus run on the netlist. Using the netlist illustrates realistic delay on signals driven by the PEX 8311. Signals driven by the test environment to the PEX 8311 are quite fast. Leading zeros for buses such as AD[31:0], LD[31:0] (C mode), or LAD[31:0] (J mode), may or may not be shown. When no value for a bus is shown while the PEX 8311 is executing a transfer, it is because the entire value cannot be displayed in the available space or is irrelevant. When the PEX 8311 is not executing a transfer on that bus, the value is not shown because it is either irrelevant or unknown (any or all signals are 1, 0, or Z).

For the J mode waveforms, the Local Address Bus pins (LA[28:2]) are optional and may or may not be shown.

Timing Diagram 7-1. BREQo and Deadlock

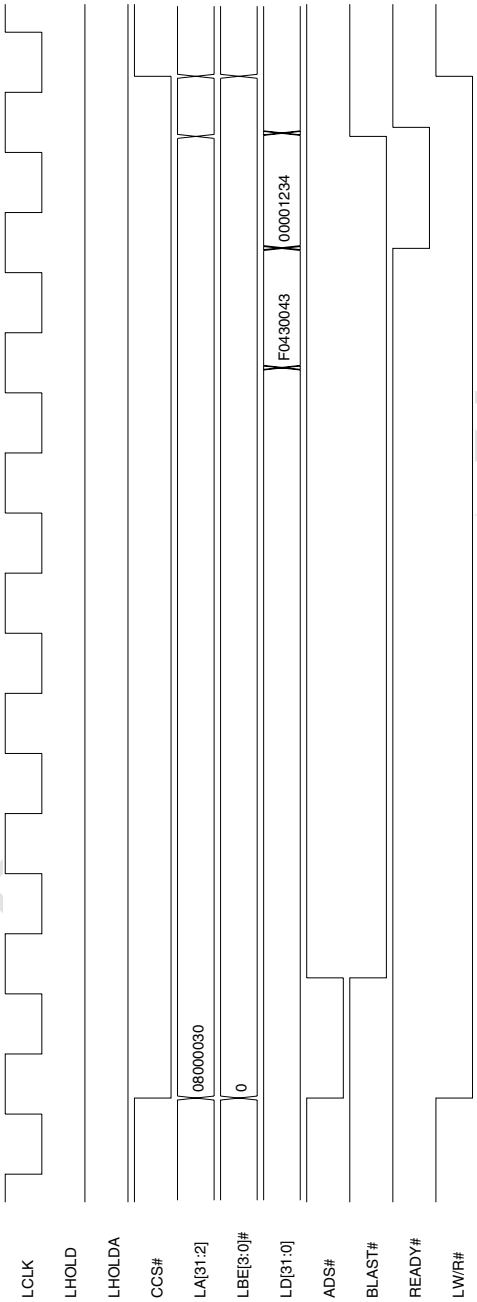


Notes: *For partial deadlock, Direct Slave Retry Delay Clocks bits (LBRD0[31:28]) is used to issue Retrys to the Direct Master attempting the Direct Slave access.*

Timing Diagram 7-1 contains C mode signals/names. The overall behavior in J mode is the same. Arrow 1 indicates that LHOLDA assertion causes the PEX 8311 to de-assert BREQo. The READY# (output and input) signals are the same pin. The PEX 8311 READY# pin is an input while processing Direct Slave reads and an output when processing Direct Master reads.

7.4.1 Configuration Timing Diagrams

Timing Diagram 7-2. Local Read of Configuration Register (C Mode)



Notes: *Local Configuration read of MBOX0 (LOC:C0h) register.*

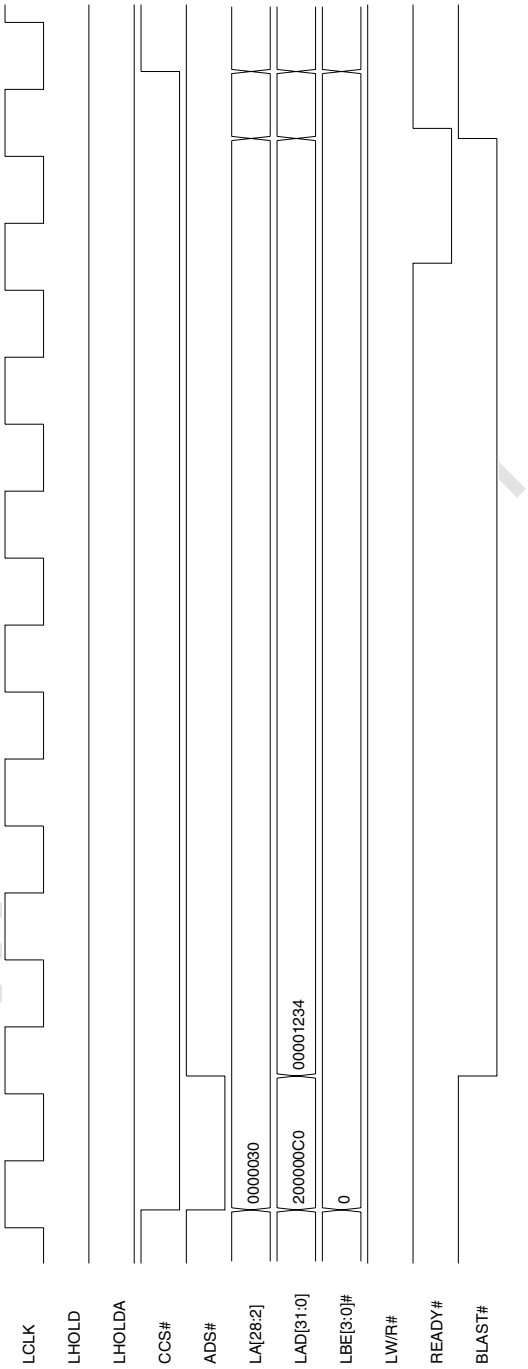
CCS# is asserted for multiple Clock cycles, but it is required asserted only during the ADS# Clock cycle.

Only the LA[8:2] signals are used to decode the register.

LA[31:2] is the Dword address (Master accesses to the PEX 8311 are always 32-bit data quantities).

The PEX 8311 starts driving the LD[31:0] bus with meaningless data (F0430043), one cycle before it asserts the READY# signal with the data read from the register.

Timing Diagram 7-3. Local Write to Configuration Register (J Mode)



Notes: *Local Configuration write to MBOX0 (LOC:C0h) register.*

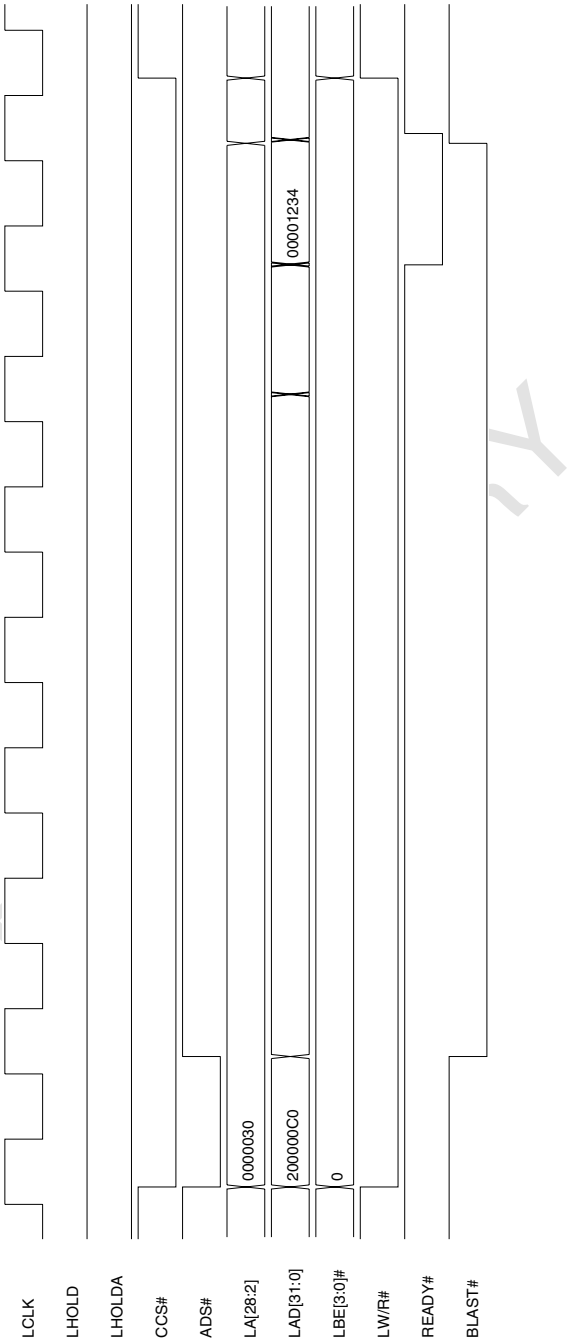
CCS# is asserted for multiple Clock cycles, but it is only required asserted during the ADS# Clock cycle (or while ALE is asserted, which is not shown).

Only the LAD[8:2] signals are used to decode the MBOX0 register.

LA[28:2] is shown, but is not used by the PEX 8311 during Local Master accesses to the PEX 8311.

Local Master accesses to the PEX 8311 are always 32-bit data quantities.

Timing Diagram 7-4. Local Read of Configuration Register (J Mode)



Notes: *Local Configuration read to MBOX0 (LOC:C0h) register.*

CCS# is asserted for multiple Clock cycles, but it is only required asserted during the ADS# Clock cycle (or while ALE is asserted, which is not shown).

Only the LAD[8:2] signals are used to decode the MBOX0 register.

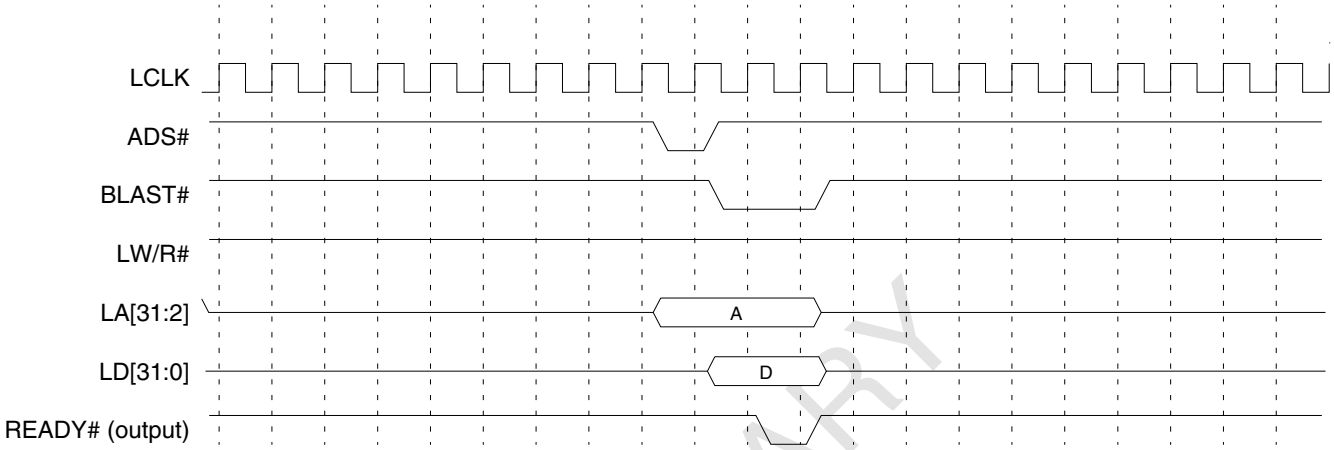
LA[28:2] is shown, but is not used by the PEX 8311 when a Local Master accesses the PEX 8311.

Local Master accesses to the PEX 8311 are always 32-bit data quantities.

7.4.2 C Mode Functional Timing Diagrams

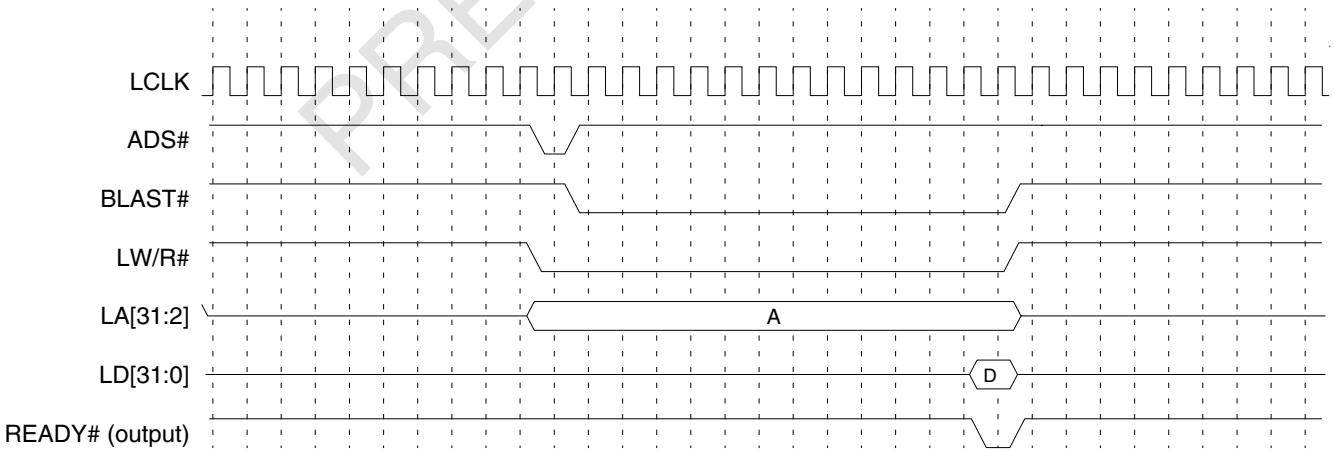
7.4.2.1 C Mode Direct Master Timing Diagrams

Timing Diagram 7-5. Direct Master Configuration Write – Type 0 or Type 1



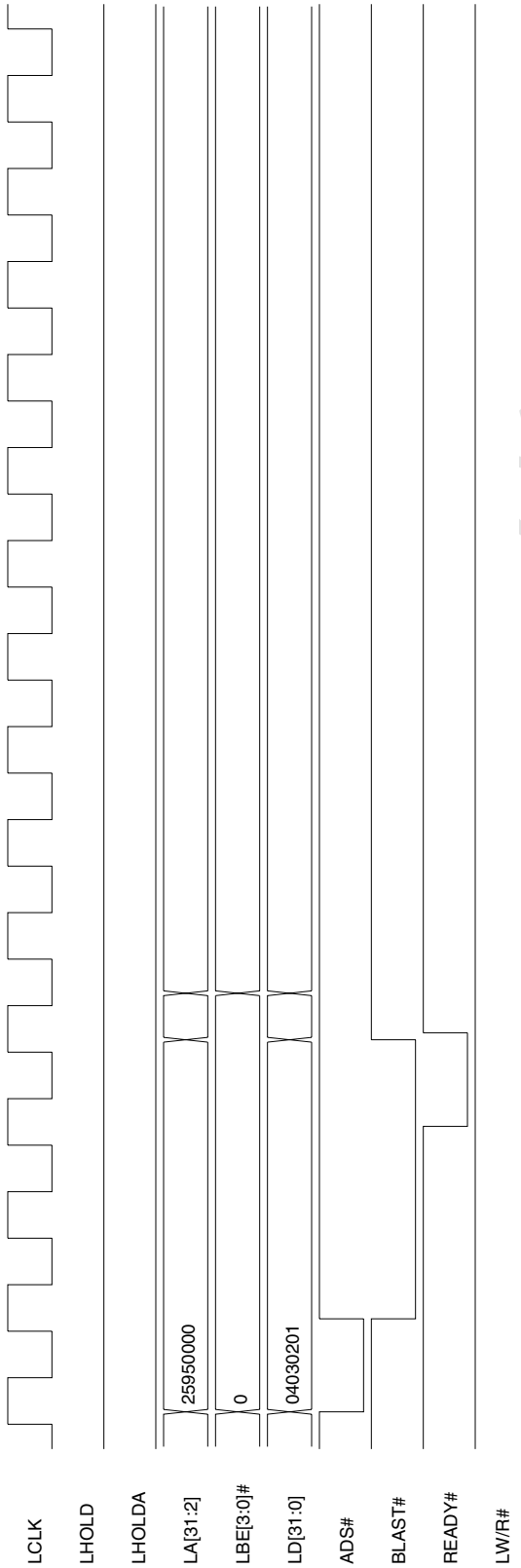
Note: *Timing Diagram 7-5 illustrates a Direct Master Configuration write that causes the PEX 8311 to generate a 32-bit PCI Type 0 or Type 1 Configuration Write cycle. Refer to Section 9.4.2.1, "Direct Master Configuration (PCI Type 0 or Type 1 Configuration Cycles)," for further details.*

Timing Diagram 7-6. Direct Master Configuration Read – Type 0 or Type 1



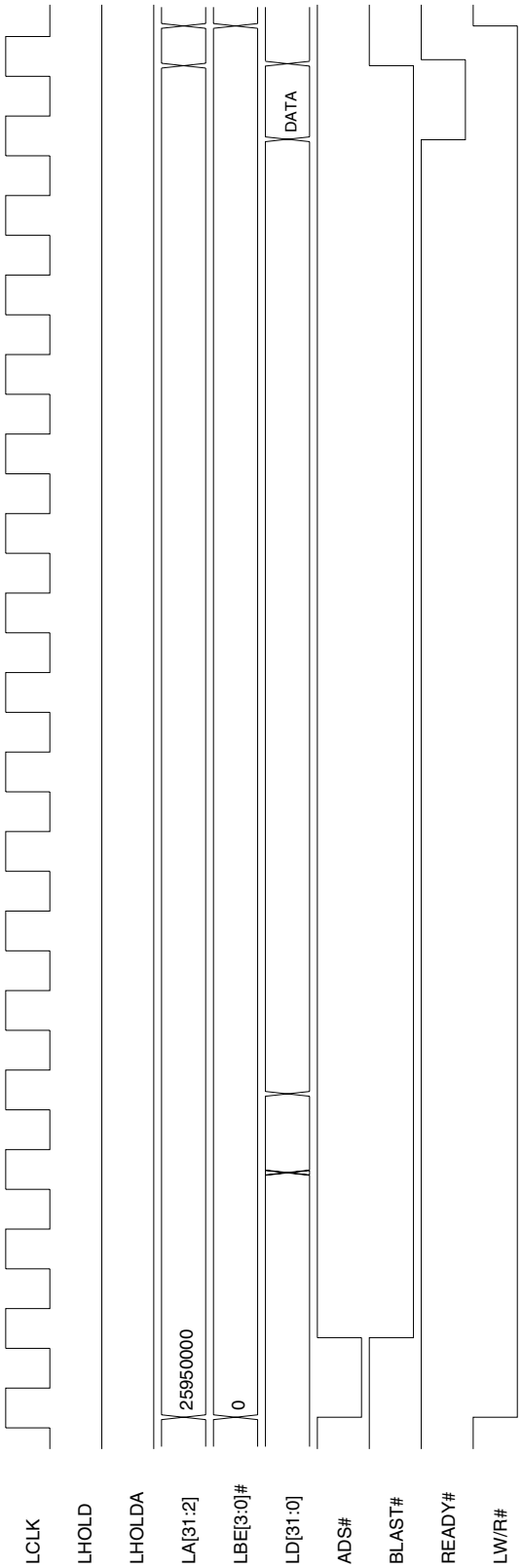
Note: *Timing Diagram 7-6 illustrates a Direct Master Configuration read that causes the PEX 8311 to generate a 32-bit PCI Type 0 or Type 1 Configuration Read cycle. Refer to Section 9.4.2.1, "Direct Master Configuration (PCI Type 0 or Type 1 Configuration Cycles)," for further details.*

Timing Diagram 7-7. Direct Master Single Cycle Write



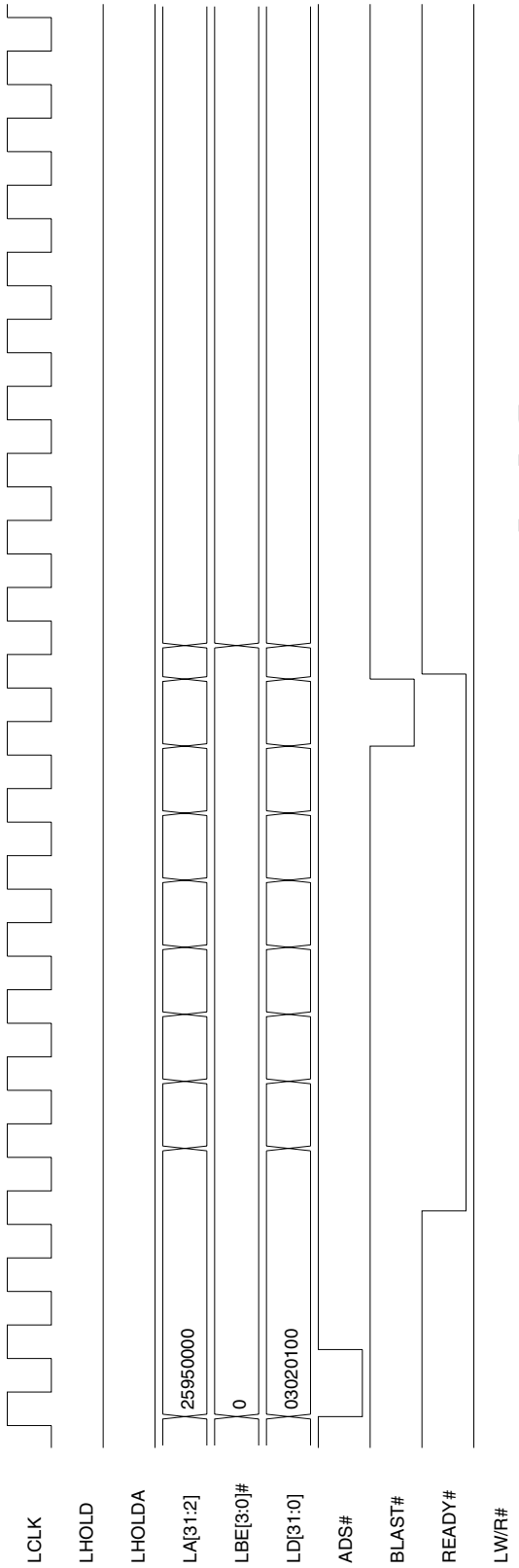
Note: *Key register value is DMPBAM[15:0]=00E3h.*

Timing Diagram 7-8. Direct Master Single Cycle Read



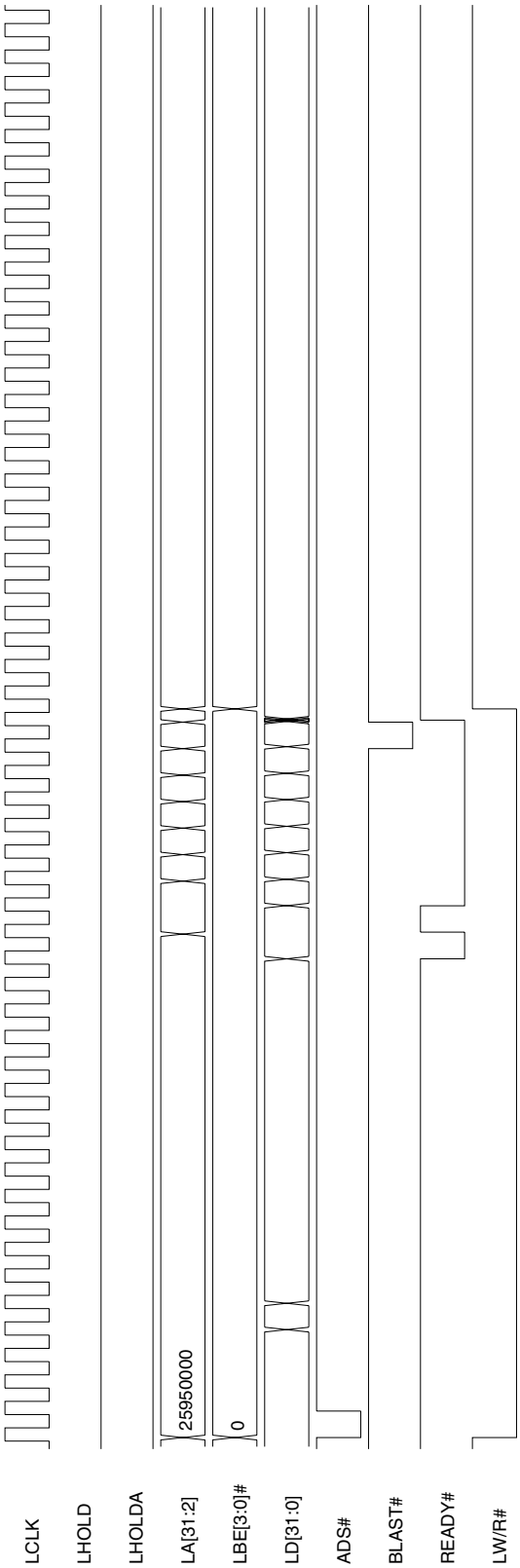
Note: *Key register value is DMPBAM[15:0]=00E3h.*

Timing Diagram 7-9. Direct Master Burst Write of 8 Dwords



Note: *Key register value is DMPBAM[15:0]=0007h.*

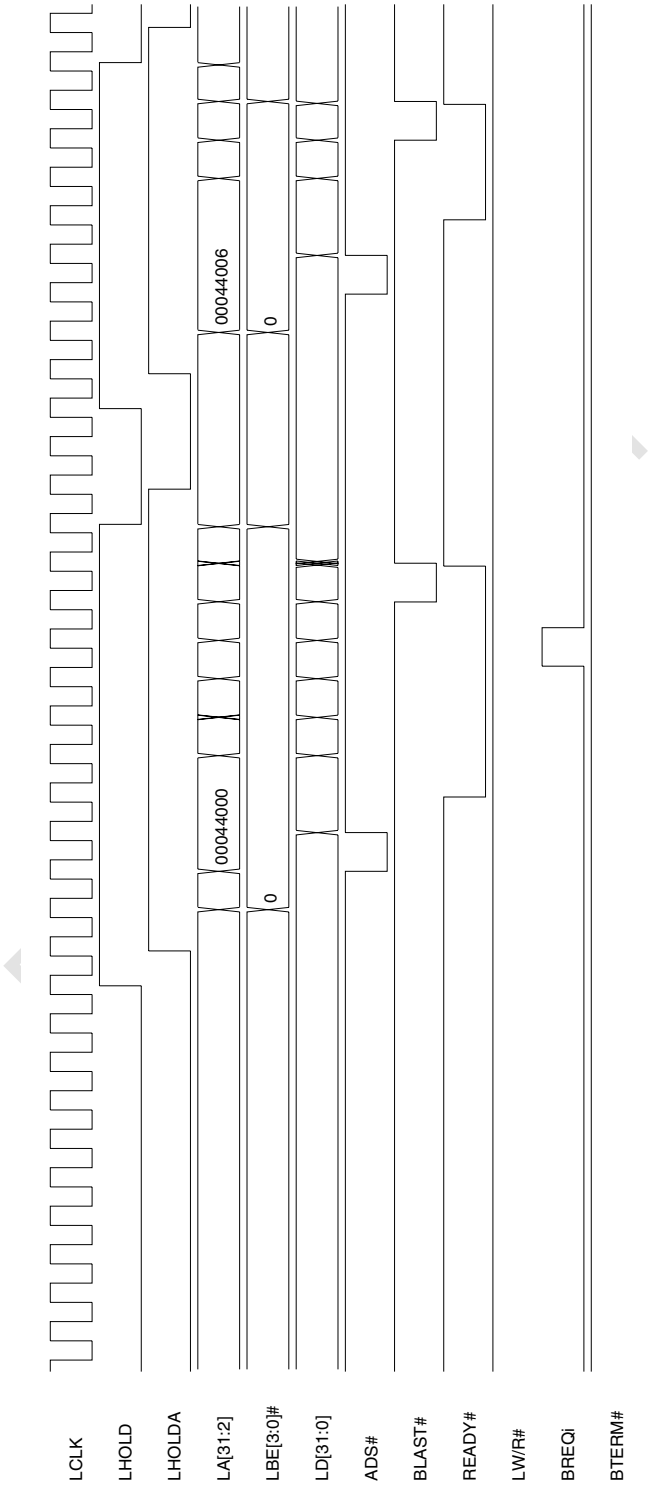
Timing Diagram 7-10. Direct Master Burst Read of 8 Dwords



Note: *Key register value is DMPBAM[15:0]=0007h.*

7.4.2.2 C Mode Direct Slave Timing Diagrams

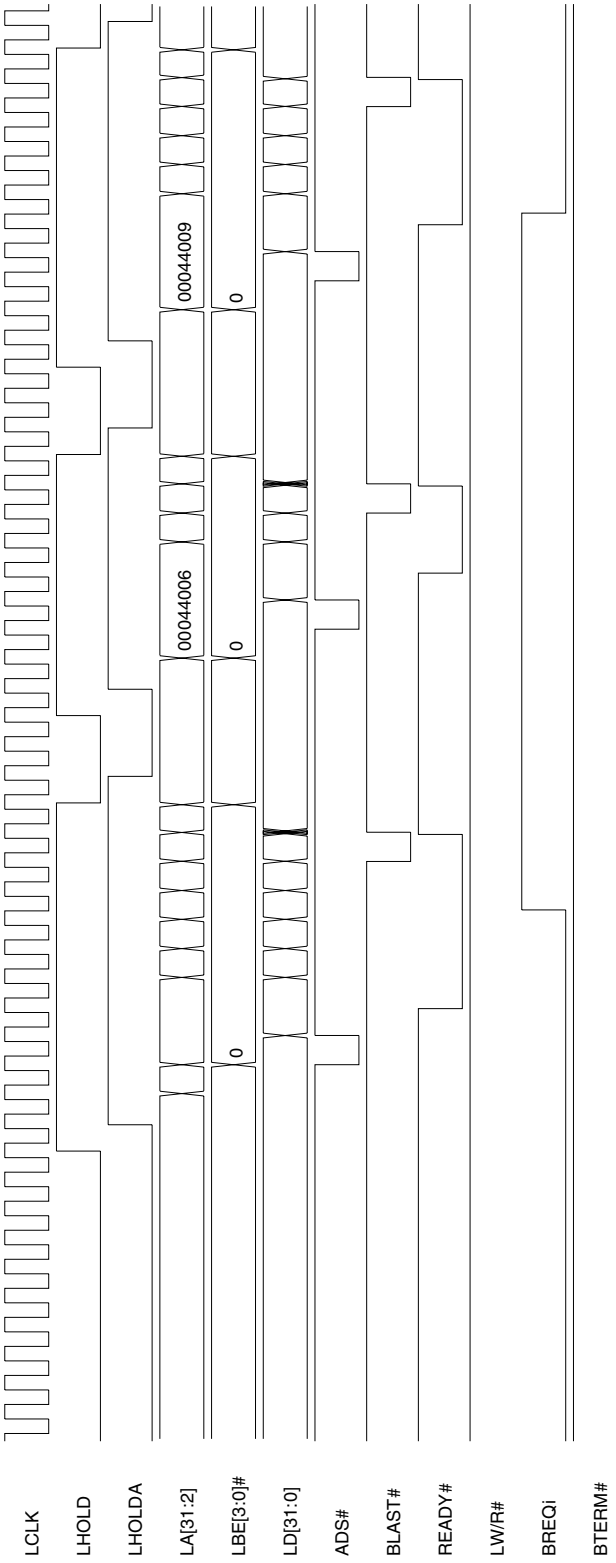
Timing Diagram 7-11. Direct Slave Burst Write Suspended by Single Cycle BREQi



Notes: *This 9-Dword Direct Slave Burst Write transfer is suspended by a one-clock cycle BREQi assertion. The remaining three Dwords are transferred after the PEX 8311 is granted the Local Bus again.*

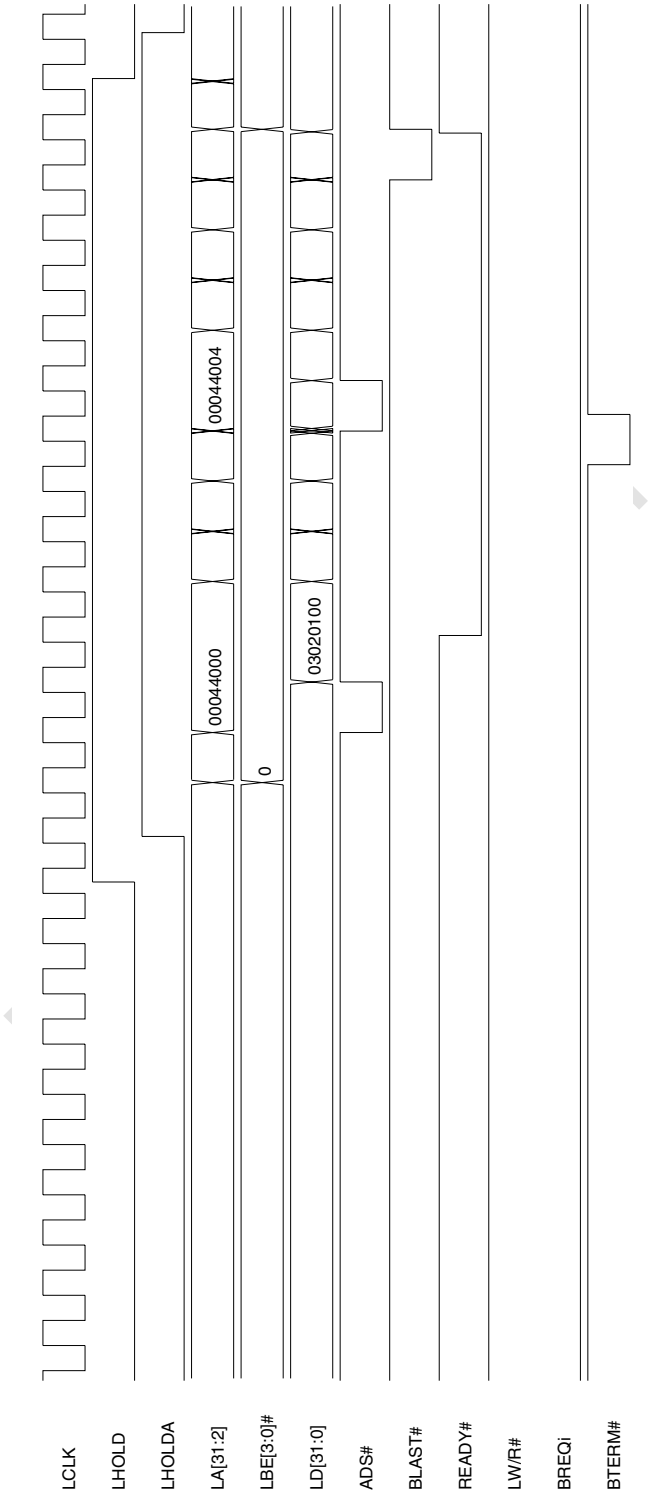
Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=45C2h.

Timing Diagram 7-12. Direct Slave Burst Write Suspended by Multi-Cycle BREQi



Notes: *This 14-Dword Direct Slave Burst Write transfer is suspended twice by a multi-clock cycle BREQi assertion. Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=45C2h.*

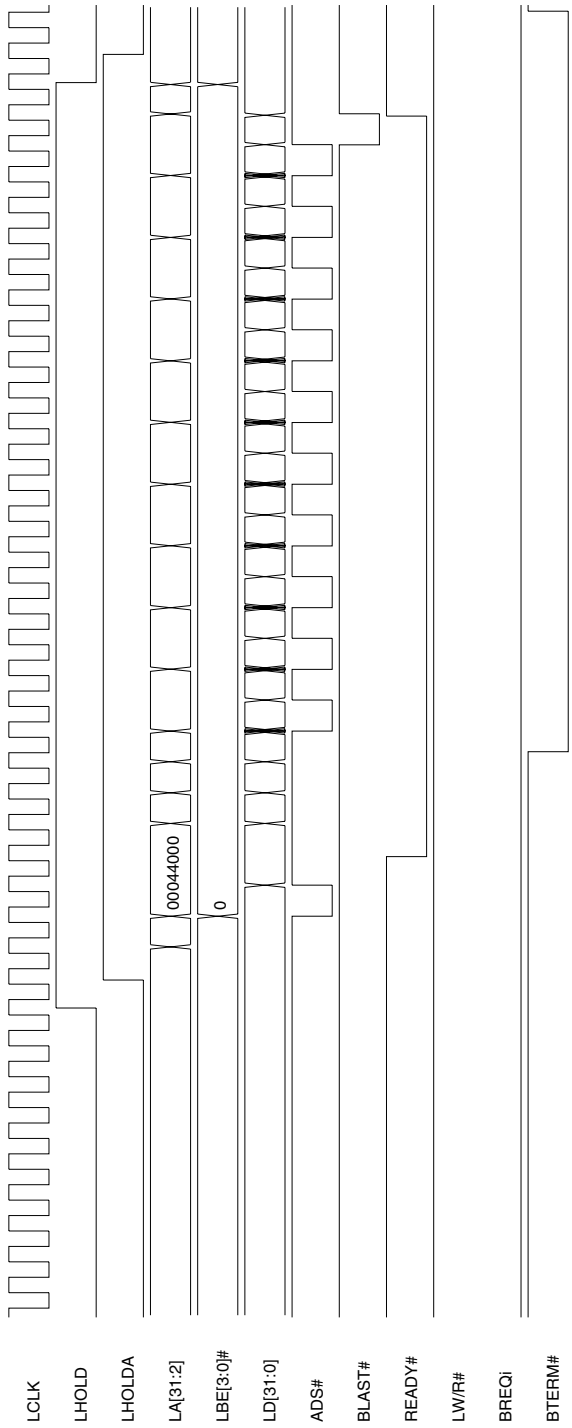
Timing Diagram 7-13. Direct Slave Burst Write Interrupted by Single Cycle BTERM#



Notes: *This 9-Dword Direct Slave Burst Write transfer is interrupted by a one-clock cycle BTERM# assertion. The remaining five Dwords are transferred after the PEX 8311 generates a new Address phase on the Local Bus.*

Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=45C2h.

Timing Diagram 7-14. Direct Slave Burst Write Interrupted by Multi-Cycle BTERM#

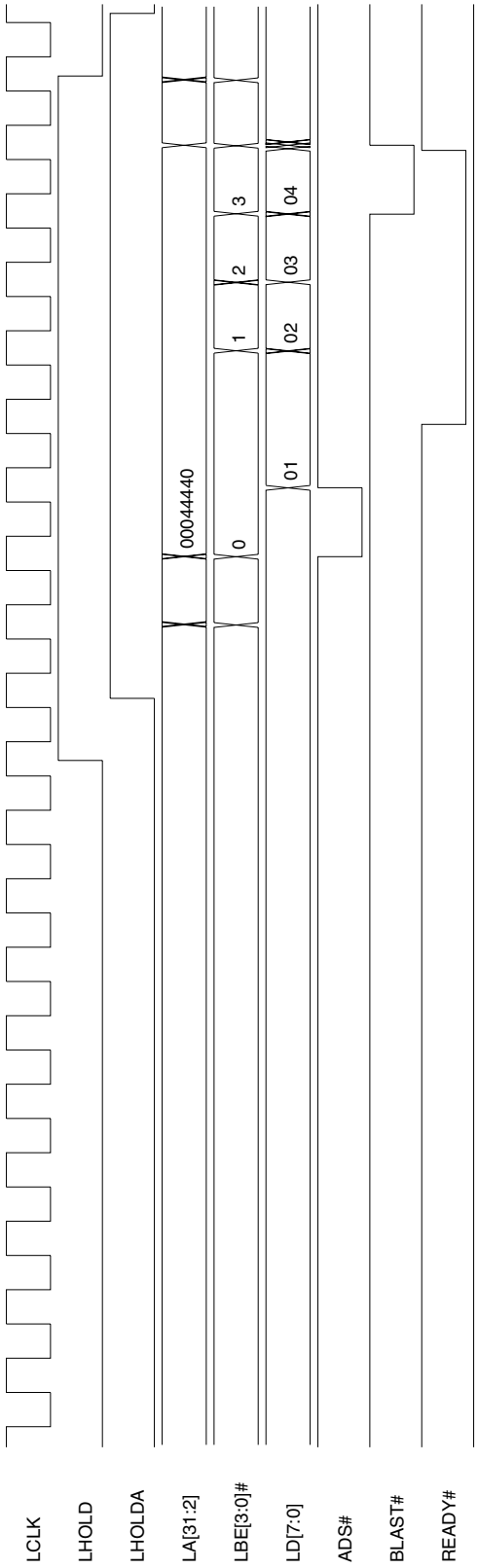


Notes: *This 14-Dword Direct Slave Burst Write transfer is interrupted multiple times by a multi-clock cycle BTERM# assertion.*

The PEX 8311 generates a new Address phase for each Dword of data transferred, when BTERM# remains asserted.

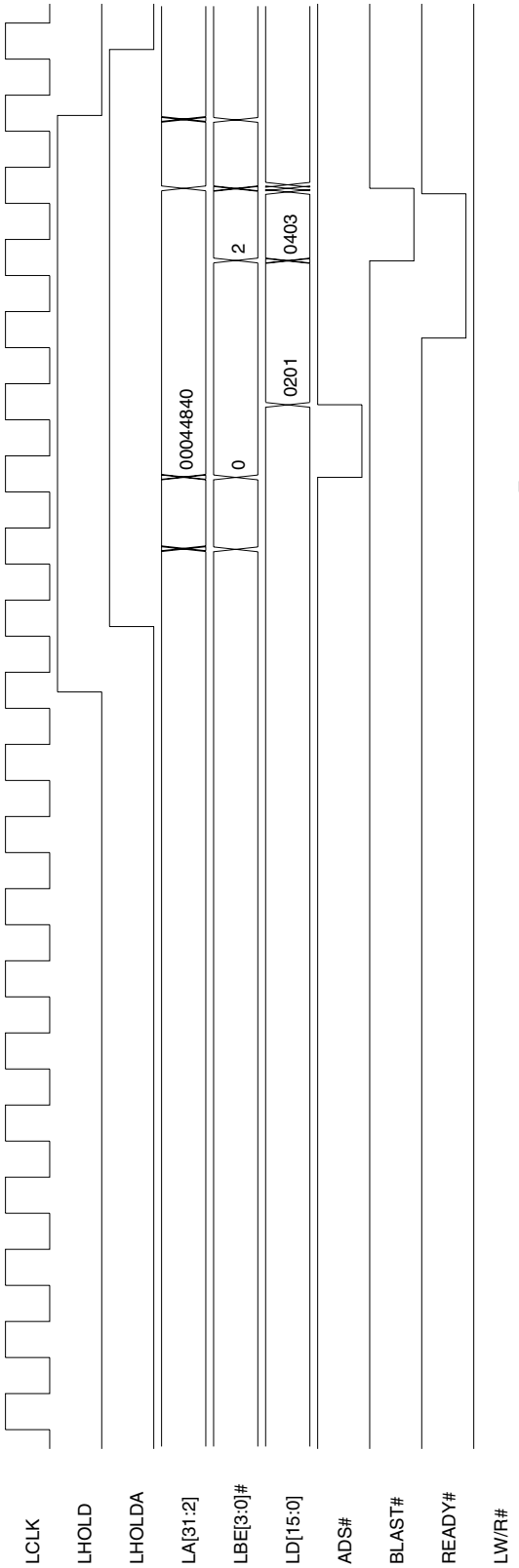
Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=45C2h.

Timing Diagram 7-15. Direct Slave Single Cycle Write (8-Bit Local Bus)



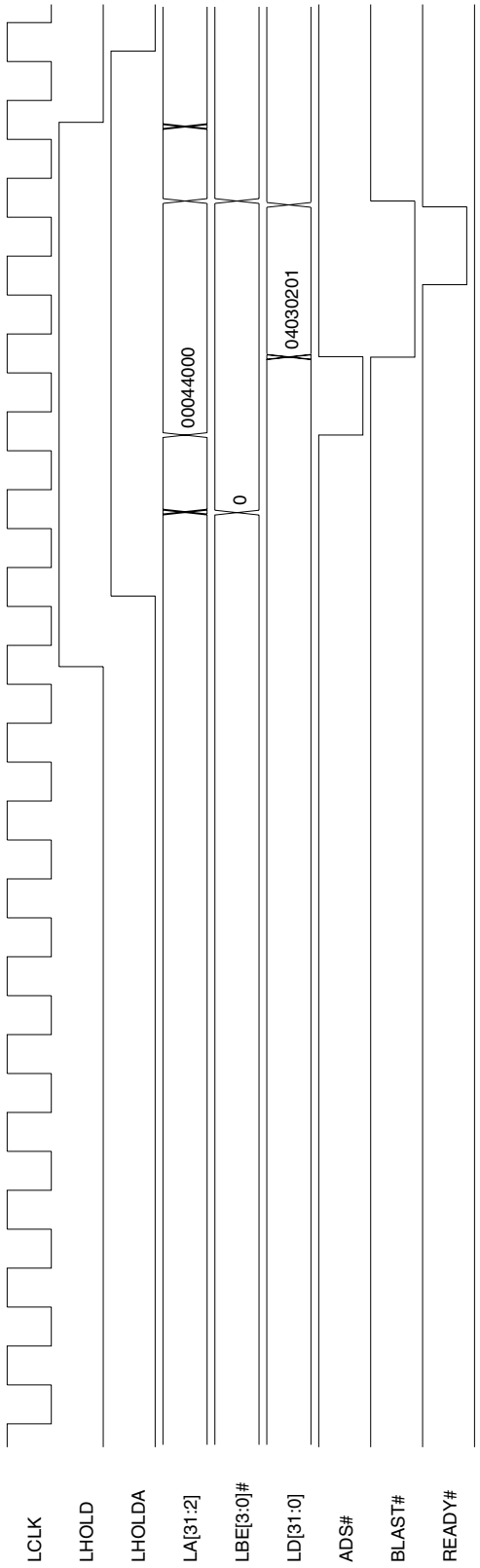
Note: *Key bit/register values are MARBR[24]=1 and LBRD1[15:0]=0D40h.*

Timing Diagram 7-16. Direct Slave Single Cycle Write (16-Bit Local Bus)



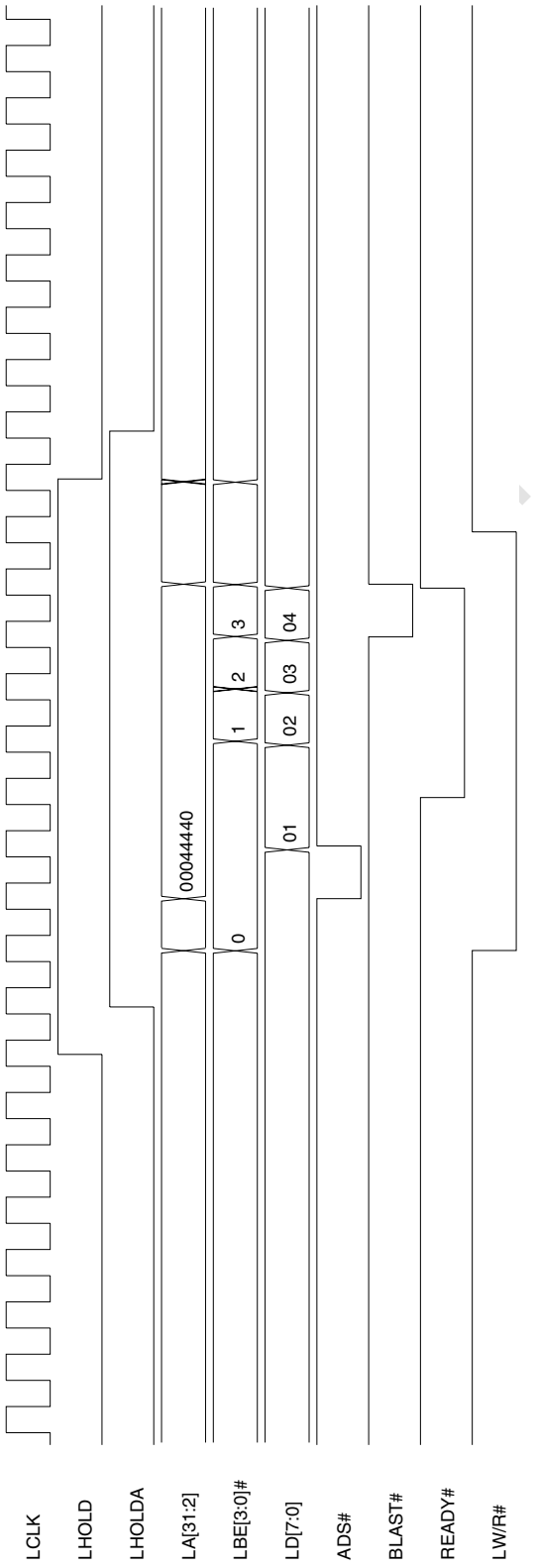
Note: *Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=1541h.*

Timing Diagram 7-17. Direct Slave Single Cycle Write (32-Bit Local Bus)



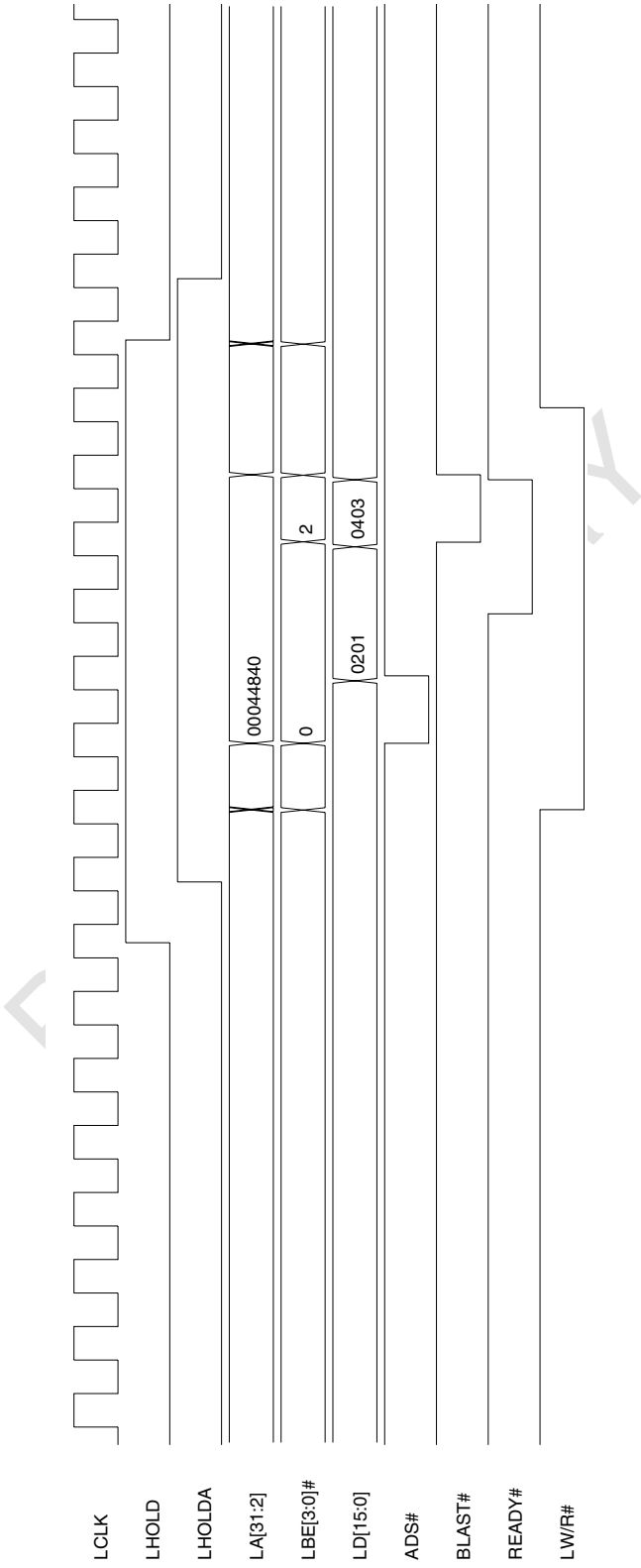
Note: *Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=0D42h.*

Timing Diagram 7-18. Direct Slave Single Cycle Read (8-Bit Local Bus)



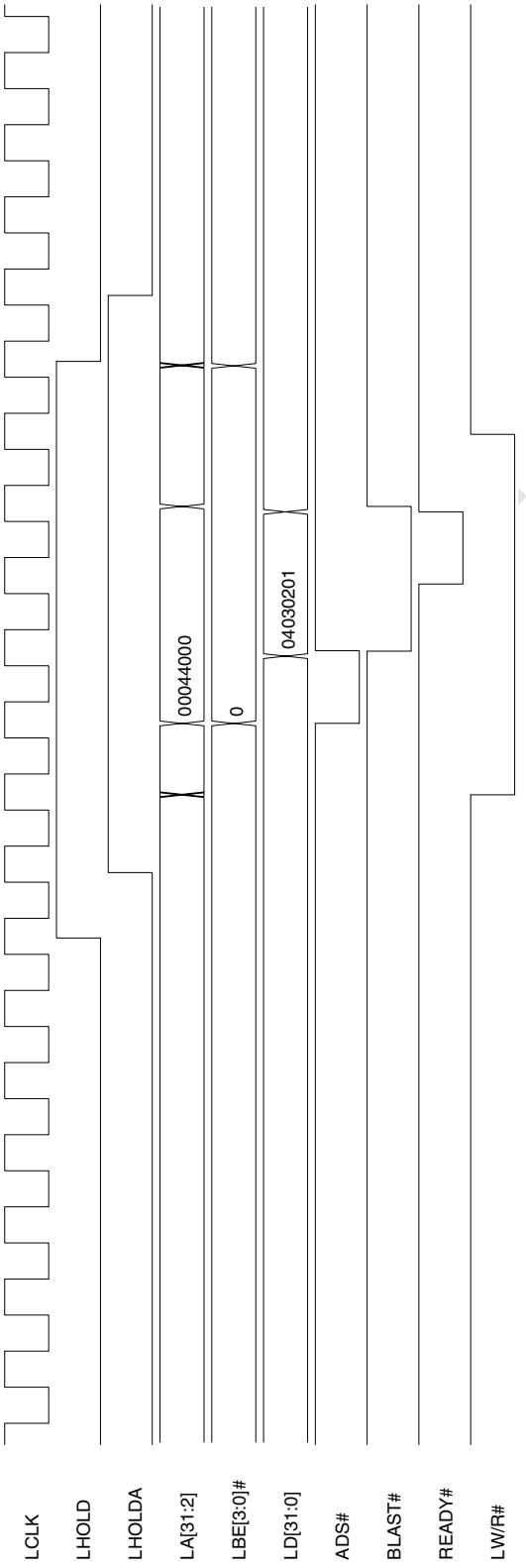
Note: *Key bit/register values are MARBR[24]=1 and LBRD1[15:0]=0D40h.*

Timing Diagram 7-19. Direct Slave Single Cycle Read (16-Bit Local Bus)



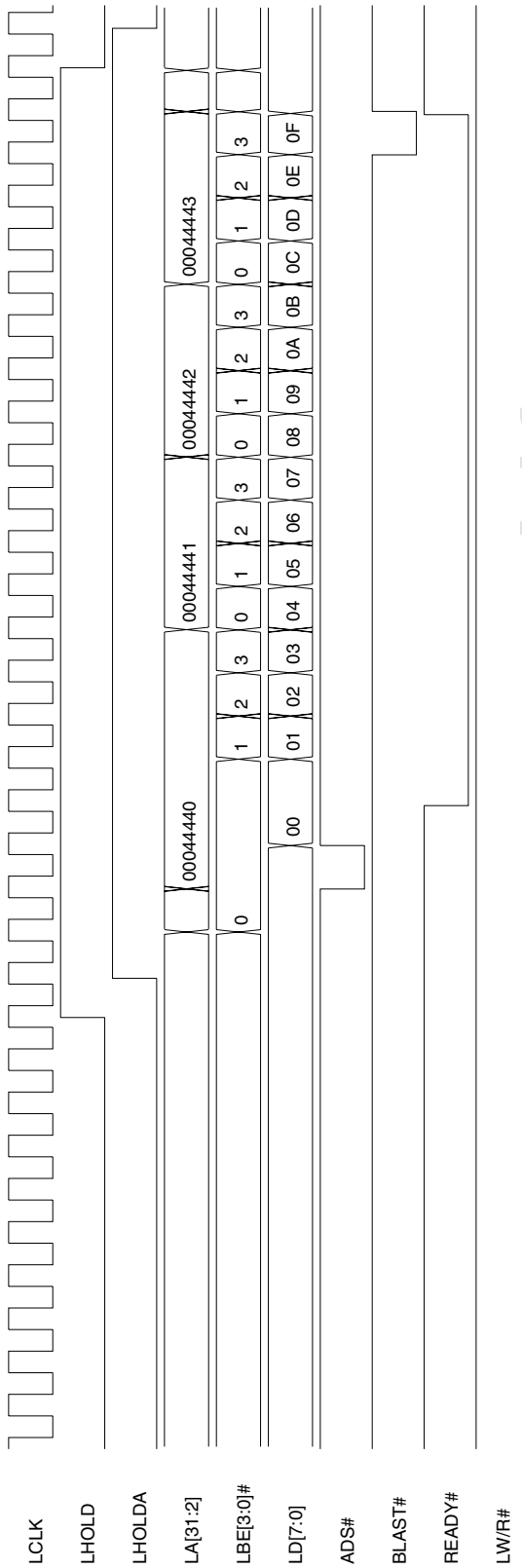
Note: *Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=1541h.*

Timing Diagram 7-20. Direct Slave Single Cycle Read (32-Bit Local Bus)



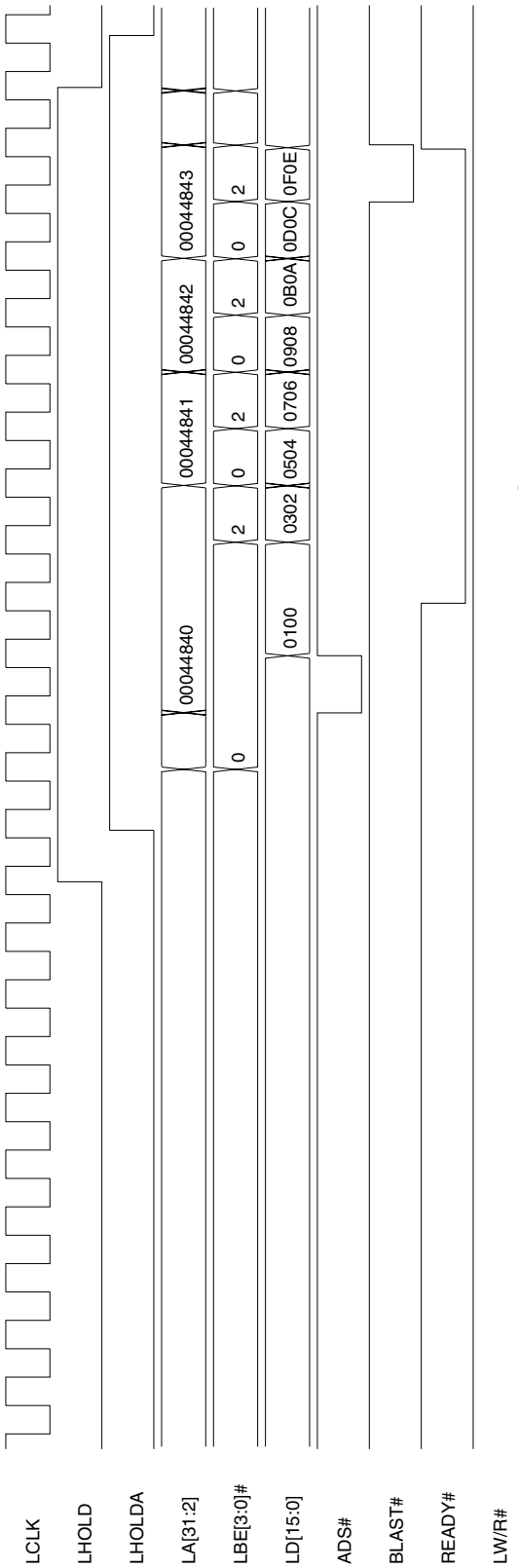
Note: *Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=0D42h.*

Timing Diagram 7-21. Direct Slave Burst Write of 4 Dwords (8-Bit Local Bus)



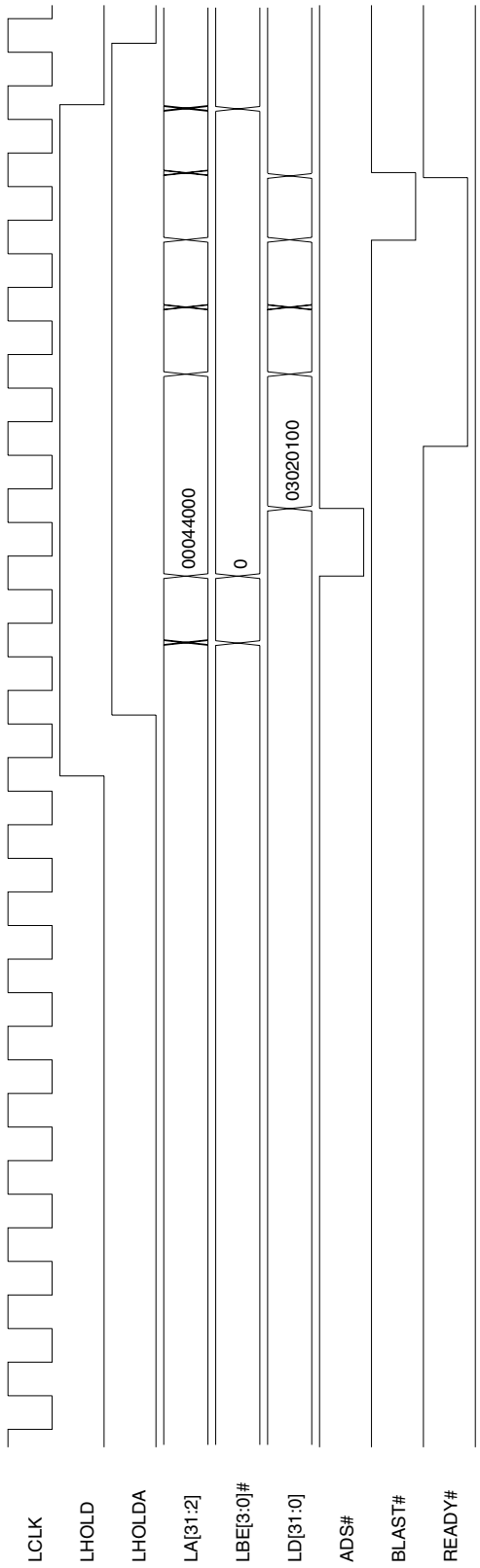
Note: *Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=25C0h.*

Timing Diagram 7-22. Direct Slave Burst Write of 4 Dwords (16-Bit Local Bus)



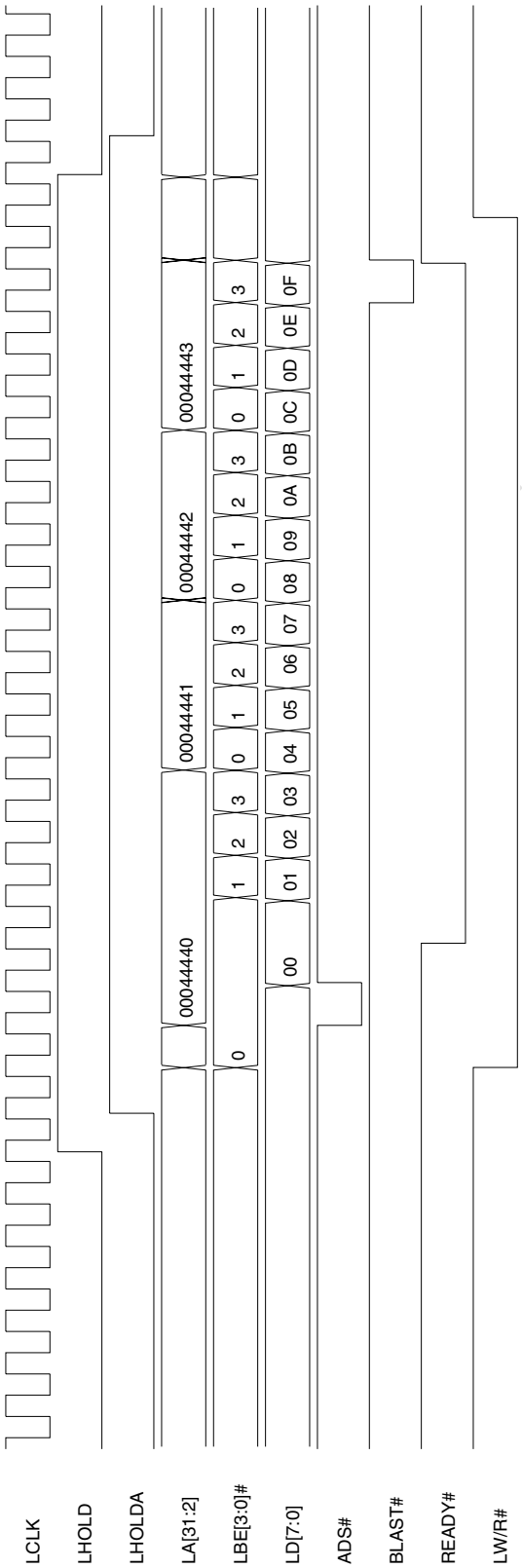
Note: *Key bit/register values are MARBR[24]=1 and LBRD1[15:0]=25C1h.*

Timing Diagram 7-23. Direct Slave Burst Write of 4 Dwords (32-Bit Local Bus)



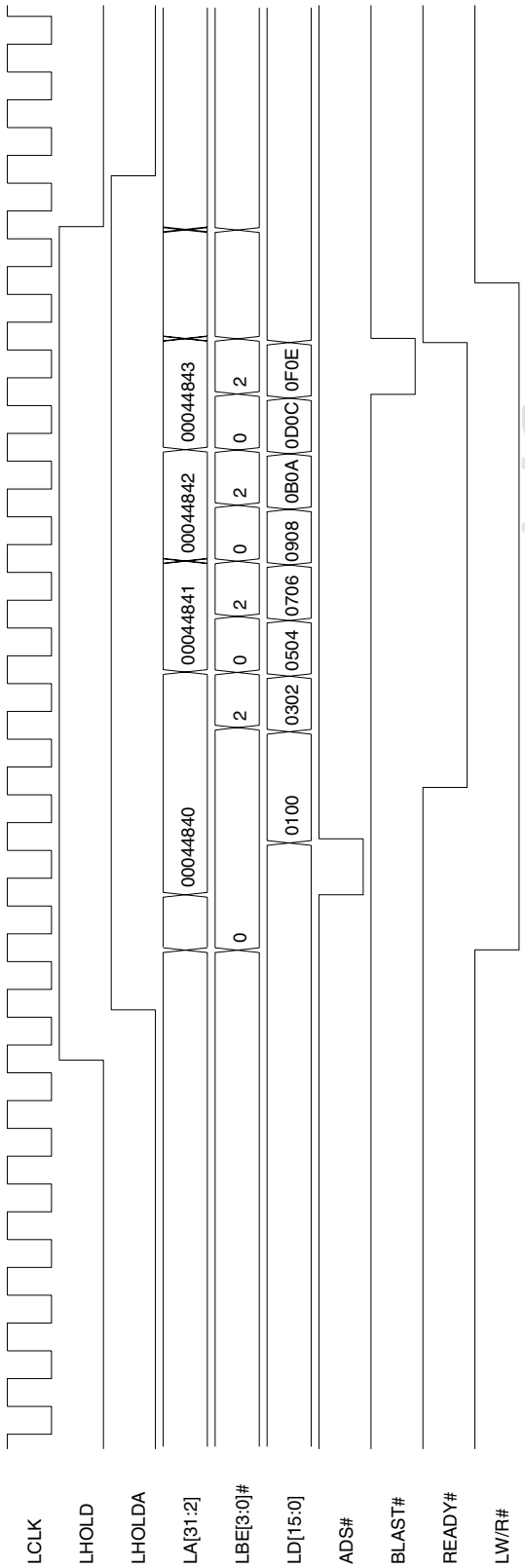
Note: *Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=25C2h.*

Timing Diagram 7-24. Direct Slave Burst Read of 4 Dwords (8-Bit Local Bus)



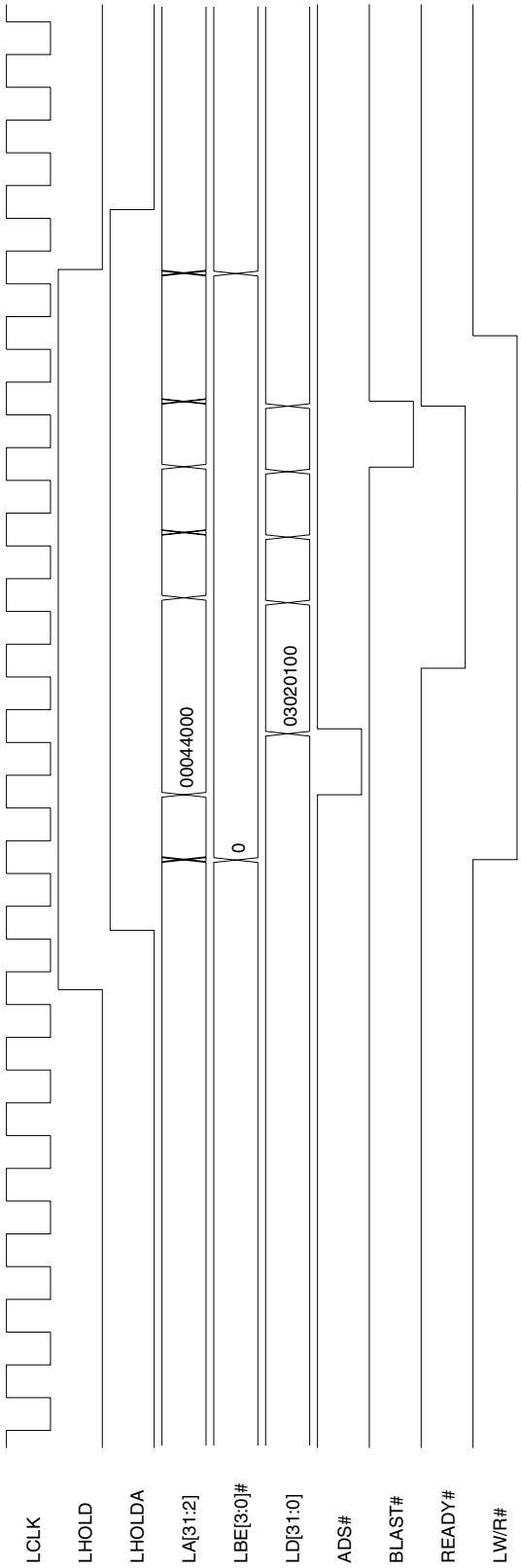
Note: *Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=25C0h.*

Timing Diagram 7-25. Direct Slave Burst Read of 4 Dwords (16-Bit Local Bus)



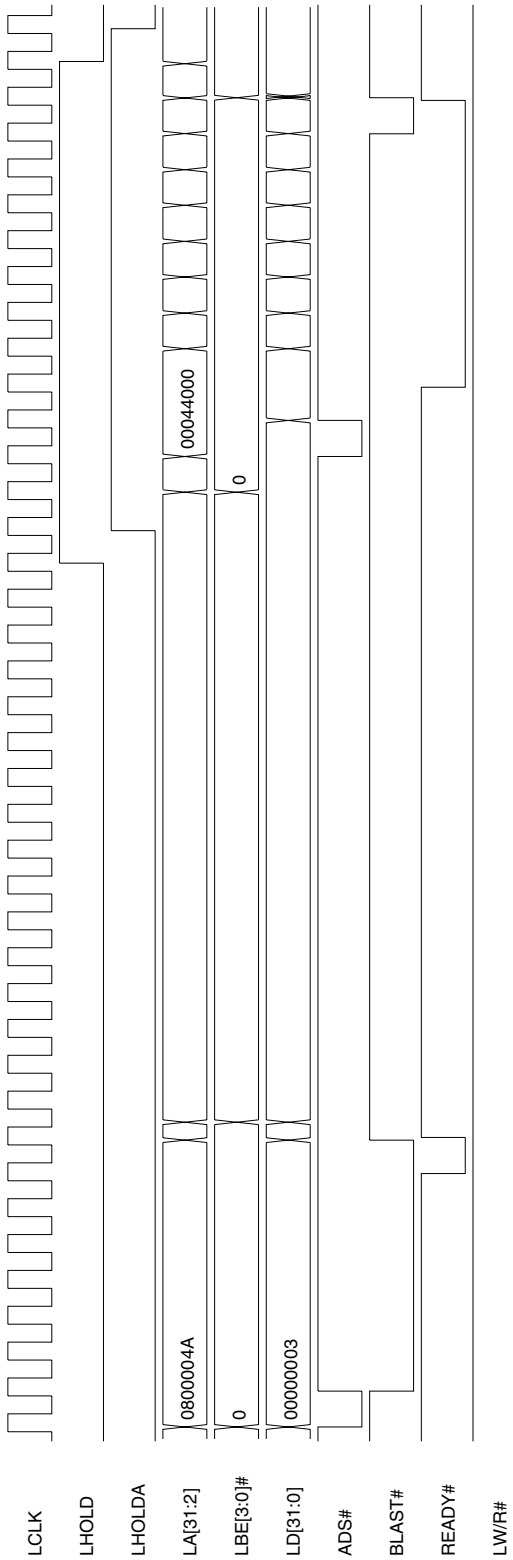
Note: *Key bit/register values are MARBR[24]=1 and LBRD1[15:0]=25C1h.*

Timing Diagram 7-26. Direct Slave Burst Read of 4 Dwords (32-Bit Local Bus)



Note: *Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=25C2h.*

Timing Diagram 7-27. DMA PCI-to-Local (32-Bit Local Bus)

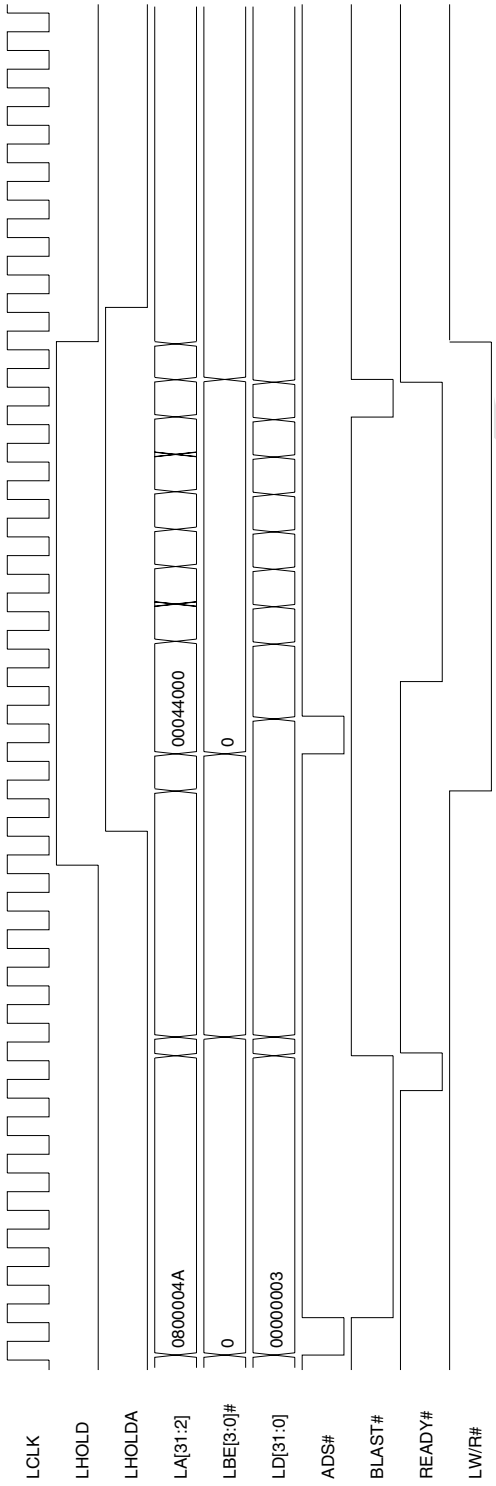


Notes: *The writing of the registers to set up this 32-byte DMA Block mode transfer using DMA Channel 0 is not shown.*

Writing the DMACSR0 register (LOC:128h) with 03h enables and starts this DMA transfer.

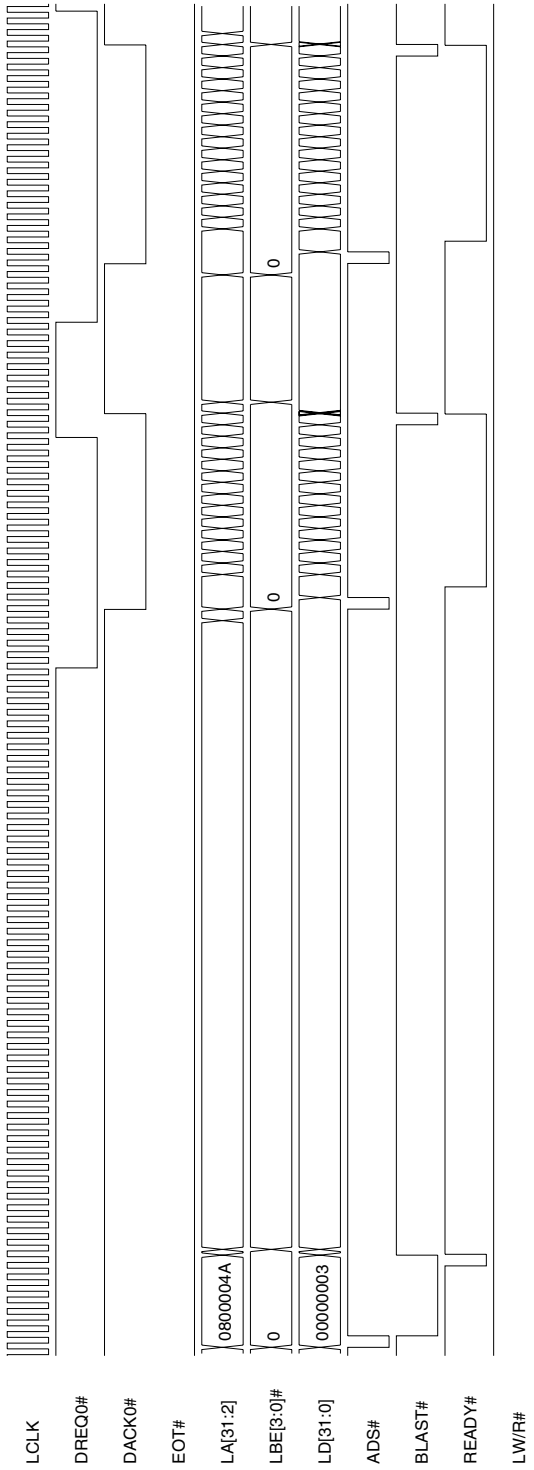
7.4.2.3 C Mode DMA Timing Diagrams

Timing Diagram 7-28. DMA Local-to-PCI (32-Bit Local Bus)



Notes: *The writing of the registers to set up this 32-byte DMA Block mode transfer using DMA Channel 0 is not shown. Writing the DMACSR0 register (LOC:128h) with 03h enables and starts this DMA transfer.*

Timing Diagram 7-29. DMA PCI-to-Local Demand Mode (32-Bit Local Bus)

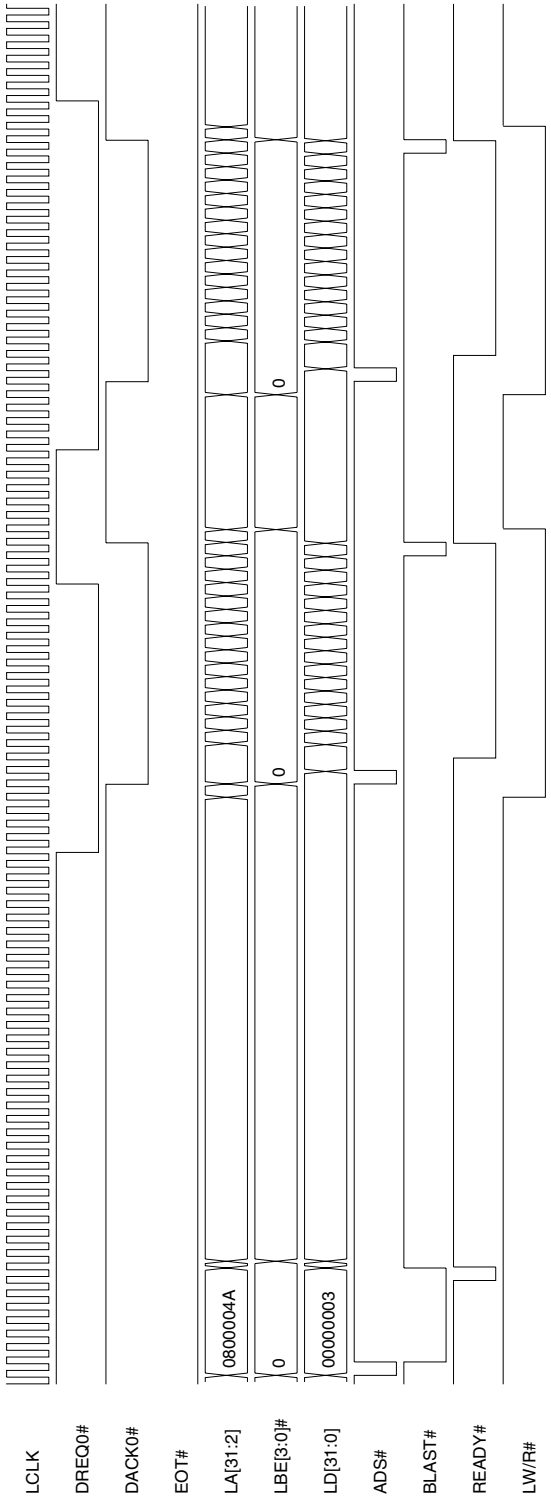


Notes: *The Channel 0 Demand mode DMA transfer starts when the DMACSR0[1:0] bits are written to 11b.*

The PEX 8311 does not attempt to arbitrate for and write data to the Local Bus until it detects the DREQ0# signal asserted.

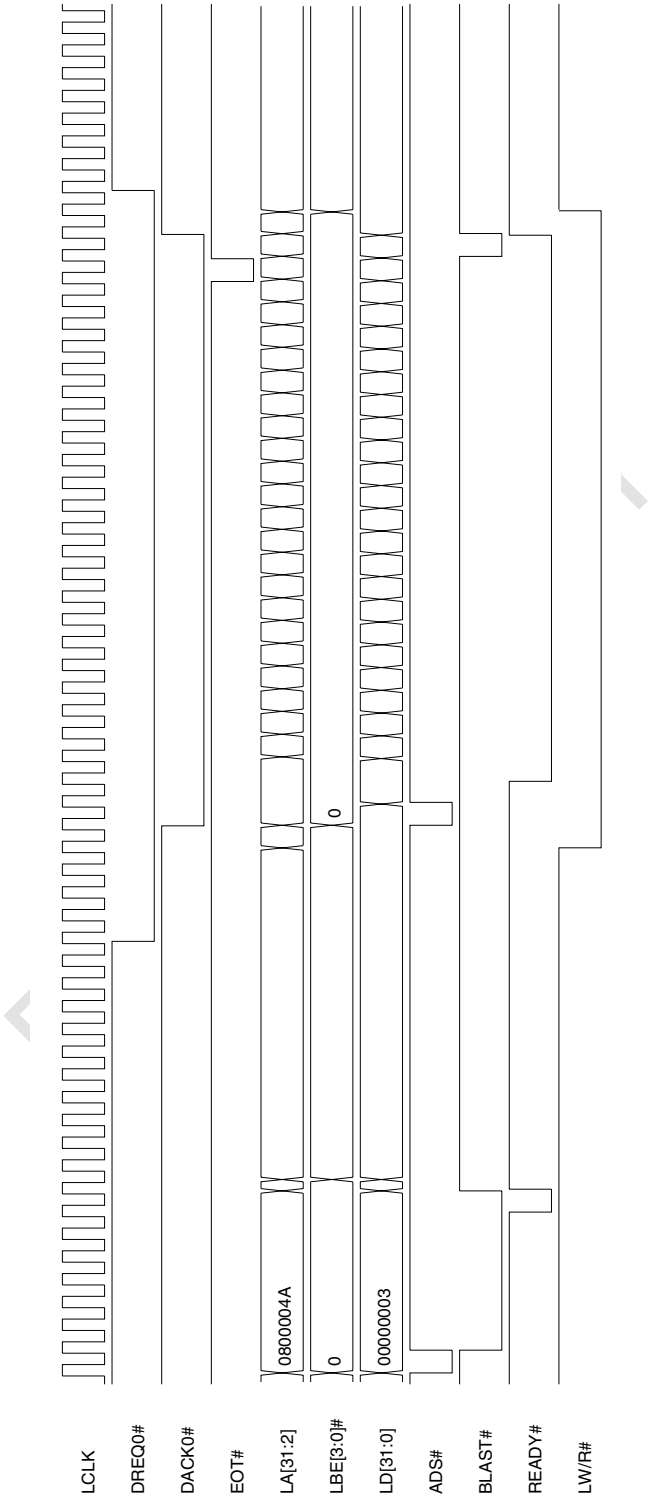
The transfer is temporarily suspended when DREQ0# is de-asserted, then resumed upon its re-assertion.

Timing Diagram 7-30. DMA Local-to-PCI Demand Mode (32-Bit Local Bus)



Note: *The Channel 0 Demand mode DMA transfer starts when the DMACSR0[1:0] bits are written to 11b and the PEX 8311 detects the DREQ0# signal asserted. Once started, the PEX 8311 arbitrates for and reads data from the Local Bus, then writes the data to the internal PCI Bus until the transfer is temporarily suspended when DREQ0# is de-asserted. The transfer resumes upon DREQ0# re-assertion.*

Timing Diagram 7-31. DMA Local-to-PCI Demand Mode with EOT# Assertion (32-Bit Local Bus)

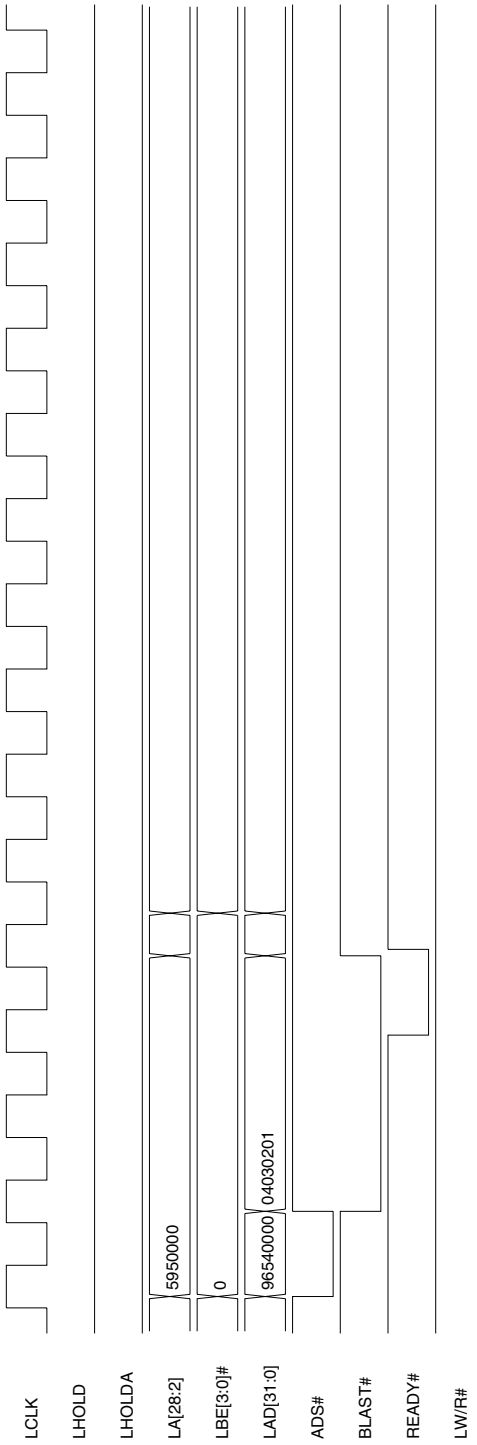


Note: *The Channel 0 Demand mode DMA transfer starts when the DMACSR0[1:0] bits are written to 11b and the PEX 8311 detects the DREQ0# signal asserted. Once started, the PEX 8311 arbitrates for and reads data from the Local Bus, then writes the data to the internal PCI Bus until the transfer is terminated with an EOT# assertion. Data read into the DMA FIFO is written to the internal PCI Bus.*

7.4.3 J Mode Functional Timing Diagrams

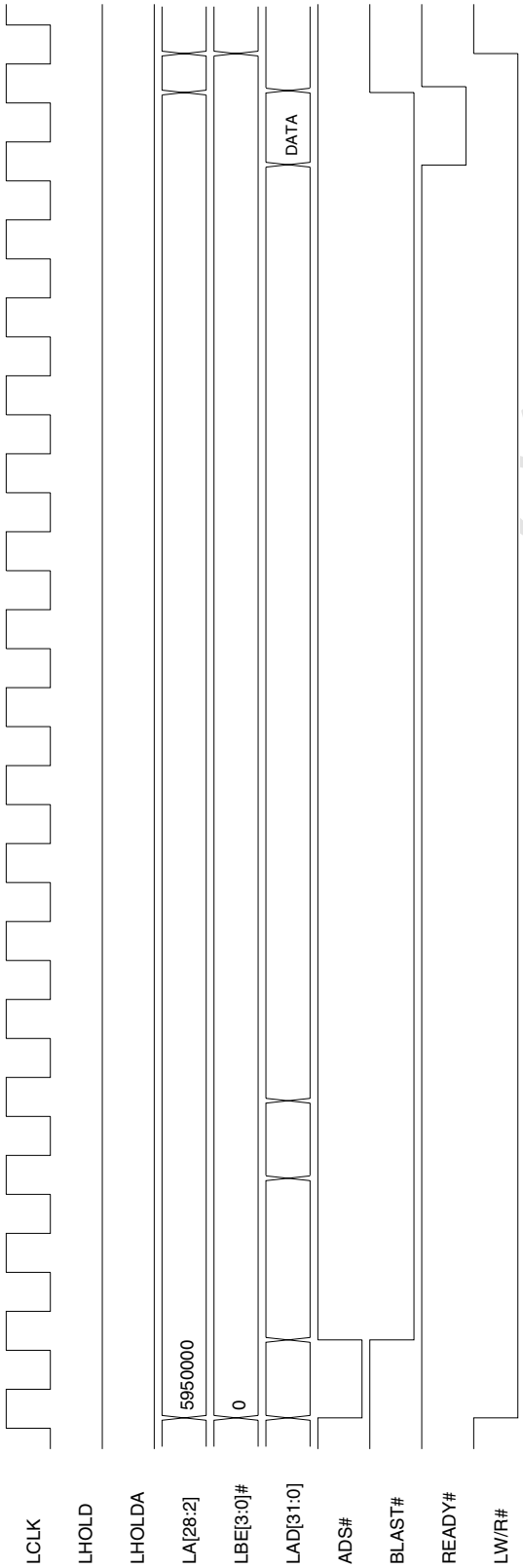
7.4.3.1 J Mode Direct Master Timing Diagrams

Timing Diagram 7-32. Direct Master Single Cycle Write



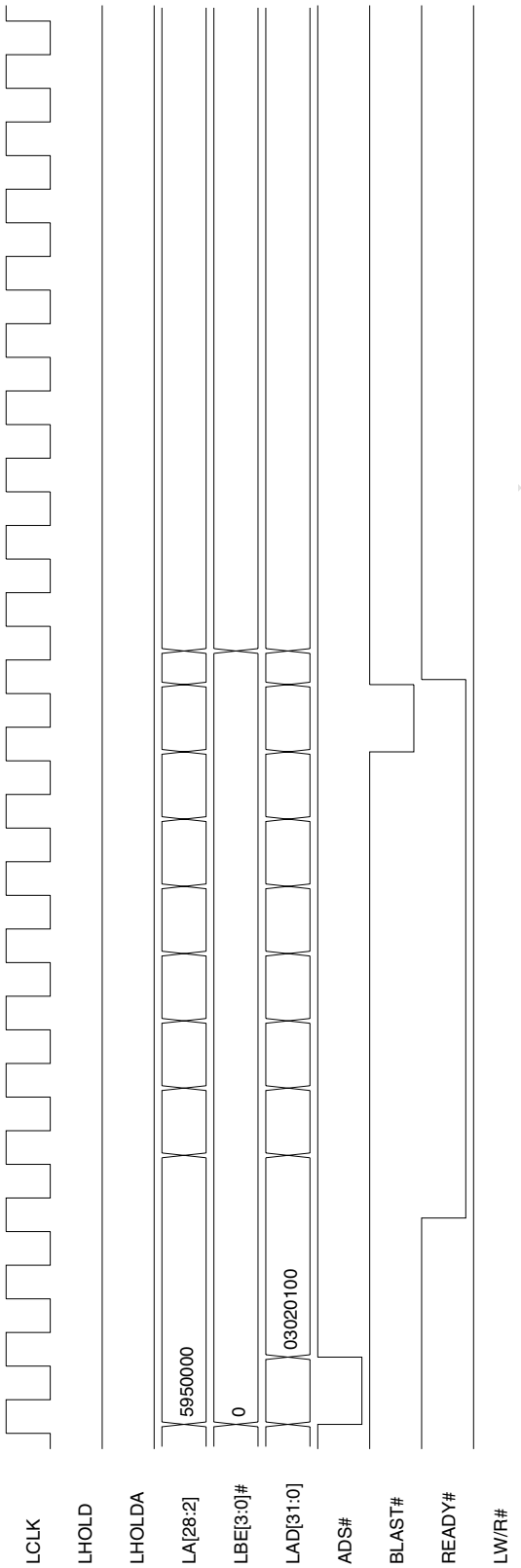
Note: *Key register value is DMPBAM[15:0]=00E3h.*

Timing Diagram 7-33. Direct Master Single Cycle Read



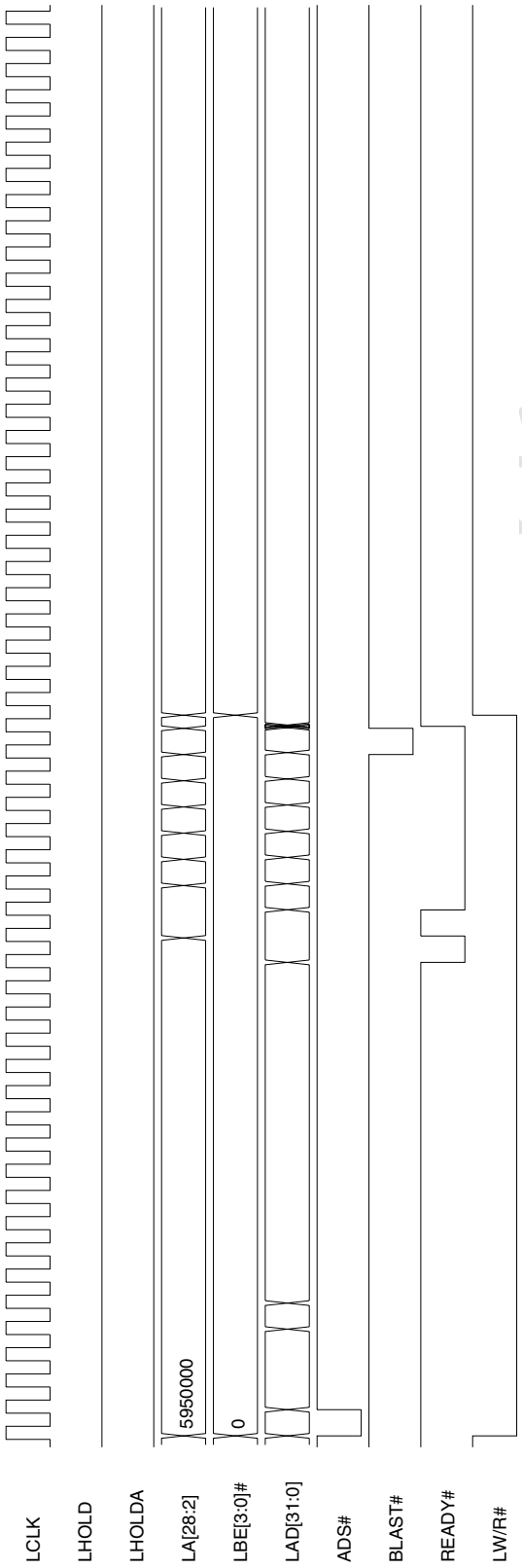
Note: *Key register value is DMPBAM[15:0]=00E3h.*

Timing Diagram 7-34. Direct Master Burst Write of 8 Dwords



Note: *Key register value is DMPBAM[15:0]=0007h.*

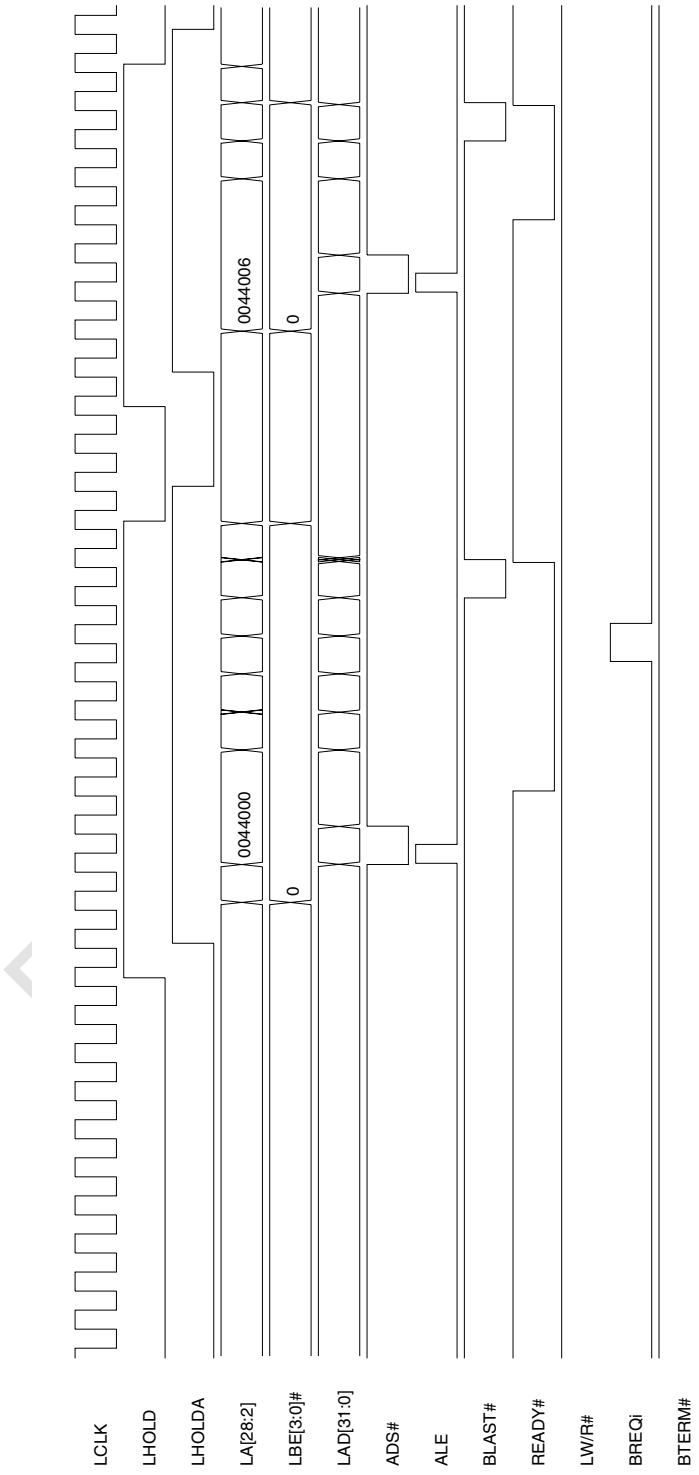
Timing Diagram 7-35. Direct Master Burst Read of 8 Dwords



Note: *Key register value is DMPBAM[15:0]=0007h.*

7.4.3.2 J Mode Direct Slave Timing Diagrams

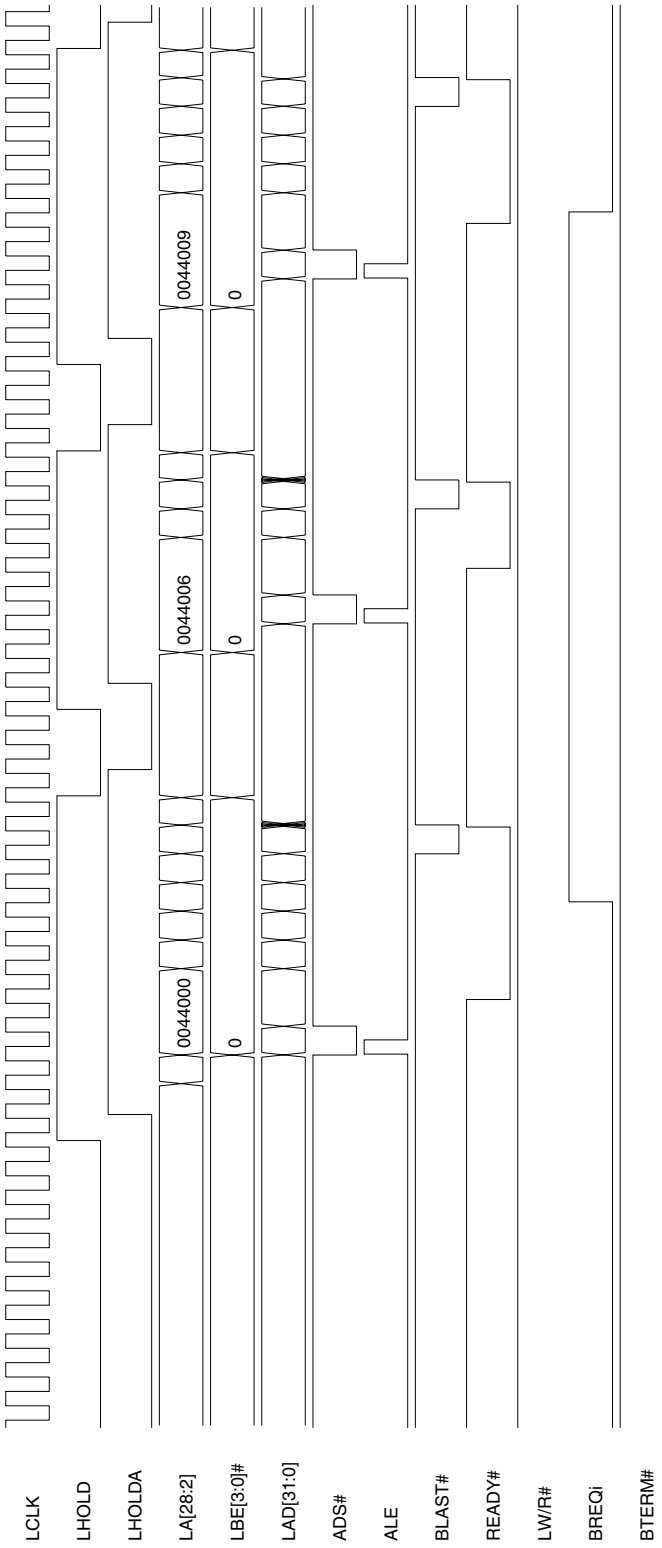
Timing Diagram 7-36. Direct Slave Burst Write Suspended by Single Cycle BREQi



Notes: *This 9-Dword Direct Slave Burst Write transfer is suspended by a one-clock cycle BREQi assertion. The remaining three Dwords are transferred after the PEX 8311 is granted the Local Bus again.*

Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=45C2h.

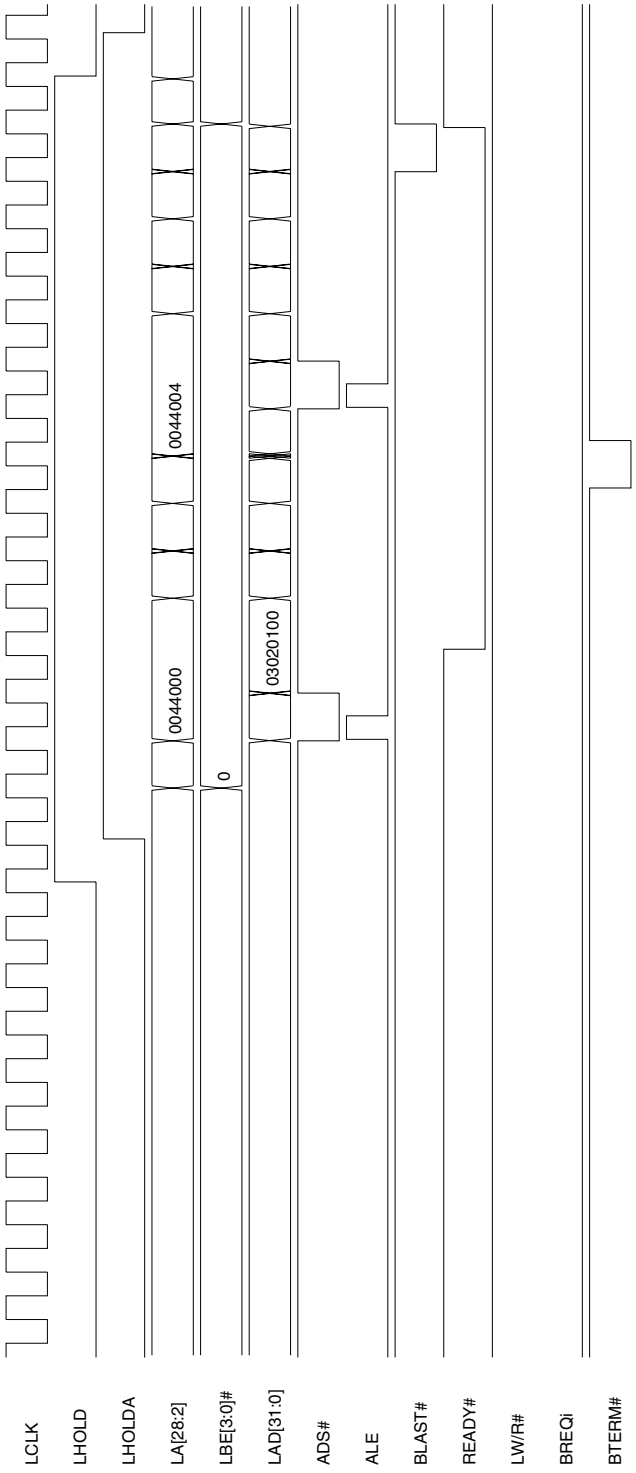
Timing Diagram 7-37. Direct Slave Burst Write Suspended by Multi-Cycle BREQi



Notes: *This 14-Dword Direct Slave Burst Write transfer is suspended twice by a multi-clock cycle BREQi assertion.*

Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=45C2h.

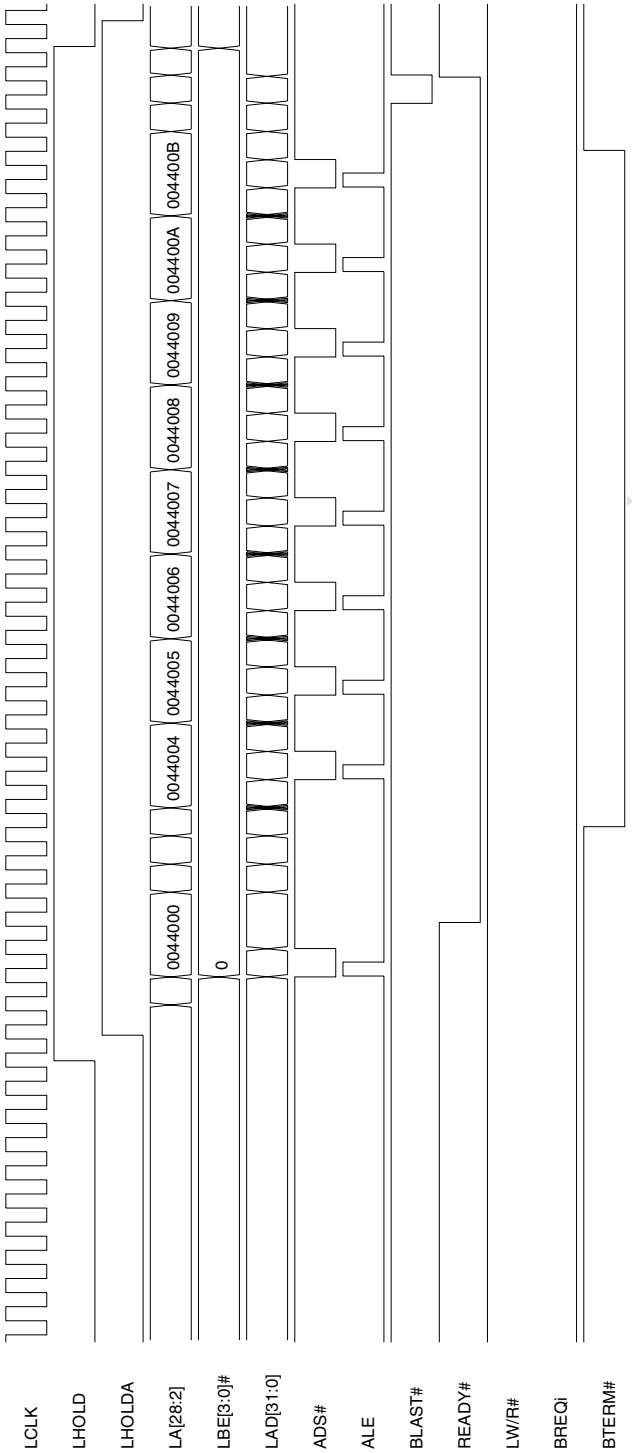
Timing Diagram 7-38. Direct Slave Burst Write Interrupted by Single Cycle BTERM#



Notes: *This 9-Dword Direct Slave Burst Write transfer is interrupted by a one clock cycle BTERM# assertion. After the Address cycle is generated as a result of BTERM# assertion, the fifth Dword of the transfer is rewritten, and the four remaining Dwords are written to complete the transfer.*

Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=45C2h.

Timing Diagram 7-39. Direct Slave Burst Write Interrupted by Multi-Cycle BTERM#

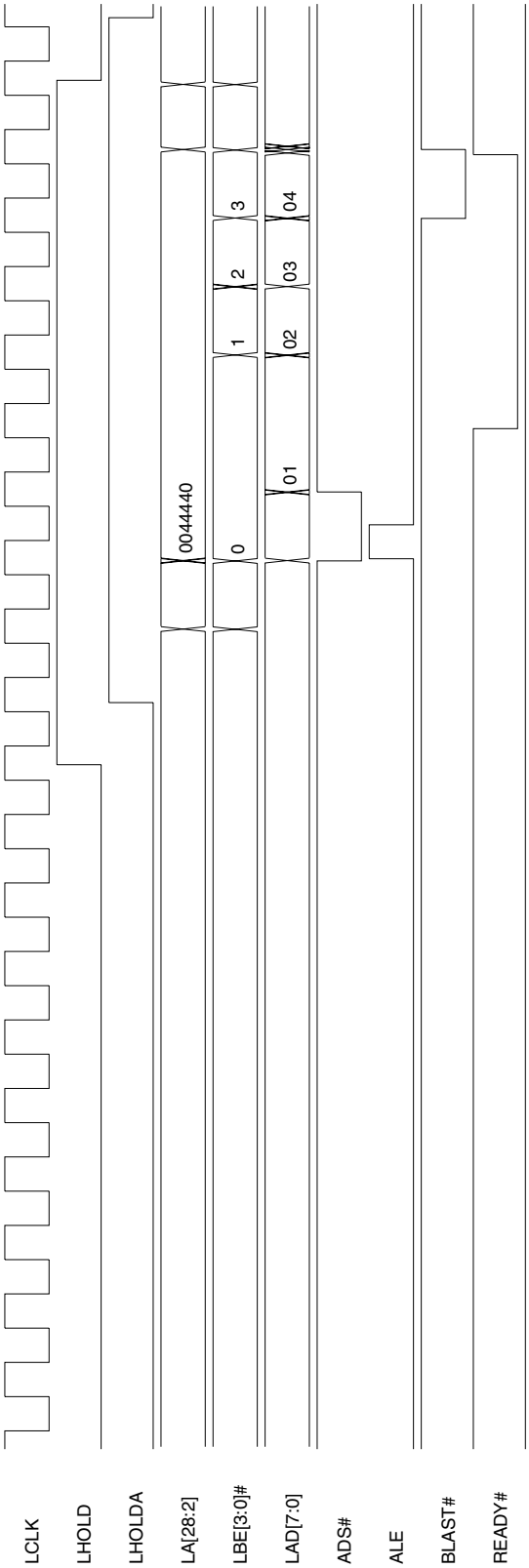


Notes: *This 14-Dword Direct Slave Burst Write transfer is interrupted multiple times by a multi-clock cycle BTERM# assertion.*

Six Dwords are written once and 8 Dwords are written a second time for each new Address phase generated.

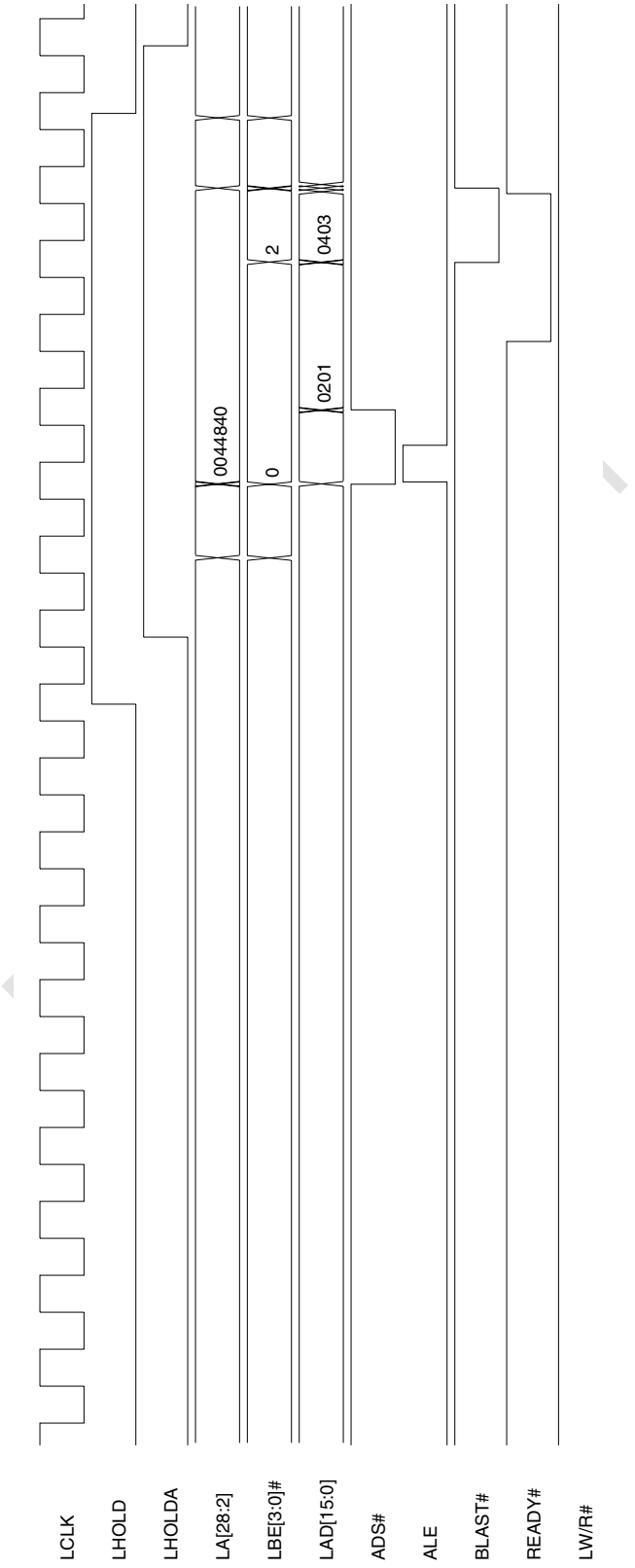
Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=45C2h.

Timing Diagram 7-40. Direct Slave Single Cycle Write (8-Bit Local Bus)



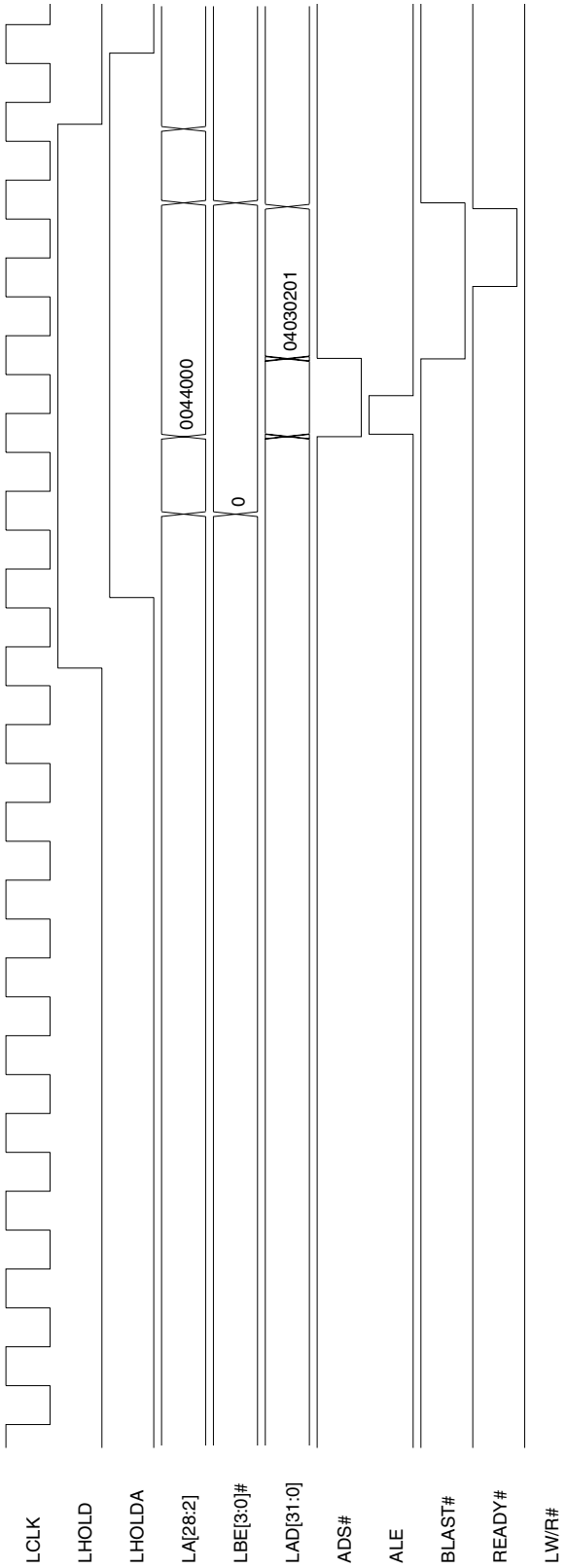
Note: *Key bit/register values are MARBR[24]=1 and LBRD1[15:0]=0D40h.*

Timing Diagram 7-41. Direct Slave Single Cycle Write (16-Bit Local Bus)



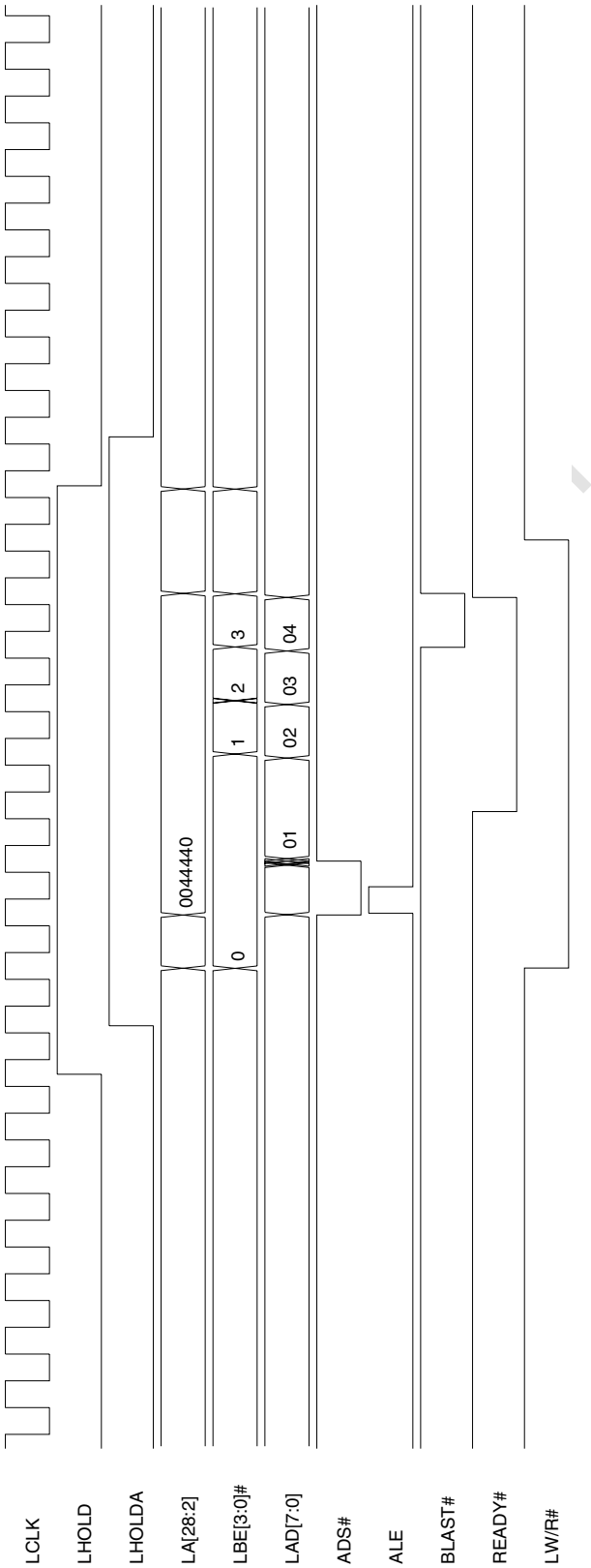
Note: *Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=1541h.*

Timing Diagram 7-42. Direct Slave Single Cycle Write (32-Bit Local Bus)



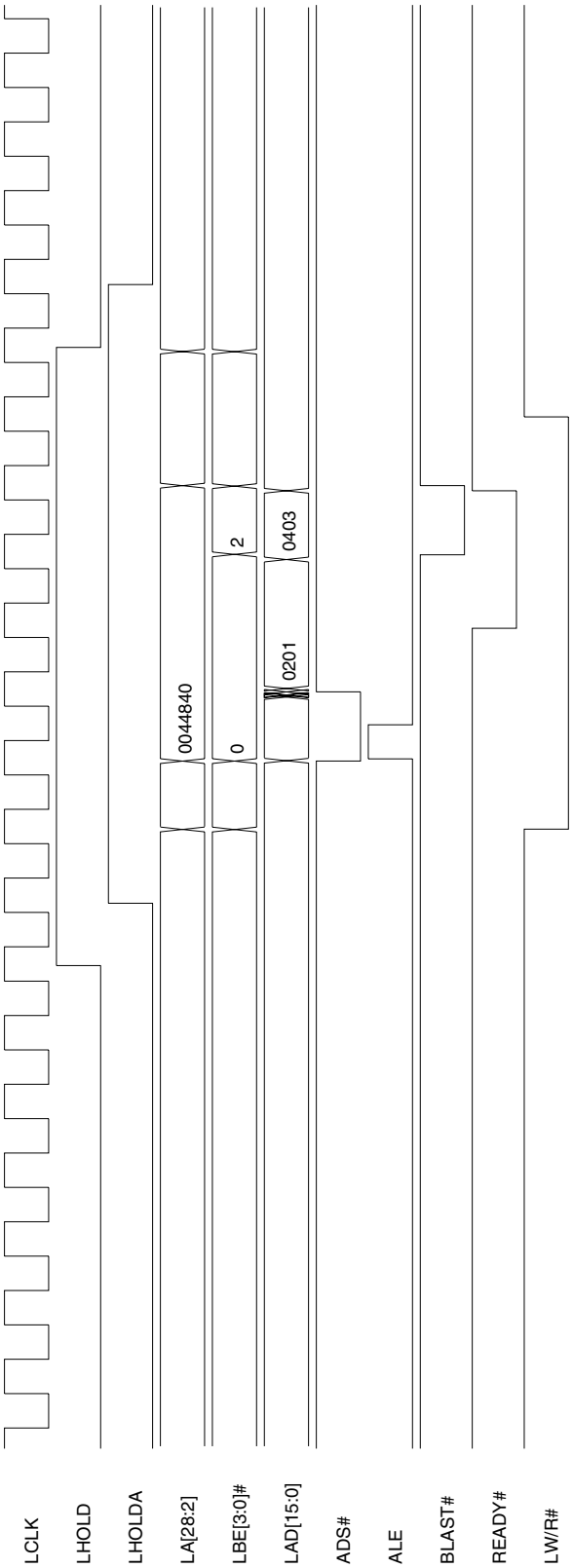
Note: *Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=0D42h.*

Timing Diagram 7-43. Direct Slave Single Cycle Read (8-Bit Local Bus)



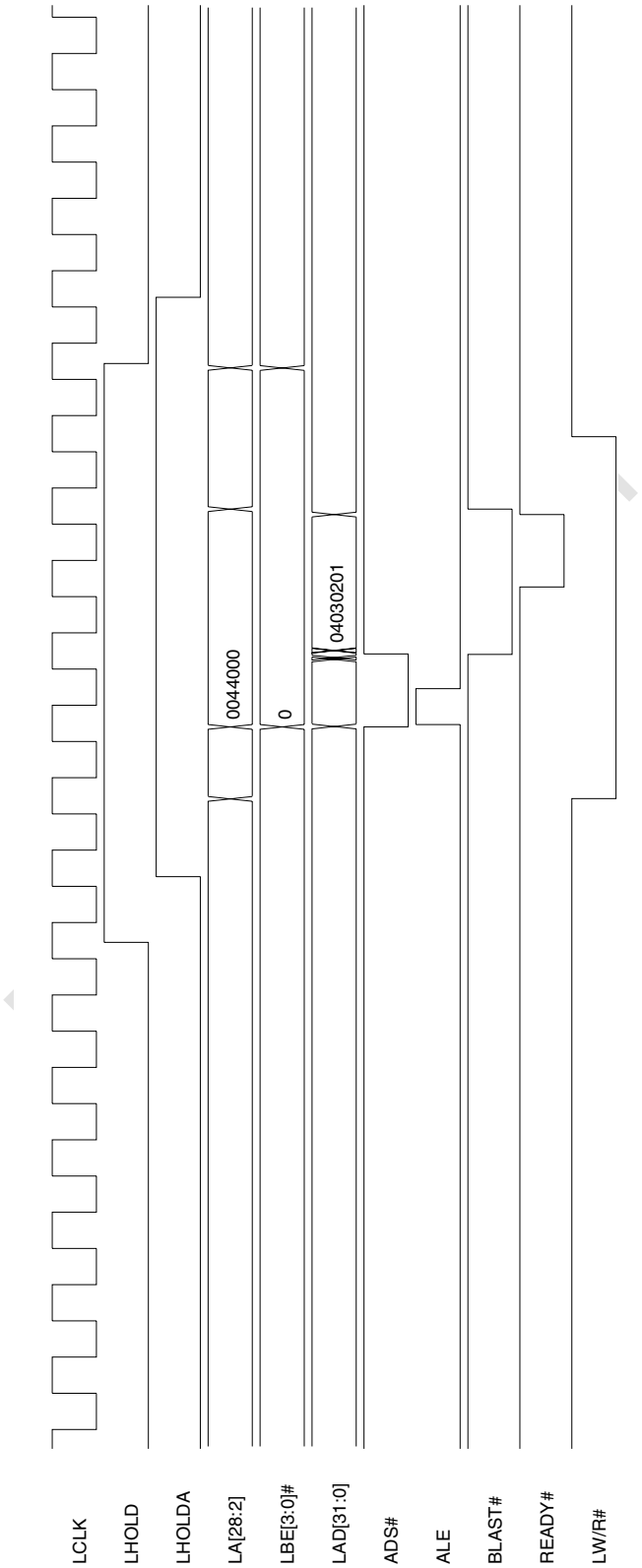
Note: *Key bit/register values are MARBR[24]=1 and LBRD1[15:0]=0D40h.*

Timing Diagram 7-44. Direct Slave Single Cycle Read (16-Bit Local Bus)



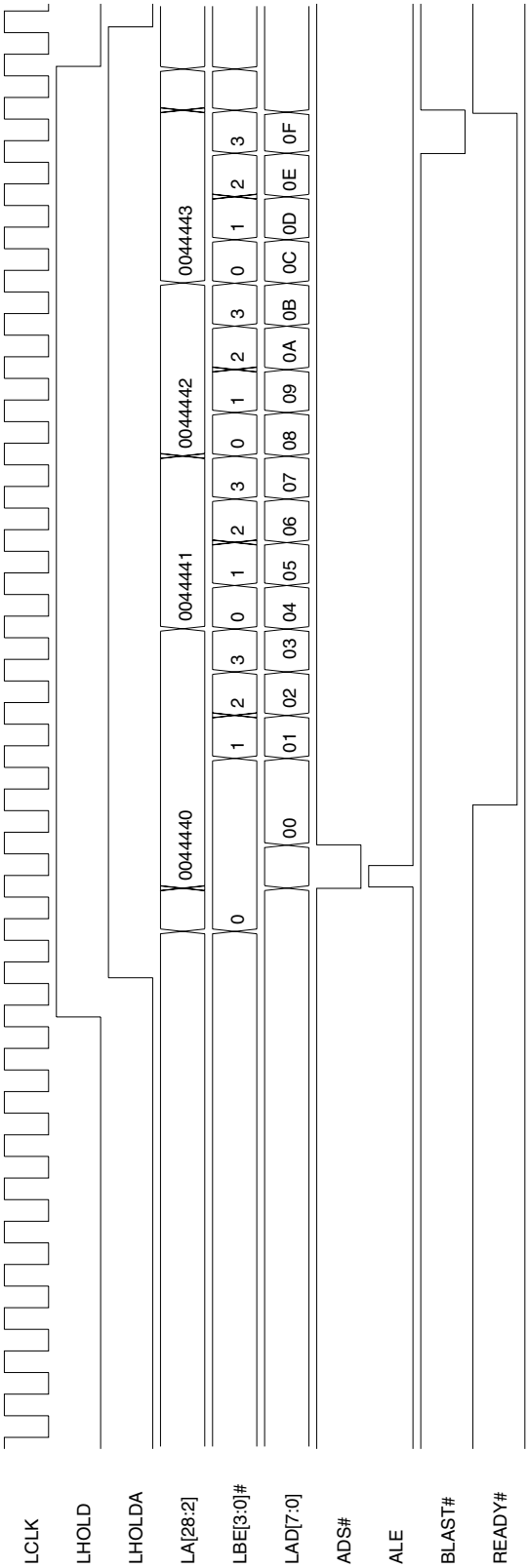
Note: *Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=1541h.*

Timing Diagram 7-45. Direct Slave Single Cycle Read (32-Bit Local Bus)



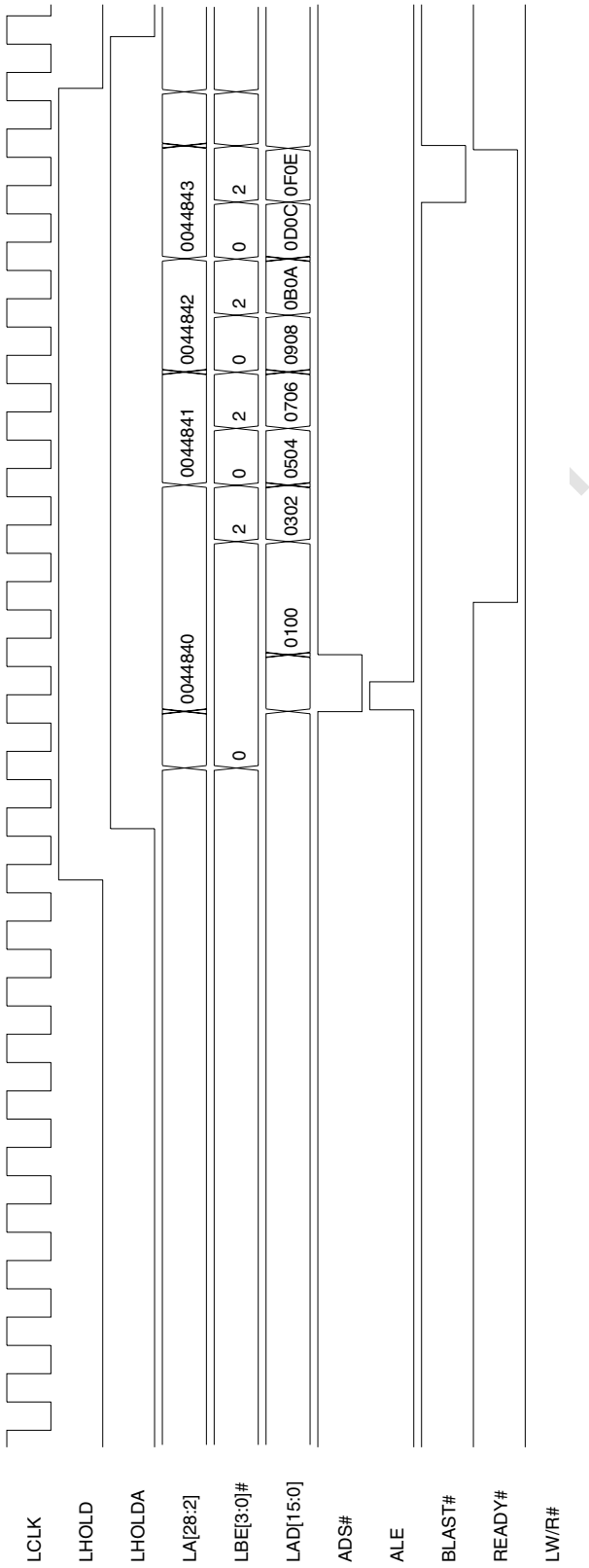
Note: *Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=0D42h.*

Timing Diagram 7-46. Direct Slave Burst Write of 4 Dwords (8-Bit Local Bus)



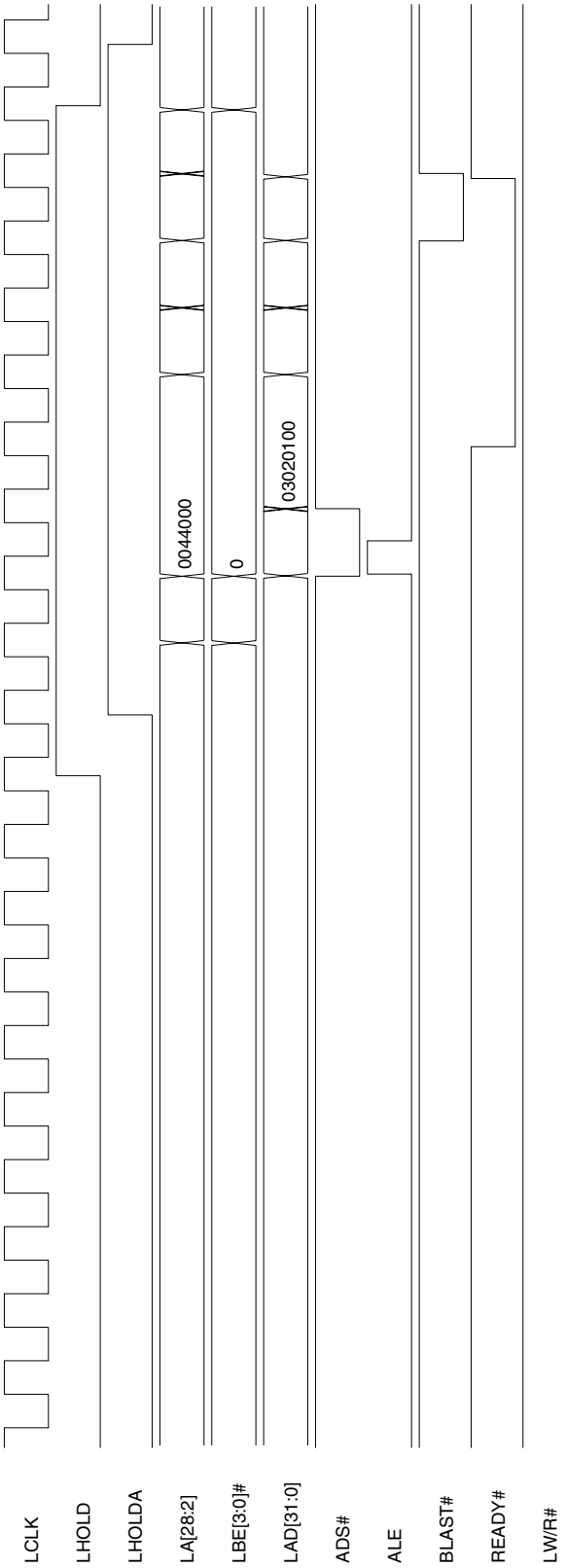
Note: *Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=25C0h.*

Timing Diagram 7-47. Direct Slave Burst Write of 4 Dwords (16-Bit Local Bus)



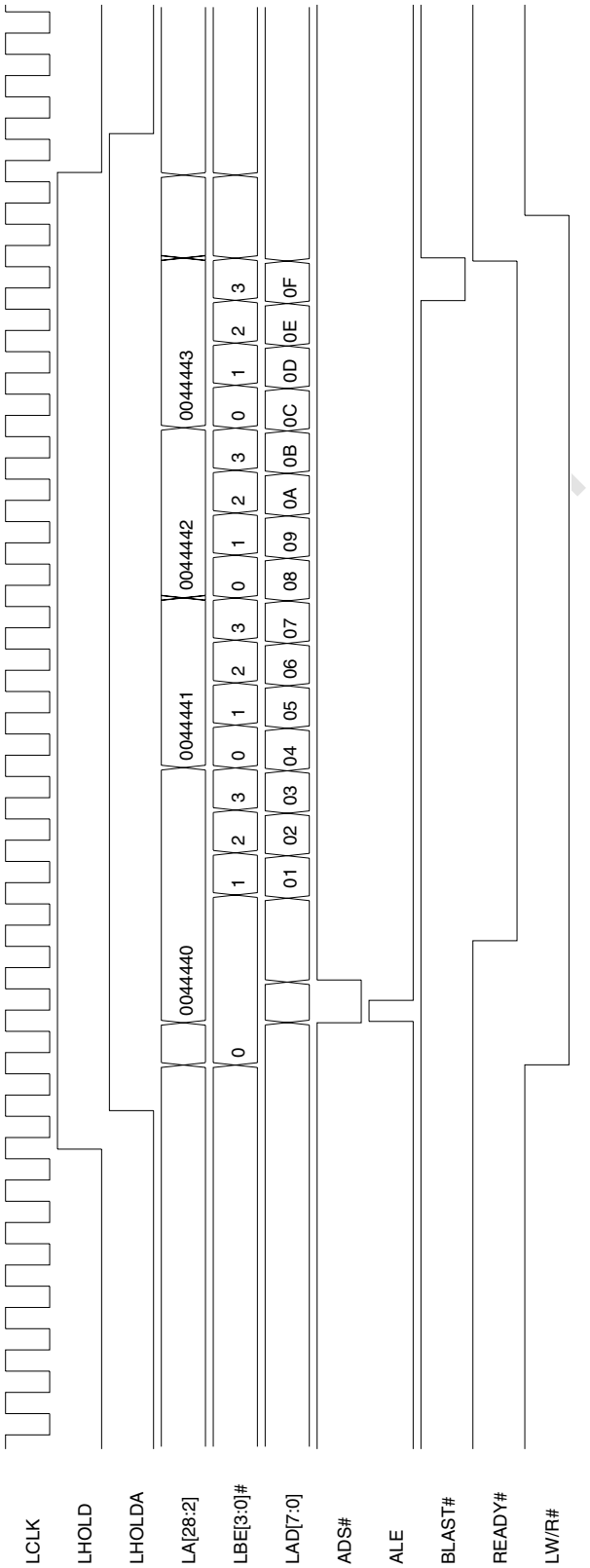
Note: *Key bit/register values are MARBR[24]=1 and LBRD1[15:0]=25C1h.*

Timing Diagram 7-48. Direct Slave Burst Write of 4 Dwords (32-Bit Local Bus)



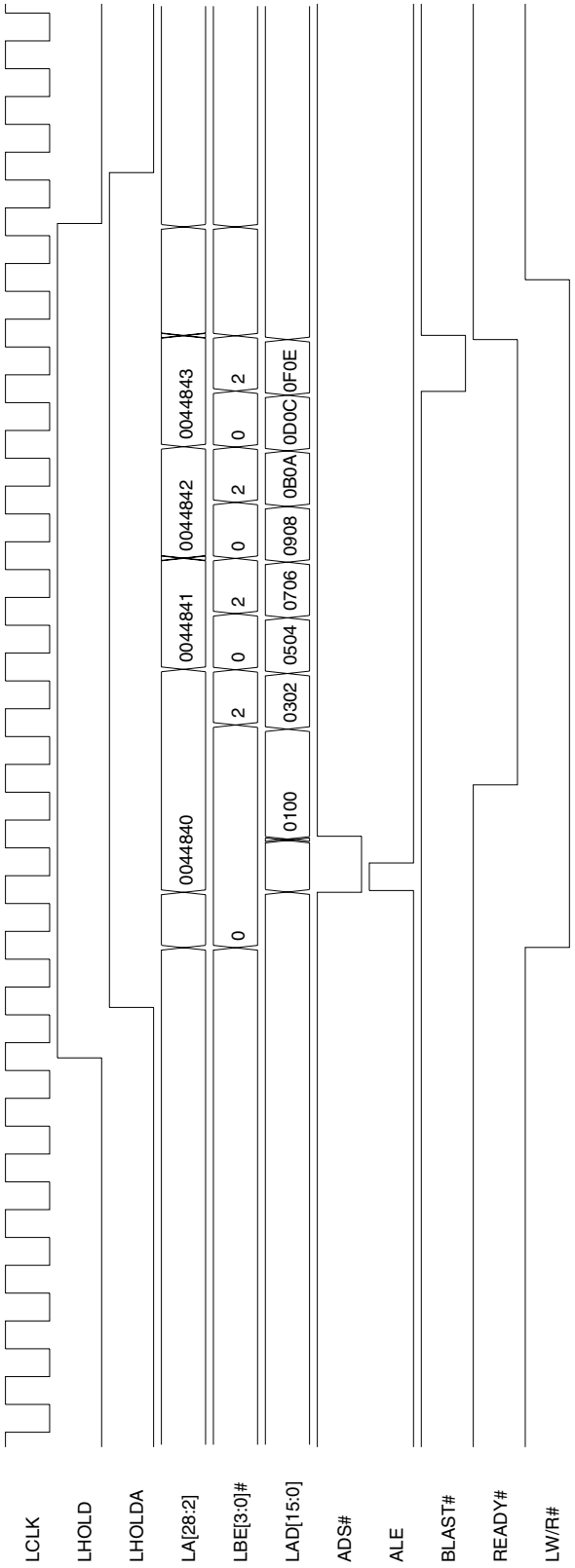
Note: *Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=25C2h.*

Timing Diagram 7-49. Direct Slave Burst Read of 4 Dwords (8-Bit Local Bus)



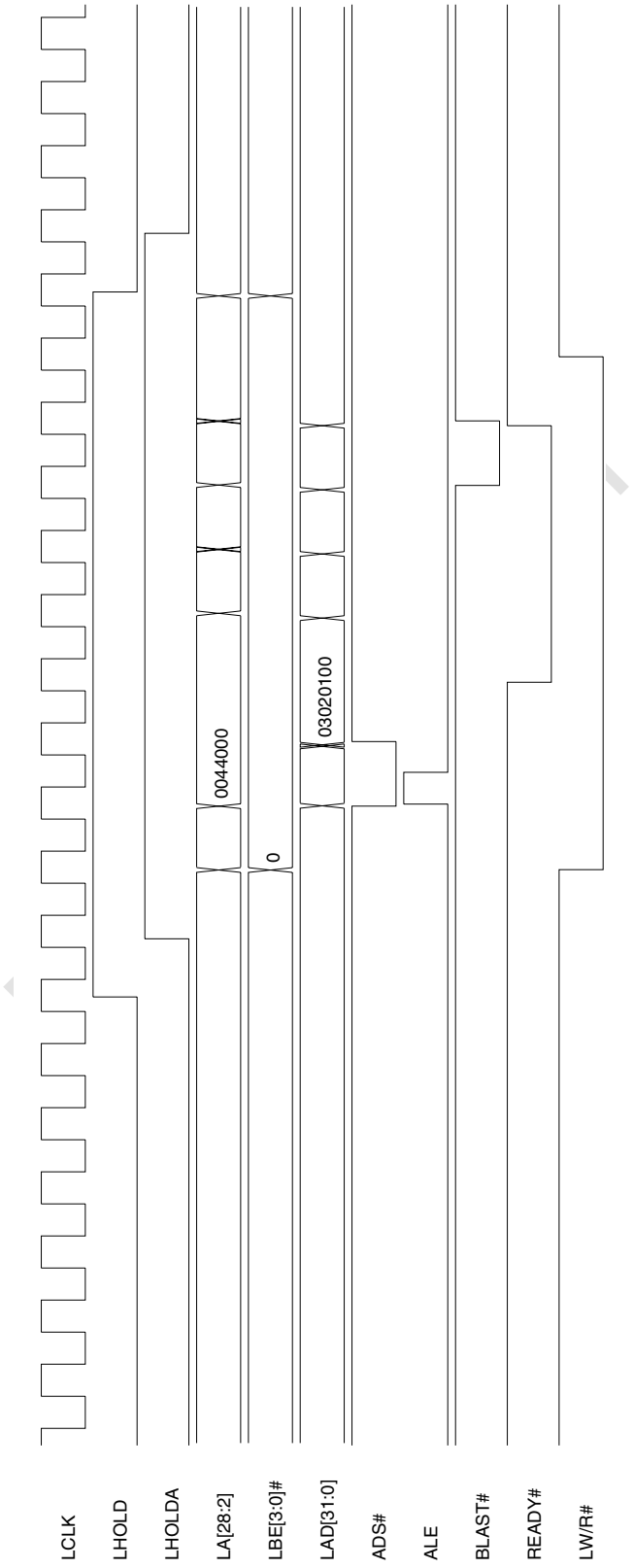
Note: *Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=25C0h.*

Timing Diagram 7-50. Direct Slave Burst Read of 4 Dwords (16-Bit Local Bus)



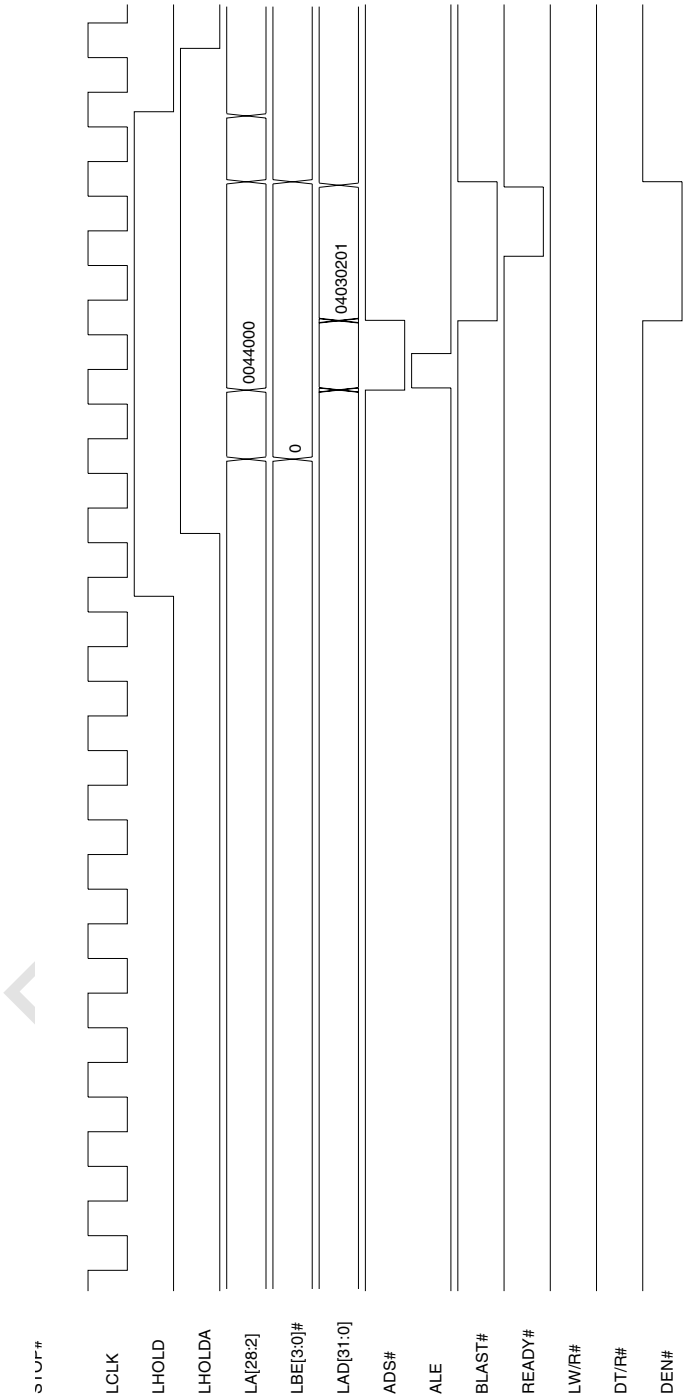
Note: *Key bit/register values are MARBR[24]=1 and LBRD1[15:0]=25C1h.*

Timing Diagram 7-51. Direct Slave Burst Read of 4 Dwords (32-Bit Local Bus)



Note: *Key bit/register values are MARBR[24]=0 and LBRD1[15:0]=25C2h.*

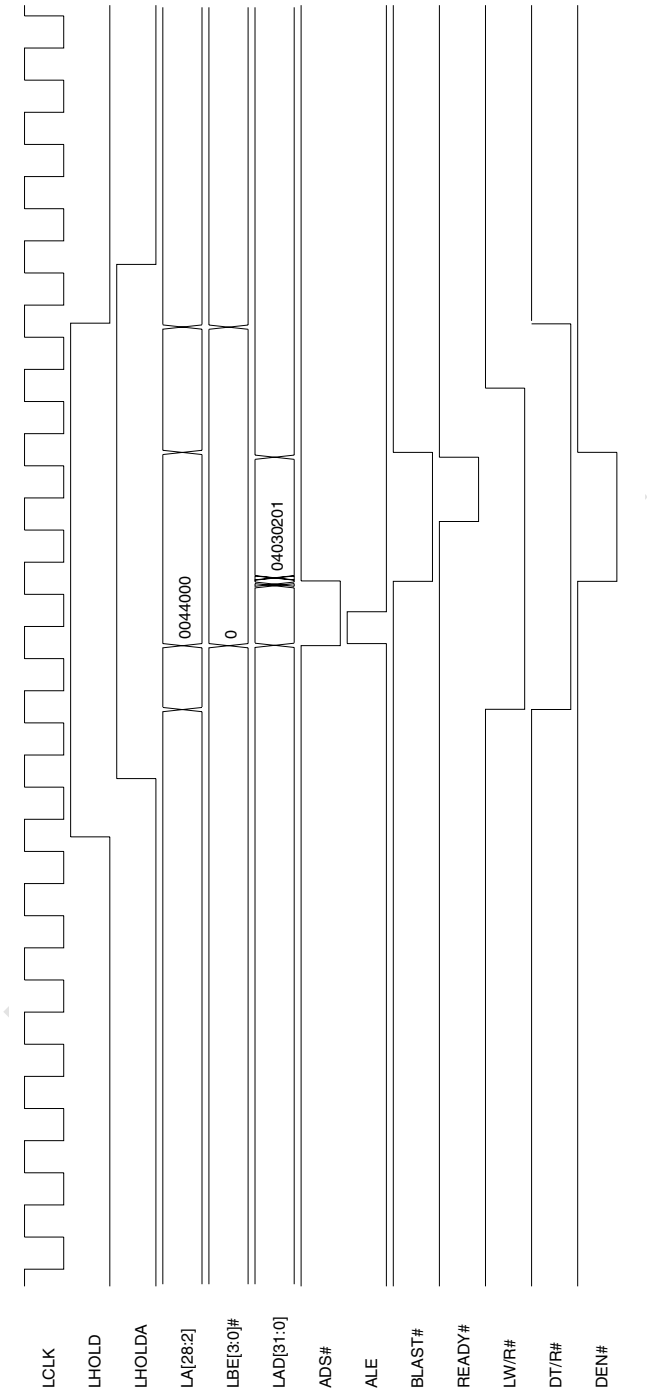
Timing Diagram 7-52. Direct Slave Write with DT/R# and DEN#



Notes: *This single cycle Direct Slave write to a 32-bit Local Bus device/transceivers timing diagram includes the DT/R# and DEN# signals.*

The PEX 8311 always three-states the DT/R# and DEN# signals, except during the time it owns the Local Bus (LHOLD and LHOLDA asserted) to process a Direct Slave or DMA transfer. Because the DT/R# and DEN# signal/pins are pulled up, they are seen as a 1 (high) in this diagram when the PEX 8311 is not driving them. DT/R# and DEN# is OR'ed to create the DIR signal for the transceiver(s).

Timing Diagram 7-53. Direct Slave Read with DT/R# and DEN#

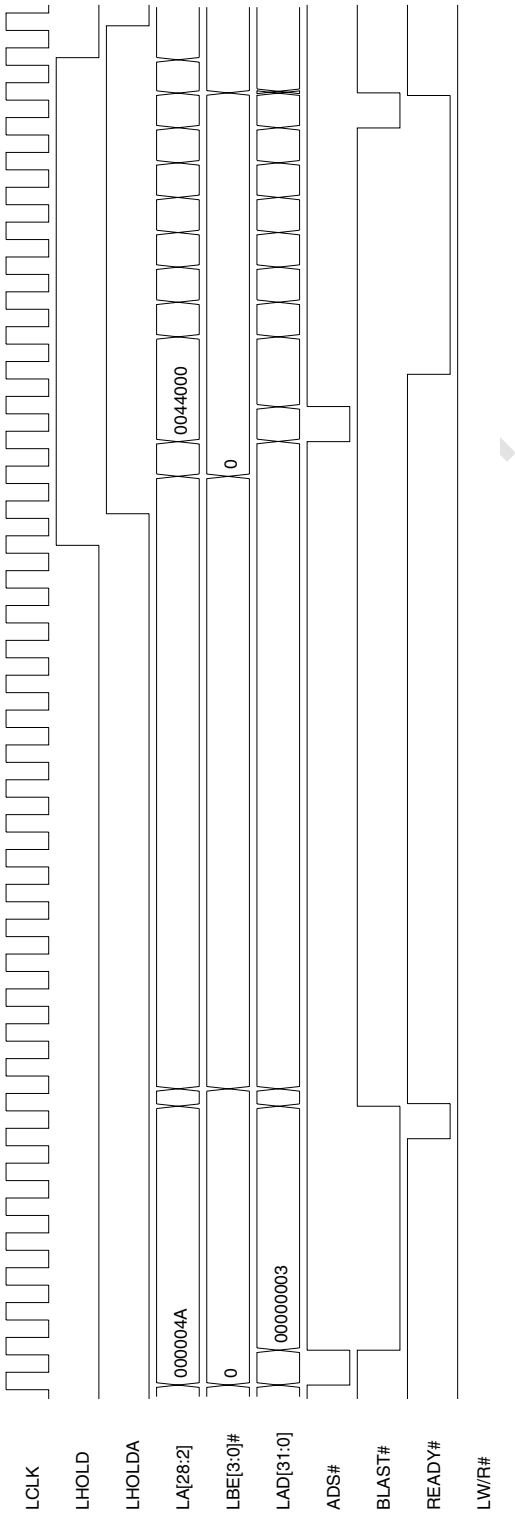


Notes: *This single cycle Direct Slave read from a 32-bit Local Bus device/transceivers timing diagram includes the DT/R# and DEN# signals.*

The PEX 8311 always three-states the DT/R# and DEN# signals, except during the time it owns the Local Bus (LHOLD and LHOLDA asserted) to process a Direct Slave or DMA transfer. Because the DT/R# and DEN# signal/pins are pulled up, they are seen as a 1 (high) in this diagram when the PEX 8311 is not driving them. DT/R# and DEN# is OR'ed to create the DIR signal for the transceiver(s).

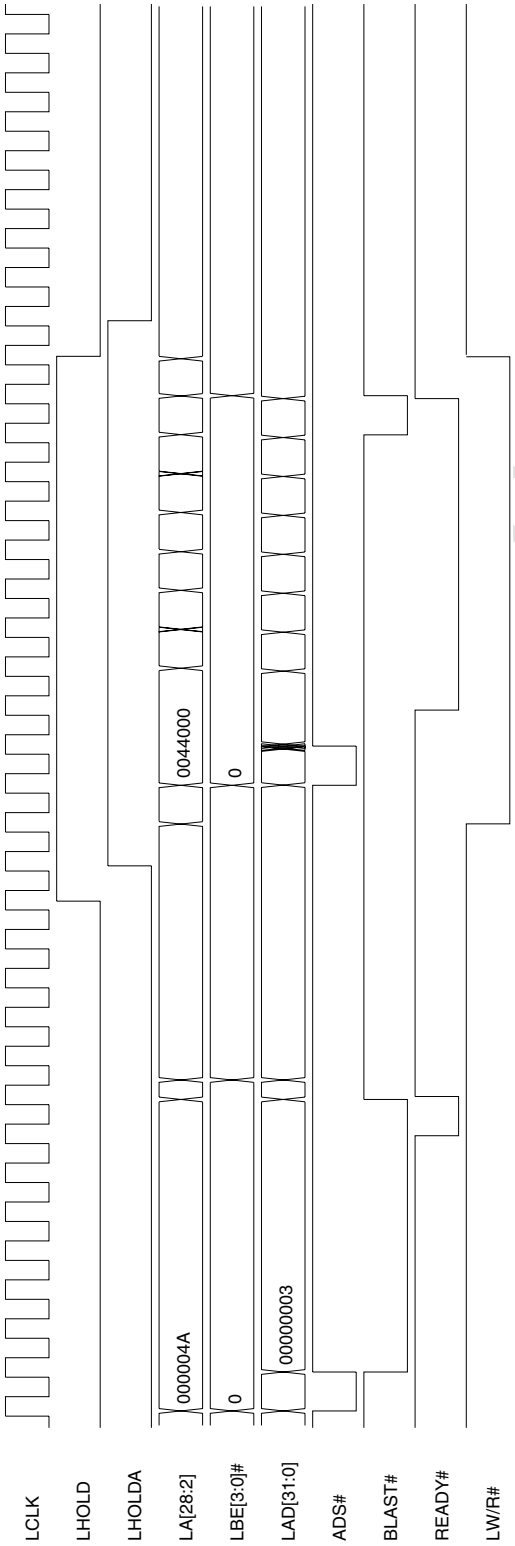
7.4.3.3 J Mode DMA Timing Diagrams

Timing Diagram 7-54. DMA PCI-to-Local (32-Bit Local Bus)



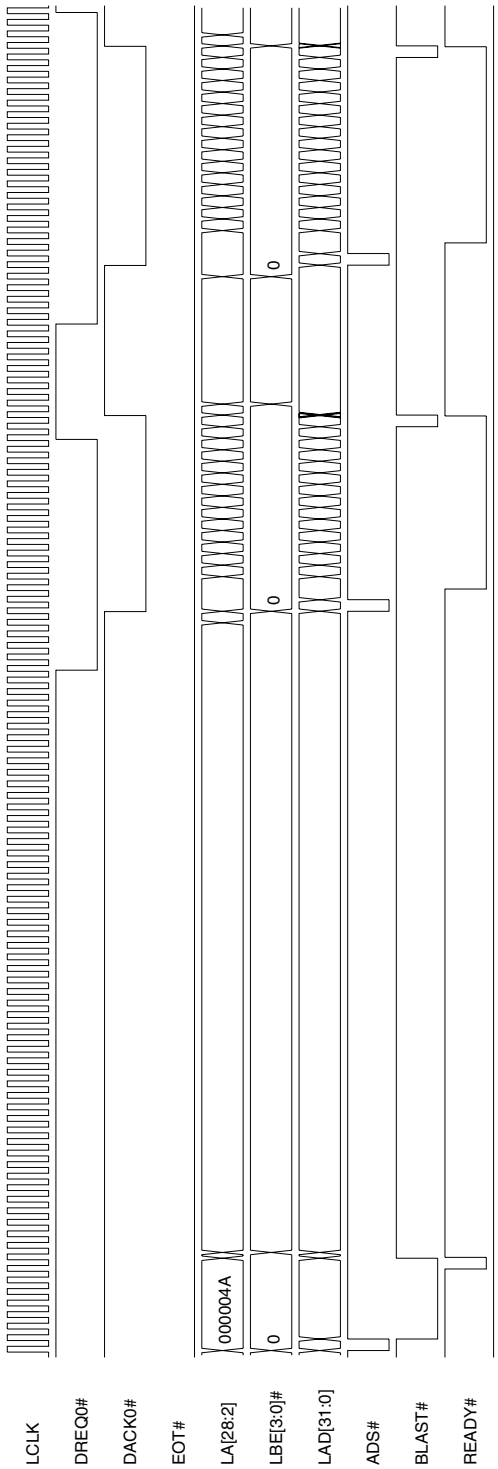
Notes: *The writing of the registers to set up this 32-byte DMA Block mode transfer using DMA Channel 0 is not shown. Writing the DMACSR0 register (LOC:128h) with 03h enables and starts this DMA transfer.*

Timing Diagram 7-55. DMA Local-to-PCI (32-Bit Local Bus)



Notes: *The writing of the registers to set up this 32-byte DMA Block mode transfer using DMA Channel 0 is not shown. Writing the DMACSR0 register (LOC:128h) with 03h enables and starts this DMA transfer.*

Timing Diagram 7-56. DMA PCI-to-Local Demand Mode (32-Bit Local Bus)

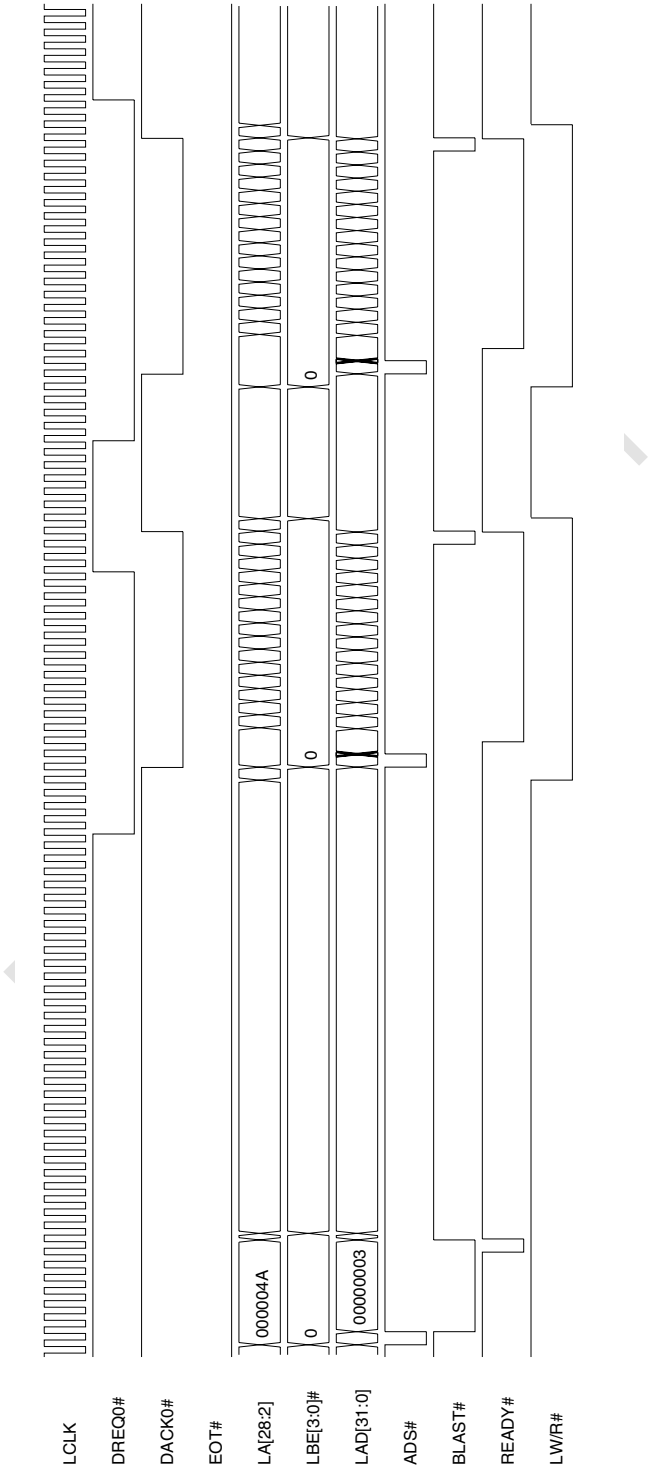


Notes: *The Channel 0 Demand mode DMA transfer starts when the DMACSR0[1:0] bits are written to 11b.*

The PEX 8311 does not attempt to arbitrate for and write data to the Local Bus until it detects the DREQ0# signal asserted.

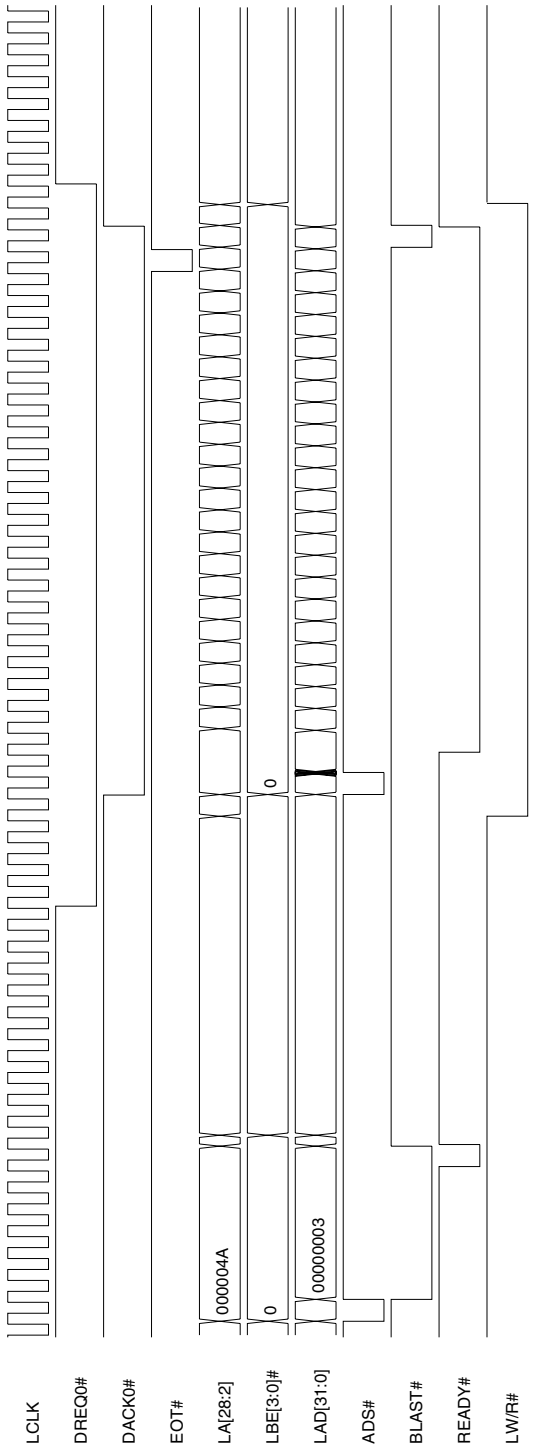
The transfer is temporarily suspended when DREQ0# is de-asserted, then resumed upon its re-assertion.

Timing Diagram 7-57. DMA Local-to-PCI Demand Mode (32-Bit Local Bus)



Note: *The Channel 0 Demand mode DMA transfer starts when the DMACSR0[1:0] bits are written to 11b and the PEX 8311 detects the DREQ0# signal asserted. Once started, the PEX 8311 arbitrates for and reads data from the Local Bus, then writes the data to the internal PCI Bus until the transfer is temporarily suspended when DREQ0# is de-asserted. The transfer resumes upon DREQ0# re-assertion.*

Timing Diagram 7-58. DMA Local-to-PCI Demand Mode with EOT# assertion (32-Bit Local Bus)



Note: *The Channel 0 Demand mode DMA transfer starts when the DMACSR0[1:0] bits are written to 11b and the PEX 8311 detects the DREQ0# signal asserted. Once started, the PEX 8311 arbitrates for and reads data from the Local Bus, then writes the data to the internal PCI Bus until the transfer is terminated with an EOT# assertion. Data read into the DMA FIFO is written to the internal PCI Bus.*

Chapter 8 Direct Data Transfer Modes

8.1 Introduction

The PEX 8311 Local Bus supports three Direct Data Transfer modes:

- **Direct Master** – Local CPU accesses PCI Express memory or I/O
- **Direct Slave** – PCI Express Initiator accesses Local memory or I/O
- **DMA** – PEX 8311 DMA Controller(s) generates Read/Write requests to PCI Express memory to/from Local memory

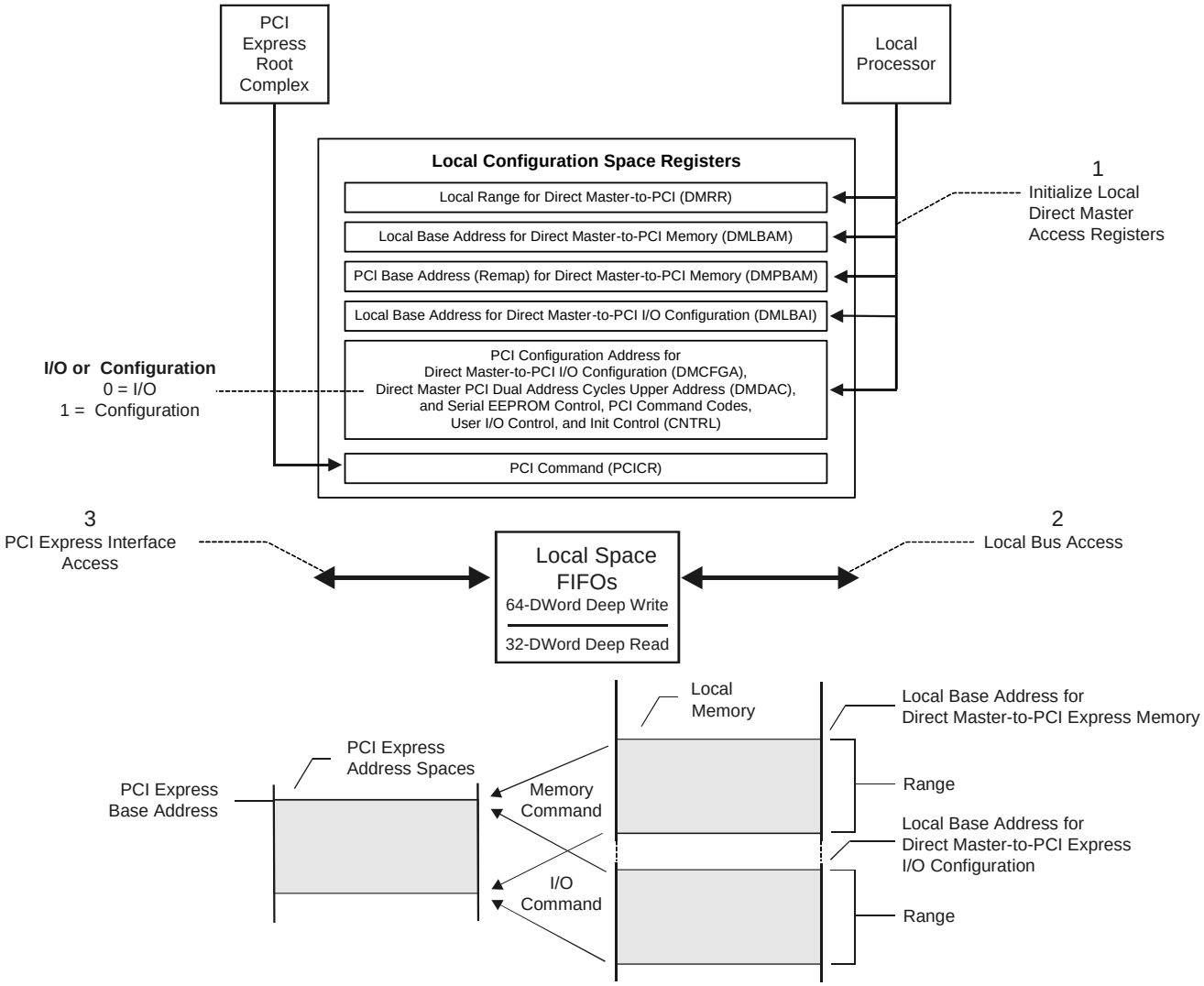
Direct Slave Write Data Transfer mode does not generate dummy cycles. However, in special cases, it passes dummy cycles from the PCI Express interface to the Local Bus. The Local Bus LBE[3:0]# balls must be monitored for dummy cycles to be recognized on the Local Bus because no other Data Transfer modes generate dummy cycles. The PEX 8311 internally suppresses dummy cycles, to avoid generating them on the PCI Express interface and Local Bus.

8.2 Direct Master Operation

The PEX 8311 supports a direct access to the PCI Express interface, the Local processor, or an intelligent controller by mapping Direct Master Memory and/or I/O space to any PCI Express Space described in Chapter 5, "Address Spaces." Master mode must be enabled in the **PCI Command** register (**PCICR**[2]=1) for the Local Bus and PCI Express interface. The following registers define Local-to-PCI accesses (refer to Figure 8-1):

- Direct Master Memory and I/O Range (**DMRR**)
- Local Base Address for Direct Master to PCI Memory (**DMLBAM**)
- Local Base Address for Direct Master to PCI I/O and Configuration (**DMLBAI**)
- PCI Base Address (**DMPBAM**)
- Direct Master Configuration (**DMCFGA**)
- Direct Master PCI Dual Address Cycles (**DMDAC**)
- Master Enable (**PCICR**)
- PCI Command Code (**CNTRL**)

Figure 8-1. Direct Master Access of PCI Express Interface



8.2.1 Direct Master Memory and I/O Decode

The Range register and the Local Base Address specify the Local Address bits to use for decoding a Local-to-PCI Express Space access (Direct Master). The Memory or I/O space range must be a power of 2 and the Range register value must be two's complement of the range value. In addition, the Local Base Address must be a multiple of the range value.

Any Local Master Address starting from the Direct Master Local Base Address (Memory or I/O) to the range value is recognized as a Direct Master access by the PEX 8311. Direct Master cycles are then decoded as Memory, I/O, or Type 0 or Type 1 Configuration to one of the three PCI Express Spaces in the PEX 8311. Moreover, a Direct Master Memory or I/O cycle is remapped according to the Remap register value, which must be a multiple of the Direct Master range value (not the Range register value).

The PEX 8311 can accept Memory cycles only from the Local processor. The Local Base Address and range determine whether Memory or I/O transactions occur to one of the PCI Express Space within the PEX 8311.

8.2.2 Direct Master FIFOs

For Direct Master Memory access to one of the three PCI Express Spaces and then to the PCI Express interface, the PEX 8311 has a 64-Dword (256-byte) Write FIFO and a 32-Dword (128-byte) Read FIFO. Each FIFO is designed such that one FIFO location can store 2 Dwords of data. The FIFOs enable the Local Bus to operate independently with the PEX 8311 PCI Express Spaces and allows high-performance bursting between Direct Master Space and PCI Express Space internally to the PEX 8311, as well as the Local Bus. In a Direct Master Write, the Local processor (Master) writes data to the PCI Express interface. In a Direct Master Read, the Local processor (Master) reads data from the PCI Express interface by issuing a TLP Read request and accepting a completion. Figure 8-2 and Figure 8-3 illustrate the FIFOs that function during a Direct Master Write and Read, respectively.

Figure 8-2. Direct Master Write

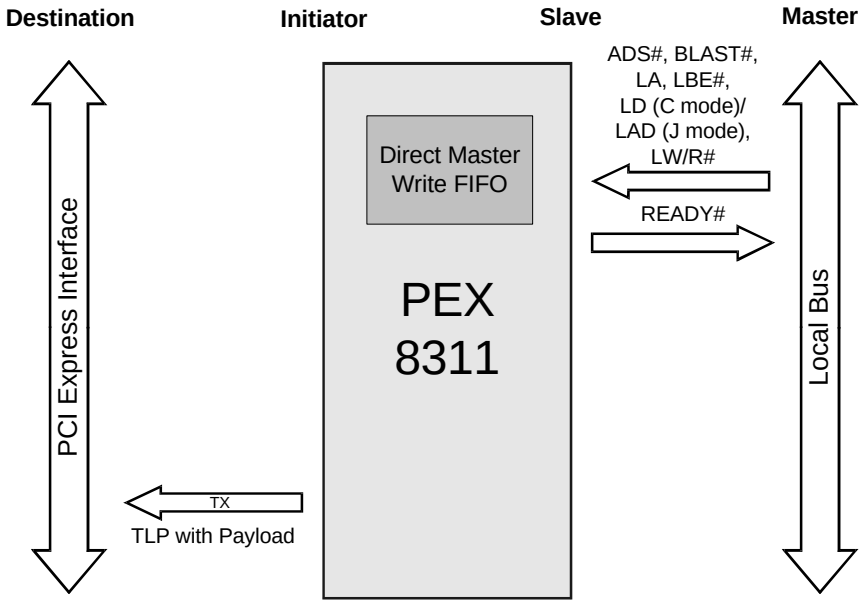
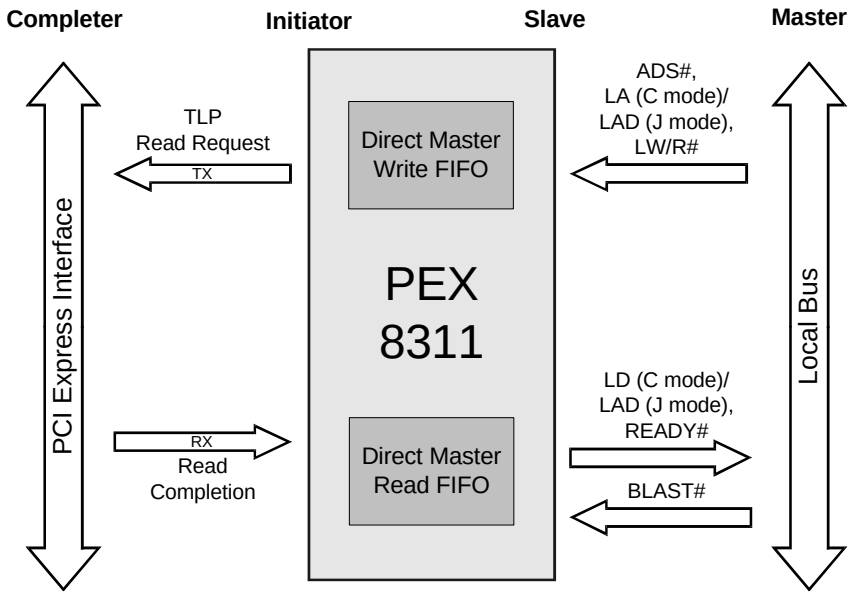


Figure 8-3. Direct Master Read



Note: *Figure 8-2 and Figure 8-3 represent a sequence of Bus cycles.*

8.2.3 Direct Master Memory Access

The Local processor transfers data through a single or Burst Read/Write Memory transaction to one of the PCI Express Spaces within the PEX 8311 and then to the PCI Express interface.

The PEX 8311 converts the parallel Local Read/Write access to serial TLP Read/Write request on to PCI Express interface accesses. The Local Address space starts from the Direct Master Local Base Address up to the range. Remap (PCI Base Address) defines the PCI starting address and PCI Express address.

A Local Bus Processor single cycle causes an internal single cycle transaction to one of the mapped PCI Express Spaces. The PCI Express performs a PCI Express TLP request with single data payload. A Local processor Burst cycle causes an internal burst transaction between Direct Master space and PCI Express Space within the PEX 8311. The PEX 8311 performs Maximum Payload Read/Write request transaction on the PCI Express interface. The PEX 8311 supports continuous Burst transfers.

The Local Bus Processor (a Local Bus Master) initiates transactions when the Memory address on the Local Bus matches the Memory space decoded for Direct Master operations.

8.2.3.1 Direct Master Command Codes to PCI Express Address Spaces

The PEX 8311 becomes an internal bus master to perform Direct Master transfers. The internal command code used by the PEX 8311 during a Direct Master transfer is specified by the value(s) contained in the PEX 8311 **LCS Control** register **CNTRL**[15:0] register bits. Except when in Memory Write and Invalidate (MWI) mode is selected in the PEX 8311 **LCS** registers (**PCICR**[4]=1; **DMPBAM**[9]=1; **PCICLSR**[7:0] = cache line size of 8 or 16 Dwords). In MWI mode for a Direct Master, when the starting address alignment is aligned with the cache line size and upon determining it can transfer at least one cache line of data, the PEX 8311 uses an internal Command Code of Fh, regardless of the **CNTRL**[15:0] register bit values.

For direct Local-to-PCI Express accesses, the PEX 8311 uses the internal commands listed in Table 8-1 through Table 8-3.

Table 8-1. Local-to-PCI Express Memory I/O or Prefetchable Address Spaces Access

Command Type	Code (C/BE[3:0]#)
Memory Read	0110b (6h)
Memory Write	0111b (7h)
Memory Read Multiple	1100b (Ch)
Dual Address Cycle	1101b (Dh)
Memory Read Line	1110b (Eh)
Memory Write and Invalidate	1111b (Fh)

Table 8-2. Local-to-PCI Express I/O Address Space Access

Command Type	Code (C/BE[3:0]#)
I/O Read	0010b (2h)
I/O Write	0011b (3h)

Table 8-3. Local-to-PCI Express I/O-Mapped Configuration Access

Command Type	Code (C/BE[3:0]#)
Configuration Memory Read	1010b (Ah)
Configuration Memory Write	1011b (Bh)

8.2.3.2 Direct Master Writes

For a Local Bus write, the Local Bus Master writes data to the Direct Master Write FIFO. When the first data is in the FIFO, the PEX 8311 internally arbitrates for the PCI Express Space, and writes its data. The PEX 8311 generates a PCI Express TLP Write request and transfers the data on the PCI Express link to its destination. The PEX 8311 continues to accept writes and returns READY# until the Direct Master Write FIFO is full. It then holds READY# de-asserted until space becomes available in the Direct Master Write FIFO. A programmable Direct Master "almost full" status output is provided (DMPAF signal). (Refer to DMPBAM[10, 8:5].)

Local Bus processor single cycle Write transactions result in PEX 8311 transfers of 1 Dword of payload to the PCI Express interface.

A Local processor, with no burst limitations and a Burst cycle Write transaction of 2 Dwords, causes the PEX 8311 to perform two single writes internally into the PCI Express Space when the Local Bus starting address is X0h or X8h. The same type of transfer with a Local Bus starting address of X4h or XCh results in a 2-Dword burst to the PCI Express Space within the PEX 8311. Three (or more) Dwords at any Dword address, with Burst cycles of any type, result in the PEX 8311 bursting data onto the PCI Express Space within the PEX 8311. The PEX 8311 generates a PCI Express TLP Write request for each Direct Master Write entered the PCI Express Space to the PCI Express interface.

8.2.3.3 Direct Master Reads

For a Local Bus read, the PEX 8311 arbitrates for the PCI Express Space, and writes a read address directly into it. The PEX 8311 generates a PCI Express TLP Read request and as Read Completion returns the PEX 8311 accepts it and directly writes the data into the Direct Master Read FIFO, through one of the PCI Express Spaces. The PEX 8311 asserts Local Bus READY# to indicate that the requested data is on the Local Bus.

The PEX 8311 holds READY# de-asserted while read data is not available from its source, PCI Express device or PEX 8311's PCI Express Space. Programmable prefetch modes are available for Direct Master have an efficient data transfer from the PCI Express Space into the Direct Master Read FIFO, when prefetch is enabled – prefetch, 4, 8, 16, or continuous data – until the Direct Master cycle ends. The Read cycle is terminated when Local BLAST# input is asserted. Unused Read data is flushed from the FIFO.

The PEX 8311 prefetch mechanism has no effect for single cycle (Local BLAST# input is asserted during the clock following ADS#) Direct Master reads unless Read Ahead mode is enabled and prefetch length is set to continuous (DMPBAM[2, 11]=10b, respectively). (Refer to Section 8.2.6 for details on Read Ahead mode.) For single cycle Direct Master reads (Read Ahead mode disabled, DMPBAM[2]=0), the PEX 8311 requests 1 Dword Read request on the PCI Express interface.

For single cycle Direct Master reads, the PEX 8311 passes the Local Byte Enables (LBE[3:0]#) to the PCI Express Space within the PEX 8311 to read only the bytes requested by the Local Master device. The PEX 8311 generates a PCI Express TLP Read request, with the byte field indicating the bytes required by the Local Master device.

For Burst Cycle reads, the PEX 8311 reads entire Dwords (all Byte Enables are asserted) within the PEX 8311, regardless of whether the Local Byte Enables are contiguous. The PEX 8311 generates a PCI Express TLP Read request with byte field of 1, indicating the Read request is contiguous, except for the first and the last data when Local Bus read is unaligned.

When the Direct Master Prefetch Limit bit is enabled (DMPBAM[11]=1), the PEX 8311 terminates a Read prefetch at 4-KB boundaries internally between Direct Master and PCI Express Space, and restarts it as a new Read Prefetch cycle at the start of a new boundary. If the bit is disabled (DMPBAM[11]=0), the Direct Master read prefetch crosses the PCI Express Space 4-KB boundaries. PCI Express does not allow the cross of 4-KB boundary; therefore, the PEX 8311 generates at least two individual PCI Express TLP Read requests for data before a 4-KB and after 4-KB boundary.

When the 4-KB Prefetch Limit bit is enabled, and the PEX 8311 started a Direct Master read to the PCI Express interface Address FF8h (2 Dwords before the 4-KB boundary), the PEX 8311 does ***not*** internally perform a Burst prefetch of 2 Dwords. The PEX 8311 instead performs an internal prefetch of two single cycle Dwords between Direct Master and PCI Express Space, to prevent crossing the PCI Express Space 4-KB boundary limit. The cycle then continues by starting at the new boundary.

8.2.4 Direct Master I/O

The main purpose of the Direct Master I/O space is for the Local Bus Master (Intelligent device) to generate Type 0 Configuration accesses to access the **PECS** registers and to generate Type 1 Configuration accesses to the PCI Express downstream devices. Type 0 and Type 1 Configuration accesses can only be generated by upstream devices (*that is*, this feature is used only when the PEX 8311 is in Root Complex mode).

Direct Master I/O space can also be used to generate I/O-Mapped transactions to the PEX 8311's Address space, which then is used to generate I/O transactions on the PCI Express interface. Refer to Section 9.4.2.1, "Direct Master Configuration (PCI Type 0 or Type 1 Configuration Cycles)," for detailed descriptions of Type 0 and Type 1 Configuration accesses generation.

When the Configuration Enable bit is cleared (DMCFGA[31]=0), a single I/O access is made to the internal PCI Express Space within the PEX 8311. The *Local Address, Remapped Decode Address* bits, and *Local Byte Enables* are encoded to provide the address and are output with an I/O Read or Write command during a PCI Address cycle. When the Configuration Enable bit is set (DMCFGA[31]=1), the cycle becomes a Type 0 or Type 1 PCI Configuration cycle. (Refer to Section 9.4.2.1, "Direct Master Configuration (PCI Type 0 or Type 1 Configuration Cycles)," and the **DMCFGA** register for details.)

When the I/O Remap Select bit is set (DMPBAM[13]=1), the Address bits [31:16] (when internally accessing PCI Express Space from within the PEX 8311) are forced to 0 for the 64-KB I/O Address limit. When the I/O Remap Select bit is cleared (DMPBAM[13]=0), DMPBAM[31:16] are used as the remap addresses for the PCI Express Space accesses.

For writes, data is loaded into the Direct Master Write FIFO and READY# is returned to the Local Bus. For reads, the PEX 8311 holds READY# de-asserted while receiving a Dword from the PCI Express interface.

Local Burst accesses are internally broken into single I/O (Address/Data) cycles when accessing PCI Express Space. The PEX 8311 does not prefetch Read data for I/O and Configuration reads.

For Direct Master I/O and Configuration cycles, the PEX 8311 internally passes Local Byte Enables to the PCI Express Space, which are then used to generate PCI Express TLP requests with exact byte fields required by the Local Bus Master.

8.2.5 Direct Master Delayed Write Mode

The PEX 8311 supports Direct Master Delayed Write mode transactions, in which Posted Write data accumulates in the Direct Master Write FIFO before the PEX 8311 internally requests arbitration to the PCI Express Space. Direct Master Delayed Write mode is programmable to delay the internal arbitration for the number of internal clocks selected in DMPBAM[15:14]. This feature is useful for gaining higher throughput during Direct Master Write Burst transactions for conditions in which the Local clock frequency is slower than the internal clock frequency, as well as for the PEX 8311 PCI Express interface to collect sufficient data to generate a PCI Express TLP Write request with Maximum Payload Size.

The PEX 8311 only utilizes the Delay Counter and accumulates data in the Direct Master Write FIFO for Burst transactions on the Local Bus. A single cycle write on the Local Bus immediately starts the internal arbitration to the PCI Express Space (ignores delay setting).

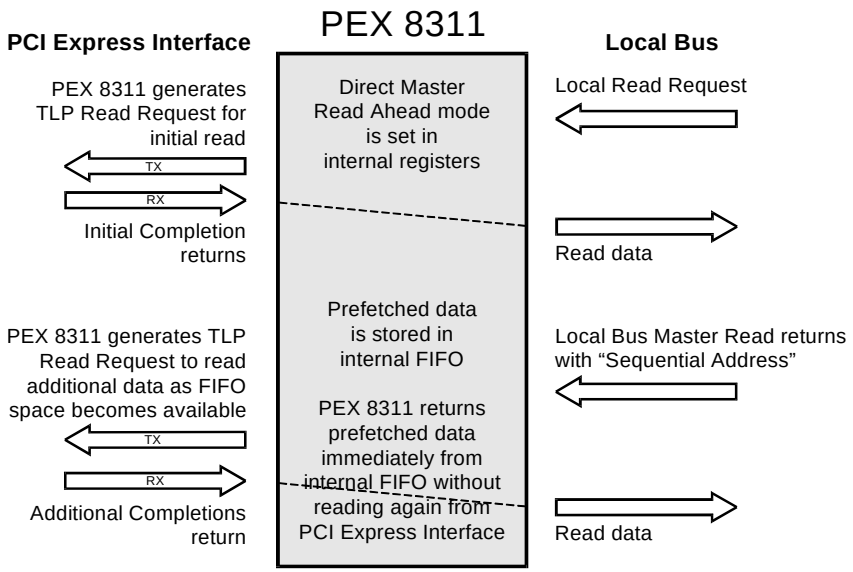
8.2.6 Direct Master Read Ahead Mode

The PEX 8311 only supports Direct Master Read Ahead mode (DMPBAM[2]=1) when the Direct Master Read Prefetch Size Control bits are set to continuous prefetch (DMPBAM[12, 3]=00b). Other Direct Master Read Prefetch Size Control bit settings turn off Direct Master Read Ahead mode. Direct Master Read Ahead mode allows prefetched data to be read from the PEX 8311 internal FIFO instead of the PCI Express interface. The address must be contiguous to the previous address and Dword-aligned (next address = current address + 4). Direct Master Read Ahead mode functions is used with or without Direct Master Delayed Read mode.

A Local Bus single cycle Direct Master transaction, with Direct Master Read Ahead mode enabled results in the PEX 8311 processing continuous PCI Express TLP Read request generation to stay ahead of what the Local Bus Master is reading, when the Direct Master Read Prefetch Size Control bits are set to continuous prefetch (DMPBAM[12, 3]=00b). (Refer to Figure 8-4.)

Caution: *To prevent constant locking of the internal interface between Direct Master and PCI Express Spaces, do* ***not*** *simultaneously enable Direct Master Read Ahead and Direct Master PCI Read modes (DMPBAM[2, 4]≠11b, respectively).*

Figure 8-4. Direct Master Read Ahead Mode



Note: *Figure 8-4 represents a sequence of Bus cycles.*

Table 8-4. Example of PCI Express Behavior with Direct Master Read Ahead Mode Enabled

Direct Master Local Bus Cycle to PEX 8311	Direct Master PCI Express Interface Behavior with Direct Master Read Prefetch Size Control Bits Not Set to Continuous Prefetch (DMPBAM[12, 3]≠00b)	Direct Master PCI Express Interface Behavior with Direct Master Read Prefetch Size Control Bits Set to Continuous Prefetch (DMPBAM[12, 3]=00b)
Single cycle read followed by single cycle read	Two individual PCI Express TLP Dword Read request generation	Single PCI Express TLP Read request generation with Maximum Read payload
Single cycle read followed by consecutive address Burst Read cycle	Single PCI Express TLP Dword Read request generation followed by another PCI Express TLP Read request generation with Maximum Read payload	Single PCI Express TLP Read request generation with Maximum Read payload followed by another Single PCI Express TLP Read request generation for additional data with Read Ahead
Burst cycle read of four Data cycles, followed by consecutive address Burst cycle read of four Data cycles	Two individual PCI Express TLP Read requests are generated for each Local Bus Read cycle	Single PCI Express TLP Read request generation with Maximum Read payload followed by another PCI Express Read request with Maximum Read payload when additional data is required
Burst cycle read of four Data cycles, followed by consecutive address single cycle read	Single PCI Express TLP Read request generation with Maximum payload followed by another PCI Express TLP Dword Read request generation	Single PCI Express TLP Read request generation with Maximum Read payload followed by another PCI Express Read request with Maximum Read payload when additional data is required

8.2.7 Direct Master PCI Express Long Address Format

The PEX 8311 supports Long Address Format generation, a 64-bit addressing to access devices located above the 4-GB Address Boundary space by utilizing Direct Master Dual Address Cycle (DAC) register (**DMDAC**) for Direct Master transactions. The Direct Master space must be mapped to PCI Express Prefetchable space and the DMDAC register must be programmed to a non-zero value for 64-bit addressing to occur on the PCI Express interface. (Refer to Section 5.4.3, "64-Bit Addressing," for further details.) When the DMDAC register contains a value of 0h (feature enabled when DMDAC register value is ***not*** 0h), the PEX 8311 performs a Short Address Format on the PCI Express interface.

8.2.8 Internal Interface Master/Target Abort

This section describes how the PEX 8311 logic handles internal Master/Target Aborts between Local and PCI Express Spaces, as well as Unsupported requests and Completion Aborts received on the PCI Express interface.

For accesses originated on the Local Bus by the Local Bus Master to the PEX 8311 Local Bus Spaces that are incorrectly mapped to the PEX 8311 PCI Express Spaces result in Master Aborts. As the result, the PEX 8311 Local Bus logic sets the Received Master Abort in the PCI Status (**PCISR**) register. The Local Bus Master must clear the Received Master Abort bit (**PCISR**[13]=0) and continue by processing the next task.

When internal to the PEX 8311, a Master/Target Abort or 256 consecutive Master Retry timeout to the PCI Express Address spaces is encountered during a transfer, the PEX 8311 asserts LSERR#, when enabled [**INTCSR**[0]=1, which is used as a Non-Maskable Interrupt (NMI)]. (Refer to Chapter 10, "Error Handling," for LSERR# usage model.)

When Direct Master writes are posted and internal to the PEX 8311 Master/Target Abort occurs, this causes LSERR# assertion, when enabled (**INTCSR**[0]=1). When a Local Bus Master is waiting for READY#, it is asserted along with BTERM# only for Direct Master Read operations. The Local Bus Master's interrupt handler can take the appropriate application-specific action. It can then clear the internal Received Master or Target Abort bit (**PCISR**[13 or 12]=1, respectively; writing 1 clears the bit to 0) to de-assert the LSERR# interrupt and re-enable Direct Master transfers.

When internal to the PEX 8311 Master/Target Abort or Retry Timeout is encountered during a Direct Master transfer with multiple Direct Master operations posted in the Direct Master Write FIFO (*for example*, an address, followed by data, followed by another address, followed by data) the PEX 8311 flushes the entire Direct Master Write FIFO when Direct Master Write FIFO Flush during an internal Master Abort is enabled (LMISC1[3]=1). When the bit is disabled (**LMISC1**[3]=0), the PEX 8311 flushes only the aborted Direct Master operation in the Direct Master Write FIFO and skips to the next available address in the FIFO entry. The PEX 8311 does not perform internal arbitration to the PEX 8311 PCI Express Address spaces until the internal Received Master/Target Abort bits are cleared (**PCISR**[13:12]=00b, respectively).

When a Local Bus Master is attempting a Burst read to the PEX 8311 PCI Express Address space that is not responding (internal Master/Target Abort), it receives READY# and BTERM# until the Local Bus completes a transfer. In addition, the PEX 8311 asserts LSERR# when **INTCSR**[1:0]=11b (which is used as an NMI). When the Local processor cannot terminate its Burst cycle, it can cause the Local processor to hang. The Local Bus must then be reset from the PCI Express interface. Ensure that when a Local Bus Master cannot terminate its cycle with BTERM# output, it does ***not*** perform Burst cycles when attempting to determine whether the PEX 8311 exists on the PCI Express interface.

When internal to the PEX 8311, a Master/Target Abort is encountered during a Direct Master transfer to the PEX 8311 PCI Express Address space, the PEX 8311 stores the Abort address into **PABTADR**[31:0] and sets the internal Received Master/Target Abort bits (**PCISR**[13:12]=11b, respectively). The PEX 8311 disables internal accesses to the PCI Express Address spaces within the PEX 8311 when **PCISR**[13:12]=11b. Therefore, in this condition, the PEX 8311 does not perform internal arbitrations to the PCI Express Address Spaces to execute new or pending Direct Master or DMA transfers. Read the internal Received Master/Target Abort bits and clear before starting new Direct Master or DMA transfers. The Abort Address register bits (**PABTADR**[31:0]) contents are updated for each Master/Target Abort. (For details about DMA internal Master/Target Abort, refer to Section 8.5.17.)

The PEX 8311 internal Master/Target Abort logic is used by a Local Bus Master to perform a Direct Master Bus poll of devices, to determine whether devices exist (typically when the Local Bus performs Configuration cycles to the PCI Express interface, in Root Complex mode only).

8.2.9 Direct Master Memory Write and Invalidate

The PEX 8311 can be programmed to perform Memory Write and Invalidate (MWI) cycles internally between Direct Master and PCI Express Address spaces. The PEX 8311 supports generating internal MWI transfers for cache line sizes of 8 or 16 Dwords. Size is specified in the System Cache Line Size bits (**PCICLSR**[7:0]) Local Configuration registers. When a size other than 8 or 16 is specified, the PEX 8311 performs internal Write transfers (using the command code programmed in **CNTRL**[7:4]) rather than MWI transfers. Internal MWI accesses to the PCI Express Spaces do not affect PEX 8311 TLP Write request generation and performance on the PCI Express interface.

Direct Master MWI transfers are enabled when the MWI Mode and MWI Enable bits are set (**DMPBAM**[9]=1 and **PCICR**[4]=1, respectively).

In MWI mode, when the start address of the Direct Master transfer is on a cache line boundary, the PEX 8311 waits until the number of Dwords required for the specified cache line size are written from the Local Bus before starting an internal MWI access to PCI Express Address Space. This ensures a complete cache line write can complete in one internal write cycle.

When the start address is not on a cache line boundary, the PEX 8311 defaults an internal Write access using the command codes from the **CNTRL**[15:12] bits, and the PEX 8311 does not terminate a non-MWI Write at an MWI cache boundary. The non-MWI Write transfer continues until the Data transfer is complete. When PCI Express Address Space disconnects before a cache line is completed, the PEX 8311 completes the remainder of that cache line, using non-MWI Writes.

When the Direct Master write is less than the cache line size, the PEX 8311 waits until the next Direct Master write begins before starting an internal arbitration to the PCI Express Address Space. The internal write retains the MWI command, regardless of the number of Dwords in the Direct Master Write FIFO, which can result in internal write completing an MWI cycle with less than a cache line of data. For this reason, ensure that Burst writes are equal to, or multiples of, the cache line size.

8.2.10 Direct Master Write FIFO Programmable Almost Full, DMPAF Flag

The PEX 8311 supports the Direct Master Write FIFO Programmable Full Flag (**DMPBAM**[10, 8:5]. The DMPAF signal is used as a hardware indicator Direct Master Write FIFO Full Flag. An alternative method (software polling a register bit) is also provided to check the Direct Master Write FIFO Full Status Flag (**MARBR**[30]). To enable DMPAF signal functionality and disable EOT#, clear the DMA EOT# Enable bit(s) to 0 (**DMAMODE*x***[14]=0; default configuration).

DMPAF output assertion relies on the programmable value in **DMPBAM**[10, 8:5] to determine when to signal that the Direct Master Write FIFO is almost full. After DMPAF assertion, the PEX 8311 de-asserts DMPAF upon the last word of the transfer entering into the internal PCI Data Out Holding latch before entering the PCI Express Address space within the PEX 8311. The DMPAF signal indicates the Direct Master Write FIFO status, ***not*** transfer status completion.

8.3 Direct Slave Operation

For Direct Slave writes, the PCI Express interface writes data to the Local Bus. Direct Slave is Write/Read requests that are initiated from the PCI Express interface, with the highest priority.

For Direct Slave reads, the PCI Express device initiates Read requests to the PEX 8311. The PEX 8311 arbitrates on the Local Bus and becomes the Local Bus Master. The PEX 8311 reads data from the Local Bus Slave into the Direct Slave Read FIFO and transfers it to the PCI Express Address Space. The PEX 8311 returns the data to the PCI Express Read requester by way of initiating PCI Express Read Completion. Direct Slave or Direct Master preempts DMA; however, Direct Slave does ***not*** preempt Direct Master on the Local Bus. (Refer to Section 8.3.9.)

The PEX 8311 supports Burst Memory-Mapped Transfer accesses and I/O-Mapped, Single-Transfer PCI Express-to-Local Bus accesses through a 32-Dword (128-byte) Direct Slave Read FIFO and a 64-Dword (256-byte) Direct Slave Write FIFO on the Local Bus. The PCI Base Address registers on the PEX 8311 Local Bus are provided to set the adapter location in respect to the PCI Express Address spaces as either Memory- or I/O-Mapped space. In addition, Local mapping registers allow Address Translation from the PCI Express Address space to the Local Address space.

Three Local Address Spaces are available:

- Space 0
- Space 1
- Expansion ROM[1] (Expansion ROM is intended to support a bootable Host ROM device)

Direct Slave supports on-the-fly Local Bus Endian conversion for Space 0, Space 1, and Expansion ROM space.

Each Local space is programmed to operate with an 8-, 16-, or 32-bit Local Bus data width. The PEX 8311 includes an internal wait state generator and READY# input signal that is used to externally assert wait states. READY# is selectively enabled or disabled for each Local Address Space (**LBRD0**[6] for Space 0, **LBRD1**[6] for Space 1, and/or **LBRD0**[22] for Expansion ROM).

Independent of the PCI Express interface, the Local Bus can perform:

- Bursts when data is available (Continuous Burst mode)
- Bursts of 4 Dwords, words, or bytes at a time (Burst4 mode, recommended)
- Continuous single cycles (default)

1. Expansion ROM is not restricted to ROM devices. It is used as another Memory-Mapped space to the Local Bus devices.

The Direct Slave Retry Delay Clock bits (LBRD0[31:28] is used to program the period of time in which the PEX 8311 internally holds PCI Express Address space accesses in a wait state (TRDY# de-asserted). The PEX 8311 internally issues a Retry to the PCI Express Address Space Transaction when the programmed time period expires. This occurs when the PEX 8311 cannot gain control of the Local Bus and accept more data from the PCI Express Address space within the programmed time period (assert TRDY#).

8.3.1 Direct Slave Writes

For a PCI Express interface Write, the PCI Express device initiates a Write request and writes data to the PEX 8311 PCI Express Address Space. Internally, within the PEX 8311 the PCI Express Address Space arbitrates to complete the Direct Slave Write transfer by transferring payload data to the Direct Slave Write FIFO. When the first data is in the FIFO, the PEX 8311 arbitrates for the Local Bus, becomes the Local Bus Master, and writes data to a Local slave device. The PEX 8311 continues to accept writes internally until the Direct Slave Write FIFO is full. It then issues internal wait states (holds TRDY# de-asserted) between PCI Express and Local Bus Address spaces until space becomes available in the Direct Slave Write FIFO, or issues a Retry to the PCI Express Address space (asserts STOP# and internally Retries the Direct Slave Write transaction), dependent upon the LBRD0[27] register bit setting.

A PCI Express single data (1-Dword) cycle Write transaction results in a PEX 8311 transfer of 1 Dword of data onto the Local Bus. A PCI Express multiple Data (2 or more Dwords) cycle results in a PEX 8311 Burst transfer of multiple data (2 or more Dwords) onto the Local Bus, when the Burst bit(s) is enabled (LBRD0[24]=1 for Space 0, LBRD1[8]=1 for Space 1, and/or LBRD0[26]=1 for Expansion ROM).

The PEX 8311 can be programmed to place PCI Express Address Space accesses into internal wait states (de-asserting TRDY#), when the Direct Slave Write FIFO becomes full on the PEX 8311 Local Bus. The PEX 8311 can also be programmed to retain the Local Bus and continue asserting LHOLD, when the Direct Slave Write FIFO becomes empty. If the Local Bus Latency Timer is enabled (MARBR[16]=1) and expires (MARBR[7:0]), the Local Bus is dropped.

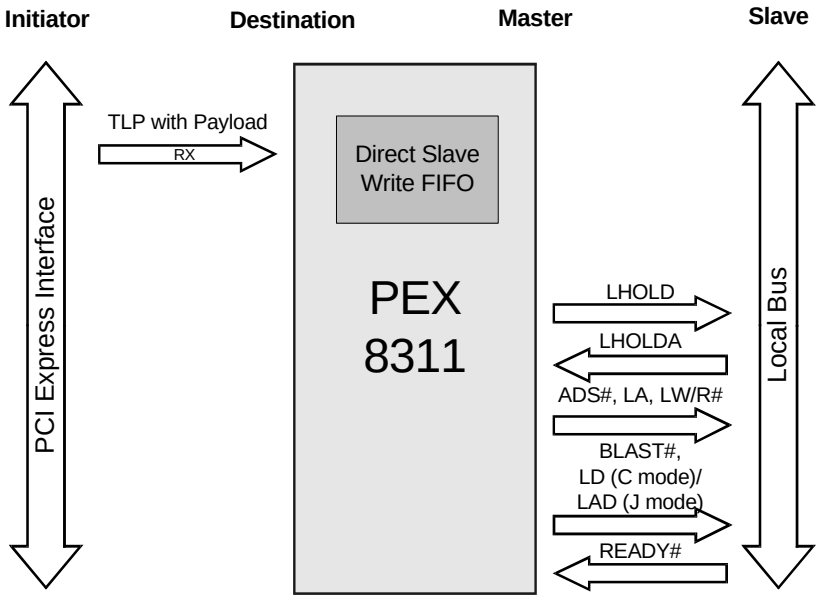
A continues Write cycle (multiple Dwords in one payload) from the PCI Express interface through the PEX 8311 performs a Local Bus Burst transaction, when the following conditions are true:

- The address is Dword-aligned,
- The Direct Slave Write FIFO contains at least 2 Dwords, and
- The PCI Express single payload contains contiguous data. Default by the *PCI Express Base 1.0a*.

The PEX 8311 transfers dummy data by way of a dummy cycle, with LBE[3:0]#=Fh when the last data of the PCI Express payload is dummy data (Byte Field = 0h and the Local Bus data width is 32 bits). The PEX 8311 suppresses all other dummy cycles, other than the last data of the burst, and/or the Local Bus data width is 8 or 16 bits.

Figure 8-5 illustrates the FIFOs that function during a Direct Slave Write.

Figure 8-5. Direct Slave Write



Note: *Figure 8-5 represents a sequence of Bus cycles.*

8.3.2 Direct Slave Reads

The PEX 8311 issues internal wait states to the PCI Express Address space as a Read request is processed (holds TRDY# de-asserted). The PEX 8311 Local Bus receives a Dword from the Local Bus Slave, unless the PCI Compliance Enable bit is set (**MARBR**[24]=1). (Refer to Section 8.3.4.) Programmable Prefetch modes are available, when prefetch is enabled – prefetch, 1 to 16, or continuous data – until the Direct Slave read ends. The Local prefetch continues several clocks after PCI Express Address space receives all read data required to complete the PCI Express-initiated Read request or the PEX 8311 issues a Retry or disconnect internally. Extra prefetched data is flushed from the FIFO unless Direct Slave Read Ahead mode is enabled (**MARBR**[28]=1).

For the highest data transfer rate, the PEX 8311 can be programmed to prefetch data for any PCI Express Read request on the Local Bus. When Prefetch is enabled (**LBRD0**[8]=0 for Space 0, **LBRD1**[9]=0 for Space 1, and/or **LBRD0**[9]=0 for Expansion ROM), prefetch is from 1 to 16 Dwords or until all PCI Express Read requests are completed. When the PEX 8311 prefetches, it drops the Local Bus after reaching the Prefetch Counter limit. In Continuous Prefetch mode, the PEX 8311 prefetches when FIFO space is available and stops prefetching when the PCI Express Address space stops requesting Read data. When Read prefetching is disabled, the PEX 8311 disconnects from the Local Bus after each Read transfer is performed.

For PCI Express interface Direct Slave Prefetch Read transfers starting at a Dword-aligned boundary, the PEX 8311 prefetches the amount specified in the Prefetch Counter(s). When a Direct Slave Prefetch Burst Read transfer is performed to a Local Bus device that cannot burst, and READY# is asserted for only one clock period, the PEX 8311 retains the Read data in the Direct Slave Read FIFO without ever transferring to the PCI Express Address space to generate a Read Completion TLP. This occurs because the PEX 8311 Local Bus interface is built with 2-Dword FIFO architecture per each Direct Slave FIFO location, and a prefetch mechanism is required to prefetch further data for transferring to occur. Under such conditions, it is necessary to disable a Prefetch or Burst feature.

In addition to Prefetch mode, the PEX 8311 supports Direct Slave Read Ahead mode (**MARBR**[28]=1). (Refer to Section 8.3.6.)

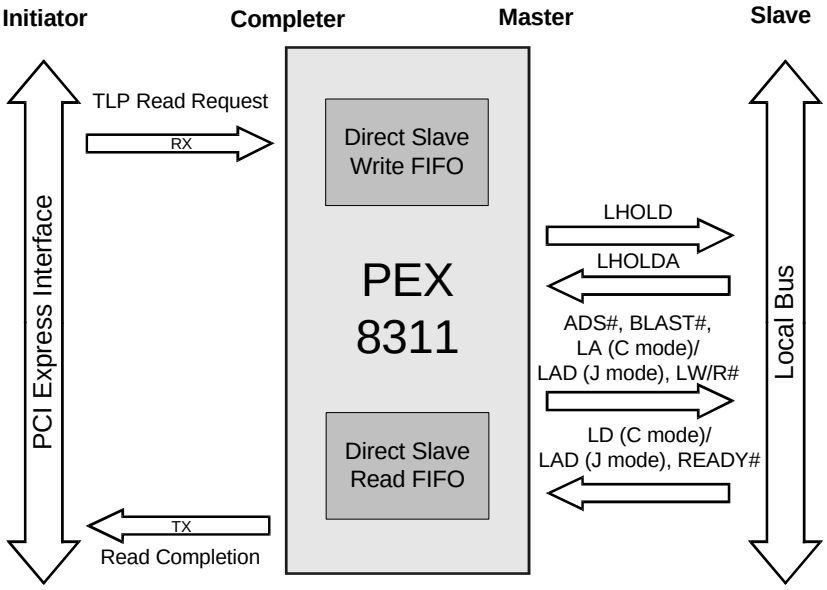
Only PCI Express single Dword Read requests result in the PEX 8311 passing requested Byte Enables (TLP Byte Field) to a Local Bus Target device by way of LBE[3:0]# assertion back to a PCI Express Read requester. This transaction results in the PEX 8311 reading 1 Dword or partial Dword data. For all other types of Read transactions (PCI Express multiple data Read request Dword Aligned and Unaligned), the PEX 8311 reads Local Bus data with all bytes asserted (LBE[3:0]#=0h).

The PEX 8311 disconnects after one transfer for all Direct Slave I/O accesses by the PCI Express Address Space to the Local Bus Address Space, when Direct Slave Space(s) is I/O-mapped.

The PEX 8311 can be programmed to retain the Local Bus and continue asserting LHOLD when the Direct Slave Read FIFO becomes full. When the Local Bus Latency Timer is enabled (**MARBR**[16]=1) and expires (**MARBR**[7:0]), the Local Bus is dropped.

Figure 8-6 illustrates the FIFOs that function during a Direct Slave Read.

Figure 8-6. Direct Slave Read



Note: *Figure 8-6 represents a sequence of Bus cycles.*

8.3.3 Direct Slave Lock

The PEX 8311 supports direct PCI Express-to-Local Bus exclusive accesses (locked atomic operations). A PCI Express-locked operation to the Local Bus results in the entire address Space 0, Space 1, and Expansion ROM space being locked until they are released by the PCI Express. Locked operations are enabled or disabled with the Memory Read Locked request on the PCI Express interface and Enable bit (**MARBR**[22]) for internal LOCK# signal.

8.3.4 PCI Compliance Enable

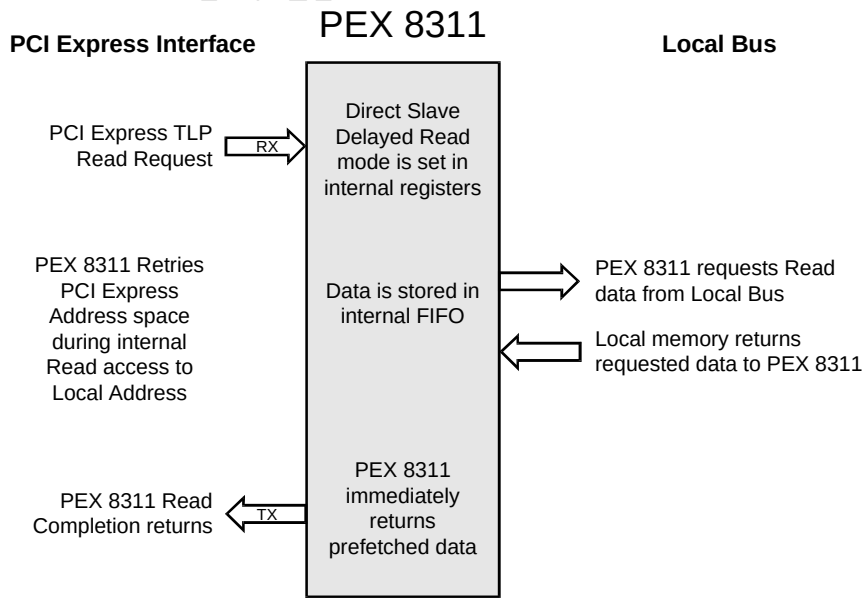
The PEX 8311 can be programmed through the *PCI Compliance Enable* bit to perform Read/Write transactions between PCI Express and Local Bus Spaces in compliance with *PCI r2.2* (**MARBR**[24]=1). The following sections describe the behavior of the PEX 8311 when MARBR[24]=1.

8.3.4.1 Direct Slave Delayed Read Mode

PCI Express single Dword or partial Dword Direct Slave Read request always result in a 1-Dword single cycle transfer on the Local Bus, with corresponding Local Byte Enables (LBE[3:0]#) asserted to reflect the PCI Express Byte Field of the requester unless the PCI Read No Flush Mode bit is enabled (**MARBR**[28]=1). (Refer to Section 8.3.6.) This causes the PEX 8311 to Retry internal PCI Express Address Space accesses to the Local Bus Spaces that follow, until the original Read Address and Byte Field of the Read request are matched.

PCI Express multiple data Dword aligned and unaligned Direct Slave Read requests result in a Prefetch Burst Read Cycle transfer on the Local Bus, with all Local Byte Enables (LBE[3:0]#=0h) asserted, when the Burst bit(s) is enabled (**LBRD0**[24]=1 for Space 0, **LBRD1**[8]=1 for Space 1, and/or **LBRD0**[26]=1 for Expansion ROM). (Refer to Figure 8-7.)

Figure 8-7. Direct Slave Delayed Read Mode



Note: *Figure 8-7 represents a sequence of Bus cycles.*

8.3.4.2 2^{15} Internal Clock Timeout

When the PEX 8311 PCI Express Address Space does not complete the originally requested Direct Slave Delayed Read transfer, the PEX 8311 flushes the Direct Slave Read FIFO after 2^{15} internal clocks and accepts a new Direct Slave Read access. All other Direct Slave Read accesses before the 2^{15} internal clock timeout are Retried internally between PCI Express Address space and Local Bus spaces within the PEX 8311.

8.3.4.3 *PCI r2.2* 16- and 8-Clock Rule

The PEX 8311 internally guarantees that when the first Direct Slave Write data coming from the PCI Express Address Spaces cannot be accepted by the PEX 8311 Local Spaces and/or the first Direct Slave Read data cannot be returned by the PEX 8311 Local spaces to the PCI Express Address spaces within 16 internal clocks from the beginning of internal start of the transfer (FRAME# asserted), the PEX 8311 issues an internal Retry (STOP# asserted) to the PCI Express Address space(s).

During successful Direct Slave Read and/or Write accesses, the subsequent data after the first access must be accepted for writes or returned for reads within 8 internal clocks (TRDY# asserted). Otherwise, the PEX 8311 issues internal disconnect (STOP# asserted) to the PCI Express Address Space(s). In addition, the PEX 8311 internally supports the following *PCI r2.2* functions between PCI Express Address spaces and Local spaces:

- No write while a Delayed Read is pending (PCI Retries for writes) (**MARBR**[25])
- Write and flush pending Delayed Read (**MARBR**[26])

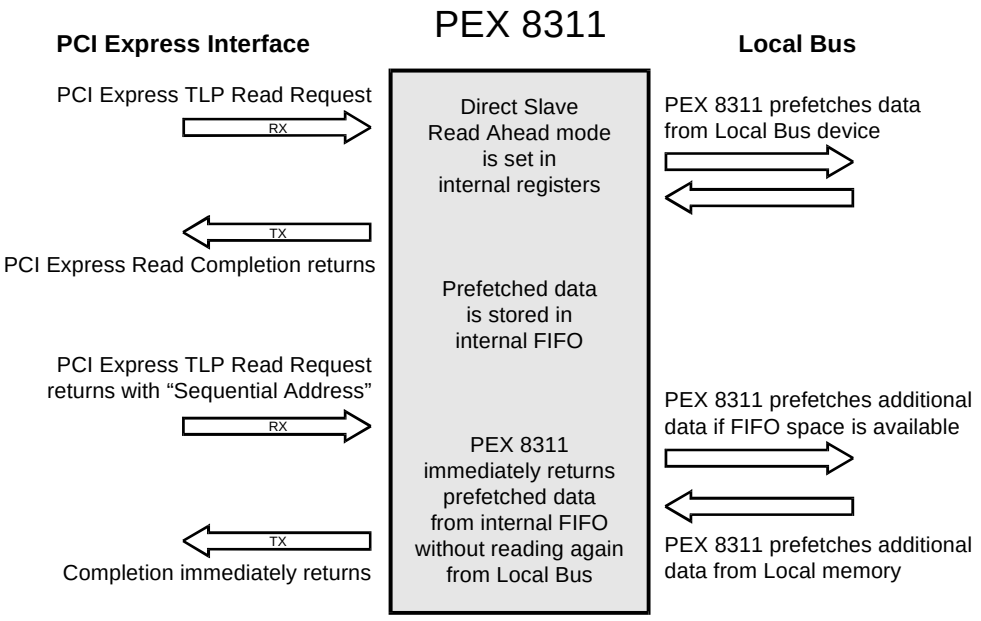
8.3.5 Direct Slave Delayed Write Mode

The PEX 8311 supports Direct Slave Delayed Write mode transactions, in which Posted Write data coming from PCI Express Address Spaces accumulates in the Direct Slave Write FIFO before the PEX 8311 requests ownership of the Local Bus (LHOLD assertion). The Direct Slave Delayed Write mode is programmable to delay LHOLD assertion for the number of Local clocks specified in **LMISC2**[4:2].

8.3.6 Direct Slave Read Ahead Mode

The PEX 8311 also supports Direct Slave Read Ahead mode (**MARBR**[28]=1) in Local Spaces, wherein prefetched data is read from the internal Direct Slave FIFO by the PCI Express Address Spaces instead of directly from the Local Bus. For these features to be in effect, all PCI Express Read requests must be subsequent to the previous address and Dword-aligned (next address = current address + 4) for Direct Slave Read request transfers. Direct Slave Read Ahead mode functions are used with or without Direct Slave Delayed Read mode. (Refer to Figure 8-8.)

Figure 8-8. Direct Slave Read Ahead Mode



Note: *Figure 8-8 represents a sequence of Bus cycles.*

8.3.7 Direct Slave Local Bus READY# Timeout Mode

Direct Slave Local Bus READY# Timeout mode is enabled/disabled by **LMISC2**[0].

When Direct Slave Local Bus READY# Timeout mode is disabled (**LMISC2**[0]=0), *and* the PEX 8311 is mastering the Local Bus during a Direct Slave Read or Write Data transfer, *and* no Local Bus device asserts READY# in response to the Local Bus address generated by the PEX 8311, the PEX 8311 hangs on the Local Bus waiting for READY# assertion. To recover, reset the PEX 8311.

When Direct Slave Local Bus READY# Timeout mode is enabled (**LMISC2**[0]=1), *and* the PEX 8311 is mastering the Local Bus during a Direct Slave Read or Write Data transfer, the PEX 8311 uses the READY# Timeout Select bit (**LMISC2**[1]) to determine when to timeout while waiting for a Local Bus device to assert READY# in response to the Local Bus address generated by the PEX 8311. When **LMISC2**[1]=0, the PEX 8311 waits 32 Local Bus clocks for READY# assertion before timing out. When **LMISC2**[1]=1, the PEX 8311 waits 1,024 Local Bus clocks for READY# assertion before timing out.

When a Direct Slave Local Bus READY# Timeout occurs during a Direct Slave Read (PCI Express Read request), the PEX 8311 issues a Target Abort to the PCI Express Address space(s) which is then converted into the PCI Express Completion Abort to the PCI Express Read requester. When the PCI Express Address Space is in process of accessing Local space(s) (*that is*, the PEX 8311 Local Address Space(s) is not awaiting a PCI Express Address Space Retry of the Direct Slave read), the Target Abort is immediately issued to the PCI Express Address space(s), which is converted to the PCI Express Completion Abort to the PCI Express Read requester. When the PCI Express Address Space is not currently accessing Local Address space(s) the PEX 8311 (*that is*, the PEX 8311 Local Address space(s) is awaiting a PCI Express Address Space Retry of the Direct Slave Read), the PEX 8311 issues a Target Abort the next time the PCI Express Address Space(s) repeats the Direct Slave read, which then is converted to the PCI Express Completion Abort to the PCI Express Read requester.

When a Direct Slave Local Bus READY# Timeout occurs during a Direct Slave Write (PCI Express Write request) *and* the PCI Express Address Space(s) is currently accessing Local Address spaces the PEX 8311 (*that is*, the PCI Express Address Space(s) has not posted the Direct Slave Write into the Local Address space(s) within the PEX 8311), the PEX 8311 immediately issues a Target Abort to the PCI Express Address space(s), which is then converted to ERR_NONFATAL message. (Refer to Chapter 10, "Error Handling," for details.) When the PCI Express Address space(s) is not currently accessing Local Address space(s) the PEX 8311 (*that is*, the PCI Express Address space(s) has posted the Direct Slave write into the Local Address space), the PEX 8311 does ***not*** issue to the PCI Express Address space(s) any indication that the timeout occurred.

Caution: *Only use the PEX 8311 Direct Slave Local Bus READY# Timeout feature during design debug. This feature allows illegal Local Bus addresses to be easily detected and debugged. After the design is debugged and legal addresses are guaranteed, disable Direct Slave Local Bus READY# Timeout mode to avoid unreported timeouts during Direct Slave writes.*

8.3.8 Direct Slave PCI Express-to-Local Address Mapping

Three Local Address spaces – Space 0, Space 1, and Expansion ROM – are accessible from the PCI Express interface through the PEX 8311 PCI Address spaces. Each is defined by a set of three registers:

- **LCS Direct Slave Local Address Space Range** (**LAS0RR**, **LAS1RR**, and/or **EROMRR**)
- **LCS Direct Slave Local Address Space Local Base Address** (Remap) (**LAS0BA**, **LAS1BA**, and/or **EROMBA**)
- **LCS PCI Base Address** (**PCIBAR2**, **PCIBAR3**, and/or **PCIERBAR**)

A fourth register, the **Bus Region Descriptor** register(s) for PCI-to-Local Accesses (**LBRD0** and/or **LBRD1**), defines the Local Bus characteristics for the Direct Slave regions. (Refer to Figure 8-9.)

Each PCI Express-to-Local Address space is defined as part of reset initialization, as described in Section 8.3.8.1. These Local Bus characteristics are modified at any time before actual data transactions.

8.3.8.1 Direct Slave Local Bus Initialization

Range – Specifies which PCI Express Address bits of PCI Express Address space(s) to use for decoding a PCI Express access to Local Bus space. Each bit corresponds to a PCI Express Address bit. Bit 31 corresponds to Address bit 31. Write 1 to all bits that must be included in decode and 0 to all others.

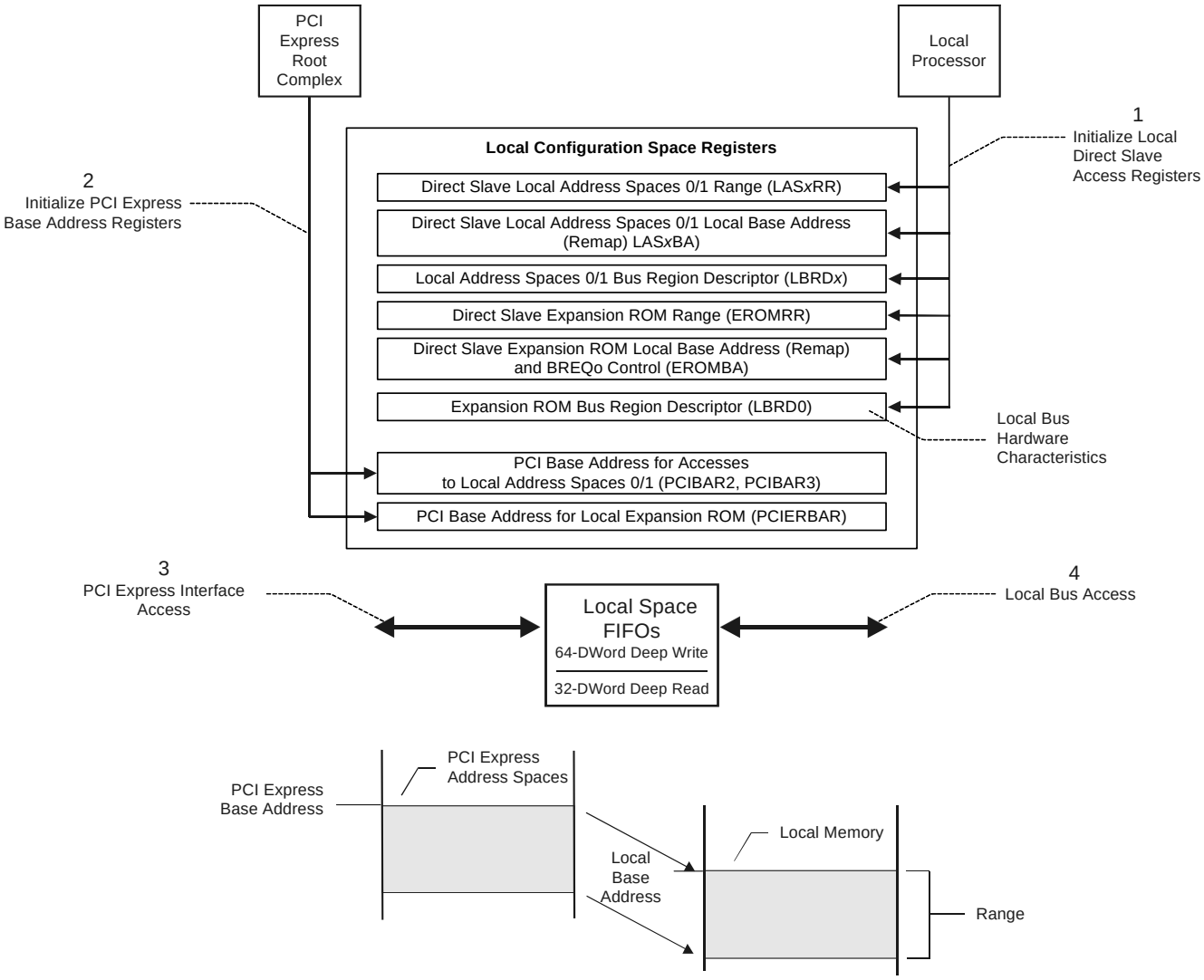
Remap PCI Express-to-Local Addresses into a Local Address Space – Bits in this register remap (replace) the PCI Express Address bits used in decode as the Local Address bits.

Local Bus Region Descriptor – Specifies the Local Bus characteristics.

8.3.8.2 Direct Slave PCI Express Initialization

After a PCI Express reset (PERST#), the software determines what PCI Express Address spaces are present and the amount of resource allocation required by each. It then configures the subordinate bus, the internal bus of the PEX 8311 between PCI Express Address spaces and Local Bus Spaces and determines the amount of Address space required by writing all ones (1) to a PCI Base Address register and then reading back the value. The PEX 8311 Local Bus Space (PCI Base Address registers) returns zeros (0) in the "don't care" Address bits, effectively specifying the Address space required. The PCI Express software then maps the Local Address space into the PCI Express Address space, by programming the PCI Base Address register. (Refer to Figure 8-9.)

Figure 8-9. Local Bus Direct Slave Access



8.3.8.3 Direct Slave PCI Express Initialization Example

A 1-MB Local Address Space, 12300000h through 123FFFFFh, is accessible by the PCI Express Address Space using internal PEX 8311 Bus at PCI addresses 78900000h through 789FFFFFh.

1. Local initialization software or the serial EEPROM contents set the Range and Local Base Address registers, as follows:
   - **Range** – FFF00000h (1 MB, decode the upper 12 PCI Address bits).
   - **Local Base Address (Remap)** – 123XXXXXh (Local Base Address for PCI-to-Local accesses [Space Enable bit(s) must be set, to be recognized by the PCI Host (**LAS*x*BA**[0]=1, where *x* is the Local Address Space number)].
2. PCI Express Initialization software writes all ones (1) to the PEX 8311 Local Bus, PCI Base Address, then reads it back again.
   - The PEX 8311 returns a value of FFF00000h. The PCI Express software then writes to the PCI Base Address register(s).
   - **PCI Base Address** – 789XXXXXh (the PEX 8311 Local Bus, PCI Base Address for Access to the Local Address Space registers, **PCIBAR2** and **PCIBAR3**).

8.3.8.4 Direct Slave Byte Enables (C Mode)

During a Direct Slave transfer, each of three spaces (Space 0, Space 1, and Expansion ROM) are programmed to operate in an 8-, 16-, or 32-bit Local Bus data width, by encoding the Local Byte Enables (LBE[3:0]#) as follows:

32-Bit Bus – The four Byte Enables indicate which of the four bytes are valid during a Data cycle:

- LBE3# Byte Enable 3 – LD[31:24]
- LBE2# Byte Enable 2 – LD[23:16]
- LBE1# Byte Enable 1 – LD[15:8]
- LBE0# Byte Enable 0 – LD[7:0]

16-Bit Bus – LBE[3, 1:0]# are encoded to provide BHE#, LA1, and BLE#, respectively:

- LBE3# Byte High Enable (BHE#) – LD[15:8]
- LBE2# ***not used***
- LBE1# Address bit 1 (LA1)
- LBE0# Byte Low Enable (BLE#) – LD[7:0]

8-Bit Bus – LBE[1:0]# are encoded to provide LA[1:0], respectively:

- LBE3# ***not used***
- LBE2# ***not used***
- LBE1# Address bit 1 (LA1)
- LBE0# Address bit 0 (LA0)

8.3.8.5 Direct Slave Byte Enables (J Mode)

During a Direct Slave transfer, each of three spaces (Space 0, Space 1, and Expansion ROM) are programmed to operate in an 8-, 16-, or 32-bit Local Bus data width, by encoding the Local Byte Enables (LBE[3:0]#) as follows:

32-Bit Bus – The four Byte Enables indicate which of the four bytes are valid during a Data cycle:

- LBE3# Byte Enable 3 – LAD[31:24]
- LBE2# Byte Enable 2 – LAD[23:16]
- LBE1# Byte Enable 1 – LAD[15:8]
- LBE0# Byte Enable 0 – LAD[7:0]

16-Bit Bus – LBE[3, 1:0]# are encoded to provide BHE#, LA1, and BLE#, respectively:

- LBE3# Byte High Enable (BHE#) – LAD[15:8]
- LBE2# ***not used***
- LBE1# Address bit 1 (LA1)
- LBE0# Byte Low Enable (BLE#) – LAD[7:0]

8-Bit Bus – LBE[1:0]# are encoded to provide LA[1:0], respectively:

- LBE3# ***not used***
- LBE2# ***not used***
- LBE1# Address bit 1 (LA1)
- LBE0# Address bit 0 (LA0)

8.3.9 Direct Slave Priority

Direct Slave accesses on the Local Bus maintain a higher priority than DMA accesses, thereby preempting DMA transfers. During a DMA transfer, when the PEX 8311 detects a pending Direct Slave access (PCI Express Posted Write request), it releases the Local Bus. The PEX 8311 resumes the DMA operation after the Direct Slave access completes on the Local Bus.

When the PEX 8311 DMA Controller(s) owns the Local Bus, its LHOLD output and LHOLDA input are asserted. When a Direct Slave access occurs, the PEX 8311 releases the Local Bus by de-asserting LHOLD and floating the Local Bus outputs. After the PEX 8311 senses that LHOLDA is de-asserted, it requests the Local Bus for a Direct Slave transfer by asserting LHOLD. When the PEX 8311 receives LHOLDA, it performs the Direct Slave transfer. After completing a Direct Slave transfer, the PEX 8311 releases the Local Bus by de-asserting LHOLD and floating the Local Bus outputs. After the PEX 8311 senses that LHOLDA is de-asserted and the Local Bus Pause Timer Counter is zero (**MARBR**[15:8]=0h) or disabled (**MARBR**[17]=0), it requests the Local Bus to complete the DMA transfer by re-asserting LHOLD. When the PEX 8311 receives LHOLDA and LHOLD=1, it drives the bus and continues the DMA transfer.

8.4 Deadlock Conditions

A deadlock can occur internally within the PEX 8311 when a PCI Express Address Space must access the PEX 8311 Local Bus at the same time a Master on the PEX 8311 Local Bus must access the PCI Express Address Space to transfer data to the PCI Express interface. This type of deadlock is a *Partial Deadlock*.

Note: *Full deadlock is impossible to encounter in the PEX 8311 bridge with PCI Express Ingress/ Egress direction, as well as the internal interface between PCI Express Address and Local space architecture.*

Partial deadlock occurs when the PCI Express device tries to access the PEX 8311 Local Bus concurrently with the PEX 8311 Local Master trying to access the PCI Express device Local Bus. This applies only to Direct Master and Direct Slave accesses through the PEX 8311. Deadlock does ***not*** occur in transfers through the PEX 8311 DMA channels or internal registers (*such as*, Mailboxes).

For partial deadlock, accesses by the PCI Express Address spaces to the Local Spaces times out (Direct Slave Retry Delay Clocks, **LBRD0**[31:28]) and the PEX 8311 responds with internal Retry. This allows the Direct Master to complete and free up the Local Bus. Possible solutions are described in the following sections for cases in which internal timeout is undesirable, and back off the Local Bus Master is used to resolve deadlock conditions.

8.4.1 Backoff

The backoff sequence is used to break a deadlocked condition. The PEX 8311 BREQo signal indicates that a deadlock condition has occurred.

The PEX 8311 starts the Backoff Timer (refer to the **EROMBA** register for further details) when it detects the following conditions:

- PCI Express Address Space is attempting to access memory or an I/O device on the Local Bus through the Local Address Space and is not gaining access (*for example*, LHOLDA is not received).
- Local Bus Master is performing a Direct Bus Master Read access to the PCI Express Address Space to generate a TLP Read request on the PCI Express interface. Or, a Local Bus Master is performing a Direct Bus Master Write access to the PCI Express Address Space to generate a TLP Write request on the PCI Express interface and the PEX 8311 Direct Master Write FIFO cannot accept another Write cycle.

When Local Bus Backoff is enabled (**EROMBA**[4]=1), the Backoff Timer expires, and the PEX 8311 has not received LHOLDA, the PEX 8311 asserts BREQo. External bus logic can use BREQo to perform backoff.

The Backoff cycle is device/bus architecture dependent. External logic (an arbiter) can assert the necessary signals to cause a Local Bus Master to release a Local Bus (backoff). After the Local Bus Master backs off, it can grant the bus to the PEX 8311 by asserting LHOLDA.

After BREQo is asserted, READY# for the current Data cycle is never asserted (the Local Bus Master must perform backoff). When the PEX 8311 detects LHOLDA, it proceeds with the PCI Express-to-Local Bus access. When this access completes and the PEX 8311 releases the Local Bus, external logic can release the backoff and the Local Bus Master can resume the cycle interrupted by the Backoff cycle. The PEX 8311 Direct Master Write FIFO retains accepted data (*that is*, the last data for which READY# was asserted).

After the backoff condition ends, the Local Bus Master restarts the last cycle with ADS#. Ensure that for writes, data following ADS# is data the PEX 8311 did not acknowledge prior to the Backoff cycle (*for example*, the last data for which READY# is not asserted).

For Direct Master Read cycles (the PEX 8311 generated PCI Express TLP Read request), when the PEX 8311 is able to receive a Read Completion as the Local Bus Master that initiated the Direct Master Read cycle is backed off, the Local Bus Master receives that data when the Local Master restarts the same last cycle (data is ***not*** read twice). The PEX 8311 is ***not*** allowed to perform a new read.

8.4.1.1 Software/Hardware Solution for Systems without Backoff Capability

For adapters that do not support backoff, a possible deadlock solution is as follows.

PCI Express Root Complex software/driver, external Local Bus hardware, general-purpose output USERo and general-purpose input USERi is used to prevent deadlock. USERo is asserted to request that the external Local Bus Arbiter not grant the bus to any Local Bus Master except the PEX 8311. Status output from the Local Bus Arbiter is connected to USERi to indicate that no Local Bus Master owns the Local Bus, or the PCI Express transaction-initiating device to determine that no Local Bus Master that currently owns the Local Bus can read input. The PCI Express transaction initiating device can then perform Direct Slave access (PCI Express-to-Local Bus Write/Read request). When the PCI Express device finishes, it de-asserts USERo.

8.4.1.2 Preempt Solution

For devices that support preempt, USERo is used to preempt the current Local Bus Master device. When USERo is asserted, the current Local Bus Master device completes its current cycle and releases the Local Bus, de-asserting LHOLD.

8.4.1.3 Software Solutions to Deadlock

Both PCI Express and Local Bus software can use a combination of Mailbox registers, Doorbell registers, interrupts, Direct Local-to-PCI Express accesses, and Direct PCI Express-to-Local accesses to avoid deadlock.

8.4.2 Local Bus Direct Slave Data Transfer Modes

The PEX 8311 supports C and J modes with three Local Bus Data Transfer modes:

- Single Cycle
- Burst-4
- Continuous Burst

Single Cycle mode is the default Data Transfer mode. Continuous Burst mode provides the highest throughput.

Table 8-5 summarizes the register settings used to select Local Bus Data Transfer modes. It also indicates the data quantity transferred per Address Cycle (ADS#).

Note: *The term* Burst Forever *was formerly used to describe* Continuous Burst.

Table 8-5. Local Bus Data Transfer Modes

Mode	Burst Enable Bit	BTERM# Input Enable Bit	Result
Single Cycle (default)	0	X	One ADS# per data.
Burst-4	1	0	One ADS# per four Data cycles (recommended for i960 and PPC401).
Continuous Burst	1	1	One ADS# per data burst or until BTERM# is asserted.

Note: *"X" is "Don't Care."*

8.4.2.1 Single Cycle Mode

Single Cycle mode is the default Data Transfer mode. In Single Cycle mode, the PEX 8311 issues one ADS# per data cycle. The starting address for a single cycle Data transfer resides on any address.

For single cycle Data transfers, Burst mode is disabled (**LBRD0**[24]=0 for Space 0, **LBRD1**[8]=0 for Space 1, and/or **LBRD0**[26]=0 for Expansion ROM). For a 32-bit Local Bus, when a starting address in a Direct Slave transfer is ***not*** aligned to a Dword boundary, the PEX 8311 performs a single cycle until the next Dword boundary.

Partial Data Accesses

Partial Data accesses (not all Byte Enables are asserted) are broken into single cycles. When there is remaining data that is ***not*** Dword-aligned during the transfer, it results in a single cycle Data transfer.

8.4.2.2 Burst-4 Mode

Burst-4 mode forces the PEX 8311 to perform Data transfers as bursts of four Data cycles (4 Dwords, four 16-bit words, or 4 bytes to a 32-, 16-, or 8-bit bus, respectively).

Burst-4 mode Data transfers are set up by enabling bursting and clearing the BTERM# Input Enable bit(s) (**LBRD0**[24, 7]=10b for Space 0, **LBRD1**[8:7]=10b for Space 1, and/or **LBRD0**[26, 23]=10b for Expansion ROM, respectively).

Burst-4 mode bursting starts on any data boundary and bursts to the next four-data boundary. The first burst starts on any address and moves to the data boundary. The next bursts are four Data cycles. The first or last burst can be less than four Data cycles. The PEX 8311 can continue to burst by asserting ADS# and performing another burst. For a 32-bit Local Bus, when a starting address in a Direct Slave transfer is ***not*** aligned to a Dword boundary, the PEX 8311 performs a single cycle until the next Dword boundary. (Refer to Table 8-6.)

Table 8-6. Burst-4 Mode

Local Bus Data Width	Burst-4
32 bit	4 Dwords start/stop at a 4-Dword boundary
16 bit	4 words start/stop at a 4-word boundary
8 bit	4 bytes start/stop at a 4-byte boundary

Note: *The first or last burst can be less than four Data cycles.*

Partial Data (<4 Bytes) Accesses

Partial Data accesses occur when either the first, last, or both PCI Express data are unaligned, Byte Enable Field are ***not*** all asserted. For a 32-bit Local Bus, they are broken in single cycles until the next Dword boundary.

8.4.2.3 Continuous Burst Mode

Continuous Burst mode enables the PEX 8311 to perform data bursts of longer than four Data cycles. However, special external interface devices are required that can accept bursts longer than four Data cycles.

Continuous Burst mode Data transfers are set up by enabling bursting and setting the BTERM# Input Enable bit(s) (**LBRD0**[24, 7]=11b for Space 0, **LBRD1**[8:7]=11b for Space 1, and/or **LBRD0**[26, 23]=11b for Expansion ROM, respectively).

The PEX 8311 asserts one ADS# cycle and continues to burst data. When a Slave device requires a new Address cycle (ADS#), it can assert the BTERM# input. The PEX 8311 completes the current Data transfer and stops the burst. The PEX 8311 continues the transfer by asserting ADS# and beginning a new burst at the next address.

8.4.3 Local Bus Write Accesses

For Local Bus writes, only bytes specified by a PCI Express transaction initiator or PEX 8311 DMA Controller(s) are written.

8.4.4 Local Bus Read Accesses

For Single Cycle Local Bus Read accesses, when the PEX 8311 is the Local Bus Master, the PEX 8311 reads only bytes corresponding to Byte Enables requested by the PCI Express Read request initiator. For Burst Read cycles, the PEX 8311 passes all bytes and is programmed to:

- Prefetch
- Perform Direct Slave Read Ahead mode
- Generate internal wait states
- Enable external wait control (READY# input)
- Enable type of Burst mode to perform

8.4.5 Direct Slave Accesses to 8- or 16-Bit Local Bus

PCI Express access to an 8- or 16-bit Local Bus results in the Local Data being broken into multiple Local Bus width transfers. For each transfer, Byte Enables are encoded to provide Local Address bits C mode, LA[1:0]. In J mode, LAD[1:0] also provide these Address bits during the Address phase.

8.4.6 Local Bus Data Parity

Generation or use of Local Bus data parity is optional. The Local Bus Parity Check is passive and provides only parity information to the Local processor during Direct Master, Direct Slave.

There is one data parity ball for each byte lane of the PEX 8311 data bus (DP[3:0]). “Even data parity” is asserted for each lane during Local Bus reads from the PEX 8311 and during PEX 8311 Master writes to the Local Bus.

Even data parity is checked for Direct Slave reads, Direct Master writes. When an error is detected, the PEX 8311 sets the Direct Master Write/Direct Slave Read Local Data Parity Check Error Status bit (**INTCSR**[7]=1) and asserts an interrupt (LSERR#), when enabled (**INTCSR**[0, 6]=11b, respectively). This occurs in the Clock cycle following the data being checked.

For applications in which READY# is disabled in the PEX 8311 registers, an external pull-down resistor is required for READY# to allow **INTCSR**[7] to be set and the LSERR# interrupt asserted.

8.5 DMA Operation

The PEX 8311 supports two independent DMA channels – Channel 0 and Channel 1 – capable of transferring data from PCI Express-to-Local and Local-to-PCI Express.

Each channel consists of a DMA Controller and a dedicated bi-directional FIFO. Both channels support DMA Block, Scatter/Gather, and Demand Mode transfers, with or without End of Transfer (EOT#). Master mode must be enabled for both the Local Spaces and PCI Express Address Spaces (PCI Command, **PCICR**[2]=1) before the PEX 8311 begins generating TLPs on the PCI Express interface. In addition, DMA Channel 0 and Channel 1 are programmed to:

- Operate with 8-, 16-, or 32-bit Local Bus data widths
- Use zero to 15 internal wait states (Local Bus)
- Enable/disable external wait states (Local Bus)
- Enable/disable Local Bus burst capability
- Set Local Bus mode (refer to Table 8-7)
- Hold Local address constant (Local Slave is FIFO) or incremented
- Internally perform Memory Write and Invalidate (Command Code = Fh) or normal Memory Write (Command Code = 7h) to PCI Express Address spaces
- Stop/pause Local transfer with or without BLAST# (DMA Fast/Slow Terminate mode)
- Operate in DMA Clear Count mode

The PEX 8311 supports generating internal PCI Dual Address Cycles (DAC) to the PCI Express Prefetchable Address Space with the upper 32-bit register(s) (**DMADAC*x***) which then is translated to TLP Long Address format generation on the PCI Express interface, to access devices located above the 4-GB Address Boundary space. The PEX 8311 suppresses dummy cycles generation internally the PCI Express Address spaces and on the Local Bus. (Refer to Table 8-7.)

The Local Bus Latency Timer (**MARBR**[7:0]) determines the number of Local clocks the PEX 8311 can burst data before relinquishing Local Bus ownership. The Local Pause Timer (**MARBR**[15:8]) sets how soon (after the Latency Timer times out) the DMA channel can re-request the Local Bus.

Table 8-7. DMA Local Burst Mode

Burst Enable Bit(s)	BTERM# Input Enable Bit(s)	Result
Disabled (0)	X	Single cycle (default Local Burst mode)
Enabled (1)	Disabled (0)	Burst up to four Data cycles
Enabled (1)	Enabled (1)	Continuous Burst (terminate when BTERM# is asserted or transfer is completed)

Note: *"X" is "Don't Care.*

8.5.1 Master Command Codes

The PEX 8311 becomes an internal bus master to perform DMA transfers. The internal command code used by the PEX 8311 during DMA transfers is specified by the value(s) contained in the PEX 8311 **LCS Control** (**CNTRL**[15:0]) register bits. However, in Memory Write and Invalidate (MWI) mode, it is specified in the PEX 8311 **LCS** registers (**PCICR**[4]=1; **DMAMODE*x***[13]=1; **PCICLSR**[7:0] = Cache Line Size of 8 or 16 Dwords). In MWI mode for DMA Local-to-PCI Express transfers, when the starting address alignment is aligned with the Cache Line Size and upon determining it can transfer at least one Cache Line of data, the PEX 8311 uses an internal Command Code of Fh, regardless of the **CNTRL**[15:0] register bit values.

For DMA Local-to-PCI Express accesses, the PEX 8311 uses the internal commands delineated in Table 8-8.

Table 8-8. DMA-to-PCI Express Memory I/O-Mapped and/or Prefetchable Memory Address Spaces Access Command Codes

Command Type	Code (C/BE[3:0]#)
Memory Read	0110b (6h)
Memory Write	0111b (7h)
Memory Read Multiple	1100b (Ch)
Dual Address Cycle	1101b (Dh)
Memory Read Line	1110b (Eh)
Memory Write and Invalidate	1111b (Fh)

Note: *DMA can only perform Memory accesses. DMA **cannot** perform I/O or Configuration accesses.*

8.5.2 DMA PCI Express Long Address Format

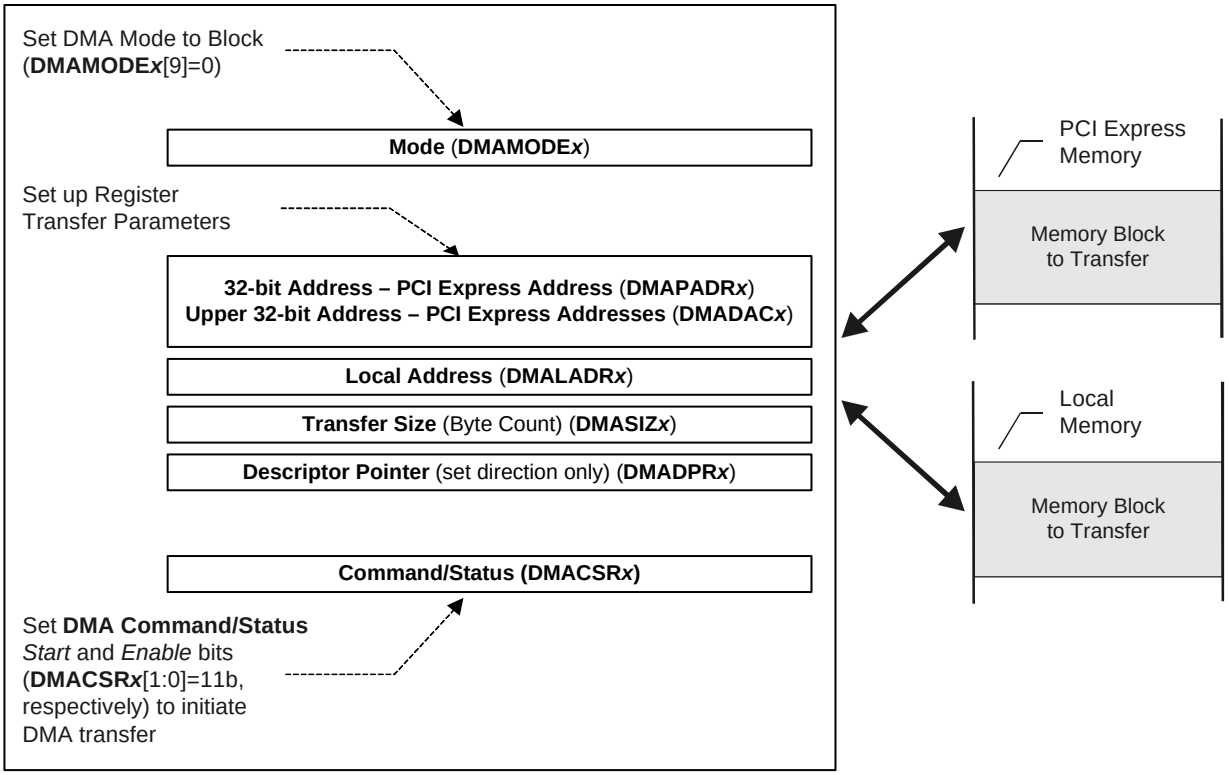
The PEX 8311 supports Long Address Format generation, a 64-bit addressing to access devices located above the 4-GB Address Boundary space by utilizing DMA Dual Address Cycle (DAC) register (**DMADAC*x***) for DMA Block Mode transactions. DMA Scatter/Gather mode can utilize the DAC function by way of the **DMADAC*x*** register(s) or **DMAMODE*x***[18]. The DMA space must be mapped to PCI Express Prefetchable space and **DMADAC*x*** and/or **DMAMODE*x***[18] register(s) must be programmed to a non-zero value and enabled, respectively, for 64-bit addressing to occur on the PCI Express interface. (Refer to Section 5.4.3, "64-Bit Addressing," for further details.) When the **DMADAC*x*** register(s) contains a value of 0h (feature enabled when DMADAC*x* register value is ***not*** 0h), the PEX 8311 performs a Short Address Format on the PCI Express interface.

8.5.3 DMA Block Mode

The PCI Express device or Local processor sets the DMA PCI and Local starting addresses, transfer byte count, and transfer direction. The PCI Express device or Local processor then sets the DMA Channel Start and Enable bits (**DMACSR*x***[1:0]=11b) to initiate a transfer. The PEX 8311 internally accesses PCI Express Address spaces to generate a TLP on the PCI Express interface and Local Bus, and transfers data. After the transfer completes, the PEX 8311 sets the Channel Done bit(s) (**DMACSR*x***[4]=1) and asserts an interrupt(s) (**INTCSR**[16], **INTCSR**[8], **DMAMODE*x***[17], and/or **DMAMODE*x***[10]) to the Local processor or the PCI Express (programmable). The Channel Done bit(s) are polled, instead of interrupt generation, to indicate the DMA transfer status.

DMA registers are accessible from the PCI Express interface and Local Bus. (Refer to Figure 8-10.)

Figure 8-10. DMA Block Mode Initialization (Single Address or Dual Address PCI)



During DMA transfers, the PEX 8311 is transaction initiator (generates TLP) on the PCI Express interface and Master on the Local Bus. For simultaneous access, Direct Slave or Direct Master has a higher priority than DMA.

The PEX 8311 releases internal interface between DMA Local spaces and PCI Express Address spaces when one of the following conditions occur (refer to Figure 8-11 and Figure 8-12):

- Local DMA FIFO is full (PCI Express-to-Local)
- Local DMA FIFO is empty (Local-to-PCI Express)
- Terminal count is reached
- Internal PCI Bus Latency Timer expires (**PCILTR**[7:0]) – normally programmed by the System BIOS according to the PCI Maximum Latency (**PCIMLR**) register value
- PCI Express Address Space as a Target asserts STOP# to the Local DMA space(s)

The PEX 8311 releases the Local Bus, when one of the following conditions occurs:

- Local DMA FIFO is empty (PCI Express-to-Local)
- Local DMA FIFO is full (Local-to-PCI Express)
- Terminal count is reached
- Local Bus Latency Timer is enabled (**MARBR**[16]=1) and expires (**MARBR**[7:0])
- BREQi is asserted
- Direct Slave (PCI Express-to-Local Read/Write) request is pending

Figure 8-11. DMA, PCI Express-to-Local Bus

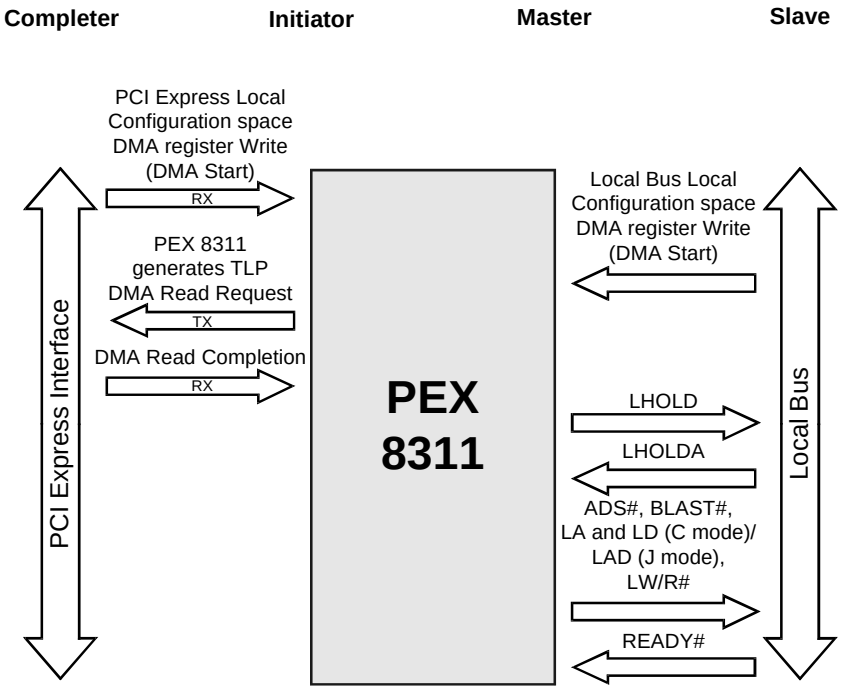
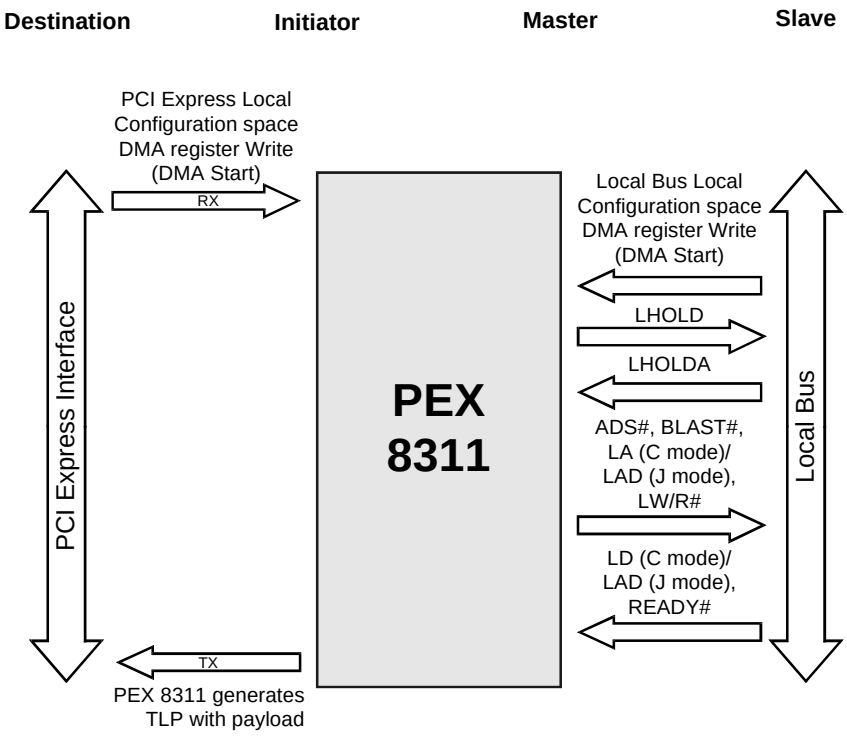


Figure 8-12. DMA, Local-to-PCI Express



Note: *Figure 8-11 and Figure 8-12 represent a sequence of Bus cycles.*

8.5.3.1 DMA Block Mode PCI Dual Address Cycles

The PEX 8311 supports generation of PCI Express TLP Long Address format (64-bit address) to accesses devices located above the 4-GB Address Boundary space. The DMA Local Space must be mapped to PCI Express Prefetch Address Space internally for 64-bit address to generate in DMA Block mode. When the **DMADAC*x*** register(s) contains a value of 0h, the PEX 8311 generates PCI Express TLP Short Address format (32-bit address). Other values cause a Dual Address to internally generate between DMA Local Space and PCI Express Prefetchable Address Space causing PCI Express TLP Long Address format to generate on the PCI Express.

8.5.4 DMA Scatter/Gather Mode

In DMA Scatter/Gather mode, the PCI Express device or Local processor sets up descriptor blocks in PCI Express or Local memory composed of PCI and Local addresses, transfer count, transfer direction, and address of the next descriptor block. (Refer to Figure 8-13 and Figure 8-14.) The PCI Express device or Local processor then:

- Enables the DMA Scatter/Gather mode bit(s) (**DMAMODE*x***[9]=1)
- Sets up the address of initial descriptor block in the PEX 8311 Descriptor Pointer register(s) (**DMADPR*x***)
- Initiates the transfer by setting a control bit(s) (**DMACSR*x***[1:0]=11b)

The PEX 8311 supports zero wait state Descriptor Block bursts from the Local Bus when the *Local Burst Enable* bit(s) is enabled (**DMAMODE*x***[8]=1).

The PEX 8311 loads the first descriptor block and initiates the Data transfer. The PEX 8311 continues to load descriptor blocks and transfer data until it detects the *End of Chain* bit(s) is set (**DMADPR*x***[1]=1). When the *End of Chain* bit(s) is detected, the PEX 8311 completes the current descriptor block, sets the *DMA Done* bit(s) (**DMACSR*x***[4]=1), and asserts a PCI Express or Local interrupt (Assert_INTA or LINTo#, respectively), when the interrupt is enabled (**DMAMODE*x***[10]=1).

The PEX 8311 can also be programmed to assert PCI Express or Local interrupts after each descriptor is loaded, and the corresponding Data transfer is finished.

The DMA Controller(s) are programmed to clear the transfer size at completion of each DMA transfer, using the *DMA Clear Count Mode* bit(s) (**DMAMODE*x***[16]=1).

Notes: *In DMA Scatter/Gather mode, the descriptor includes the PCI and Local Address Space, transfer size, and next descriptor pointer. It also includes a PCI Express 64-bit address value, when the DAC Chain Load bit(s) is enabled (**DMAMODEx**[18]=1). Otherwise, the **DMADACx** register values are used. The Descriptor Pointer register(s) (**DMADPRx**) contains descriptor location (bit 0), end of chain (bit 1), interrupt after terminal count (bit 2), direction of transfer (bit 3), and next descriptor address (bits [31:4]) bits.*

DMA descriptors stored on the Local Bus are accessed using the same bus data width as programmed for the Data transfer.

A DMA descriptor can be located on PCI Express or Local memory, or both (for example, one descriptor on Local memory, another descriptor on PCI Express memory and vice-versa). The descriptors can also be located in the PCI Express Shared Memory, within the PEX 8311 bridge.

Figure 8-13. DMA Scatter/Gather Mode from PCI Express-to-Local Bus (Control Access from Local Bus)

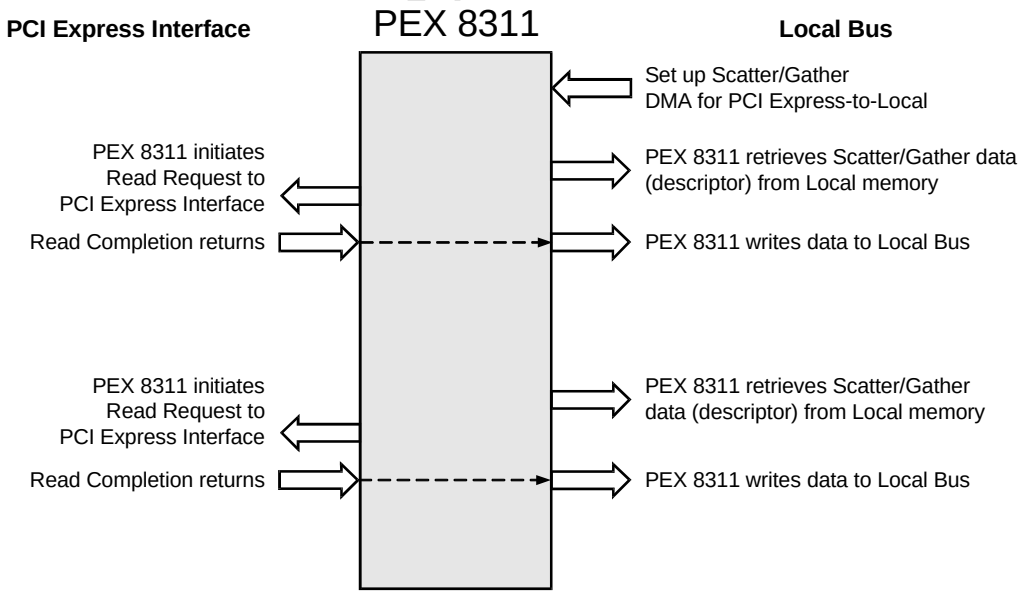
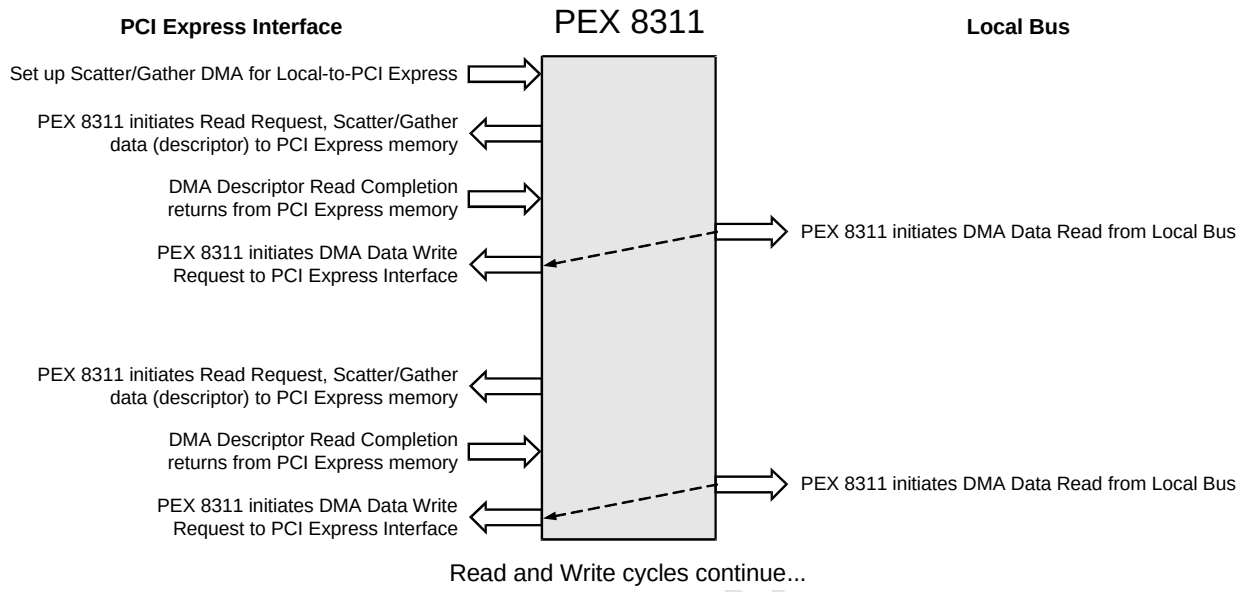


Figure 8-14. DMA Scatter/Gather Mode from Local-to-PCI Express (Control Access from PCI Express Interface)



Note: *Figure 8-13 and Figure 8-14 represent a sequence of Bus cycles.*

8.5.4.1 DMA Scatter/Gather PCI Express Long Address Format

The PEX 8311 supports generation of the PCI Express Long Address format to access devices located above the 4-GB Address Boundary space in DMA Scatter/Gather mode for Data transfers only. Ensure that descriptor blocks reside below the 4-GB Address Boundary space. For PCI Express Long Address generation support the Local DMA space must be mapped to the PCI Express Prefetchable Address space. The PEX 8311 offers three different options of how PCI Express Long Address format DMA Scatter/Gather is utilized. Assuming the descriptor blocks are located on the PCI Express interface:

- **DMADAC*x*** contain(s) a non-zero value. **DMAMODE*x***[18] is cleared to 0. The PEX 8311 performs a PCI Express Short Address format (32-bit address) 4-Dword descriptor block load from PCI Express memory and DMA transfer with PCI Express Long Address format on the PCI Express interface. (Refer to Figure 8-15.) Ensure that the DMA descriptor block starting addresses are 16-byte-aligned.
- **DMADAC*x*** contain(s) a value of 0h. **DMAMODE*x***[18] is set to 1. The PEX 8311 performs a PCI Express Short Address format 5-Dword descriptor block load from PCI Express Memory and DMA transfer with PCI Express Long Address format on the PCI Express interface. (Refer to Figure 8-16.) Ensure that the DMA descriptor block starting addresses are 32-byte-aligned.
- **DMADAC*x*** contain(s) a non-zero value. **DMAMODE*x***[18] is set to 1. The PEX 8311 performs a PCI Express Short Address format 5-Dword descriptor block load from PCI Express memory and DMA transfer with PCI Express Long Address format on the PCI Express interface. The fifth descriptor overwrites the value of the **DMADAC*x*** register(s). (Refer to Figure 8-16.) Ensure that the DMA descriptor block starting addresses are 32-byte-aligned.

Figure 8-15. DMA Scatter/Gather Mode Descriptor Initialization [PCI Express Short/Long Address Format PCI Express Address (DMADAC*x*) Register Dependent]

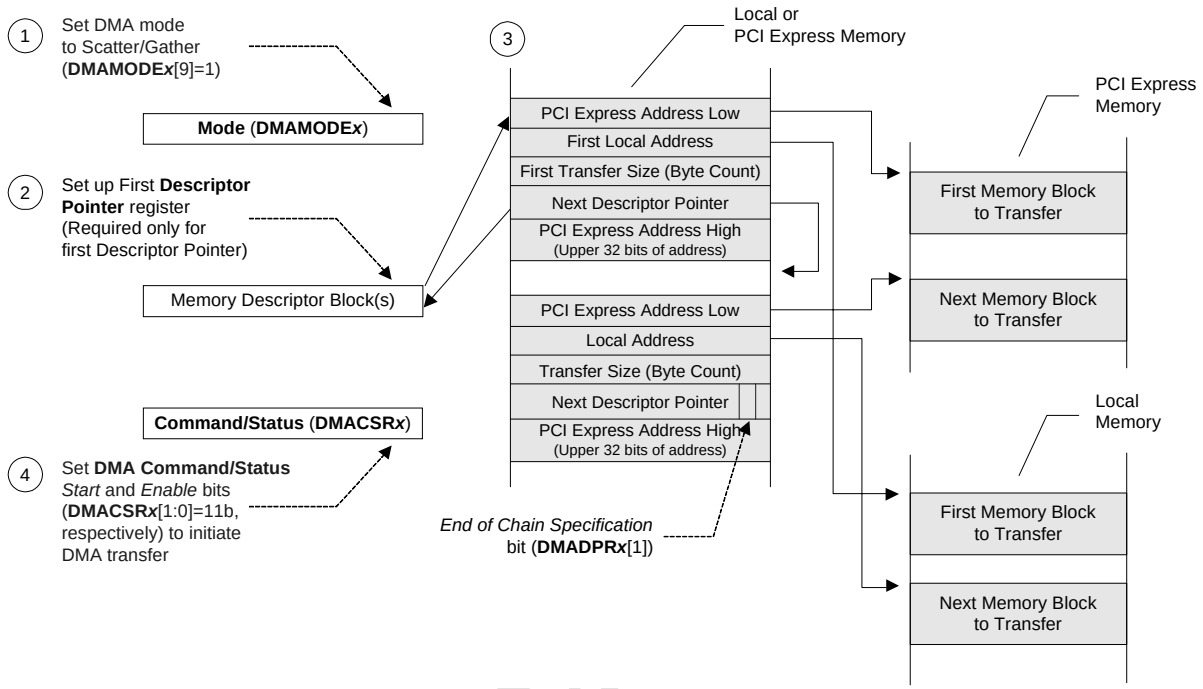
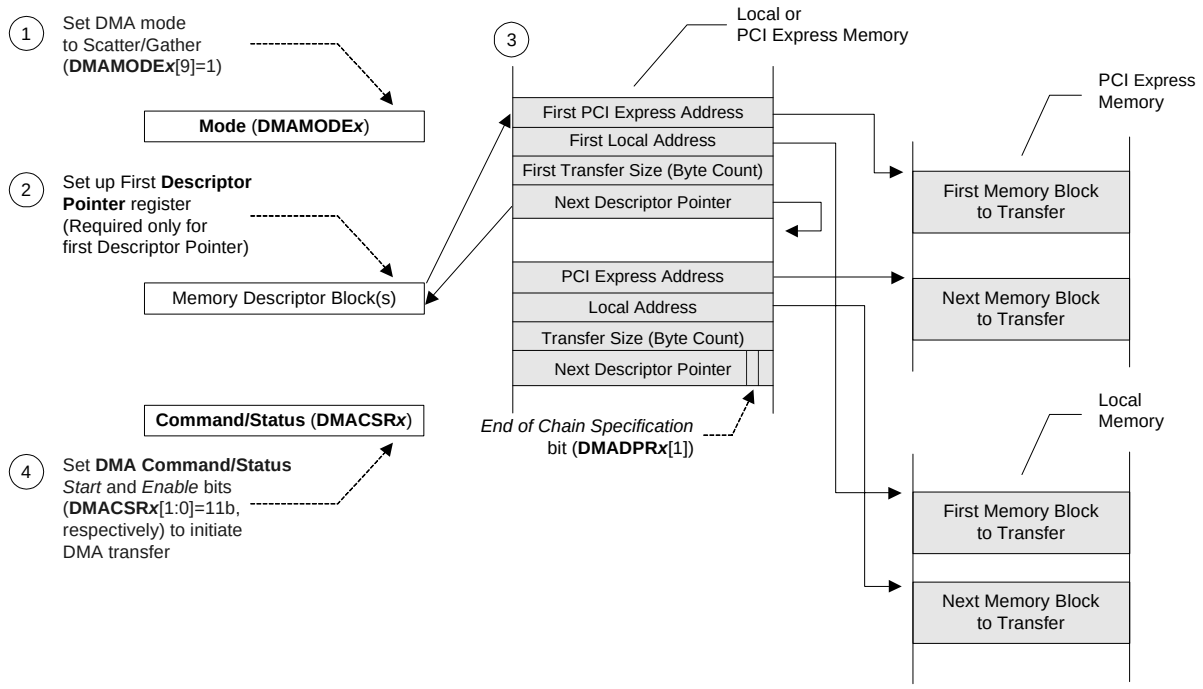


Figure 8-16. DMA Scatter/Gather Mode Descriptor Initialization [PCI Express Long Address Format (DMAMODE*x*[18]) Descriptor Dependent (PCI Express Address High Added)



8.5.4.2 DMA Clear Count Mode

The PEX 8311 supports DMA Clear Count mode (Write-Back feature, **DMAMODE*x***[16]). The PEX 8311 clears each transfer size descriptor to zero (0) by writing to its location on the PCI Express and/or Local Bus memory at the end of each transfer chain. This feature is available for DMA descriptors located on the PCI Express interface and Local Bus.

The DMA Clear Count mode can also be used in conjunction with the EOT feature (**DMAMODE*x***[14]). EOT# assertion during DMA Data transfers causes the PEX 8311 to write back the amount of data bytes not transferred to the destination bus.

When encountering a PCI Master/Target Abort internally between Local DMA Spaces and PCI Express Address Spaces or Unsupported Request/Completer Abort on the PCI Express interface on a DMA Data transfer, the PEX 8311 writes random values when the descriptor is on the Local Bus. No write occurs when the descriptor is on the PCI Express interface.

Note: *DMA Clear Count mode works only when there is more than one descriptor in the descriptor chain, because the first descriptor is written directly into the PEX 8311 DMA Configuration registers and the remainder are loaded from PCI Express or Local memory.*

8.5.4.3 DMA Ring Management (Valid Mode)

In DMA Scatter/Gather mode, when the *Ring Management Valid Mode Enable* bit(s) is cleared to 0 (**DMAMODE*x***[20]=0), the Valid bit(s) [bit(s) 31 of transfer count] is ignored. When the *Ring Management Valid Mode Enable bit(s)* is set to 1 (**DMAMODE*x***[20]=1), the DMA descriptor proceeds only when the *Ring Management Valid* bit(s) is set (**DMASIZ*x***[31]=1). When the Valid bit(s) is set, the transfer count is 0, the descriptor is not the last descriptor, and the DMA Controller(s) moves on to the next descriptor in the chain.

When the Ring Management Valid Stop Control bit(s) is cleared to 0 (**DMAMODE*x***[21]=0), the DMA Scatter/Gather Controller continuously polls the descriptor with the Valid bit(s) cleared to 0 (invalid descriptor) until the Valid bit(s) is read as 1, which initiates the DMA transfer. When the Valid bit(s) is read as 1, the DMA transfer begins. When the *Ring Management Valid Stop Control* bit(s) is set to 1 (**DMAMODE*x***[21]=1), the DMA Scatter/Gather Controller pauses when a Valid bit(s) with a value of 0 is detected. In this case, the processor must restart the DMA Controller(s) by setting the DMA Channel Start bit(s) (**DMACSR*x***[1]=1). The DMA Clear Count mode bit(s) must be enabled (**DMAMODE*x***[16]=1) for the Ring Management Valid bit(s) (**DMASIZ*x***[31]) to clear at the completion of each descriptor. (Refer to Figure 8-17 and/or Figure 8-18 for the DMA Ring Management descriptor load sequence for PCI Express Short and Long Address formats.)

Notes: *In DMA Ring Management Scatter/Gather mode, the descriptor includes the transfer size with a valid descriptor bit, PCI Express and Local Address Space, and next descriptor pointer. It also includes a PCI Express 64-bit Address value when the DAC Chain Load bit(s) is enabled (**DMAMODEx**[18]=1). Otherwise, the **DMADACx** register value is used.*

In Ring Management mode, the transfer size is loaded before the PCI Express address.

Figure 8-17. DMA Ring Management Scatter/Gather Mode Descriptor Initialization [PCI Express Short/Long Address Format PCI Express Address (DMADAC*x*) Register Dependent]

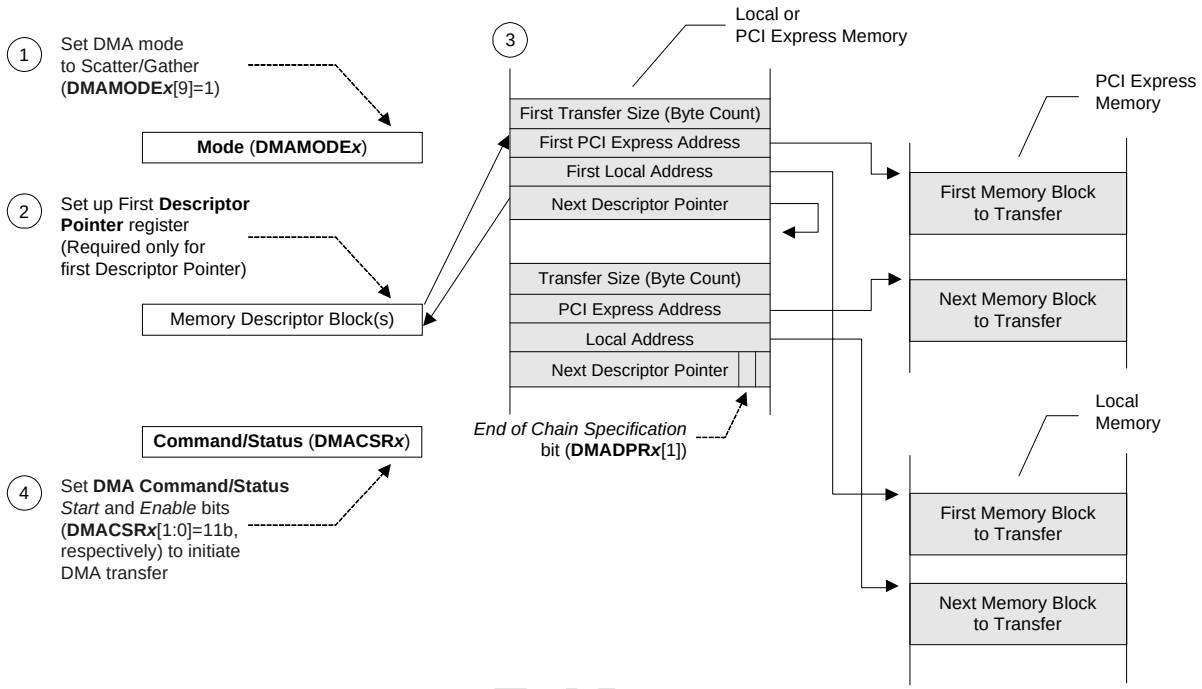
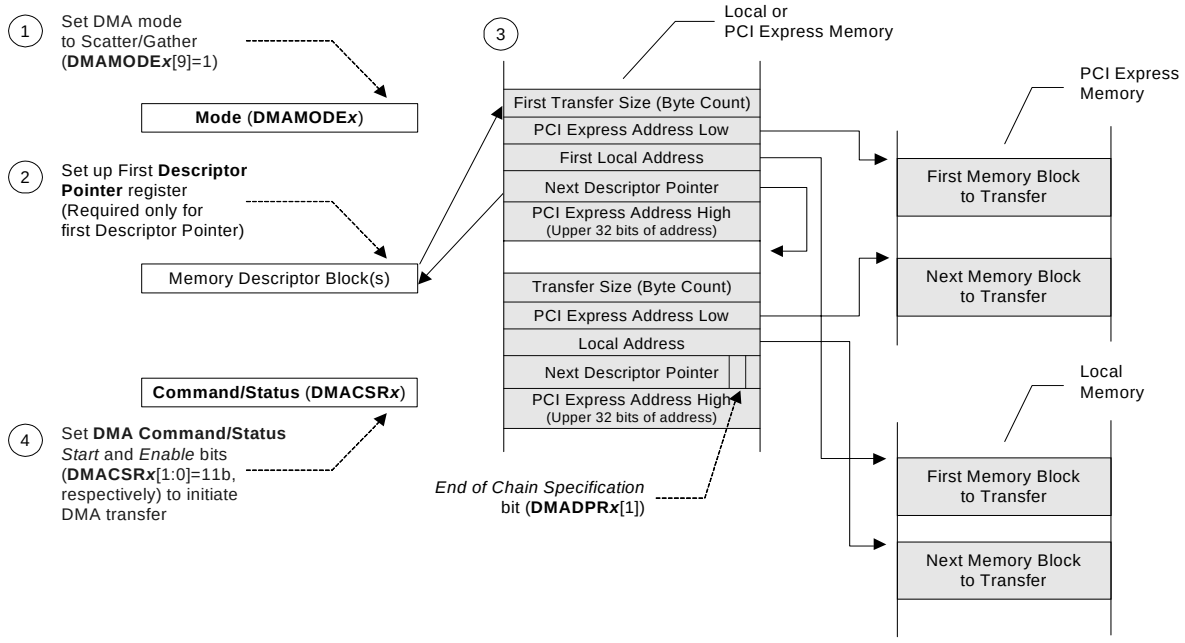


Figure 8-18. DMA Ring Management Scatter/Gather Mode Descriptor Initialization [PCI Express Long Address Format (DMAMODE*x*[18]) Descriptor Dependent (PCI Express Address High Added)



8.5.5 DMA Memory Write and Invalidate

The PEX 8311 can be programmed to perform Memory Write and Invalidate (MWI) cycles between Local DMA Spaces and PCI Express Address Spaces for DMA transfers, as well as Direct Master (Local-to-PCI Express) transfers. (Refer to Section 8.2.9.) The PEX 8311 supports MWI transfers for cache line sizes of 8 or 16 Dwords. Size is specified in the Local Bus register *System Cache Line Size* bits (**PCICLSR**[7:0]). When a size other than 8 or 16 is specified, the PEX 8311 performs Write transfers (using the Command Code programmed in **CNTRL**[7:4]), rather than MWI transfers. Internal MWI accesses to the PCI Express Spaces do not affect PEX 8311 TLP Write request generation and performance on the PCI Express interface.

DMA MWI transfers are enabled when the Memory Write and Invalidate Mode for DMA Transfers and the Memory Write and Invalidate Enable bits are set (**DMAMODE*x***[13]=1 and Local Bus register **PCICR**[4]=1, respectively).

In MWI mode, the PEX 8311 waits until the number of Dwords required for specified cache line size are read from the Local Bus before starting the internal access from Local DMA Space to PCI Express Address Space. This ensures a complete cache line write can complete in one internal transaction. When a PCI Express Space disconnects before internal cache line completes, the Local DMA Space completes the remainder of that cache line, using normal writes before resuming MWI transfers. When an MWI cycle is internally in progress, the PEX 8311 continues to burst when another cache line is read from the Local Bus before the cycle completes. Otherwise, the PEX 8311 terminates the burst and waits for the next cache line to be read from the Local Bus. When the final transfer is not a complete cache line, the PEX 8311 completes the DMA transfer, using normal writes.

An EOT# assertion, or DREQ*x*# de-assertion in DMA Demand mode occurring before the cache line is read from the Local Bus, results in a normal internal Write transaction from Local DMA Space to PCI Express Address Space write of the data read into a DMA FIFO. When the DMA Data transfer starts from a non-cache line boundary, it first performs normal writes until it reaches the cache line boundary internally within PEX 8311. When the DMA Data transfer possesses more than one line of data in the DMA FIFO, it starts the MWI transfer.

8.5.6 DMA Abort

DMA transfers can be aborted by software commands, or by issuing the EOT# signal. (Refer to Section 8.5.12 for further details about EOT#.)

To abort a DMA transfer:

1. Clear the DMA Channel Enable bit(s) (**DMACSR*x***[0]=0).
2. Abort the DMA transfer by setting the DMA Channel Abort bit(s) along with the corresponding DMA Channel Start bit(s) (**DMACSR*x***[2:1]=11b, respectively).
3. Wait until the DMA Channel Done bit(s) is set (**DMACSR*x***[4]=1).

Note: *One to two Data transfers occur after the Abort bit(s) is set. Software can simultaneously set **DMACSRx**[2:0]. Setting software commands to abort a DMA transfer when no DMA cycles are in progress causes the next DMA transfer to abort.*

8.5.7 DMA Channel Priority

The DMA Channel Priority bits (**MARBR**[20:19]) are used to specify the priorities listed in Table 8-9.

Table 8-9. DMA Channel Priority Bit Specifications

MARBR[20:19]	Channel Priority
00b	Rotating
01b	DMA Channel 0
10b	DMA Channel 1
11b	***Reserved***

8.5.8 DMA Channel *x* Interrupts

A DMA channel can generate PCI Express Wire Interrupt (INTA#) or MSI, as well as assert Local interrupts when done (transfer complete) or after a transfer is complete for the current descriptor in DMA Scatter/Gather mode. The DMA Channel Interrupt Select bit(s) determine whether to assert a PCI Express or Local interrupt (**DMAMODE*x***[17]=1 or 0, respectively). The PCI Express device or Local processor can read the DMA Channel Interrupt Active bit(s) to determine whether a DMA Channel interrupt is pending (**INTCSR**[22 and/or 21]=1).

The DMA Channel Done bit(s) (DMACSR*x*[4]) are used to determine whether an interrupt is one of the following:

- DMA Done interrupt
- Transfer complete for current descriptor interrupt

Setting **DMAMODE*x***[10]=1 enables a DMA Channel Done interrupt. In DMA Scatter/Gather mode, the Descriptor Pointer register Interrupt after Terminal Count bit(s) (**DMADPR*x***[2], loaded from Local memory) specifies whether to assert an interrupt at the end of the transfer for the current descriptor.

Setting **DMACSR*x***[3]=1 clears a DMA Channel interrupt.

8.5.9 DMA Data Transfers

The PEX 8311 DMA Controllers can be programmed to transfer data from the PCI Express-to-Local or Local-to-PCI Express, as illustrated in Figure 8-19 and Figure 8-20, respectively.

Figure 8-19. PCI Express-to-Local DMA Data Transfer Operation

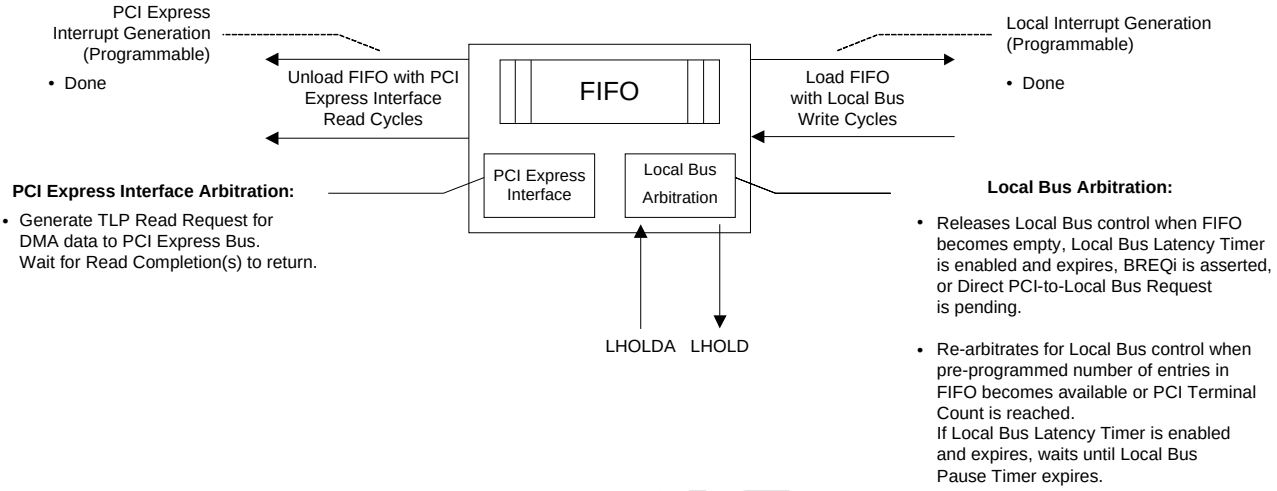
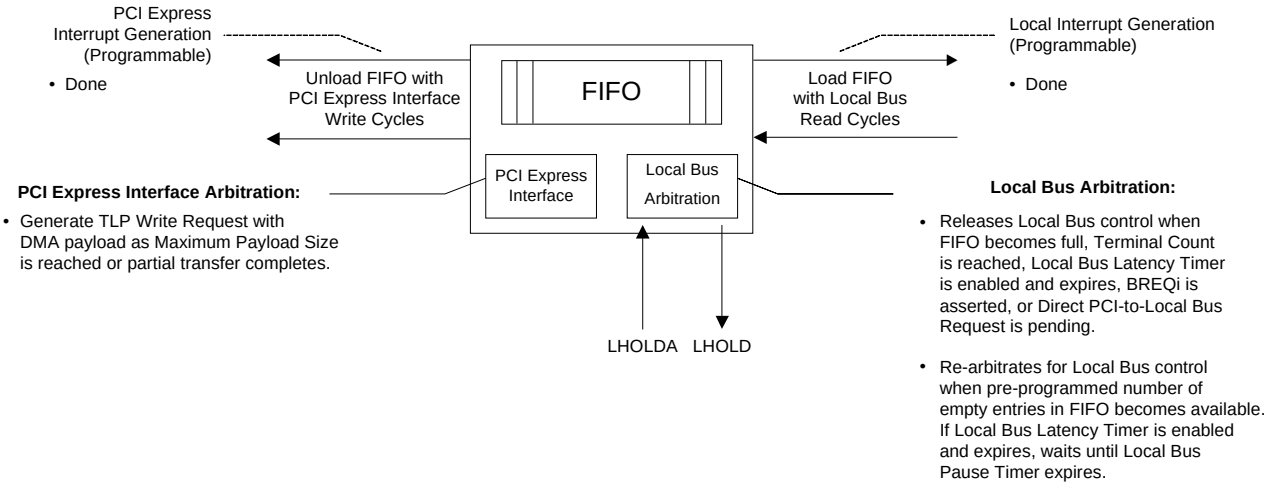


Figure 8-20. Local-to-PCI Express DMA Data Transfer Operation



8.5.10 DMA Unaligned Transfers

For unaligned Local-to-PCI Express transfers, the PEX 8311 reads a partial Dword from the Local Bus. It continues to read Dwords from the Local Bus. Dwords are assembled, aligned to the PCI Express interface address, and loaded into the FIFO, then the data is passed to the PCI Express Address Space for TLP Write request to generate.

For PCI Express-to-Local transfers, a TLP Read request is generated (PCI Express allows the first and the last data to unalign). As PCI Express Read Completion is received the data is passed from the PCI Express Space to Local DMA Space (FIFO), Dwords are assembled from the FIFO, aligned to the Local Bus address and written to the Local Bus.

The Byte Enables for writes determine least significant Address bits for the start of a transfer on the Local Bus, as well as on the internal bus between Local DMA and PCI Express Address spaces. For the last transfer, Byte Enables specify the bytes to write.

8.5.11 DMA Demand Mode, Channel *x*

DMA Demand mode allows the data transfer to be controlled by DREQ*x*# inputs. When DREQ*x*# is asserted, the PEX 8311 performs a DMA transfer, based on values in the DMA registers. DACK*x*# assertion indicates that the transfer is in progress on the Local Bus. Register settings for Fast/Slow Terminate and EOT modes modify the functionality of the DMA Demand Mode transfer when DREQ*x*# is asserted.

With 2 Dwords per each DMA FIFO location, DMA Demand mode single cycle (DREQ*x*# is toggled for one Local clock only), Local-to-PCI Express transfers require 2 Dwords to be read into the DMA FIFO from the Local Bus to guarantee successful data transfer to the PCI Express interface. DREQ*x*# assertion until DACK*x*# is asserted is recommended. PCI Express-to-Local Bus transfers (PCI Express Read request is generated) require a PCI Express Read Completion of 2 Dwords are returned by the PCI Express device to write into the DMA FIFO from the PCI Express interface, but only 1 Dword is transferred at a time by a single toggle of DREQ*x*#.

The unaligned Local-to-PCI Express DMA Demand mode transfer requires a minimum number of bytes to read on the Local Bus to generate a PCI Express Write request, which is determined by the PCI Express starting address. As a result, there can be seven or fewer bytes remaining in the DMA FIFO due to the nature of unaligned transfers. Further, at the start of a DMA Demand Mode transfer (DREQ*x*# asserted), it can become necessary to read more bytes on the Local Bus than are required on the PCI Express interface to start a DMA transfer. When bytes remain in the DMA FIFO, and DREQ*x*# assertion resumes, the data is transferred to the PCI Express interface. When the DREQ*x*# assertion never resumes for ongoing transfers, a DMA Abort procedure can be applied to flush the DMA FIFO.

During a PCI Express-to-Local Bus DMA Demand Mode transfer, the PEX 8311 generates PCI Express Read request and receives a Read Completion, independently of DREQ*x*# assertion. It then waits for DREQ*x*# assertion to arbitrate on the Local Bus. DACK*x*# de-assertion always indicates end of transfer. No data is written to the Local Bus when DACK*x*# is high. DREQ*x*# de-assertion before DACK*x*# assertion, but after LHOLD assertion, results in one Dword transfer to a Local Bus, with BLAST# assertion.

During a Local-to-PCI Express DMA Demand mode transfer, the PEX 8311 does not arbitrate on the Local Bus to read data into the DMA FIFO until DREQ*x*# is asserted. Due to the allocation of 2 Dwords per DMA FIFO location, reading of data into the DMA FIFO always occurs in 2-Dword quantities. Therefore, DREQ*x*# de-assertion causes the DMA Controller(s) to stop reading data into the DMA FIFO at the X0h or X8h Address boundary [Local Address LA[2:0]=000b (C mode) or LAD[2:0]=000b (J mode)]. DACK*x*# de-assertion always indicates end of transfer. No data is read from the Local Bus when DACK*x*# is high. The following are exceptions to the above, for transfers from starting addresses X0h and X8h:

- Destination PCI Express Address starts at X0h/X8h, and DREQ*x*# is asserted for one Local Bus period, which results in the DMA Controller(s) reading 2 Dwords into the DMA FIFO. This data is successfully transferred to the PCI Express interface.
- Destination PCI Express Address starts at X4h/XCh, and DREQ*x*# is asserted for one Local Bus period, which results in the DMA Controller(s) reading 1 Dword into the DMA FIFO. This data is successfully transferred to the PCI Express interface.
- Destination PCI Express Address starts at X0h/X8h, and DREQ*x*# is de-asserted after reading 4 Dwords into the DMA FIFO, which results in the DMA Controller(s) reading two additional Dwords into the DMA FIFO. Read data is successfully transferred to the PCI Express interface.
- Destination PCI Express Address starts at X0h/X8h, and DREQ*x*# is de-asserted after reading 5 Dwords into the DMA FIFO, which results in the DMA Controller(s) reading two additional Dwords into the DMA FIFO. Read data is successfully transferred to the PCI Express interface.
- Destination PCI Express Address starts at X4h/XCh, and DREQ*x*# is de-asserted after reading 4 Dwords into the DMA FIFO, which results in the DMA Controller(s) reading one additional Dword into the DMA FIFO. Read data is successfully transferred to the PCI Express interface.
- Destination PCI Express Address starts at X4h/XCh, and DREQ*x*# is de-asserted after reading 5 Dwords into the DMA FIFO, which results in the DMA Controller(s) reading two additional Dwords into the DMA FIFO. Read data is successfully transferred to the PCI Express interface.

DREQ*x*# controls only the number of Dword transfers. For an 8-bit bus, the PEX 8311 releases the bus after transferring the last byte for the Dword. For a 16-bit bus, the PEX 8311 releases the bus after transferring the last word for the Dword.

When the DMA Local-to-PCI Express FIFO is full, DREQ*x*# assertion is ignored and subsequent transfers do not occur until DACK*x*# is re-asserted.

8.5.11.1 Fast Terminate Mode Operation

The Fast/Slow Terminate Mode Select bit(s) (**DMAMODE*x***[15]) determines the number of Dwords to transfer after the DMA Controller(s) DREQ*x*# input is de-asserted. In Fast Terminate mode (**DMAMODE*x***[15]=1) (*that is*, BLAST# output is ***not*** required for the last Dword of a DMA transfer), the DMA Controller releases the Data Bus only when Local Address [Local Address LA[2:0]=000b (C mode) or LAD[2:0]=000b (J mode), X0h or X8h], DREQ*x*#=1 (de-asserted), and external READY#=0 (asserted), or the internal Wait State Counter(s) decrements to 0 for the current Dword. When the DMA Controller is currently bursting data, which is not the last Data phase for the burst, BLAST# is ***not*** asserted.

When DREQ*x*# is de-asserted during a PCI Express-to-Local Bus DMA transfer, the PEX 8311 pauses the DMA transfer on the Local Bus after DREQx# is de-asserted, followed by a single 1-Dword transfer without BLAST# assertion. EOT# assertion (along with DREQ*x*# de-assertion) causes the PEX 8311 to immediately terminate the ongoing Data transfer and flush the DMA FIFO, without BLAST# being asserted.

- DREQ*x*# assertion for one Local clock period or de-assertion for two Local clock periods after DACK*x*# assertion, results in one Dword transfer to a Local Bus, without BLAST# assertion, respectively.
- DREQ*x*# de-assertion, three or more Local clock periods after DACK*x*# assertion, results in two or more Dword transfers to a Local Bus, without BLAST# assertion, respectively. BLAST# is asserted only at the last Data transfer of the DMA Transfer Size, Local Bus Latency Timer expires, or at the EOT# transfer termination.

When DREQ*x*# is de-asserted during a Local-to-PCI Express DMA transfer, the PEX 8311 pauses the DMA transfer on the Local Bus with 1- or 2-Dword (when DREQ*x*# de-asserted on the Qword boundary) transfers after DREQ*x*# de-asserted without BLAST# assertion. EOT# assertion (along with DREQ*x*# de-assertion) causes the PEX 8311 to immediately terminate the ongoing Data transfer and flush the DMA FIFO, without BLAST# being asserted.

- DREQ*x*# assertion for one Local clock period or de-assertion for three Local clock periods after DACK*x*# assertion, results in two Dword transfers to the PCI Express interface, without BLAST# assertion, respectively.
- DREQ*x*# de-assertion, four Local clock periods after DACK*x*# assertion, results in four Dword transfers (the PEX 8311 receives the Qword base amount of data) to the PCI Express interface, without BLAST# assertion, respectively.

8.5.11.2 Slow Terminate Mode Operation

In Slow Terminate mode (**DMAMODE*x***[15]=0) (*that is*, BLAST# output is required for the last Dword of the DMA transfer), the DMA Controller(s) handles a Data transfer differently between the PCI Express-to-Local versus Local-to-PCI Express direction.

When DREQ*x*# is de-asserted during a PCI Express-to-Local Bus DMA transfer, the PEX 8311 pauses the DMA transfer on the Local Bus with two additional Dword transfers after DREQ*x*# is de-asserted, with BLAST# being asserted at the last data. EOT# assertion (along with DREQ*x*# de-assertion) causes the PEX 8311 to pause the DMA transfer on the Local Bus with one additional Dword transfer to terminate the ongoing Data transfer and flush the DMA FIFO, with BLAST# being asserted at the last data.

- DREQ*x*# assertion for one Local clock period or de-assertion at the Local clock period of DACK*x*# assertion results in one Dword transfer to the Local Bus, with BLAST# assertion, respectively.
- DREQ*x*# de-assertion, one or more Local clock periods after DACK*x*# assertion, results in two or more Dword transfers to a Local Bus, with BLAST# assertion, respectively.

When DREQ*x*# is de-asserted during a Local-to-PCI Express DMA transfer, the PEX 8311 pauses the DMA transfer on the Local Bus after DREQ*x*# is de-asserted, followed by two Dword transfers, with BLAST# being asserted at the last data. EOT# assertion (along with DREQ*x*# de-assertion) causes the PEX 8311 to pause the DMA transfer on the Local Bus with one additional Dword transfer to terminate the ongoing Data transfer and flush the DMA FIFO, with BLAST# being asserted at the last data.

- DREQ*x*# assertion for one Local clock period or de-assertion for two Local clock periods after DACK*x*# assertion, results in two Dword transfers to the PCI Express interface, with BLAST# assertion, respectively.
- DREQ*x*# de-assertion, three or more Local clock periods after DACK*x*# assertion, results in three or more Dword transfers to the PCI Express interface, with BLAST# assertion, respectively.

8.5.12 End of Transfer (EOT#) Input

EOT# is a one-clock wide pulse that ends a DMA transfer. Assert only when the PEX 8311 owns the Local Bus. Depending on whether Fast or Slow Terminate mode is selected, the DMA transfer ends without a BLAST# assertion (Fast Terminate mode) or with BLAST# asserted (Slow Terminate mode). The **DMAMODE*x***[15:14] bits enable and control how the PEX 8311 responds to an EOT# input assertion.

In Fast Terminate mode, when EOT# is asserted while the PEX 8311 receives an external READY# signal assertion, the DMA Controller(s) ends the DMA transfer and releases the Local Bus. In Slow Terminate mode, when EOT# is asserted while the PEX 8311 receives an external READY# signal assertion, the DMA Controller(s) completes the current Dword and one additional Dword. When the DMA FIFO is full or empty after the Data phase in which EOT# is asserted, the second Dword is not transferred.

When the PEX 8311 does not require that BLAST# output be driven for the last data transferred when a DMA transfer is terminated using EOT#, the Fast Terminate mode setting (**DMAMODE*x***[15]=1) can be used. When EOT# is asserted in Fast Terminate mode, the DMA Controller(s) terminates the DMA transfer and releases the Local Bus upon receiving an external READY# signal assertion. Or, the internal Wait State Counter(s) decrements to 0 for the current Dword when EOT# is asserted. When the data is the last data in the transfer, BLAST# is asserted on the last transfer.

When the PEX 8311 requires that BLAST# output be asserted on the last data transfer when a DMA transfer is terminated using EOT#, then the Slow Terminate mode setting (**DMAMODE*x***[15]=0) must be used. When EOT# is asserted in Slow Terminate mode, the DMA Controller(s) transfers one or two additional Dwords, depending upon the Local Bus data width and the address when EOT# is asserted.

The DMA Controller(s) terminates a transfer on a Dword boundary after EOT# is asserted. For an 8-bit bus, the PEX 8311 terminates after transferring the last byte for the Dword. For a 16-bit bus, the PEX 8311 terminates after transferring the last word for the Dword.

During the descriptor loading on the Local Bus, EOT# assertion causes a complete descriptor load and no subsequent Data transfer; however, this is ***not*** recommended. EOT# has no effect when loading the descriptor from the PCI Express interface.

8.5.13 DMA Arbitration

The PEX 8311 DMA Controller(s) releases control of the Local Bus (de-asserts LHOLD) when the following conditions occur:

- Local Bus Latency Timer is enabled (MARBR[16]=1) and expires (**MARBR**[7:0])
- BREQi is asserted (BREQi is enabled or disabled, or gated with a Local Bus Latency Timer before the PEX 8311 releases the Local Bus)
- Direct Slave (direct PCI Express-to-Local Bus) access is pending
- EOT# input is received (when enabled)

The DMA Controller(s) releases control of the internal interface between Local DMA and PCI Express Address Space when one of the following conditions occurs:

- FIFOs are full or empty
- Bus Latency Timer expires (**PCILTR**[7:0])
- Target disconnect response is received

The DMA Controller(s) internally de-asserts REQ# for a minimum of two internal clocks.

8.5.14 Local Bus DMA Priority

The PEX 8311 supports programmable Local Bus arbitration priority for DMA Channel 0 and Channel 1, when both channels are active (priority set with **MARBR**[20:19]). DMA Block and Scatter/Gather modes have priority over DMA Demand mode. DMA transfer direction does ***not*** influence DMA channel priority.

There are three types of priorities:

- **Channel 0 Priority** – DMA Channel 0 completes the transfer on the Local Bus before Channel 1. If Channel 1 is performing a Data transfer, with Channel 0 set as highest priority and started, Channel 1 continues its transfer until the Local Bus Latency Timer (**MARBR**[7:0]) expires, preempted by a Direct Slave Data transfer, or another termination occurs (EOT# assertion, DREQx# de-assertion, or BREQi# assertion). Channel 0 then owns the Local Bus until transfer completion, before Channel 1 can continue the interrupted transfer, unless Channel 1 previously completed its transfer.
- **Channel 1 Priority** – DMA Channel 1 completes its transfer on the Local Bus before Channel 0. If Channel 0 is performing a Data transfer, with Channel 1 set as highest priority and started, Channel 0 continues its transfer until the Local Bus Latency Timer expires, preempted by a Direct Slave Data transfer, or another termination occurs (EOT# assertion, DREQx# de-assertion, or BREQi# assertion). Channel 1 then owns the Local Bus until transfer completion, before Channel 0 can continue the interrupted transfer, unless Channel 0 previously completed its transfer.

- **Rotational Priority** – Depends on the transfer direction, however, when the starting bus is the same for both DMA channels, in the freshly started DMA, Channel 0 always starts first. Rotational priority does not start unless the ongoing DMA channel Data transfer is interrupted by the Local Bus Latency Timer expiration, preempted by a Direct Slave Data transfer, or another termination occurs (EOT# assertion, DREQx# de-assertion, or BREQi# assertion). The other DMA channel then owns the Local Bus until the previously described interrupts or terminations occur. Rotational priority occurs each time a DMA channel loses Local Bus ownership, unless one of the DMA channels previously completed its transfer.

8.5.15 Local Bus Latency and Pause Timers

The Local Bus Latency and Pause Timers are programmable with the Mode/DMA Arbitration register (**MARBR**[7:0, 15:8], respectively). When the Local Bus Latency Timer is enabled (**MARBR**[16]=1) and expires (**MARBR**[7:0]), the PEX 8311 completes the current Dword transfer and releases LHOLD. After its programmable Pause Timer expires, the PEX 8311 reasserts LHOLD. The PEX 8311 continues to transfer when it receives LHOLDA.

The DMA transfer is paused by writing 0 to the Channel Enable bit(s) (**DMACSR*x***[0]=0). To acknowledge the disable, the PEX 8311 receives at least one data from the bus before it stops. However, this is ***not*** recommended during a burst.

The DMA Local Bus Latency Timer starts after the Local Bus is granted to the PEX 8311, and the Local Bus Pause Timer starts after the external Local Bus Arbiter de-asserts LHOLDA.

8.5.16 DMA FIFO Programmable Threshold

The PEX 8311 supports programmable DMA FIFO threshold (**DMATHR**). The **DMATHR** register can be programmed with any of four different FIFO Full/Empty conditions, for DMA Channel 0 and/or Channel 1, as listed in Table 8-10. (Refer to the **DMATHR** register and Table 19-9, "DMA Threshold Nybble Values," for further details.)

Table 8-10. DMATHR FIFO Threshold

DMA Transfer	Condition	Description
PCI Express-to-Local	DMA Channel *x* FIFO Almost Full	Number of full (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the Local Bus for writes.
	DMA Channel *x* FIFO Almost Empty	Number of empty (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the PCI Express Address to initiate TLP Read requests on the PCI Express interface.
Local-to-PCI Express	DMA Channel *x* FIFO Almost Full	Number of full (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the PCI Express Address to initiate TLP Write requests on the PCI Express interface.
	DMA Channel *x* FIFO Almost Empty	Number of empty (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the Local Bus for reads.

8.5.17 DMA Internal Interface Master/Target Abort

The following describes how the PEX 8311 logic handles internal Master/Target Abort between Local and PCI Express Spaces, as well as Unsupported Requests and Completion Aborts received on the PCI Express interface.

During a DMA transaction on the PCI Express interface and upon encountering either internal Master/Target Abort between Local DMA and PCI Express Address space, or receiving PCI Express UR/CA, the PEX 8311 Master/Target Abort logic enables the PEX 8311 to successfully recover during transfers. The Local Bus Master must clear the Received Master or Target Abort bit (**PCISR**[13 or 12]=0, respectively) and continue by processing the next task as they get set when Aborts are encountered. Not clearing the bit prevents the PEX 8311 from initiating PCI Express transactions.

If internal to the PEX 8311, a Master/Target Abort or 256 consecutive Master Retry timeout to the PCI Express Address Spaces is encountered during a transfer, the PEX 8311 asserts LSERR#, when enabled [**INTCSR**[0]=1, which can be used as a Non-Maskable Interrupt (NMI)]. (Refer to Chapter 10, "Error Handling," for error handling behavior.) The PEX 8311 also flushes internal Master FIFOs (DMA and Direct Master).

The PEX 8311 DMA channels function independently when a Master/Target Abort occurs. When one DMA channel encounters a Master/Target Abort, the FIFO on the aborted channel is flushed. PCI Express transactions initiation capabilities for both DMA channels are disabled until the Received Master/Target Abort bits are cleared (Local Bus register **PCISR**[13:12]=00b, respectively). However, when the second DMA channel begins a new operation while the first DMA channel is receiving an internal Master/Target Abort, the FIFO contents of the second DMA channel are not affected, and its new or pending Direct Master operations successfully complete. (For details about Direct Master Master/Target Abort, refer to Section 8.2.8.)

Note: *In applications in which both DMA channels are utilized and one of the DMA channels encounters an internal Master/Target Abort, clear the Received Master/Target Abort bits (PCISR[13:12]=00b, respectively) and allow the non-aborted DMA channel to complete its Data transfer before the aborted DMA channel's registers are re-initialized and the transfer restarted.*

If internal Master/Target Abort is encountered during a DMA transfer, the PEX 8311 stores the Abort Address into **PABTADR**[31:0]. **PABTADR** contents are updated for each internal Master/Target Abort. Read and clear the Received Master/Target Abort bits before starting a new DMA or Direct Master, Type 0 or Type 1 Configuration transfer (Root Complex mode only).

Table 8-11 delineates special internal Master/Target Abort conditions for DMA mode Data transfers between Local DMA and PCI Express Address spaces.

Table 8-11. DMA Mode Data Transfer Special PCI Express/Master/Target Abort Conditions

DMA Mode Data Transfer Type	PCI Express Master/Target Abort Condition
DMA Local-to-PCI Express in Slow Terminate Mode (**DMAMODE*x***[15]=0	After encountering an internal Master/Target Abort, the PEX 8311 immediately terminates data transfer internally between Local DMA and PCI Express Address Spaces and continues reading additional data from the Local Bus into the DMA Local-to-PCI Express FIFO until its full or transfer count is reached. (Refer to the **DMATHR** register.) The PEX 8311 then sets the DMA Channel Done bit (**DMACSR*x***[4]=1) and the Received Master/Target Abort bits are cleared (**PCISR**[13:12]=00b, respectively).
DMA Local-to-PCI Express in Fast Terminate Mode (**DMAMODE*x***[15]=1)	After encountering an internal Master/Target Abort between Local DMA and PCI Express Address Spaces, the PEX 8311 immediately terminates data transfer on the internal and Local Buses and sets the DMA Channel Done bit (**DMACSR*x***[4]=1).
DMA PCI Express-to-Local Independent of Fast/Slow Terminate Mode (**DMAMODE*x***[15]=0 or 1)	After encountering an internal Master/Target Abort between Local DMA and PCI Express Address Spaces, the PEX 8311 immediately terminates a Burst Data transfer on the Local Bus and single cycles data from the DMA PCI Express-to-Local FIFO until it is empty.
DMA Local-to-PCI Express, with EOT# assertion on the Local Bus	Upon encountering an internal Master/Target Abort internally between Local DMA and PCI Express Address Spaces with EOT# assertion on the Local Bus, the PEX 8311 terminates data transfer on the internal and Local Buses and sets the DMA Channel Done bit (**DMACSR*x***[4]=1).
DMA PCI Express-to-Local, with EOT# assertion on the Local Bus	Upon encountering an internal Master/Target Abort internally between Local DMA and PCI Express Address Spaces with EOT# assertion on the Local Bus, the PEX 8311 flushes the DMA PCI Express-to-Local FIFO before encountering the Master/Target Abort.
DMA PCI Express-to-Local Scatter/Gather, Ring Management with EOT# assertion on the Local Bus	With the EOT# function enabled (**DMAMODE*x***[14]=1), EOT# End Link enabled (**DMAMODE*x***[19]=1), and the DMA Descriptor Links located on the Local Bus, the PEX 8311 starts the DMA Descriptor load and then transfers data after the DMA Channel Enable and Start bits are set (**DMACSR*x***[0:1]=11b, respectively). Upon receiving the internal Target Abort between Local DMA and PCI Express Address Spaces and EOT# assertion on the Local Bus during a DMA Scatter/Gather PCI Express-to-Local Data transfer, the PEX 8311 pauses the transfer in response to the Target Abort. The PEX 8311 then flushes the DMA FIFO and sets the DMA Channel Done bit (**DMACSR*x***[4]=1) after sampling EOT# asserted. No further DMA Descriptor load is performed after the Received Target Abort bit is cleared (**PCISR**[12]=0), and the DMA Scatter/Gather transfer is terminated.

8.5.18 Local Bus DMA Data Transfer Modes

The PEX 8311 supports C and J modes with three Local Bus Data Transfer modes:

- Single Cycle
- Burst-4
- Continuous Burst

Single Cycle mode is the default Data Transfer mode. Continuous Burst mode provides the highest throughput.

Table 8-12 delineates the register settings used to select Local Bus Data Transfer modes. It also indicates the data quantity transferred per Address Cycle (ADS#).

Note: *The term* Burst Forever *was formerly used to describe* Continuous Burst.

Table 8-12. Local Bus Data Transfer Modes

Mode	Burst Enable Bit	BTERM# Input Enable Bit	Result
Single Cycle (default)	0	X	One ADS# per data.
Burst-4	1	0	One ADS# per four Data cycles (recommended for i960 and PPC401).
Continuous Burst	1	1	One ADS# per data burst or until BTERM# is asserted.

Note: *"X" is "Don't Care."*

8.5.18.1 Single Cycle Mode

Single Cycle mode is the default Data Transfer mode. In Single Cycle mode, the PEX 8311 issues one ADS# per data cycle. The starting address for a single cycle Data transfer is on any address.

For single cycle Data transfers, Burst mode is disabled (**DMAMODE*x***[8]=0 for Channel *x*). For a 32-bit Local Bus, when a starting address in a DMA PCI Express-to-Local transfer is ***not*** aligned to a Dword boundary, the PEX 8311 performs a single cycle until the next Dword boundary.

Partial Data Accesses

Partial Data accesses (not all Byte Enables are asserted) are broken into single cycles. When there is remaining data that is ***not*** Dword-aligned during DMA PCI Express-to-Local transfers, it results in a single cycle Data transfer.

8.5.18.2 Burst-4 Mode

Burst-4 mode forces the PEX 8311 to perform Data transfers as bursts of four Data cycles (4 Dwords, four 16-bit words, or 4 bytes to a 32-, 16-, or 8-bit bus, respectively).

Burst-4 mode Data transfers are set up by enabling bursting and clearing the BTERM# Input Enable bit(s) (**DMAMODE*x***[8:7]=10b for Channel *x*, respectively).

Burst-4 mode bursting starts on any data boundary and bursts to the next four-data boundary. The first burst starts on any address and moves to the data boundary. The next bursts are four Data cycles. The first or last burst can be less than four Data cycles. The PEX 8311 can continue to burst by asserting ADS# and performing another burst. For a 32-bit Local Bus, when a starting address in a DMA PCI Express-to-Local transfer is ***not*** aligned to a Dword boundary, the PEX 8311 performs a single cycle until the next Dword boundary. (Refer to Table 8-13.)

For DMA, when Burst-4 mode is implemented with Address Increment disabled (**DMAMODE*x***[11]=1), the PEX 8311 defaults to Continuous Burst mode.

Table 8-13. Burst-4 Mode

Local Bus Data Width	Burst-4
32 bit	4 Dwords start/stop at a 4-Dword boundary
16 bit	4 words start/stop at a 4-word boundary
8 bit	4 bytes start/stop at a 4-byte boundary

Note: *The first or last burst can be less than four Data cycles.*

Partial Data (<4 Bytes) Accesses

Partial Data accesses occur when either the first, last, or both PCI Express data are unaligned, Byte Enable Field are ***not*** all asserted. For a 32-bit Local Bus, they are broken in single cycles until the next Dword boundary.

8.5.18.3 Continuous Burst Mode

Continuous Burst mode enables the PEX 8311 to perform data bursts of longer than four Data cycles. However, special external interface devices are required that can accept bursts longer than four Data cycles.

Continuous Burst mode Data transfers are set up by enabling bursting and setting the BTERM# Input Enable bit(s) (**DMAMODE*x***[8:7]=11b for Channel *x*, respectively).

The PEX 8311 asserts one ADS# cycle and continues to burst data. When a Slave device requires a new Address cycle (ADS#), it can assert the BTERM# input. The PEX 8311 completes the current Data transfer and stops the burst. The PEX 8311 continues the transfer by asserting ADS# and beginning a new burst at the next address.

For DMA, when Burst-4 mode is implemented with Address Increment disabled (**DMAMODE*x***[11]=1), the PEX 8311 defaults to Continuous Burst mode.

8.5.18.4 Local Bus Read Accesses

For Single Cycle Local Bus Read accesses, when the PEX 8311 is the Local Bus Master, the PEX 8311 reads only bytes corresponding to Byte Enables requested by the PCI Express Read request initiator. For Burst Read cycles, the PEX 8311 passes all bytes and is programmed to:

- Prefetch
- Perform Direct Slave Read Ahead mode
- Generate internal wait states
- Enable external wait control (READY# input)
- Enable type of Burst mode to perform

8.5.19 Local Bus Write Accesses

For Local Bus writes, only bytes specified by a PCI Express transaction initiator or PEX 8311 DMA Controller(s) are written.

8.5.20 Direct Slave Accesses to 8- or 16-Bit Local Bus

PCI Express access to an 8- or 16-bit Local Bus results in the Local Data being broken into multiple Local Bus width transfers. For each transfer, Byte Enables are encoded to provide Local Address bits C mode, LA[1:0]. In J mode, LAD[1:0] also provide these Address bits during the Address phase.

8.5.21 Local Bus Data Parity

Generation or use of Local Bus data parity is optional. The Local Bus Parity Check is passive and provides only parity information to the Local processor during DMA transfers.

There is one data parity ball for each byte lane of the PEX 8311 data bus (DP[3:0]). “Even data parity” is asserted for each lane during Local Bus reads from the PEX 8311 and during PEX 8311 Master writes to the Local Bus.

Even data parity is checked for DMA Local Bus reads. When an error is detected during DMA Local-to-PCI Express transfer, the PEX 8311 sets the Local Data Parity Check Error Status bit (INTCSR[7]=1) and asserts an interrupt (LSERR#), when enabled (**INTCSR**[0, 6]=11b, respectively). This occurs in the Clock cycle following the data being checked.

For applications in which READY# is disabled in the PEX 8311 registers, an external pull-down resistor is required for READY# to allow **INTCSR**[7] and the LSERR# interrupt to be set and asserted, respectively.

8.6 Response to Local Bus FIFO Full or Empty

Table 8-14 delineates the PEX 8311 response to full and empty Local Bus FIFOs.

Table 8-14. Response to Local Bus FIFO Full or Empty

Mode	Data Direction	FIFO	PCI Express Interface	Local Bus
Direct Master Write	Local-to-PCI Express	Full	Normal	De-asserts READY#
		Empty	Normal	Normal
Direct Master Read	PCI Express-to-Local	Full	Normal	Normal
		Empty	Normal	De-asserts READY#
Direct Slave Write	PCI Express-to-Local	Full	Normal	Normal
		Empty	Normal	De-asserts LHOLD or retains the Local Bus, asserts BLAST#[a]
Direct Slave Read	Local-to-PCI Express	Full	Normal	De-asserts LHOLD or retains the Local Bus, asserts BLAST#[a]
		Empty	Normal	Normal
DMA	Local-to-PCI Express	Full	Normal	Asserts BLAST#, de-asserts LHOLD[b]
		Empty	Normal	Normal
	PCI Express-to-Local	Full	Normal	Normal
		Empty	Normal	Asserts BLAST#, de-asserts LHOLD[b]

*a. LHOLD de-assertion depends upon the Local Bus Direct Slave Release Bus Mode bit being set (**MARBR**[21]=1).*

*b. BLAST# de-assertion depends upon the DMA Channel x Fast/Slow Terminate Mode Select bit setting (**DMAMODEx**[15]).*

Chapter 9 Configuration Transactions

9.1 Introduction

Configuration requests are initiated only by the Root Complex in a PCI Express-based system. PCI Express devices maintain a Configuration space that is accessed by way of Type 0 and Type 1 Configuration transactions:

- Type 0 Configuration transactions are used to access the internal **PECS** registers (Type 0 registers). The PCI Express Memory-Mapped transactions are used to accesses the Device-Specific registers through the **PECS PCIBAR0** register.
- Type 1 Configuration transactions are used to access the PEX 8311 internal **LCS PCI** registers in Endpoint mode. In addition, Type 1 Configuration transactions are used to access PEX 8311 downstream devices in Root Complex mode. To access **LCS Control** registers (**Local**, **Runtime**, **DMA**, and **Messaging Queue**), Memory- or I/O-Mapped transactions are used in the **LCS PCIBAR0** or **PCIBAR1** registers, respectively, in Endpoint mode. The Local Bus Master can access all **LCS** registers in Endpoint or Root Complex mode, with the CCS# signal asserted during the Local Address phase.

Table 9-1 through Table 9-4 delineate Configuration address formatting.

Table 9-1. PCI Express

31 24	23 19	18 16	15 12	11 8	7 2	1 0
Bus Number	Device Number	Function Number	*Rsvd*	Extended Register Address	Register Address	*Rsvd*

Table 9-2. Internal Type 0 (at Initiator)

31 16	15 11	10 8	7 2	1 0
Device Number single-bit decoding	*Rsvd*	Function Number	Register Number	0 0

Table 9-3. Internal Type 0 (at Target)

31 11	10 8	7 2	1 0
Rsvd	Function Number	Register Number	0 0

Table 9-4. Internal Type 1

31 24	23 16	15 11	10 8	7 2	1 0
Rsvd	Bus Number	Device Number	Function Number	Register Number	0 1

9.2 Type 0 Configuration Transactions

The PEX 8311 only responds to Type 0 Configuration transactions on the PCI Express interface (Endpoint mode). A Type 0 Configuration transaction is used to configure the PCI Express Configuration space, and is not forwarded to the PEX 8311 Local Configuration space. The PEX 8311 ignores Type 0 Configuration transactions from downstream devices. Type 0 Configuration transactions always result in the transfer of one DWORD.

A Type 1 Configuration transaction is used to configure the Local Configuration space.

When Configuration Write data is poisoned, the data is discarded and a Non-Fatal Error message is generated, when enabled.

9.3 Type 1 Configuration Transactions

Type 1 Configuration transactions are used for device configuration in a hierarchical bus system. Bridges and switches are the only types of devices that respond to Type 1 Configuration transactions.

Type 1 Configuration transactions are used when the transaction is intended for a device residing on a bus other than the one from which the Type 1 request is issued. The PEX 8311 only responds to Type 1 Configuration transactions on the PCI Express interface (Endpoint mode) when the transactions are to the PEX 8311 **LCS PCI** registers. Type 1 PCI Express Configuration transactions are internally converted to Type 0 Configuration transaction.

The *Bus Number* field in a Configuration Transaction request specifies a unique bus in the hierarchy on which the transaction target resides. The bridge compares the specified bus number with the **Secondary Bus Number** and **Subordinate Bus Number** registers to determine whether to forward a Type 1 Configuration transaction across the bridge.

When a Type 1 Configuration transaction is received on the upstream interface, the following tests are applied, in sequence, to the *Bus Number* field to determine how the transaction is handled:

- If the *Bus Number field* is equal to the **Secondary Bus Number** register value, and the conditions for converting the transaction into a special cycle transaction are met, the PEX 8311 forwards the Configuration request to the downstream device (secondary interface) as a special cycle transaction. If the conditions are not met, the PEX 8311 forwards the Configuration request to the downstream device as a Type 0 Configuration transaction.
- If the *Bus Number* field is not equal to the **Secondary Bus Number** register value but is within the range of the **Secondary Bus Number** and **Subordinate Bus Number** (inclusive) registers, the Type 1 Configuration request is specifying a bus located behind the bridge. In this case, the PEX 8311 forwards the Configuration request to the downstream device as a Type 1 Configuration transaction.
- If the *Bus Number* field does not satisfy the above criteria, the Type 1 Configuration request is specifying a bus that is not located behind the bridge. In this case, the Configuration request is invalid.
  - If the upstream interface is PCI Express, a completion with Unsupported Request status is returned.
  - If the upstream interface is Local, the Configuration request is internally ignored, resulting in a Master Abort. LSERR# is asserted on the Local Bus, when enabled (INTCSR[0]).

Note: *The primary interface is the PCI Express interface in Endpoint mode, and the Local Bus interface in Root Complex mode.*

The secondary interface is the Local Bus interface in Endpoint mode, and the PCI Express interface in Root Complex mode.

9.4 Type 1-to-Type 0 Conversion

The PEX 8311 performs a Type 1-to-Type 0 conversion when the Type 1 transaction is generated on the primary interface and is intended for a device attached directly to the downstream bus (*for example*, PCI Express Type 1 Configuration accesses to the **LCS PCI** registers are internally converted to Type 0 accesses). The PEX 8311 must convert the Type 1 Configuration transaction to Type 0 for the device to respond to it.

Type 1-to-Type 0 conversions are performed only in the downstream direction. The PEX 8311 only generates Type 0 configuration transactions on the secondary interface, never on the primary interface.

Note: *The primary interface is the PCI Express interface in Endpoint mode, and the Local Bus in Root Complex mode.*

The secondary interface is the Local Bus interface in Endpoint mode, and the PCI Express interface in Root Complex mode.

9.4.1 Endpoint Mode

The PEX 8311 internally forwards a Type 1 transaction on the PCI Express interface to a Type 0 transaction, to provide accessibility to the **LCS PCI** registers when the following are true:

- Type 1 *Bus Number* field of the Configuration request is equal to the **Secondary Bus Number** register value
- Conditions for conversion to a special cycle transaction are not met

The PEX 8311 then performs the following on the Local Bus interface:

1. Clears Address bits AD[1:0] to 00b.
2. Derives Address bits AD[7:2] directly from the Configuration request *Register Address* field.
3. Derives Address bits AD[10:8] directly from the Configuration request *Function Number* field.
4. Clears Address bits AD[15:11] to 0h.
5. Decodes the *Device Number* field and set a single Address bit, AD[20], during the Address phase.
6. Verifies that the *Extended Register Address* field in the configuration request is zero (0h). When the value is non-zero, the PEX 8311 does not forward the transaction, and treats it as an Unsupported request on the PCI Express interface, and a received Master Abort on the internal PCI Bus.

Type 1-to-Type 0 transactions are performed as Non-Posted transactions.

Perform Memory- or I/O-Mapped accesses to access the remainder of **LCS** (**Local**, **Runtime**, **DMA**, and **Messaging Queue**) registers on the PCI Express interface through the **LCS PCIBAR0** or **PCIBAR1** register.

9.4.2 Root Complex Mode

The Local Bus Master configures the **LCS** registers (**Type 1 PCI**, **Local**, **Runtime**, and **DMA**) by Direct Master access, using the CCS# Local Bus ball. Type 0 Configuration accesses must be generated internally by the Local Bus Master, to configure the PCI Express Configuration space. Type 1 Configuration accesses must be generated internally by the Local Bus Master, to configure downstream devices on the PCI Express interface. The internal Type 1 Configuration access is converted to Type 0 on the PCI Express interface of the PEX 8311 bridge.

9.4.2.1 Direct Master Configuration (PCI Type 0 or Type 1 Configuration Cycles)

When the Configuration Enable bit is set (**DMCFGA**[31]=1), a Configuration access is made internally to the PCI Express interface. In addition to enabling this bit, all register information must be provided. (Refer to the **DMCFGA** register.) The Register Number and Device Number bits (**DMCFGA**[7:2, 15:11], respectively) must be modified and a new Direct Master Read/Write cycle must be performed at the Direct Master I/O Base address for each Configuration register. Type 0 Configuration transactions are used to perform accesses to **PECS** registers within the PEX 8311. Type 1 Configuration transactions are used to accesses other **PECS** registers of devices downstream from the PEX 8311. Before performing Non-Configuration cycles (plain I/O accesses), the Configuration Enable bit must be cleared (**DMCFGA**[31]=0).

When the PCI Configuration Address register selects a Type 0 command, **DMCFGA**[10:0] are copied to Address bits [10:0]. **DMCFGA**[15:11] (Device Number) are translated into a single bit being set in PCI Address bits [31:11]. PCI Address bit [24] is hardwired for the PEX 8311 **PECS** register accesses, and is internally used as a device select (IDSEL). In addition, PCI Address bit [24], device Dh, must be programmed into the **DMCFGA**[15:11] register before Type 0 Configuration accesses begin.

For a Type 1 command, **DMCFGA**[23:0] are copied to PCI Address bits [23:0]. The PCI Address bits [31:24] are cleared to 0. A Configuration Read or Write command code is output with the address during the PCI Address cycle. (Refer to the **DMCFGA** register.)

For writes, Local data is loaded into the Write FIFO and READY# is returned. For reads, the PEX 8311 holds READY# de-asserted while receiving a Dword from the PCI Express interface.

Note: *Per the PCI Express Base 1.0a, the Type 0 and Type 1 Configuration cycles can only be preformed by upstream devices. Therefore, the PEX 8311 supports Type 0 and Type 1 Configuration access generation only in Root Complex mode (ROOT_COMPLEX#=0).*

Direct Master Type 0 Configuration Cycle Example

To perform a Type 0 Configuration cycle to the PEX 8311 PCI Express Configuration registers, device on internal AD[24]:

1. PEX 8311 must be configured to allow Direct Master access to the PEX 8311 internal bus interface. The PEX 8311 must also be enabled to master the internal bus interface (**PCICR**[2]=1).

   In addition, Direct Master Memory and I/O access must be enabled (**DMPBAM**[1:0]=11b).
2. Local memory map selects the Direct Master range. For this example, use a range of 1 MB:

   1 MB = 2^{20} = 00100000h
3. Value to program into the Range register is two's complement of 00100000h:

   DMRR = FFF00000h
4. Local memory map determines the Local Base Address for the Direct Master-to-PCI I/O Configuration register. For this example, use 40000000h:

   DMLBAI = 40000000h
5. PCI device and PCI Configuration register the PCI Configuration cycle is accessing must be known. In this example, the internal AD[24] (logical device #13=0Dh) is used as it is hardwired internally and connected to the PCI Express interface. Also, access **PCIBAR0** (the fourth register, counting

from 0; use Table 18-6, "PCI-Compatible Configuration Registers (Type 1)," for reference). Set **DMCFGA**[31, 23:0], as listed in Table 9-5.

After these registers are configured, a single Local Master Memory cycle to the I/O Base address is necessary to generate an internal Configuration Read or Write cycle within the PEX 8311. The PEX 8311 takes the Local Bus Master Memory cycle and checks for the *Configuration Enable* bit (DMCFGA[31]). When set to 1, the PEX 8311 internally converts the current cycle to a PCI Configuration cycle, using the **DMCFGA** register and the Write/Read signal (LW/R#).

Table 9-5. Direct Master Configuration Cycle Example DMCFGA[31, 23:0] Settings

Bits	Description	Value
1:0	Type 0 Configuration.	00b
7:2	Register Number. Fourth register. Must program a "4" into this value, beginning with bit 2.	000100b
10:8	Function Number.	000b
15:11	Device Number *n*-11, where *n* is the value in AD[*n*]=24-11 = 13.	01101b
23:16	Bus Number.	0h
31	Configuration Enable.	1

Direct Master Type 1 Configuration Cycle Example

The PEX 8311 forwards an internally generated Type 1 transaction to a Type 0 transaction on the PCI Express interface when the following is true during the access:

- Address bits AD[1:0] are 01b.
- Type 1 Configuration Request Bus Number field (AD[23:16]) is equal to the **Secondary Bus Number** register value.
- Bus command on the internal interface is a Configuration Read or Write.
- Type 1 Configuration Request *Device Number* field (AD[15:11]) is zero (0). When the field is non-zero, the transaction is ignored, resulting in a Master Abort. Local Bus LSERR# is asserted to indicate a Master Abort condition, when enabled (INTCSR[0]).

The PEX 8311 then creates a PCI Express Configuration request according to the following steps:

1. Sets the request Type field to Configuration Type 0.
2. Derives the *Register Address* field [7:2] directly from the Configuration Request *Register Address* field.
3. Clears the *Extended Register Address* field [11:8] to 0h.
4. Derive the *Function Number* field [18:16] directly from the Configuration Request *Function Number* field.
5. Derives the *Device Number* field [23:19] directly from the Configuration Request *Device Number* field (forced to zero).
6. Derives the *Bus Number* field [31:24] directly from the Configuration Request *Bus Number* field.

Type 1 to Type 0 transactions are performed as non-posted (delayed) transactions.

9.5 Type 1-to-Type 1 Forwarding

Type 1-to-Type 1 transaction forwarding provides a hierarchical Configuration mechanism when two or more levels of bridges/switches are used. When the PEX 8311 detects a Type 1 Configuration transaction intended for a PCI Bus downstream from the downstream bus, it forwards the transaction unchanged to the downstream bus.

In this case, the transaction target does not reside on the secondary interface, but is located on a bus segment further downstream. Ultimately, this transaction is converted to a Type 0 or special cycle transaction by a downstream bridge/switch device.

Note: *The secondary interface is the Local Bus interface in Endpoint mode, and the PCI Express interface in Root Complex mode.*

9.5.1 Root Complex Mode Configuration

The PEX 8311 forwards a Type 1 transaction from the internal interface to a Type 1 transaction on the PCI Express interface, when the following are true during the access:

- Address bits AD[1:0] are 01b.
- Value specified by the Bus Number field is within the range of bus numbers between the **Secondary Bus Number** (exclusive) and the **Subordinate Bus Number** (inclusive).
- Bus command on the internal interface is a Configuration Read or Write.

The PEX 8311 then creates a PCI Express Configuration request according to the following steps:

1. Sets the request Type field to Configuration Type 1.
2. Derives the *Register Address* field [7:2] directly from the Configuration Request *Register Address* field.
3. Clears the *Extended Register Address* field [11:8] to 0h.
4. Derives the *Function Number* field [18:16] directly from the Configuration Request *Function Number* field.
5. Derives the *Device Number* field [23:19] directly from the Configuration Request *Device Number* field (forced to 0h).
6. Derives the *Bus Number* field [31:24] directly from the Configuration Request *Bus Number* field.

Type 1-to-Type 1 Forwarding transactions are performed as Non-Posted (Delayed) transactions.

9.6 Type 1-to-Special Cycle Forwarding

The Type 1 Configuration mechanism is used to generate special cycle transactions in hierarchical systems. When acting as a target, the PEX 8311 ignores special cycle transactions, and does not forward the transactions to the PCI Express interface.

- In Endpoint mode, special cycle transactions can only be generated in the downstream direction (PCI Express to the Local PCI Configuration space)
- In Root Complex mode, special cycle transactions are also generated in the downstream direction (Direct Master Type 1 transactions to PCI Express)

Note: *The primary interface is the PCI Express interface in Endpoint mode, and the Local Bus in Root Complex mode.*

The secondary interface is the Local Bus interface in Endpoint mode, and the PCI Express interface in Root Complex mode.

A Type 1 Configuration Write request on the PCI Express interface is converted to a special cycle on the internal interface to the PEX 8311 **LCS PCI** registers, when all the following conditions are met:

- Type 1 Configuration Request Bus Number field is equal to the **Secondary Bus Number** register value.
- *Device Number* field is all ones (1h)
- *Function Number* field is all ones (1h)
- *Register Address* field is all zeros (0h)
- *Extended Register Address* field is all zeros (0h)

When the PEX 8311 initiates the transaction on the internal interface, the bus command is converted from a Configuration Write to a special cycle. The Address and Data fields are forwarded, unchanged, from PCI Express to the internal interface. Because the PEX 8311 does not support internal special cycles, a Master Abort is generated. After the Master Abort is detected, a Successful Completion TLP is returned to the PCI Express.

9.7 PCI Express Enhanced Configuration Mechanisms

The PCI Express Enhanced Configuration mechanism adds four extra bits to the Register Address field to expand the space to 4,096 bytes. The PEX 8311 forwards configuration transactions only when the Extended Register Address bits are all zeros (0h). This prevents address aliasing for Direct Master Type 0/Type 1 Configuration accesses, which do not support Extended Register Addressing.

When a Configuration transaction targets the PEX 8311 **LCS PCI** register and retains a non-zero value in the Extended Register Address, the PEX 8311 treats the transaction as if it received a Master Abort on the internal bus.

The PEX 8311 then performs the following:

1. Sets the appropriate status bits for the destination bus as if the transaction executed and received a Master Abort
2. Generates a PCI Express completion with Unsupported Request status

9.7.1 Memory-Mapped Indirect (Root Complex Mode Only)

In Root Complex mode, the PEX 8311 provides the capability for a Local Bus Master (LCPU or similar) to access downstream PCI Express Configuration registers using Direct Master Memory-Mapped transactions. The 4-KB region of the Memory range defined by the **PCI Base Address 0 (PCIBASE0)** register (located in PCI Express Configuration space) is used for this mechanism. Memory Reads and Writes to **PCI Base Address 0 (PCIBASE0)**, offsets 2000h to 2FFFh, result in a PCI Express Configuration transaction. The transaction address is determined by the **ECFGADDR** register. This Address register format is delineated in Table 9-6.

After the **Enhanced Configuration Address (ECFGADDR)** register is programmed to point to a particular device, the entire 4-KB Configuration space of a PCI Express endpoint is directly accessed, using Memory Read and Write transactions. Only single DWORDs are transferred during Enhanced Configuration transactions.

Table 9-6. EFCGADDR Address Register Format

31	30 28	27 20	19 15	14 12	11 0
Enhanced Enable	*Rsvd*	Bus Number	Device Number	Function Number	*Rsvd*

9.8 Configuration Retry Mechanism

9.8.1 Endpoint Mode Configuration

The PEX 8311 supports returning completions for Configuration requests that target the PEX 8311 **LCS PCI** registers prior to the Completion Timeout Timer expiration in the Root Complex. This requires the PEX 8311to take ownership of Configuration requests forwarded across the internal interface:

- When the Configuration request to the **LCS PCI** registers successfully completes prior to the Completion Timeout Timer expiration, the PEX 8311 returns a completion with Successful Status to PCI Express.
- When the Configuration request to the **LCS PCI** registers encounters an error condition prior to the Completion Timeout Timer expiration, the PEX 8311 returns an appropriate error completion to PCI Express.
- When the Configuration request to the **LCS PCI** registers does not complete, either successfully or with an error, prior to Completion Timeout Timer expiration, the PEX 8311 returns a completion with Configuration Retry Status (CRS) to PCI Express.

After the PEX 8311 returns a completion with CRS to PCI Express, the PEX 8311 continues to internally keep the configuration transaction alive, until at least one DWORD is transferred. The PEX 8311 Retries the transaction until it completes internally, or until the internal timer expires.

When another **PECS-to-LCS PCI** registers transaction is detected while the previous one is being retried, a completion with CRS is immediately returned.

When the configuration transaction internally completes after the return of a completion with CRS on PCI Express, the PEX 8311 discards the completion information. PCI Express devices that implement this option are also required to implement bit 15 of the **PECS PCI Express Device Control** register as the *Bridge Configuration Retry Enable* bit.

When this bit is cleared, the PEX 8311 does not return a completion with CRS on behalf of Configuration requests that targeted the PEX 8311 **LCS PCI** registers. The lack of a completion is to result in eventual Completion Timeout at the Root Complex.

By default, the PEX 8311 does not return CRS for Configuration requests for access performed to the **LCS PCI** registers. This can result in lengthy completion delays that must be comprehended by the Completion Timeout value in the Root Complex.

9.8.2 Root Complex Mode Configuration

In Root Complex mode, the PEX 8311 can detect a completion with CRS status from a downstream PCI Express device. The **Device Specific Control (DEVSPECCTL)** register *CRS Retry Control* field determines the PEX 8311 response in Root Complex mode when a Direct Master Type 1-to-PCI Express Configuration transaction is terminated with a Configuration Request Retry status, as delineated in Table 9-7.

Table 9-7. CRS Retry Control

CRS Retry Control	Response
00b	Retry once after 1s. When another CRS is received, Target Abort internally generated. Local Bus LSERR# is asserted, when enabled (INTCSR[0]).
01b	Retry eight times, once per second. When another CRS is received, Target Abort is internally generated. Local Bus LSERR# is asserted, when enabled (INTCSR[0]).
10b	Retry once per second until successful completion.
11b	***Reserved***

Chapter 10 Error Handling

10.1 Endpoint Mode Error Handling

When it detects errors, the PEX 8311 sets the appropriate error status bits [Conventional PCI Error bit(s) and PCI Express Error Status bit(s)], and optionally generates an error message on PCI Express. Each error condition has a default error severity level, and a corresponding error message generated on the PCI Express interface.

Error message generation on the PCI Express interface is controlled by four **PECS** Control bits:

- **PCI Command** register *Internal SERR# Enable* bit
- **PECS PCI Express Device Control** register *Fatal Error Reporting Enable* bit
- **PECS PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit
- **PECS PCI Express Device Control** register *Correctable Error Reporting Enable* bit

Error message generation on the PCI Express interface is also controlled by two **LCS** register Control bits:

- **LCS PCI Command** register *Internal SERR# Enable* bit (**PCICR**[8])
- **LCS PCI Command** register *Parity Error Response Enable* bit (**PCICR**[6])

PCI Express ERR_FATAL messages are enabled for transmission when the *Internal SERR# Enable* or *Fatal Error Reporting Enable* bit is set. ERR_NONFATAL messages are enabled for transmission when the *Internal SERR# Enable* or *Non-Fatal Error Reporting Enable* bit is set. ERR_COR messages are enabled for transmission when the *Correctable Error Reporting Enable* bit is set.

PCI Express Device Status (DEVSTAT) register *Fatal Error Detected*, *Non-Fatal Error Detected*, and *Correctable Error Detected* status bits are set for the corresponding errors on the PCI Express, regardless of the error Reporting Enable bits.

10.1.1 PCI Express Originating Interface (PCI Express-to-Local Bus)

This section describes error support for transactions that originate on the PCI Express interface, and that targeted to the PEX 8311 Local Configuration space, as well as the Local Bus. When a Write request or Read Completion is received with a poisoned TLP, the entire data payload of the PCI Express transaction must be considered as corrupt. Invert the parity for data when completing the transaction.

Table 10-1 delineates the translation a bridge must perform when it forwards a Non-Posted PCI Express request (Read or Write) to the PEX 8311 Local Configuration space or Local Bus, and the request is immediately completed, either normally or with an error condition. The PEX 8311 internal interface error condition status bits are checked in the **LCS PCISR** register. Internal error status bits are set, regardless of respective error interrupt enable bit values.

Table 10-1. Translation Performed when Bridge Forwards Non-Posted PCI Express Request

Immediate Local or Internal Bus Termination	PCI Express Completion Status
Data Transfer with Parity error (Reads)	Successful (poisoned TLP)
Completion with Parity error (Non-Posted Writes)	Unsupported Request
Internal Master Abort (Abort to Local Address space)	Unsupported Request
Internal Target Abort (Abort to Local Address space)	Completer Abort

10.1.1.1 Received Poisoned TLP

When the PEX 8311 PCI Express interface receives a Write request or Read Completion with poisoned data, the following occur:

- **PECS** and **LCS PCI Status** registers *Detected Parity Error* bits are set.
- **PECS PCI Status** register *Master Data Parity Error* bit is set when the poisoned TLP is a Read Completion and the **PCI Command** register *Parity Error Response Enable* bit is set.
- ERR_NONFATAL message is generated on PCI Express, when the following conditions are met:
  - **PECS** and **LCS PCI Command** registers *Internal SERR# Enable* bits are set –OR–
  - **PECS PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
- **PECS** and **LCS PCI Status** register *Signaled System Error* bit is set when the *Internal SERR# Enable* bits are set.
- Parity bit associated with each DWORD of data is inverted.
- For a poisoned Write request, the **PECS Secondary Status** register *Secondary Master Data Parity Error* bit is set when the **PECS Bridge Control** register *Secondary Parity Error Response Enable* bit is set,
- **LCS Interrupt Control/Status** register Local System Error (LSERR#) is asserted, when enabled (INTCSR[0]=1).

10.1.1.2 Internal Bus Uncorrectable Data Errors

The following sections describe how errors are handled when forwarding non-poisoned PCI Express transactions to the PEX 8311 Local Bus and an Uncorrectable Internal error is detected.

Immediate Reads

When the PEX 8311 forwards a Read request (I/O, Memory, or Configuration) from the PCI Express to the Local Bus and detects an Uncorrectable Data error on the internal bus while receiving an immediate response from the completer (Local Address spaces, Local Configuration space, or Local Bus Target), the following occur.

1. **PECS Secondary Status** register *Secondary Master Data Parity Error* bit is set when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set.
2. **PECS Secondary Status** register *Secondary Detected Parity Error* bit is set.
3. Parity Error signal is asserted on the internal bus interface when the **PECS Bridge Control** register *Secondary Parity Error Response Enable* bit is set.
4. **LCS Interrupt Control/Status** register *Local Data Parity Check Error* bit is set (INTCSR[7]=1), when enabled (INTCSR[6]=1).
5. Local System Error (LSERR#) is asserted, when enabled (INTCSR[0]=1).

After detecting an Uncorrectable Data error on the destination bus for an Immediate Read transaction, the PEX 8311 continues to fetch data until the Byte Count is satisfied or the target ends the transaction. When the PEX 8311 creates the PCI Express completion, it forwards it with Successful Completion and poisons the TLP.

Posted Writes

The PEX 8311 ignores Local Bus Parity errors asserted by Local Bus Targets. When the PEX 8311 detects a Parity error asserted by the Local Address space on the internal interface while forwarding a non-poisoned Posted Write transaction from PCI Express-to-Local Bus, the following occur:

1. **PECS Secondary Status** register *Secondary Master Data Parity Error* bit is set when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set.
2. ERR_NONFATAL message is generated on PCI Express, when the following conditions are met:
   - **PECS** and **LCS PCI Command** registers *Internal SERR# Enable* bits are set –OR–
   - **PECS Device Control** register *Non-Fatal Error Reporting Enable* bit is set
3. **PECS** and **LCS PCI Status** registers *Signaled System Error* bits are set when the *Internal SERR# Enable* bits are set.
4. After the error is detected, remainder of the data is forwarded.
5. **LCS PCI Status** register *Detected Parity Error* bit is set.
6. **LCS Interrupt Control/Status** register *Local System Error* (LSERR#) is asserted, when enabled (INTCSR[0]=1).

Non-Posted Writes

The PEX 8311 ignores Local Bus Parity errors asserted by Local Bus Targets. When the PEX 8311 detects a Parity error asserted by the Local Address space on the internal interface while forwarding a non-poisoned Non-Posted Write transaction from PCI Express-to-Local Bus, the following occur:

1. **PECS Secondary Status** register *Secondary Master Data Parity Error* bit is set when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set.
2. ERR_NONFATAL message is generated on PCI Express, when the following conditions are met:
   - **PECS** and **LCS PCI Command** registers *Internal SERR# Enable* bits are set –OR–
   - **PECS Device Control** register *Non-Fatal Error Reporting Enable* bit is set
3. **PECS** and **LCS PCI Status** registers *Signaled System Error* bits are set when the *Internal SERR# Enable* bits are set.
4. After the error is detected, remainder of the data is forwarded.
5. **LCS PCI Status** register *Detected Parity Error* bit is set.
6. **LCS Interrupt Control/Status** register *Local System Error* (LSERR#) is asserted, when enabled (INTCSR[0]=1).

10.1.1.3 Internal Bus Address Errors

When the PEX 8311 forwards transactions from PCI Express-to-Local Bus, PCI Address errors are internally reported by Parity and System Error signal assertion. When the PEX 8311 detects an internal System Error signal asserted, the following occur:

1. **PECS Secondary Status** register *Secondary Received System Error* bit is set.
2. ERR_FATAL message is generated on PCI Express, when the following conditions are met:
   - **PECS Bridge Control** register *Secondary Internal SERR# Enable* bit is set
   - **PECS** and **LCS PCI Command** registers *Internal SERR# Enable* bits are set or **PECS PCI Express Device Control** register *Fatal Error Reporting Enable* bit is set
3. **PECS** and **LCS PCI Status** registers *Signaled System Error* bits are set when the *Secondary Internal SERR# Enable* and *Internal SERR# Enable* bits are set.
4. **LCS PCI Status register** *Detected Parity Error* and *Signaled System Error* bits are set when forwarded Address Parity was internally detected, when enabled.
5. **LCS Interrupt Control/Status** register *Local System Error* (LSERR#) is asserted, when enabled (INTCSR[0]=1).

10.1.1.4 Internal Bus Master Abort on Posted Transaction

When a Posted Write transaction forwarded from PCI Express-to-Local Bus results in a Master Abort on the internal bus (**LCS PCISR**[11]), the following occur:

1. Entire transaction is discarded.
2. **PECS Secondary Status** register *Secondary Received Master Abort* bit is set.
3. ERR_NONFATAL message is generated on PCI Express when the following conditions are met:
   - **PECS Bridge Control** register Master Abort Mode bit is set
   - **PECS PCI Command** register *Internal SERR# Enable* bit or **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
4. **PECS PCI Status** register *Signaled System Error* bit is set when the *Master Abort Mode* and *Internal SERR# Enable* bits are set.

10.1.1.5 Internal Bus Master Abort on Non-Posted Transaction

When a Non-Posted transaction forwarded from PCI Express-to-Local Bus results in a Master Abort on the internal bus, the following occur:

1. Completion with Unsupported Request status is returned on the PCI Express.
2. **PECS Secondary Status** register *Secondary Received Master Abort* bit is set.

10.1.1.6 Internal Bus Target Abort on Posted Transaction

When a transaction forwarded from PCI Express-to-Local Bus results in a Target Abort on the internal bus (**LCS PCISR**[11]), the following occur:

1. Entire transaction is discarded.
2. **PECS Secondary Status** register *Secondary Received Target Abort* bit is set.
3. ERR_NONFATAL message is generated on PCI Express when the following conditions are met:
   - **PECS PCI Command** register *Internal SERR# Enable* bit is set –OR–
   - **PECS PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
4. **PECS PCI Status** register *Signaled System Error* bit is set when the *Internal SERR# Enable* bit is set.
5. **LCS PCI Status** register *Signaled Target Abort* bit is set (**PCISR**[11]=1).

10.1.1.7 Internal Bus Target Abort on Non-Posted Transaction

When a transaction forwarded from PCI Express-to-Local Bus results in a Target Abort on the internal bus (**LCS PCISR**[11]), the following occur:

1. Completion with Completer Abort status is returned on the PCI Express.
2. **PECS Secondary Status** register *Secondary Received Target Abort* bit is set.
3. **PECS** and **LCS PCI Status** registers *Signaled Target Abort* bits are set.
4. ERR_NONFATAL message is generated on PCI Express when the following conditions are met:
   - **PECS PCI Command** register *Internal SERR# Enable* bit is set –OR–
   - **PECS PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
5. **PECS PCI Status** register *Signaled System Error* bit is set when the *Internal SERR# Enable* bits are set.
6. **LCS PCI Status** register *Signaled Target Abort* bit is set (**PCISR**[11]=1).

10.1.1.8 Internal Bus Retry Abort on Posted Transaction

When a transaction forwarded from PCI Express-to-Local Bus results in the maximum number of internal bus Retries (PCI Retries) (selectable in the **PCI Control** register), the following occur:

1. Remaining data is discarded.
2. **PECS (IRQSTAT**) register *PCI Express to PCI Retry Interrupt* bit is set.

10.1.1.9 Internal Bus Retry Abort on Non-Posted Transaction

When a transaction forwarded from PCI Express-to-Local Bus results in the maximum number of internal bus Retries (PCI Retries) (selectable in the **PCI Control** register), the following occur:

1. Completion with Completer Abort status is returned on the PCI Express.
2. **PECS Interrupt Request Status** (**IRQSTAT)** register *PCI Express to PCI Retry Interrupt* bit is set.
3. **PECS** and **LCS PCI Status** registers *Signaled Target Abort* bits are set.

10.1.2 Local Bus Originating Interface (Internal to PCI Express)

This section describes error support for transactions that cross the PEX 8311 when the originating side is the Local Bus, and the destination side is PCI Express. The PEX 8311 supports TLP poisoning as a transmitter to permit proper forwarding of Parity errors that occur on the Local Bus or PEX 8311 internal interface. Posted Write data received from the Local Bus with bad parity is forwarded to PCI Express as a Poisoned TLPs.

Table 10-2 provides the error forwarding requirements for Uncorrectable Data errors detected by the PEX 8311 when a transaction targets the PCI Express interface.

Table 10-3 describes the bridge behavior on an internal bus Delayed transaction that is forwarded by the PEX 8311 to PCI Express as a Memory Read or I/O Read/Write request, and the PCI Express interface returns a completion with UR or CA status for the request.

Table 10-2. Error Forwarding Requirements

Received Local or Internal Bus Error	Forwarded PCI Express Error
Write with Parity error	Write request with poisoned TLP
Read Completion with Parity error in Data phase	Read completion with poisoned TLP
Configuration or I/O Completion with Parity error in Data phase	Read/Write completion with Completer Abort status

Table 10-3. Bridge Behavior on Internal Bus Delayed Transaction

PCI Express Completion Status	Internal Bus Immediate Response to Local Bus	
	Master Abort Mode = 1	Master Abort Mode = 0
Unsupported Request (on Memory Read or I/O Read)	Internal Target Abort	Normal completion, return FFFFFFFFh
Unsupported Request (on I/O Write)	Internal Target Abort	Normal completion
Completer Abort	Internal Target Abort	

10.1.2.1 Received Internal Errors

Uncorrectable Data Error on Non-Posted Write

When a Non-Posted Write is addressed such that it crosses the PEX 8311 bridge, and the PEX 8311 detects an Uncorrectable Data error on the internal interface, the following occur:

1. **PECS Secondary Status** register *Secondary Detected Parity Error* status bit is set.
2. If the **PECS Bridge Control** register *Secondary Parity Error Response Enable* bit is set, the transaction is discarded and not forwarded to PCI Express. The Parity Error signal is asserted on the internal bus.
3. If the **PECS Bridge Control** register *Secondary Parity Error Response Enable* bit is not set, the data is forwarded to PCI Express as a poisoned TLP. Also, the **PCI Status** register *Master Data Parity Error* bit is set when the **PCI Command** register *Parity Error Response Enable* bit is set. The Parity Error signal is not asserted on the internal bus.
4. **LCS PCI Status** register *Master Data Parity Error* bit is set.
5. **LCS PCI Status** register *Detected Parity Error* bit is set.
6. **LCS Interrupt Control/Status** register *Local Data Parity Error Check* bit is set, when enabled (INTCSR[6]=1), and Local Data Parity is detected
7. Local Bus System Error (LSERR#) is asserted, when enabled (INTCSR[0]=1), and Local Data Parity and internal Parity Error are detected

Uncorrectable Data Error on Posted Write

When the PEX 8311 detects an Uncorrectable Data error on the internal interface for a Posted Write transaction from the Local Bus, the following occur:

1. Internal Parity Error signal is asserted, when the **PECS Bridge Control** register *Secondary Parity Error Response Enable* bit is set.
2. **PECS Secondary Status** register *Secondary Detected Parity Error* status bit is set.
3. Posted Write transaction is forwarded to PCI Express as a poisoned TLP.
4. **PECS PCI Status** register *Master Data Parity Error* bit is set when the **PCI Command** register *Parity Error Response Enable* bit is set.
5. **LCS PCI Status** register *Master Data Parity Error* bit is set.
6. **LCS PCI Status** register *Detected Parity Error* bit is set.
7. **LCS Interrupt Control/Status** register *Local Data Parity Error Check* bit is set, when enabled (INTCSR[6]=1) and Local Data Parity is detected.
8. Local Bus System Error (LSERR#) is asserted, when enabled (INTCSR[0]=1), and Local Data Parity and internal Parity error are detected.

Uncorrectable Data Error on Internal Delayed Read Completions

When the PEX 8311 forwards a non-poisoned Read Completion from PCI Express-to-Local Bus, and it detects the Parity Error signal asserted on the internal bus, remainder of the completion is forwarded.

When the PEX 8311 forwards a poisoned Read Completion from PCI Express-to-Local Bus, the PEX 8311 proceeds with the previously mentioned actions when it detects the Parity Error signal asserted internally by the PCI master, but no error message is generated on PCI Express. Error conditions are passed to the Local Bus when the following occur:

1. **LCS PCI Status** register *Master Data Parity Error* bit is set.
2. **LCS PCI Status** register *Detected Parity Error* bit is set.
3. **LCS Interrupt Control/Status** register *Local Data Parity Error Check* bit is set, when enabled (INTCSR[6]=1), and Local Data Parity is detected.
4. Local Bus System Error (LSERR#) is asserted, when enabled (INTCSR[0]=1), and Local Data Parity and internal Parity error are detected.
5. **LCS PCI Status** register *Signaled System Error* bit is set when internal Data Parity error is detected.

Uncorrectable Address Error

When the PEX 8311 detects an Uncorrectable Address error, and Parity error detection is enabled by way of the **PECS Bridge Control** register *Secondary Parity Error Response Enable* bit, the following occur:

1. Transaction is terminated with internal Target Abort.
2. **PECS Secondary Status** register *Secondary Detected Parity Error* status bit is set, independent of the **Bridge Control** register *Secondary Parity Error Response Enable* bit value.
3. **PECS PCI Status** register *Secondary Signaled Target Abort* bit is set.
4. ERR_FATAL message is generated on PCI Express when the following conditions are met:
   - **PECS PCI Command** register *Internal SERR# Enable* bit is set –OR–
   - **PECS PCI Express Device Control** register *Fatal Error Reporting Enable* bit is set
5. **PECS PCI Status** register *Signaled System Error* bit is set when the *Internal SERR# Enable* bit is set.
6. **LCS PCI Status** register *Received Target Abort* bit is set (**PCISR**[12]=1).
7. **LCS Interrupt Control/Status** register *Local System Error* signal (LSERR#) is asserted, when enabled (**INTCSR**[0]=1).
8. **LCS Interrupt Control/Status** register *PCI Abort Interrupt Active* bit set, when enabled (**INTCSR**[10]=1). This causes a PCI Express Interrupt message to generate to the PCI Express interface.

10.1.2.2 Unsupported Request (UR) Completion Status

The PEX 8311 provides two methods for handling a PCI Express completion received with Unsupported Request (UR) status in response to a request originated by the Local Bus (Direct Master or DMA). The response is controlled by the **PECS Bridge Control** register *Master Abort Mode* bit. In either case, the **PECS PCI Status** register *Received Master Abort* bit is set.

Master Abort Mode Bit Cleared

This is the default (PCI compatibility) mode, and an Unsupported Request is not considered as an error.

When a Non-Posted Write transaction results in a completion with Unsupported Request status, the PEX 8311 completes the Write transaction on the originating bus normally and discards the Write data.

When a Local Bus-initiated Read transaction results in the return of a completion with Unsupported Request status, the PEX 8311 returns FFFFFFFFh to the Local Bus Master and normally terminates the Read transaction on the Local Bus.

Master Abort Mode Bit Set

When the **PECS Bridge Control** register *Master Abort Mode* bit is set, the PEX 8311 signals an internal Target Abort to the Local Bus-originated cycle of an upstream Read or Non-Posted Write transaction when the corresponding request on the PCI Express interface results in a completion with UR Status. The following occur:

1. **PECS PCI Status** register *Secondary Signaled Target Abort* bit is set.
2. **LCS PCI Status** register *Received Target Abort* bit is set.
3. **LCS Interrupt Control/Status** register Local System Error (LSERR#) is asserted, when enabled (INTCSR[0]=1).
4. **LCS Interrupt Control/Status** register *PCI Abort Interrupt Active* bit is set, when enabled (INTCSR[10]=1). Causes a PCI Express Interrupt message to generate to the PCI Express interface.

10.1.2.3 Completer Abort (CA) Completion Status

When the PEX 8311 receives a completion with Completer Abort status on the PCI Express interface, in response to a forwarded Non-Posted transaction from Local Bus, the **PECS** and **LCS PCI Status** registers *Received Target Abort* bits are set. A CA response results in a Delayed Transaction Target Abort on the internal bus. The PEX 8311 provides data to the Local Bus Read requester, up to the point where data was successfully returned from the PCI Express interface, then signals the internal Target Abort. The **PECS PCI Status** register *Secondary Signaled Target Abort* bit is set when signaling an internal Target Abort. The following occur:

1. **LCS PCI Status** register *Received Target Abort* bit is set.
2. **LCS Interrupt Control/Status** register Local System Error (LSERR#) is asserted, when enabled (**INTCSR**[0]=1).
3. **LCS Interrupt Control/Status** register *PCI Abort Interrupt Active* bit is set, when enabled (**INTCSR**[10]=1). Causes a PCI Express Interrupt message to generate to the PCI Express interface.

10.1.3 Timeout Errors

10.1.3.1 PCI Express Completion Timeout Errors

The PCI Express Completion Timeout mechanism allows requesters to abort a Non-Posted request when a completion does not arrive within a reasonable length of time. The PEX 8311, when acting as initiator on PCI Express on behalf of internally generated requests or when forwarding requests from a Local Bus, takes ownership of the transaction.

When a Completion Timeout is detected and the link is up, the PEX 8311 responds as if it received a completion with Unsupported Request status. The following occur:

1. ERR_NONFATAL message is generated on PCI Express when the following conditions are met:
   - **PECS PCI Command** register *Internal SERR# Enable* bit is set –OR–
   - **PECS PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
2. **PECS PCI Status** register *Signaled System Error* bit is set when the *Internal SERR# Enable* bit is set.
3. **LCS PCI Status** register *Received Master Abort* bit is set.
4. **LCS Interrupt Control/Status** register Local System Error (LSERR#) is asserted, when enabled (**INTCSR**[0]=1).
5. **LCS Interrupt Control/Status** register *PCI Abort Interrupt Active* bit is set, when enabled (**INTCSR**[10]=1). Causes a PCI Express Interrupt message to generate to the PCI Express interface.

When the link is down, the **PECS PCICTL** register *P2PE_RETRY_COUNT* field determines the amount of internal bus Retries that occur before a Master Abort is internally returned. When a Master Abort is internally encountered, the LSERR# signal is asserted on the Local Bus, when enabled (**INTCSR**[0]=1).

10.1.3.2 Internal Bus Delayed Transaction Timeout Errors

The PEX 8311 contains Delayed Transaction Timers for each queued Delayed transaction. When a Delayed Transaction Timeout is detected, the following occur:

1. ERR_NONFATAL message is generated on PCI Express when the following conditions are met:
   - **PECS Bridge Control** register *Discard Timer Internal SERR# Enable* bit is set
   - **PECS PCI Command** register *Internal SERR# Enable* bit or **PCI Express Device Control** register *Non-Fatal Error Reporting Enable* bit is set
2. **PECS PCI Status** register *Signaled System Error* bit is set when the *Internal SERR# Enable* bit is set.
3. **PECS Bridge Control** register *Discard Timer Status* bit is set.

The PEX 8311 supports converting internal Retries to PCI Express Address spaces into a Target Abort, when enabled (**LCS INTCSR**[12]=1). When enabled and the Retry Counter expires, the following occur:

1. **LCS PCI Status** register *Received Target Abort* bit set.
2. **LCS Interrupt Control/Status** register *Local System Error* (LSERR#) asserted, when enabled (**INTCSR**[0]=1).
3. **LCS Interrupt Control/Status** register *PCI Abort Interrupt Active* bit is set, when enabled (**INTCSR**[10]=1). Causes a PCI Express Interrupt message to generate to the PCI Express interface.

10.1.4 Other Errors

The PEX 8311 Local Bus logic can generate an Internal Bus System Error, when enabled (**LCS PCICR**[8]=1), that compromises system integrity. When the PEX 8311 detects Internal Bus System Error asserted, the following occur:

1. **PECS Secondary Status** register *Secondary Received System Error* bit is set.
2. ERR_FATAL message is generated on PCI Express, when the following conditions are met:
   - **PECS Bridge Control** register *Secondary Internal SERR# Enable* bit is set
   - **PECS** and **LCS PCI Command** registers *Internal SERR# Enable* bits are set or **PECS PCI Express Device Control** register *Fatal Error Reporting Enable* bit is set
3. **PECS** and **LCS PCI Status** registers *Signaled System Error* bits are set when the *Secondary Internal SERR# Enable* and *Internal SERR# Enable* bits are set.

10.2 Root Complex Mode Error Handling

For errors detected by the PEX 8311, it sets the appropriate error status bit [both Conventional PCI Error bit(s) and PCI Express Error Status bit(s)]. PCI Express Error messages are not generated in Root Complex mode.

10.2.1 PCI Express Originating Interface (PCI Express-to-Local Bus)

This section describes error support for transactions that cross the PEX 8311 when the originating side is the PCI Express (downstream) interface, and the destination side is Local Bus (upstream) interface.

When a Write Request or Read Completion is received with a poisoned TLP, the entire data payload of the PCI Express transaction is considered corrupt. The PEX 8311 inverts the parity for data when completing the transaction on the Local Bus. The internal Parity Error is generated [**LCS PCISR**[15] is set and Local System Error (LSERR#) is asserted, when enabled (**INTCSR**[0]=1].

Table 10-4 delineates the translation the PEX 8311 performs when it forwards a non-posted PCI Express request (read or write) to the internal interface and then to the Local Bus, and the request is immediately completed on the internal bus, either normally or with an error condition. The PEX 8311 internal interface error condition status bits are checked in the **LCS PCISR** register. Internal error status bits are set, regardless of whether their respective error interrupt is enabled. The PEX 8311 ignores Parity error reporting on the destination Local Bus.

Table 10-4. PEX 8311 Translation – Non-Posted PCI Express Request

Immediate Internal Interface and Local Bus Termination	PCI Express Completion Status
Data Transfer with Parity error (reads)	Successful (poisoned TLP)
Completion with Parity error (Non-Posted Writes)	Unsupported Request
Internal Master Abort (Abort to Local Address space)	Unsupported Request
Internal Target Abort (Abort to Local Address space)	Completer Abort

10.2.1.1 Received Poisoned TLP

When the PEX 8311 PCI Express interface receives a Write Request or Read Completion with poisoned data, the following occur:

1. **PECS Secondary Status** register *Secondary Detected Parity Error* bit is set.
2. **PECS Secondary Status** register *Secondary Master Data Parity Error* bit is set when the poisoned TLP is a Read Completion and the **PECS Bridge Control** register *Secondary Parity Error Response Enable* bit is set.
3. *Parity* bit associated with each DWORD of data is inverted.
4. For a poisoned Write request, the PEX 8311 **PECS PCI Status** register *Master Data Parity Error* bit is set when the **PECS PCI Command** register *Parity Error Response Enable* bit is set, and the bridge sees the internal Parity Error signal asserted when the PEX 8311 Local Bus Address space detects inverted parity.
5. **LCS PCI Status** register *Detected Parity Error* bit is set.
6. **LCS Interrupt Control/Status** register Local System Error (LSERR#) signal is asserted, when enabled (INTCSR[0]=1).

10.2.1.2 Internal Uncorrectable Data Errors

The following sections describe how errors are handled when forwarding non-poisoned PCI Express transactions to the PEX 8311 Local Bus, and an Uncorrectable Error is internally detected.

Immediate Reads

When the PEX 8311 forwards a Read request (I/O or Memory) from the PCI Express interface to the Local Bus interface, and detects an Uncorrectable Data error on the internal bus while receiving an immediate response from the PEX 8311 Local Bus logic, the following occur:

1. **PECS PCI Status** register *Master Data Parity Error* bit is set when the **PECS PCI Command** register *Parity Error Response Enable* bit is set.
2. **PECS PCI Status** register *Detected Parity Error* bit is set.
3. Parity Error signal (**LCS PCICR**[6] and **PCISR**[15]) is asserted on the internal interface when the PEX 8311 **PECS PCI Command** register *Parity Error Response Enable* bit is set.
4. **LCS Interrupt Control/Status** register *Local Data Parity Check Error* bit is set when a Local Data Parity error is detected.
5. **LCS Interrupt Control/Status** register Local System Error (LSERR#) signal is asserted, when enabled (INTCSR[6, 0]=11b).

After detecting an Uncorrectable Data error on the destination bus for an Immediate Read transaction, the PEX 8311 continues to fetch data until the Byte Count is satisfied or the target ends the transaction.

When the PEX 8311 creates the PCI Express completion, it forwards it with Successful Completion status and poisons the TLP.

Non-Posted Writes

When the PEX 8311 detects internal Parity Error signal asserted on the internal interface while forwarding a non-poisoned Non-Posted Write transaction from PCI Express to the Local Bus, the following occur:

1. **PECS PCI Status** register *Master Data Parity Error* bit is set when the **PCI Command** register *Parity Error Response Enable* bit is set.
2. PCI Express completion with Unsupported Request status is returned.
3. **LCS PCI Status** register *Detected Parity Error* bit is set.
4. **LCS Interrupt Control/Status** register *Local System Error* (LSERR#) signal is asserted, when enabled (INTCSR[0]=1).

Posted Writes

When the PEX 8311 detects the internal Parity Error signal asserted on the internal interface while forwarding a non-poisoned Posted Write transaction from PCI Express to the Local Bus, the following occur:

1. **PECS PCI Status** register *Master Data Parity Error* bit is set when the **PCI Command** register *Parity Error Response Enable* bit is set
2. After the error is detected, remainder of the data is forwarded.
3. **LCS PCI Status** register *Detected Parity Error* bit is set.
4. **LCS Interrupt Control/Status** register *Local System Error* (LSERR#) signal is asserted, when enabled (INTCSR[0]=1).

10.2.1.3 Internal Address Errors

When the PEX 8311 forwards transactions from PCI Express-to-Local Bus, Address errors are reported by the PEX 8311 internal Parity Error signal assertion, when enabled (**LCS PCICR**[6]=1). In addition, the PEX 8311 can generate a Local System Error (LSERR#), when enabled (**INTCSR**[0]=1), and allows the Local Bus Master (Root Complex device) to service the error. The internal Error status bits must be monitored (**LCS PCISR** register). When an Address error is encountered, the following occur:

1. **LCS PCI Status** register *Detected Parity Error* bit is set.
2. **LCS Interrupt Control/Status** register *Local System Error* (LSERR#) signal is asserted, when enabled (INTCSR[0]=1).

10.2.1.4 Internal Master Abort on Posted Transaction

When a transaction forwarded from PCI Express-to-Local Bus results in internal Master Abort, the following occur:

1. Entire transaction is discarded.
2. **PECS PCI Status** register *Received Master Abort* bit is set.

10.2.1.5 Internal Master Abort on Non-Posted Transaction

When a Non-Posted transaction forwarded from PCI Express-to-Local Bus results in an internal Master Abort, the following occur:

1. PCI Express completion with Unsupported Request status is returned.
2. Set the **PECS PCI Status** register *Received Master Abort* bit.

10.2.1.6 Internal Target Abort on Posted Transaction

When a Posted transaction forwarded from PCI Express-to-Local Bus results in an internal Target Abort, the following occur:

1. Entire transaction is discarded.
2. **PECS PCI Status** register *Received Target Abort* bit is set.
3. **LCS PCI Status** register *Signaled Target Abort* bit is set.
4. **LCS Interrupt Control/Status** register *Local System Error* (LSERR#) signal is asserted, when enabled (INTCSR[0]=1).

10.2.1.7 Internal Target Abort on Non-Posted Transaction

When a Non-Posted transaction forwarded from PCI Express-to-Local Bus results in an internal Target Abort, the following occur:

1. PCI Express completion with Completer Abort status is returned.
2. **PECS PCI Status** register *Received Target Abort* bit is set.
3. **LCS PCI Status** register *Signaled Target Abort* bit is set.
4. **LCS Interrupt Control/Status** register *Local System Error* (LSERR#) signal is asserted, when enabled (INTCSR[0]=1).

10.2.1.8 Internal Retry Abort on Posted Transaction

When a Posted transaction forwarded from PCI Express-to-Local Bus results in a Retry Abort on the internal Bus, the following occur:

1. Entire transaction is discarded.
2. **PECS (IRQSTAT)** register *PCI Express to PCI Retry Interrupt* bit is set.

10.2.1.9 Internal Retry Abort on Non-Posted Transaction

When a Non-Posted transaction forwarded from PCI Express-to-Local Bus results in a Retry Abort on the internal bus, the following occur:

1. PCI Express completion with Completer Abort status is returned.
2. **PECS (IRQSTAT)** register *PCI Express to PCI Retry Interrupt* bit is set.
3. **PECS Secondary Status** register *Secondary Signaled Target Abort* bit is set.

10.2.2 Local Originating Interface (Local-to-PCI Express)

This section describes error support for transactions that cross the bridge when the originating side is the Local Bus (downstream) interface, and the destination side is PCI Express (upstream) interface. The PEX 8311 supports TLP poisoning as a transmitter to permit proper forwarding of Parity errors that occur on either the PEX 8311 Local Bus or internal interface. Posted Write data received on the Local Bus with bad parity are forwarded, to PCI Express as poisoned TLPs.

Table 10-5 delineates the error forwarding requirements for Uncorrectable Data errors detected by the PEX 8311 when a transaction targets the PCI Express interface.

Table 10-6 describes the bridge behavior on an internal Delayed transaction between Local Bus and PCI Express Address spaces that is forwarded to PCI Express as a Memory Read or I/O Read/Write request, and the PCI Express interface returns a completion with UR or CA status for the request.

Table 10-5. Error Forwarding Requirements

Received Local or Internal Bus Error	Forwarded PCI Express Error
Write with Parity error	Write request with poisoned TLP
Read Completion with Parity error in Data phase	Read completion with poisoned TLP
Configuration or I/O Completion with Parity error in Data phase	Read/Write completion with Completer Abort status

Table 10-6. Bridge Behavior on Internal Delayed Transaction

PCI Express Completion Status	Internal Bus Immediate Response to Local Bus	
	Master Abort Mode = 1	Master Abort Mode = 0
Unsupported Request (on Memory Read or I/O Read)	Target Abort. The PEX 8311 **LCS** *Received Target Abort* bit is set (**PCISR**[12]=1). LSERR# is asserted, when enabled (**INTCSR**[0]=1)	Normal completion, return FFFFFFFFh
Unsupported Request (on I/O Write)	Target Abort. The PEX 8311 **LCS** *Received Target Abort* bit is set (**PCISR**[12]=1). LSERR# is asserted, when enabled (**INTCSR**[0]=1)	Normal completion
Completer Abort	Target Abort. The PEX 8311 **LCS** *Received Target Abort* bit is set (**PCISR**[12]=1). LSERR# is asserted, when enabled (**INTCSR**[0]=1)	

10.2.2.1 Received Internal Errors

Uncorrectable Data Error on Non-Posted Write

When a Non-Posted Write is addressed such that its destination is the PCI Express interface, and the PEX 8311 detects an Uncorrectable Data error on the internal interface, the following occur:

1. **PECS PCI Status** register *Detected Parity Error* status bit is set.
2. If the **PECS PCI Command** register *Parity Error Response Enable* bit is set, the transaction is discarded and not forwarded to PCI Express. The internal Parity Error signal is asserted to the Local Bus Address space.
3. If the **PECS PCI Command** register *Parity Error Response Enable* bit is not set, the data is forwarded to PCI Express as a poisoned TLP. The **Secondary Status** register *Secondary Master Data Parity Error* bit is set when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set. The internal Parity Error signal is not asserted to the PEX 8311 Local Bus Address space.
4. **LCS PCI Status** register *Master Data Parity Error* bit is set.
5. **LCS PCI Status** register *Detected Parity Error* bit is set.
6. **LCS Interrupt Control/Status** register *Local Data Parity Check Error* bit is set.
7. Local Bus System Error (LSERR#) signal is asserted, when enabled (INTCSR[6, 0]=11b), when a Local Data Parity Error is encountered.

Uncorrectable Data Error on Posted Write

When the PEX 8311 detects an Uncorrectable Data error on the internal interface for a Posted Write transaction that is targeted to the PCI Express interface, the following occur:

1. Internal Parity Error signal is asserted to the Local Bus Address space, when the **PECS PCI Command** register *Parity Error Response Enable* bit is set.
2. **PECS PCI Status** register *Detected Parity Error* status bit is set.
3. Posted Write transaction is forwarded to PCI Express as a poisoned TLP.
4. **PECS Secondary Status** register *Secondary Master Data Parity Error* bit is set when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set.
5. **LCS PCI Status** register *Master Data Parity Error* bit is set.
6. **LCS PCI Status** register *Detected Parity Error* bit is set.
7. **LCS Interrupt Control/Status** register *Local Data Parity Check Error* bit is set.
8. Local Bus System Error (LSERR#) signal is asserted, when enabled (INTCSR[6, 0]=11b), when a Local Data Parity Error is encountered.

Uncorrectable Data Error on Internal Delayed Read Completions

When the PEX 8311 forwards a non-poisoned or poisoned Read Completion from PCI Express-to-Local Bus, and internal Parity Error signal is asserted by the PEX 8311 Local Bus logic (requester of the read), the following occur:

1. Remainder of completion is forwarded.
2. Local Bus Master (Root Complex) services the internal Parity Error assertion. Local System Error (LSERR#) is asserted, when enabled (**INTCSR**[1:0]=11b).
3. **LCS PCI Status** register *Master Data Parity Error* bit is set.
4. **LCS PCI Status** register *Detected Parity Error* bit is set.
5. Local Bus System Error (LSERR#) signal is asserted, when enabled (**INTCSR**[0]=1), due to the internal Parity Error detection.

Uncorrectable Address Error

When the PEX 8311 detects an Uncorrectable Address error and Parity error detection is enabled by the **PECS PCI Command** register *Parity Error Response Enable* bit, the following occur:

1. Transaction is terminated with an internal Target Abort. LSERR# is asserted, when enabled (**INTCSR**[0]=1).
2. **PECS PCI Status** register *Signaled Target Abort* bit is set.
3. **PECS PCI Status** register *Detected Parity Error* status bit is set, independent of the setting of the **PCI Command** register *Parity Error Response Enable* bit.
4. Internal System Error is asserted, when enabled, by way of the PEX 8311 **PECS PCI Command** register. LSERR# is asserted, when enabled (**INTCSR**[1:0]=11b).
5. **PECS PCI Command** register *Internal SERR# Enable* bit is set.
6. **PECS PCI Status** register *Signaled System Error* bit is set when the internal System Error signal is asserted.
7. **LCS PCI Status** register *Received Target Abort* bit is set.
8. Local Bus System Error (LSERR#) signal is asserted, when enabled (**INTCSR**[1:0]=11b), due to the internal Target Abort and System Error signal assertion.

Internal Master Abort

When Local Bus access (Local Address space) encounters an internally generated Master Abort, the entire transaction is discarded and not forwarded to the PCI Express interface. The BTERM# signal is asserted to the Local Bus Master when it is a Read cycle only and the following occur:

1. **LCS PCI Status** register *Received Master Abort* bit is set.
2. Local System Error (LSERR#) signal is asserted, when enabled (**INTCSR**[0]=1).

10.2.2.2 Unsupported Request (UR) Completion Status

The PEX 8311 provides two methods for handling a PCI Express completion received with Unsupported Request (UR) status in response to a request originated by the Local Bus. The response is controlled by the **PECS Bridge Control** register *Master Abort Mode* bit. In either case, the **PECS Secondary Status** register *Secondary Received Master Abort* bit is set.

Master Abort Mode Bit Cleared

This is the default compatibility mode, and an Unsupported Request is not considered as an error. When a Local Bus-initiated Read transaction results in the return of a completion with UR status, the PEX 8311 returns FFFFFFFFh to the Local Bus (originating Local Bus Master) and successfully terminates the Read transaction. When a Non-Posted Write transaction results in a completion with UR status, the PEX 8311 completes the Write transaction on the Local Bus normally and discards the Write data.

Master Abort Mode Bit Set

When the *Master Abort Mode* bit is set, the PEX 8311 signals an internal Target Abort to the Local Bus. As a result, the initiator of a downstream Read or Non-Posted Write transaction when the corresponding request on the PCI Express interface completes with UR status. The following occur:

1. **PECS PCI Status** register *Signaled Target Abort* bit is set.
2. Local Bus System Error (LSERR#) signal is asserted, when enabled (INTCSR[1:0]=11b).
3. **LCS PCI Status** register *Received Target Abort* bit is set.

10.2.2.3 Completer Abort (CA) Completion Status

When the PEX 8311 receives a completion with Completer Abort status on the PCI Express interface in response to a forwarded Non-Posted Local Bus transaction, the **PECS Secondary Status** register *Secondary Received Target Abort* bit is set. A completion with CA status results in a Delayed Transaction Target Abort on the internal bus. The PEX 8311 provides data to the requesting Local Bus Master, up to the point where data was successfully returned from the PCI Express interface prior to encountering CA. The following occur:

1. **PECS PCI Status** register *Signaled Target Abort* status bit is set when signaling Target Abort.
2. Local Bus System Error (LSERR#) is asserted, when enabled (INTCSR[0]=1).
3. **LCS PCI Status** register *Received Target Abort* bit is set.

10.2.3 Timeout Errors

10.2.3.1 PCI Delayed Transaction Timeout Errors

The PCI Express Completion Timeout mechanism allows requesters to abort a Non-Posted request when a completion does not arrive within a reasonable time. The PEX 8311, when acting as initiators on PCI Express on behalf of internally generated requests and requests forwarded from the PCI Express interface, behave as endpoints for requests of which they take ownership. When a Completion Timeout is detected and the link is up, the PEX 8311 responds as if an Unsupported Request Completion was received.

When the link is down, the **PECS PCICTL** register *P2PE_RETRY_COUNT* field determines the number of internally generated Retries to occur before an internal Master Abort is returned to the PEX 8311 Local Bus logic.

10.2.3.2 Internal Delayed Transaction Timeout Errors

The PEX 83111 contains Delayed Transaction Timers for each queued Delayed transaction. When a Delayed Transaction Timeout is detected, the following occur:

1. **PECS Bridge Control** register *Discard Timer Status* bit is set.
2. Delayed request is removed from the Non-Posted Transaction queue.
3. Internal System Error signal is asserted, when the **PECS PCI Command** register *Internal SERR# Enable* bit is set.
4. Local System Error (LSERR#) signal is asserted, when enabled (INTCSR[1:0]=11b).

10.2.4 Other Errors

When detecting errors, internal System Error signal assertion can compromise system integrity. The PEX 8311 ignores Internal System Error signal assertion in Root Complex mode, and allows the Local Bus Master (Root Complex) to service the LSERR# interrupt, when enabled and generated. The LSERR# bits – **INTCSR**[12, 6, 1:0] – are used to enable or disable LSERR# sources. LSERR# is a level output that remains asserted, when the Interrupt Status or Enable bits are set.

10.2.5 PCI Express Error Messages

When the PEX 8311 detects an ERR_FATAL, ERR_NONFATAL, or ERR_COR error, or receives an ERR_FATAL, ERR_NONFATAL, or ERR_COR message, the internal System Error signal is asserted when the corresponding Reporting Enable bit in the PEX 8311 **PECS ROOTCTL** register is set, as well as Local Bus System Error (LSERR#) asserted in response to the internal System Error, when enabled (INTCSR[1:0]=11b). When an ERR_FATAL or ERR_NONFATAL message is received, the **Secondary Status** register *Secondary Received System Error* bit is set, independent of the Reporting Enable bits in the **Root Control (Root Complex Mode Only) (ROOTCTL**) register.

When an Unsupported Request is received by the PEX 8311, a **PECS Interrupt Status Request (IRQSTAT)** register interrupt status bit is set. This status bit is enabled to generate an internal PCI wire interrupt (INTA#) or MSI.

Chapter 11 Exclusive (Locked) Access

11.1 Endpoint Mode Exclusive Accesses

The exclusive access mechanism allows non-exclusive accesses to proceed concurrently with exclusive accesses. This allows a master to hold a hardware lock across several accesses, without interfering with non-exclusive Data transfers. Masters and targets not involved in the exclusive accesses are allowed to proceed with non-exclusive accesses while another master retains a bus lock.

Exclusive access support in the PEX 8311 is enabled by the **PECS PCICTL** register *Lock Enable* bit and **LCS MARBR**[22] register *Direct Slave Internal LOCK# Input Enable* bit. When the **PCICTL** register *Lock Enable* bit is clear, PCI Express Memory Read Locked requests are terminated with a completion with UR status. The PEX 8311 also supports the Local Bus LOCK (LLOCKo#) signal to assert, to monitor lock accesses. PCI Express exclusive accesses to the PEX 8311 cause Local Bus LOCK (LLOCKo#) to assert, when enabled (CNTRL[19]=1).

11.1.1 Lock Sequence across PEX 8311

Locked transaction sequences are generated by the Host CPU as one or more reads followed by a number of writes to the same locations. In Endpoint mode, the PEX 8311 only supports locked transactions in the downstream direction (PCI Express-to-Local, Direct Slave transactions). Upstream locked transactions are not allowed. The initiation of a locked transaction sequence through the PEX 8311 is as follows:

1. Locked transaction begins with a Memory Read Locked request.
2. Successive reads for the locked transaction also use Memory Read Locked requests.
3. Completions for successful Memory Read Locked requests use the CplLk Completion type, or the CplLk Completion type for unsuccessful Memory Read Locked requests.
4. When the Locked Completion for the first Locked Read request is returned, the PEX 8311 does not accept new Local Bus-initiated requests from the internal PCI Bus to PCI Express Address space. DMA and Direct Master transactions are stacked in the PEX 8311 Local FIFOs. The Local Bus LLOCKo# signal is used to monitor PCI Express exclusive lock transactions before initiating upstream transactions.
5. Writes for the locked sequence use Memory Write requests.
6. PEX 8311 remains locked until it is unlocked by the PCI Express. Unlock is then propagated to the Local Bus by terminating the locked sequence.
7. PCI Express Unlock message is used to indicate the end of a locked sequence. Upon receiving an Unlock message, the PEX 8311 unlocks itself. When the PEX 8311 is not locked, it ignores the Unlock message.

When the Locked Read request is queued in the PCI Express Address space PCI Express-to-Local Non-Posted Transaction queue, subsequent non-posted non-locked requests from the PCI Express are completed with Unsupported Request status. Requests that were queued before the Locked Read request are allowed to complete.

11.1.2 General Master Rules for Supporting LOCK# Transactions

The PEX 8311 must obey the following rules when internally performing locked sequences:

- Master can access only a single resource during a Lock operation
- First transaction of a lock operation must be a Memory Read transaction
- Internal LOCK# signal must be asserted during the Clock cycle following the Address phase and held asserted to maintain control
- Internal LOCK# signal must be released when the initial transaction of the lock request is terminated with Retry (Lock was not established)
- Internal LOCK# signal must be released when an access is internally terminated by the PEX 8311 Local Bus logic Target Abort or Master Abort
- Internal LOCK# signal must be de-asserted between consecutive Lock operations for a minimum of one Clock cycle while the bus is in the Idle state

11.1.3 Acquiring Exclusive Access across PEX 8311

When a PCI Express Memory Read Locked request appears at the output of the Non-Posted request queue, the locked request is performed to the Local Bus. The PEX 8311 monitors the Internal LOCK# signal state when attempting to establish lock. When it is asserted, the PEX 8311 does not request to start the transaction to the Local Bus.

When the PEX 8311 Local Bus logic terminates the first exclusive access transaction with an internal Retry, the PEX 8311 terminates the transaction and releases the internal LOCK# signal. After the first Data phase completes, the PEX 8311 holds the internal LOCK# signal asserted, until either the lock operation completes or an internal Master Abort or Target Abort causes early termination.

When the PCI Express Exclusive Access transaction successfully locks the PEX 8311 Local Bus logic the entire address Space 0, Space 1, and Expansion ROM space on the Local Bus are locked until they are released by the PCI Express Master. Internal locked operations are enabled or disabled with the internal *LOCK# Input Enable* bit (**LCS MARBR**[22] register).

11.1.4 Non-Posted Transactions and Lock

The PEX 8311 must consider itself locked when a Memory Read Locked request is detected on the output of the Non-Posted Request queue, although no data has transferred. This condition is referred to as a target-lock. While in target-lock, the PEX 8311 does not process any new requests on the PCI Express.

The PEX 8311 locks the Local Bus when the lock sequence on the Local Bus completes (LLOCKo# is asserted). A target-lock becomes a full-lock when the locked request completes on the PCI Express. At this point, the PCI Express master has established the lock.

11.1.5 Continuing Exclusive Access

When the PEX 8311 performs another transaction to a locked Local Bus. LLOCKo# is de-asserted during the Address phase. The locked Local Bus accepts and responds to the request. LLOCKo# is asserted one Clock cycle after the Address phase to keep the target in the locked state and allow the PEX 8311 to retain ownership of LLOCKo# signal beyond the end of the current transaction.

11.1.6 Completing Exclusive Access

When the PEX 8311 receives an Unlock Message from the PCI Express, it de-asserts the internal LOCK# and Local Bus LLOCKo# signals.

11.1.7 Invalid PCI Express Requests while Locked

When the PEX 8311 is locked, it accepts only PCI Express Memory Read Locked or Memory Write transactions that are being forwarded to the Local Bus. Other types of transactions are terminated with a completion with Unsupported Request status, including Non-Posted accesses to internal configuration registers and shared memory.

11.1.8 Locked Transaction Originating on Local Bus

Locked transactions originating on the Local Bus are not allowed to propagate to the PCI Express interface in Endpoint mode. When a locked transaction performed on the Local Bus is intended for the PEX 8311, the PEX 8311 ignores the transaction. The PEX 8311 Local Bus logic can accept the locked transaction; however, PCI Express Address space ignores it. An internal Master Abort is generated.

11.1.9 Internal Bus Errors while Locked

11.1.9.1 Internal Master Abort during Posted Transaction

When an internal Master Abort occurs during a PCI Express-to-Local Bus Locked Write transaction between PCI Express Address and Local Bus Spaces, the PEX 8311 de-asserts the internal LOCK# signal. The PCI Express interface is released from the locked state, although no Unlock message is received. Write data is discarded. The LLOCKo# signal is not asserted on the Local Bus.

Refer to Section 10.1.1.4, "Internal Bus Master Abort on Posted Transaction," for further details describing the action taken when a Master Abort is detected during a Posted transaction.

11.1.9.2 Internal Master Abort during Non-Posted Transaction

When an internal Master Abort occurs during a PCI Express-to-Local Bus Locked Read transaction, the PEX 8311 de-asserts internal LOCK# signal. The PCI Express interface is released from the locked state, although no Unlock message is received. A CplLk with Unsupported Request status is returned to the PCI Express interface.

Refer to Section 10.1.1.5, "Internal Bus Master Abort on Non-Posted Transaction," for further details describing the action taken when a Master Abort is detected during a Non-Posted transaction.

11.1.9.3 Internal Target Abort during Posted Transaction

When an internal Target Abort occurs between PCI Express Address and Local Bus Spaces during a PCI Express-to-Local Bus Locked Write transaction, the PEX 8311 de-asserts the internal LOCK# signal. The PCI Express interface is released from the locked state, although no Unlock message is received. Write data is discarded. The LLOCKo# signal is not asserted on the Local Bus.

Refer to Section 10.1.1.6, "Internal Bus Target Abort on Posted Transaction," for further details describing the action taken when a Target Abort is detected during a Posted transaction.

11.1.9.4 Internal Target Abort during Non-Posted Transaction

When an internal Target Abort occurs between PCI Express Address and Local Bus Spaces during a PCI Express-to-Local Bus Locked Read transaction, the PEX 8311 de-asserts the internal LOCK# signal. The PCI Express interface is released from the locked state, although no Unlock message is received. A CplLk with Completer Abort status is returned to the PCI Express interface. The LLOCKo# signal is not asserted on the Local Bus.

Refer to Section 10.1.1.7, "Internal Bus Target Abort on Non-Posted Transaction," for further details describing the action taken when a Target Abort is detected during a Non-Posted transaction.

11.2 Root Complex Mode Exclusive Accesses

The PEX 8311 is allowed to pass Locked transactions from the Local Bus to the PCI Express (downstream direction, Direct Master transactions). When a locked request (LLOCKi# asserted) is initiated on the Local Bus, a Memory Read Locked request is issued to the PCI Express interface. Subsequent Locked Read transactions targeting the PEX 8311 use the Memory Read Locked request on the PCI Express interface. Subsequent Locked Write transactions use the Memory Write request on the PCI Express interface. The PEX 8311 must transmit the Unlock message when Local Lock sequence is complete.

Exclusive access support in the PEX 8311 is enabled by the **PECS PCICTL** register *Lock Enable* and **LCS MARBR**[18] *Local Bus LLOCKi# Enable* bits. When these bits are clear, the LLOCKi# signal is ignored, and Locked transactions are treated as Unlocked transactions.

11.2.1 Internal Target Rules for Supporting LLOCKi#

The following are the internal target rules for supporting LLOCKi#:

- The PEX 8311, acting as the target of an access, locks itself when the LLOCKi# signal is de-asserted during the Address phase and asserted during the following Clock cycle
- Lock is established when LLOCKi# signal is de-asserted during the Address phase, asserted during the following Clock cycle, and data is transferred during the current transaction
- After lock is established, the PEX 8311 remains locked until LLOCKi# is sampled de-asserted at the Address Phase (ADS# asserted), regardless of how the transaction is terminated
- The PEX 8311 is not allowed to accept new requests (from Local Bus or PCI Express) while it remains in a locked condition, except from the owner of LLOCKi#

11.2.2 Acquiring Exclusive Access across PEX 8311

A Local Bus Master attempts to forward a Memory Read Locked transaction to the PCI Express interface. The PEX 8311 terminates the transaction with an internal Retry, and the locked request is written to the PCI Express Address Space PCI Express-to-Local Non-Posted Transaction queue. When this locked request reaches the top of the queue, the locked request is performed on the PCI Express interface as a Memory Read Locked request. When the PCI Express responds with a Locked Completion, the Locked request is updated with completion status. When the Local Bus Master Retries or the PEX 8311 internally Retries the Memory Read Locked request, the PEX 8311 responds with the lock sequence, thereby completing the transaction.

When the PEX 8311 is locked, it only accepts Local Bus locked transactions that are being forwarded to the PCI Express interface. Other bus transactions are terminated with an internal Retry, including accesses to the **PECS** registers and shared memory. The **LCS** registers can be successfully accessed. PCI Express requests are terminated with a completion with Unsupported Request status.

11.2.3 Completing Exclusive Access

When the PEX 8311 detects LLOCKi# and BLAST# de-asserted, it transmit an Unlock message to the PCI Express interface.

11.2.4 PCI Express Locked Read Request

When a Locked Read request is performed on the PCI Express interface, the PEX 8311 responds with a completion with Unsupported Request status.

Chapter 12 Power Management

12.1 Endpoint Mode Power Management

PCI Express defines Link power management states, replacing the bus power management states that were defined by the *PCI Power Mgmt. r1.1*. Link states are not visible to *PCI Power Mgmt. r1.1* legacy-compatible software, and are either derived from the power management D-states or by Active State Power Management protocols.

12.1.1 Endpoint Mode Link State Power Management

12.1.1.1 Link Power States

Table 12-1 delineates the link power states supported by the PEX 8311 in Endpoint mode.

Table 12-1. Supported Link Power States (Endpoint Mode)

Link Power State	Description
L0	Active state. PCI Express operations are enabled.
L0s	A low resume latency, energy-saving "standby" state.
L1	Higher latency, lower power "standby" state. L1 support is required for *PCI Power Mgmt. r1.1*-compatible power management. L1 is optional for Active State Link power management. Platform provided main power supplies and component reference clocks must remain active at all times in L1. The internal PLLs of the component are shut off in L1, enabling greater energy savings at a cost of increased exit latency. The L1 state is entered when downstream component functions on a given PCI Express Link are programmed to a D-state other than D0, or the downstream component requests L1 entry (Active State Link PM) and receives positive acknowledgement for the request. Exit from L1 is initiated by an upstream-initiated transaction targeting the downstream component, or by the need of the downstream component to initiate a transaction heading upstream. Transition from L1 to L0 is typically a few microseconds. TLP and DLLP communication over a Link that is in the L1 state is prohibited. The PEX 8311 only requests L1 entry for *PCI Power Mgmt. r1.1*-compatible power management. When the Local Bus requests the Power State change (internal PME# signal is asserted), the PEX 8311 requests a transition from L1 to L0.

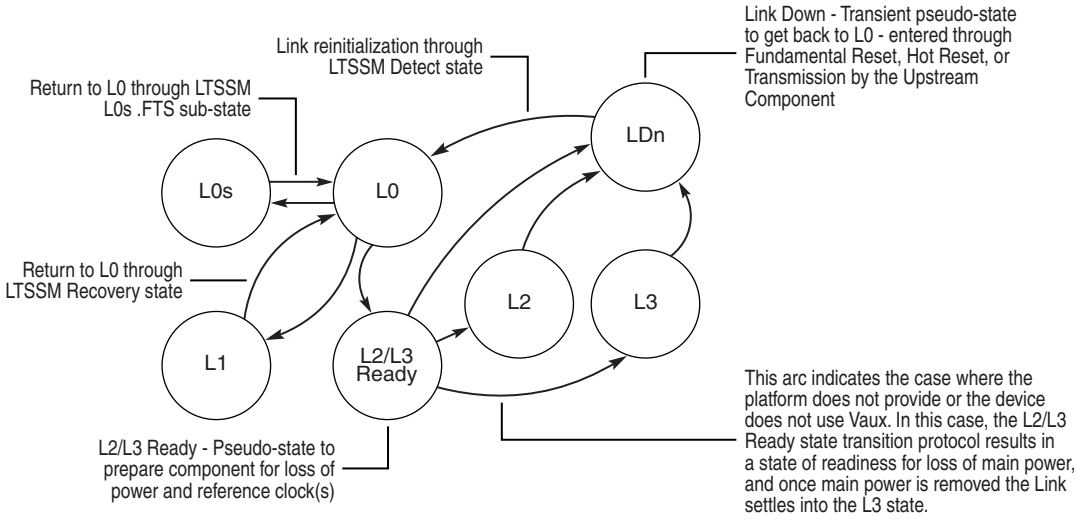
Table 12-1. Supported Link Power States (Endpoint Mode) *(Cont.)*

Link Power State	Description
L2/L3 Ready	Staging point for removal of main power. L2/L3 Ready transition protocol support is required. The L2/L3 Ready state is related to *PCI Power Mgmt. r1.1* D-state transitions. L2/L3 Ready is the state that a given Link enters into when the platform is preparing to enter its system sleep state. Following the completion of the L2/L3 Ready state transition protocol for that Link, the Link is then ready for either L2 or L3, but not actually in either of those states until main power has been removed. Depending upon the implementation choices of the platform with respect to providing a Vaux supply, after main power has been removed, the Link either settles into L2 (*that is*, Vaux is provided), or it settles into a zero power "off" state (refer to L3). The PEX 8311 does not support L2; therefore, it settles into the L3 state. The L2/L3 Ready state entry transition process must begin as soon as possible following the PME_TO_Ack TLP acknowledgment of a PM_TURN_OFF message. The downstream component initiates L2/L3 Ready entry by injecting a PM_Enter_L23 DLLP onto its transmit Port. TLP and DLLP communication over a Link that is in the L2/L3 Ready state is prohibited. Exit from L2/L3 Ready back to L0 can only be initiated by an upstream-initiated transaction targeting the downstream component in the same manner that an upstream-initiated transaction can trigger the transition from L1 back to L0. The case wherein an upstream-initiated exit from L2/L3 Ready occurs corresponds to the scenario wherein, sometime following the transition of the Link to L2/L3 Ready but before main power is removed, and the platform power manager decides not to enter the system sleep state. A Link transition into the L2/L3 Ready state is one of the final stages involving PCI Express protocol leading up to the platform entering into in a system sleep state wherein main power has been shut off (*such as*, ACPI S3 or S4 sleep state).
L2	***Not supported.*** Auxiliary powered link deep energy-saving state.
L3	Link-off state. Power-off state.

12.1.1.2 Link State Transitions

Figure 12-1 highlights the L-state transitions that can occur during the course of Link operation.

Figure 12-1. L-State Transitions during Link Operations



Note: *In this case, the L2/L3 Ready state transition protocol results in a state of readiness for loss of main power, and after removal, the Link settles into the L3 state.*

The arc indicated in Figure 12-1 indicates a case wherein the platform does not provide Vaux. Link PM Transitions from any L-state to other L-states, pass through the L0 state during the transition process with the exception of the L2/L3 Ready to L2 or L3 transitions. In this case, the Link transitions from L2/L3 Ready directly to either L2 or L3 when main power to the component is removed. (This follows along with a D-state transition from D3 for the corresponding component.)

The following sequence, leading up to entering a system sleep state, illustrates the multi-step Link state transition process:

1. System software directs all functions of a downstream component to D3hot.
2. The downstream component then initiates the transition of the Link to L1 as required.
3. System Software then causes the Root Complex to broadcast the PME_Turn_Off message in preparation for removing the main power source.
4. This message causes the subject Link to transition back to L0 to transmit it, and enable the downstream component to respond with PME_TO_Ack.
5. After the PME_TO_Ack is transmitted, the downstream component then initiates the L2/L3 Ready transition protocol.

In summary:

- L0 –> L1 –> L0 –> L2/L3 Ready
- L2/L3 Ready entry sequence is initiated at the completion of the PME_Turn_Off/PME_TO_Ack protocol handshake

It is also possible to remove power without first placing all devices into D3hot:

1. System software causes the Root Complex to broadcast the PME_Turn_Off message in preparation for removing the main power source.
2. The downstream components respond with PME_TO_Ack.
3. After the PME_TO_Ack is transmitted, the downstream component then initiates the L2/L3 Ready transition protocol.

In summary:

- L0 –> L2/L3 Ready

12.1.2 Endpoint Mode Power Management States

The PEX 8311 provides two sets of Configuration registers, each of which are treated separately by the PCI Power Management system software. The PEX 8311 also provides the support hardware required by the *PCI Power Mgmt. r1.1*. The **PECS PCICAPPTR** register points to the Base address of the **PECS Power Management** registers (offset 40h in PCI Express Configuration space). The **LCS CAP_PTR** register points to the Base address of the **LCS Power Management** register (offset 34h in Local Configuration space).

The PEX 8311 also supports the PCI Express Active State Link Power Management protocol as described in Section 12.1.1.

The PEX 8311 Local Bus logic passes Power Management information to the Local Bus devices by way of LINTo#, with no inherent power-saving feature.

The **LCS PCI Status** (**PCISR**) and **New Capability Pointer** (**CAP_PTR**) register indicate whether a new capability (Power Management function) is available. A System BIOS is able to identify a New Capability function support when the **LCS** register **PCISR**[4]=1. This bit is writable from the Local Bus, and readable from the PCI Express interface and Local Bus. **CAP_PTR** provides an offset into the **LCS PCI** register, the start location of the first item in a New Capabilities Linked List.

The **Power Management Capability ID** register (**PMCAPID**) in the **LCS PCI** register specifies the Power Management Capability ID, 01h, assigned by the PCI-SIG. The **Power Management Next Capability Pointer** register (**PMNEXT**) points to the first location of the next item in the capabilities linked list. When Power Management is the last item in the list, then clear this register to 0h. The default value is 48h.

12.1.2.1 Power States

Table 12-2 delineates the power states supported by the PEX 8311, selectable by way of the **PECS PWRMNGCSR** register *Power State* field, as well as the **LCS PCI PMC** and **PMCSR** registers *Power Management Capabilities* and *Power Management Control/Status* fields, respectively.

Note: *The D2 power state is* ***not supported****.*

Table 12-2. Supported Power States (Endpoint Mode)

Power State	Description
D0_uninitialized	Power-on default state. This state is entered when power is initially applied. The **PCI Command** register *I/O Access Enable*, *Memory Space Enable*, and *Bus Master Enable* bits are cleared to 0.
D0_active	Fully operational. At least one of the following **PCI Command** register bits must be set: • *I/O Access Enable* • *Memory Space Enable* • *Bus Master Enable*
D1	Light sleep. Only PCI Express Configuration transactions are accepted. Other types of transactions are terminated with an Unsupported Request. PCI Express requests generated by the PEX 8311 are disabled except for PME messages.
D3hot	Function context not maintained. Only PCI Express Configuration transactions are accepted. Other types of transactions are terminated with an Unsupported Request. PCI Express requests generated by the PEX 8311 are disabled except for PME messages. From this state, the next power state is D3cold or D0_uninitialized. When transitioning from D3hot to D0, the entire bridge is reset.
D3cold	Device is powered-off. A power-on sequence transitions a function from the D3cold state to the D0_uninitialized state. At this point, software must perform a full initialization of the function to re-establish all functional context, completing the restoration of the function to its D0_active state.

When transitioning from D0 to another state, the PCI Express link transitions to link state L1.

System software must allow a minimum recovery time following a D3hot to D0 transition of at least 10 ms, prior to accessing the function. *For example*, this recovery time is used by the D3hot to D0 transitioning component to bootstrap its component interfaces (*such as*, from serial ROM) prior to becoming accessible. Attempts to target the function during the recovery time (including Configuration request packets) results in undefined behavior.

From a Power Management perspective, the internal bus between PCI Express Address and Local Bus Spaces is characterized at any point in time by one of four Power Management states, delineated in Table 12-3.

All systems include an originating device, which can support one or more power states. In most cases, this creates a bridge/switch (*such as*, a Root Complex-to-PCI Express or PCI Express-to-PCI bridge).

Device power states must be at the same or lower energy state than the bus on which they reside.

Table 12-3. Supported Internal Bus Power States (Endpoint Mode)

Power State	Description
B0 (Fully On)	Bus is fully usable with full power and clock frequency. Fully operational bus activity. This is the only Power Management state in which Data transactions can occur.
B1	Intermediate Power Management state. Full power with clock frequency. Internal PME-driven bus activity. VCC is applied to all bus devices, and no transactions are allowed to occur on the bus.
B2	Intermediate Power Management state. Full power clock frequency stopped (in the low state). Internal PME-driven bus activity. V_{CC} is applied to all bus devices.
B3 (Off)	Power to the bus is switched off. Internal PME-driven bus activity. V_{CC} is removed from all devices.

12.1.3 Endpoint Mode Power Management Signaling

In Endpoint mode, Local devices assert PMEIN# to generate PM PME messages. In Root Complex mode, PMEOUT# signals Local devices, communicating the arrival of a PM PME message from PCI Express space.

Power Management messages are used to support Power Management Events signaled by the Local Bus backplane, devices downstream of the PEX 8311. System software needs to identify the source of a PCI Power Management Event that is reported by a PM_PME message. When the Power Management Event comes from the Local Bus, the PM_PME message Requester ID reports the Bus Number from which the Power Management Event was collected, and the Device Number and Function Number reported must both be 0.

When the PME message is transmitted to the host, the **Power Management Control/Status (PWRMNGCSR)** register *PME Status* bit is set and a 100 ms timer is started. When the status bit is not cleared within 100 ms, another PME message is transmitted.

For the PEX 8311 to change the power state, assert internal PME# signal, and signal PME messages or WAKEOUT# to PCI Express, a PCI Express Root Complex (upstream device) or Local Bus Master sets the **LCS PCI** register *PME_En* bit (**PMCSR**[8]=1).

When the upstream device is powering down the PEX 8311, it first places the Local Bus logic of the PEX 8311 into the D3hot state by accessing the **LCS PCI** register **PMSCR**[1:0] bits. LINTo# is asserted each time the power state in **PMCSR**[1:0] changes. The Local Master then determines to which power state the backplane changes by reading the *Power State* bits (**PMCSR**[1:0]).

The Local Master sets up the following:

- *D_1 Support* bit (**LCS PCI** register **PMC**[9], respectively) is used by the Local Master to identify power state support
- *PME Support* bits (**LCS PCI** register **PMC**[15:11]) are used by the PEX 8311 Local Bus logic to identify the internal PME# Support to the PCI Express logic corresponding to a specific power state (PMCSR[1:0])

The Local Master then sets the *PME_Status* bit (**LCS PCI** register PMCSR[15]=1), causing a PCI Express PM_PME message to generate, as a Ready Acknowledge to be placed into a different power state. To clear the bit, the upstream device must perform a Type 1 Configuration transaction to the **LCS PCI** register and write 1 to the *PME_Status* bit (**PMCSR**[15]=1), which causes the PM_PME message to regenerate on the PCI Express interface. To disable the PME# interrupt signal, either an upstream device or Local Bus Master can write 0 to the *PME_En* bit (**PMCSR**[8]=0). The PCI Express Root Complex (Power Management driver) then transmits a PCI Express PME_Turn_Off message. After the PEX 8311 receives this message, it does not transmit further PME messages upstream. The PEX 8311 then transmits a PME_TO_Ack message to the upstream device and places its link into the L2/L3 Ready state. It is now ready to power down. When the upstream device returns the PEX 8311 power state to D0, PME messages are re-enabled. The PCI Express PME_Turn_Off message terminates at the PEX 8311, and is not communicated to the Local Bus devices. The PEX 8311 does not issue a PM_PME message on behalf of a Local Bus device while its upstream Link is in the L2/L3 non-communicating state.

To avoid loss of Local Bus backplane internal PME# signal assertions in the conversion of the level-sensitive internal PME# signal to the edge-triggered PCI Express PM_PME message, the PEX 8311 polls the internal PME# signal every 256 ms. A PCI Express PM_PME message is generated when the internal PME# signal is asserted in response to the Local Bus backplane power change event.

LINTo# is asserted each time the power state in **PMCSR**[1:0] changes. The transition from the D3hot power state to the D0 power state causes a soft reset. Initiate a Soft Reset only from the PCI Express interface, because the Local Bus interface is reset during a soft reset. The PEX 8311 issues LRESET# and resets **Local Configuration** and **Messaging Queue** registers, Local Bus logic, PCI and Local DMA logic, and all FIFOs. (Refer to Section 3.1.2.2, "Local Bridge Local Bus Reset.") After power-on reset completes, the PEX 8311 reloads its original values, overwriting the **Internal PCI Interrupt Line** register (**PCIILR**) value (IRQ assignment) contents. The driver must save the **LCS PCI** register **PCIILR** register value before entering the Power Management state for restoration. To allow LINTo# to assert, set the *LINTo# Enable* and *Power Management Interrupt Enable* bits (**LCS INTCSR**[16, 4]=11b, respectively) and clear the interrupt by setting the *Power Management Interrupt* bit (**INTCSR**[5]=1).

The **LCS** *Data_Scale* bits (**PMCSR**[14:13]) register indicate the scaling factor to use when interpreting the value of the *Power Management Data* bits (**PMDATA**[7:0]). The bit values and definitions depend upon the data value specified in the *Data_Select* bits (**PMCSR**[12:9]). The *Data_Scale* bit value is unique for each *Data_Select* bit combination. For Data_Select values from 8 to 15, the *Data_Scale* bits always return a zero (**PMCSR**[14:13]=00b).

PMDATA provides static operating data, *such as* power consumed or heat dissipation.

12.1.3.1 Wakeup

When the link is in the L2 state, a device on the Local Bus signals the Root Complex to wake up the link.

The wakeup sequence of events is as follows:

1. Local Bus Master performs a write to the **LCS PCI** register **PMCSR** register to request a Wakeup event.
2. When the request is detected, the PEX 8311 drives internal PME# signal and causes the WAKEOUT# signal to assert or a beacon to be transmitted to the PCI Express interface.
3. PEX 8311 restores the PCI Express Link to L0 state.
4. PCI Express Root Complex accesses the PEX 8311 **LCS PCI** register **PMCSR** register to disable the internal PME# signal and restores the PEX 8311 Local Bus logic to the D0 power state.
5. The PEX 8311 completes the Power Management task by issuing the Local interrupt (LINTo#) to the Local Bus Master, indicating that the power mode changed.

The PEX 8311 asserts the WAKEOUT# signal or transmits a PCI Express beacon for the following:

- Local Bus Wakeup event is issued while the link is in the L2 state
- PCI Express beacon is received while the link is in the L2 state
- PCI Express PM_PME message is received

A beacon is transmitted when the following are true:

- Local Bus wakeup event is issued while the link is in the L2 state
- **Device Specific Control (DEVSPECCTL)** register *Beacon Generate Enable* bit is set
- **Power Management Control/Status (PWRMNGCSR)** register *PME Enable* bit is set

12.1.4 Endpoint Mode Set Slot Power

When a PCI Express link first comes up, or the Root Complex **SLOTCAP** register *Slot Power Limit Value* or *Slot Power Limit Scale* fields are changed, the Root Complex transmits a Set Slot Power message.

When the PEX 8311 receives this message, it updates its **DEVCAP** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields.

When the available power indicated by the **DEVCAP** register *Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields is greater than or equal to the power requirement indicated in the **POWER** register, the PWR_OK signal is asserted.

12.2 Root Complex Mode Power Management

The PEX 8311 supports Active State Power Management (ASPM) in Root Complex mode. By default, L1 is enabled and L0s is disabled.

12.2.1 Root Complex Mode Active State Power Management (ASPM)

12.2.1.1 ASPM States

Table 12-4 delineates the link power states supported by the PEX 8311 in Root Complex mode.

Table 12-4. Supported Link Power States (Root Complex Mode)

Link Power State	Description
L0	Active state. PCI Express operations are enabled.
L0s	A low-resume latency, energy-saving "standby" state. When enabled by the PCI Express serial EEPROM or external driver, the PEX 8311 transmitter transitions to L0s after a low resume latency, energy saving "standby" state. L0s support is required for Active State Link power management. It is not applicable to *PCI Power Mgmt. r1.1*-compatible power management. Main power supplies, component reference clocks, and components' internal PLLs must be active at all times during L0s.TLP and DLLP communication over a Link that is in L0s is prohibited. The L0s state is exclusively used for active-state power management. The PCI Express physical layer provides mechanisms for quick transitions from this state to the L0 state. When common (distributed) reference clocks are used on both sides of a given Link, the transition time from L0s to L0 is typically less than 100 symbol times.
L1	Higher-latency, lower-power "standby" state. L1 support is required for *PCI Power Mgmt. r1.1*-compatible power management. L1 is optional for Active State Link power management. Platform provided main power supplies and component reference clocks must remain active at all times in L1. The component's internal PLLs are shut off in L1, enabling greater energy savings at a cost of increased exit latency. The L1 state is entered when downstream component functions on a given PCI Express Link are programmed to a D-state other than D0, or when the downstream component requests L1 entry (Active State Link PM) and receives positive acknowledgement for the request. Exit from L1 is initiated by an upstream-initiated transaction targeting the downstream component, or by the downstream component's desire to initiate a transaction heading upstream. Transition from L1 to L0 is typically a few microseconds. TLP and DLLP communication over a Link that is in the L1 state is prohibited.
L2/L3 Ready	Staging point for removal of main power. L2/L3 Ready transition protocol support is required. The L2/L3 Ready state is related to *PCI Power Mgmt. r1.1* D-state transitions. L2/L3 Ready is the state that a given Link enters into when the platform is preparing to enter its system sleep state. Following the completion of the L2/L3 Ready state transition protocol for that Link, the Link is then ready for L2 or L3, but not actually in either of those states until main power is removed. Depending upon the platform's implementation choices with respect to providing a Vaux supply, after main power is removed, the Link either settles into L2 (*for example*, Vaux is provided), or it settles into a zero power "off" state (refer to L3). The PEX 8311 does not maintain Vaux capability, but can support L2 when the system Vaux supply is used as the main power to the PEX 8311. The L2/L3 Ready state entry transition process must begin as soon as possible following PME_TO_Ack TLP acknowledgment of a PM_TURN_OFF message. The downstream component initiates L2/L3 Ready entry by injecting a PM_Enter_L23 DLLP onto its transmit Port. TLP and DLLP communication over a Link that is in the L2/L3 Ready state is prohibited. Exit from L2/L3 Ready returning to L0 can only be initiated by an upstream-initiated transaction targeting the downstream component in the same manner that an upstream-initiated transaction can trigger the transition from L1 returning to L0. In the case of an upstream-initiated exit from L2/L3 Ready occurring corresponds to the scenario wherein, sometime following the transition of the Link to L2/L3 Ready but before main power is removed, and the platform power manager decides not to enter the system sleep state. A Link's transition into the L2/L3 Ready state is one of the final stages involving PCI Express protocol leading up to the platform entering into in a system sleep state wherein main power has been shut off (*for example*, ACPI S3 or S4 sleep state).
L2	Auxiliary-powered link deep energy saving state.
L3	Link off state. Power off state.

12.2.2 Root Complex Mode Power Management States

The PEX 8311 provides the Configuration registers and support hardware required by the *PCI Power Mgmt. r1.1*. The **PCICAPPTR** register points to the Base address of the **Power Management** registers (offset 40h in PCI Express Configuration space).

12.2.2.1 Power States

Table 12-5 delineates the power states supported by the PEX 8311, and selected by the **Power Management Control/Status (PWRMNGCSR)** register *Power State* field.

An interrupt, indicated by the **Interrupt Request Status (IRQSTAT)** register *Power State Change Interrupt* bit, is generated when the power state is changed.

Note: *The D2 power state is* ***not supported****.*

Table 12-5. Supported Power States (Root Complex Mode)

Power State	Description
D0_uninitialized	Power-on default state. This state is entered when power is initially applied. The **PCI Command** register *I/O Access Enable*, *Memory Space Enable*, and *Bus Master Enable* bits are cleared to 0.
D0_active	Fully operational. At least one of the following **PCI Command** register bits must be set: • *I/O Access Enable* • *Memory Space Enable* • *Bus Master Enable*
D1	Light sleep. Only PCI Configuration transactions are accepted. No master cycles are allowed, and the INTA# interrupts are disabled. The PMEOUT# signal is asserted by the PEX 8311. The Root Complex Local Bus Master clock continues to run in this state.
D3hot	Function context not maintained. Only Local Bus configuration transactions are accepted. From this state, the next power state is either D3cold or D0_uninitialized. When transitioning from D3hot to D0, the entire bridge is reset.
D3cold	Device is powered-off. A power-on sequence transitions a function from the D3cold state to the D0_uninitialized state. At this point, software must perform a full initialization of the function to re-establish all functional context, completing the restoration of the function to its D0_active state.

12.2.3 Root Complex Mode Power Down Sequence

During a link power-down, the following sequence occurs:

1. Local Bus Root Complex places the downstream PCI Express device into the D3 power state.
2. Downstream device initiates a transition to the L1 link state.
3. Local Bus Root Complex places the PEX 8311 PCI Express logic into the D3 power state.
4. PEX 8311 initiates a transition to L0 on the link.
5. PEX 8311 generates a PCI Express PME_Turn_Off message to the PCI Express downstream device.
6. Downstream device responds with a PME_TO_Ack message.
7. Downstream device transmits a DLLP to request transition to the L2/L3 Ready state (L2.Idle link state).
8. PEX 8311 acknowledges the request, completing the transition to the L2.Idle link state.
9. Local Bus PMEOUT# signal is asserted to the Local Bus Root Complex.
10. Local Bus Root Complex can now remove power from the PEX 8311.

12.2.4 Root Complex Mode Local Bus PMEOUT# Signal

PME messages from the PCI Express interface are translated to the Local Bus backplane PMEOUT# signal. The **Power Management Control/Status (PWRMNGCSR)** register *PME Status* bit is set when a PCI Express PME message is received, the WAKEIN# signal is asserted, a beacon is detected, or the link transitions to the L2/L3 Ready state. PMEOUT# is asserted when the *PME Status* bit is set and PME is enabled.

12.2.5 Root Complex Mode Set Slot Power

When a PCI Express link first comes up, or the PEX 8311 **SLOTCAP** register *Slot Power Limit Value* or *Slot Power Limit Scale* fields are changed, the PEX 8311 transmits a Set Slot Power message to the downstream PCI Express device.

When the downstream device receives this message, it updates the **DEVCAP** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields.

Chapter 13 Interrupts

13.1 Introduction

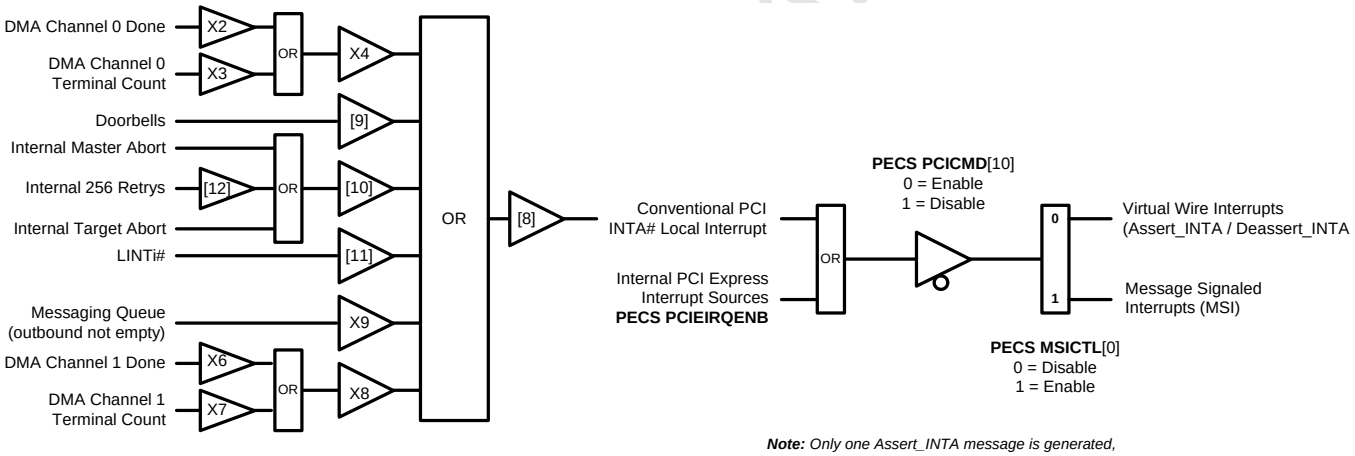
This chapter provides information about PEX 8311 interrupts, interrupt sources, and user I/O ball functionality. Figure 13-1 and Figure 13-2 illustrate the interrupts sources and output types possible for PCI Express and Local Bus spaces, respectively.

In PCI Express space, interrupts are passed using in-band messaging, and in one direction only. In Local Bus space, Local interrupts can be generated in Endpoint and Root Complex modes.

In Endpoint mode, the PEX 8311 transmits Interrupt messages to PCI Express space. In Root Complex mode, the PEX 8311 receives messages.

The following sections describe the various interrupt sources and interrupt outputs supported in Endpoint and Root Complex modes.

Figure 13-1. PCI Express Interrupt Messaging (Endpoint Mode)



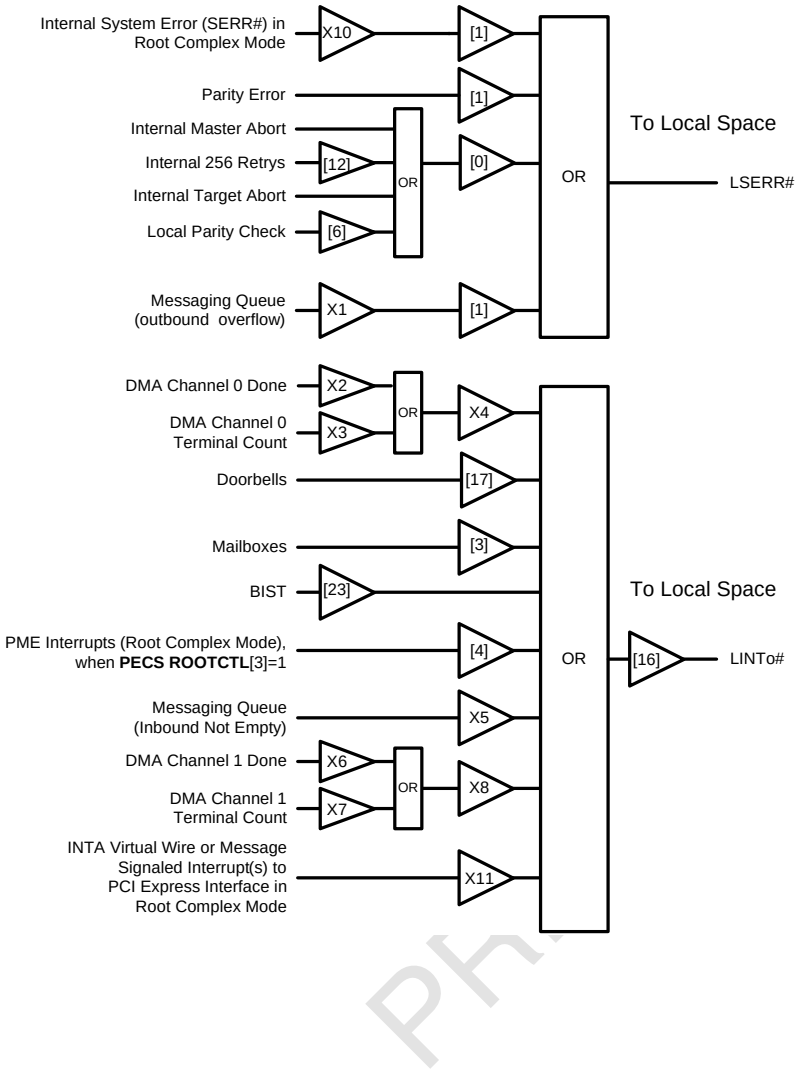
Note: *Only one Assert_INTA message is generated, regardless of how many interrupts are active. When all pending interrupts are cleared or disabled, one Deassert_INTA message is generated.*

The numbers in [brackets] represent **INTCSR** register bits.

X2 = *DMA Channel 0 Done Interrupt Enable* bit (**DMAMODE0**[10])
X3 = *DMA Channel 0 Interrupt after Terminal Count* bit (**DMADPR0**[2])
X4 = *Local DMA Channel 0 Interrupt Enable* and *Select* bits (**INTCSR**[18] and **DMAMODE0**[17], respectively)
X6 = *DMA Channel 1 Done Interrupt Enable* bit (**DMAMODE1**[10])
X7 = *DMA Channel 1 Interrupt after Terminal Count* bit (**DMADPR1**[2])
X8 = *Local DMA Channel 1 Interrupt Enable* and *Select* bits (**INTCSR**[19] and **DMAMODE1**[17], respectively)

For X4 and X8: If **DMAMODEx**[17]=0, LINTo# is asserted
If **DMAMODEx**[17]=1, INTA# is asserted

Figure 13-2. Local Interrupt and Error Sources



The numbers in [brackets] represent **INTCSR** register bits.

X1 = *Outbound Free Queue Overflow Interrupt Full* and *Mask* bits (**QSR**[7:6], respectively)
X2 = *DMA Channel 0 Done Interrupt Enable* bit (**DMAMODE0**[10])
X3 = *DMA Channel 0 Interrupt after Terminal Count* bit (**DMADPR0**[2])
X4 = *Local DMA Channel 0 Interrupt Enable* and *Select* bits (**INTCSR**[18] and **DMAMODE0**[17], respectively)
X5 = *Inbound Post Queue Interrupt Not Empty* and *Mask* bits (**QSR**[5:4], respectively)
X6 = *DMA Channel 1 Done Interrupt Enable* bit (**DMAMODE1**[10])
X7 = *DMA Channel 1 Interrupt after Terminal Count* bit (**DMADPR1**[2])
X8 = *Local DMA Channel 1 Interrupt Enable* and *Select* bits (**INTCSR**[19] and **DMAMODE1**[17], respectively)
X10 = *LSERR# Interrupt Status* bit (**CNTRL**[21])
X11 = *LINTo# Interrupt Status* bit (**CNTRL**[20])

For X4 and X8: If **DMAMODE*x***[17]=0, LINTo# is asserted
If **DMAMODE*x***[17]=1, INTA# is asserted

13.2 Endpoint Mode PCI Express Interrupts

In Endpoint mode, PCI Express Interrupt sources can be grouped into two main branches – Local interrupts and PCI Express Bridge interrupts:

- Local interrupts are gated by the **LCS INTCSR** register, and are passed to the PCI Express bridge by way of the Conventional PCI INTA# signal
- PCI Express Bridge interrupts are gated by the **PECS PCIIRQENB** register, and support several internal bridge functions

Sources of internal and external interrupts can cause the PEX 8311 to issue interrupts on the PCI Express interface.

13.2.1 Local Interrupt Sources

Local interrupts from internal sources are gated by the **LCS INTCSR** register. (Refer to Figure 13-1.) Local interrupts are passed to the PCI Express bridge by way of the Conventional PCI INTA# signal. Sources of Local interrupts are as follows:

- Mailbox registers written
- Doorbell registers written
- DMA Done or Abort
- DMA Terminal Count
- Internal interface Master/Target Aborts
- 256 Consecutive Retries between Local Address and PCI Express Address spaces
- Messaging Outbound Post queue not empty
- Local Bus Interrupt input (LINTi#) assertion

13.2.1.1 Local Configuration Space Mailbox Register Interrupts

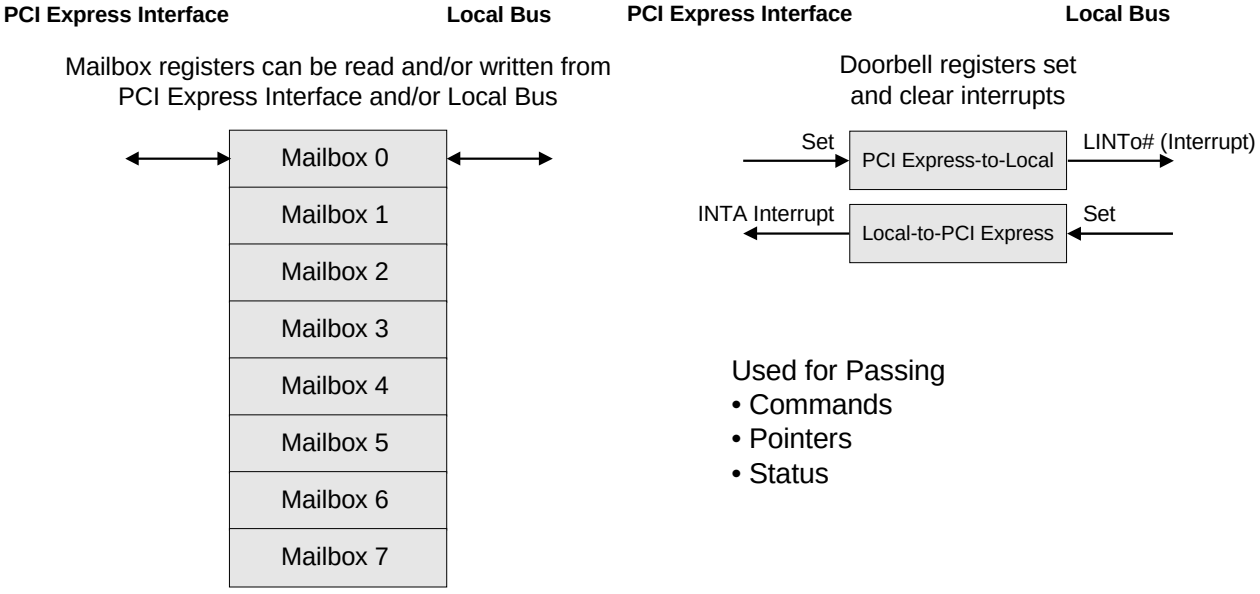
The PEX 8311 Local Bus logic has eight, 32-bit Mailbox registers that are written to and read from the PCI Express interface and Local Bus. These registers are used to pass command and status information directly between the PCI Express and Local Bus devices. (Refer to Figure 13-3.) For PCI Express to access Mailbox registers, a Type 1 Configuration access (Type 1 access is internally converted to Type 0) must be performed to the PEX 8311 Local Configuration space.

A Local interrupt (LINTo#) is asserted, when enabled (**LCS INTCSR**[3, 16]=11b), when the PCI Express Root Complex writes to one of the first four Mailbox registers (**MBOX0**, **MBOX1**, **MBOX2**, or **MBOX3**).

Regardless of whether LINTo# is enabled, a PCI Express write to one of these four Mailbox registers sets a corresponding status bit in **INTCSR**[31:28], provided the Mailbox interrupts are enabled (**INTCSR**[3]=1).

To clear the LINTo# assertion caused by the PCI Express Root Complex write(s) of any of the four Mailbox registers, a Local Bus device must read each Mailbox register that was written.

Figure 13-3. Mailbox and Doorbell Message Passing



13.2.1.2 Doorbell Registers

The PEX 8311 has two 32-bit Doorbell registers. One is assigned to the PCI Express interface; the other to the Local Bus interface.

A PCI Express Root Complex can assert a Local interrupt output (LINTo#) by writing any number other than all zeros (0) to the PCI Express-to-Local Doorbell bits (**LCS P2LDBELL**[31:0]). The Local Interrupt remains asserted until all **P2LDBELL** bits are cleared to 0. A Local processor can cause a PCI Express assert message interrupt generation by writing any number other than all zeros (0) to the Local-to-PCI Express Doorbell bits (**LCS L2PDBELL**[31:0]). The PEX 8311 generates a PCI Express de-assert PCI Express message interrupt after all **L2PDBELL** bits are cleared to 0. (Refer to Figure 13-3.)

Local-to-PCI Express Interrupt

A Local Bus Master can cause the PEX 8311 to generate PCI Express message interrupt by writing to the Local-to-PCI Express Doorbell bits (**L2PDBELL**[31:0]). The PCI Express Root Complex can read the PCI Doorbell Interrupt Active bit (**INTCSR**[13]) to determine whether a PCI Doorbell interrupt is pending; therefore, if (**INTCSR**[13]=1) read the PEX 8311 Local-to-PCI Express Doorbell register.

Each Local-to-PCI Express Doorbell register bit is individually controlled. Local-to-PCI Express Doorbell register bits are set only by the Local Bus. From the Local Bus, writing 1 to any bit position sets that bit and writing 0 has no effect. Local-to-PCI Express Doorbell register bits are cleared only from the PCI Express interface. From the PCI Express interface, writing 1 to any bit position clears that bit and writing 0 has no effect.

The PEX 8311 does not generate PCI Express de-assert interrupt messages when any of the Local-to-PCI Express Doorbell register bits are set, and the PCI Doorbell Interrupt Enable bit is set, and the PCI Interrupt is enabled (**INTCSR**[9:8]=11b, respectively).

To prevent race conditions from occurring when the PCI Express interface is accessing the Local-to-PCI Express Doorbell register (**L2PDBELL**) (or **LCS** registers), the PEX 8311 automatically de-asserts READY# output to prevent Local Bus Configuration accesses.

PCI-to-Local Express Interrupt

The PCI Root Complex can assert a Local interrupt output (LINTo#) by writing 1 to any of the PCI Express-to-Local Doorbell bits (**P2LDBELL**[31:0]). The Local processor can read the Local Doorbell Interrupt Active bit (**INTCSR**[20]) to determine whether a Local doorbell interrupt is pending; therefore, if (**INTCSR**[20]=1) read the PCI Express-to-Local Doorbell register.

Each PCI Express-to-Local Doorbell register bit is individually controlled. PCI Express-to-Local Doorbell register bits are set only by the PCI Express interface. From the PCI Express interface, writing 1 to any bit position sets that bit and writing 0 has no effect. PCI Express-to-Local Doorbell register bits are cleared only from the Local Bus. From the Local Bus, writing 1 to any bit position clears that bit and writing 0 has no effect.

Note: *When the Local Bus cannot clear a Doorbell interrupt, do* ***not*** *use the PCI Express-to-Local Doorbell register.*

The Local interrupt remains set when any PCI Express-to-Local Doorbell register bits are set and the Local Doorbell Interrupt Enable bit is set (**INTCSR**[17]=1).

To prevent race conditions when the Local Bus is accessing the PCI Express-to-Local Doorbell register (or Local Configuration registers), the PEX 8311 automatically issues an internal Retry to the PCI Express Address spaces.

13.2.1.3 Internal Master/Target Abort Interrupt

The PEX 8311 sets the internal PCI Bus Received Master or Target Abort bit (the PEX 8311 **LCS PCI** register **PCISR**[13 or 12]=1, respectively) internally when accessing PEX 8311 PCI Express Address space, and it detects an internal Master or Target Abort. These status bits cause the PCI Express message interrupt to generate when interrupts are enabled (**LCS INTCSR**[10, 8]=11b).

The interrupt remains set when the Received Master or Target Abort bit remains set and the PCI Master/Target Abort interrupt is enabled. Use PCI Type 1 (Type 1 is converted to Type 0 internally) PCI Express Configuration or Local accesses to the **LCS PCI** register to clear the internal PCI Bus Received Master and Target Abort bits (**PCISR**[13:12]=00b, respectively).

The Interrupt Control/Status bits (**INTCSR**[26:24]) are latched at the time of internal PCI Master or Target Abort interrupt. When an abort occurs, these bits provide information, *such as* which device was the Master when the abort occurred. In addition, when internal Master or Target Abort occurs, the current Address (Abort Address) is stored in the PCI Abort Address bits (**LCS PABTADR**[31:0]) register).

13.2.2 PCI Express Bridge Internally Generated Interrupts

PCI Express Bridge interrupts from internal sources are gated by the **PECS PCIIRQENB** register, and support several internal bridge functions. Sources of PCI Express Bridge interrupts are as follows:

- Serial EEPROM done
- GPIO Interrupt active
- PCI Express-to-PCI Retry interrupt
- Mailbox interrupt
- PCI Express Internal interrupt

13.2.2.1 PCI Express Configuration Space Mailbox Register Interrupts

The PEX 8311 PCI Express interface logic has four, 32-bit Mailbox registers that are written to and read from the PCI Express interface and Local Bus. These registers are used to pass command and status information directly between the PCI Express and Local Bus devices. (Refer to Figure 13-3.) For PCI Express and Local Bus Master to access Mailbox registers a Memory- or I/O-Mapped access through the **PECS PCIBASE0** register must be performed.

In Endpoint mode, the PEX 8311 is programmed to generate PCI Express interrupts (either virtual wire or message interrupt) only as a result of the Mailbox Write accesses, when enabled (**PCIEIRQENB** register). The Mailbox interrupt statuses are located in the **Interrupt Request Status (IRQSTAT)** register. Writing 1 to a Mailbox interrupt status register clears the respective Mailbox interrupt.

13.3 PCI Express Interrupt Messaging

There are two types of messaging supported for PCI Express Interrupts

- Virtual Wire (INTA#) messaging, as defined in the *PCI Express Base 1.0a*
- Message Signaled Interrupts (MSI), as defined in the *PCI r3.0*

These two messaging types are mutually exclusive, and only one or the other can be used in a system design.

13.3.1 Virtual Wire Interrupts

When MSI is disabled, virtual wire interrupts are used to support internal interrupt events. Internal interrupt sources are masked by the **PECS PCI Command** register *Interrupt Disable* bit and are routed to one of the virtual interrupts using the **Internal PCI Wire Interrupt** register. PCI Express Assert_INTA and Deassert_INTA messages are not masked by the **PCI Command** register *Bus Master Enable* bit. The internal interrupt is processed the same as the external Local LINTi# signal.

Local interrupts are "virtualized" in PCI Express, using Assert_INTA and Deassert_INTA messages for the internal PCI wire interrupt. This message pairing provides a mechanism to preserve the level-sensitive semantics of the PCI interrupts. The Assert_INTA and Deassert_INTA messages transmitted on the PCI Express link capture the asserting/de-asserting edge of the respective source of the interrupt.

For example, if all interrupt sources are enabled and not active, activation of one interrupt source causes an Assert_INTA message to be sent to PCI Express space. Subsequent assertions of other interrupt sources, provided at least one interrupt source remains asserted, do not cause subsequent Assert_INTA messages. When all pending interrupts are cleared or disabled, a Deassert_INTA message is sent to PCI Express Space.

The Requester ID used in the PCI Express Assert_INTA and Deassert_INTA messages transmitted by the PEX 8311 (irrespective of whether the source is internal or external to the bridge) equals the bridge PCI Express interface Bus and Device Numbers. The Function Number subfield is cleared to 0.

13.3.2 Message Signaled Interrupts

The PEX 8311 supports interrupts using Message Signaled Interrupts (MSI), as defined in the *PCI r3.0*. With this mechanism, the PEX 8311 signals an interrupt by writing to a specific memory location. The PEX 8311 uses the 64-bit Message Address version of the MSI capability structure and clears the *No Snoop* and *Relaxed Ordering* bits in the Requester Attributes. **PECS MSIADDR**, **MSIUPPERADDR**, and **MSIDATA** registers are associated with the MSI feature. (Refer to Chapter 18, "PCI Express Configuration Registers," for details.) When an internal interrupt event occurs, the value in the MSI Data Configuration register is written to the PCI Express address specified by the **MSI Address Configuration** registers.

The MSI feature is enabled by the **Message Signaled Interrupts Control** (**MSICTL)** register *MSI Enable* bit. When MSI is enabled, the virtual wire interrupt feature is disabled. MSI interrupts are generated independently of the **PCI Command** register *Interrupt Disable* bit. MSI interrupts are gated by the **PCI Command** register *Bus Master Enable* bit.

Note: *The No Snoop and Relaxed Ordering bits are cleared because the PEX 8311 does not support these features.*

13.3.3 Local Interrupt Output (LINTo#)

The PEX 8311 Local Interrupt output (LINTo#) is asserted, when enabled (**INTCSR**[16]=1), by one of the following:

- PCI Express-to-Local Doorbell register Write access
- PCI Express-to-Local Mailbox register (**MBOX0**, **MBOX1**, **MBOX2**, and/or **MBOX3**) Write access
- Internal Built-In Self-Test interrupt
- DMA Channel *x* Done or Abort interrupt
- DMA Channel *x* Terminal Count is reached
- Messaging Inbound Post Queue is not empty
- Power management state change
- Local Data Parity Error for Direct Master Write, Direct Slave Read, and DMA Local-to-PCI Express transactions

LINTo#, or individual sources of an interrupt, are enabled, disabled, or cleared, using the PEX 8311 register bit(s) described in this section. In addition, interrupt status bits for each interrupt source are provided.

13.3.4 Local System Error, LSERR# (Local NMI)

An LSERR# interrupt is asserted when any of the following conditions occur:

- Internal PCI Bus Received Master Abort (UR) or Target Abort (CA) bit is set (PCISR[13 or 12]=1, respectively)
- Detected Parity Error bit is set (PCISR[15]=1)
- Direct Master Write/Direct Slave Read Local Data Parity Check Error Status bit is set (INTCSR[7]=1)
- Messaging Outbound Free queue overflows
- Fatal and Non-Fatal error (internal SERR#) assertion when ROOT_COMPLEX# is asserted low

LSERR# is always enabled. INTCSR[12, 6, 1:0] is used to enable or disable LSERR# sources. (Refer to Figure 13-2.) Local Parity errors are masked from asserting LSERR#, using INTCSR[6]. LSERR# is a level output that remains asserted when the Interrupt Status or Enable bits are set.

13.3.5 Built-In Self-Test Interrupt (BIST)

A PCI Express Root Complex can assert a Local interrupt by performing a PCI Express Type 1 Configuration write to Local Configuration space (Type 1 is internally converted to Type 0) that sets the *PCI Built-In Self-Test Interrupt Enable* bit (**PCIBISTR**[6]=1). A Local processor can read the BIST Interrupt Active bit (**INTCSR**[23]) to determine whether a BIST interrupt is pending.

The Local interrupt and **INTCSR**[23] remain set when **PCIBISTR**[6]=1. The Local Bus then resets **INTCSR**[23] by way of **PCIBISTR**[6] when the BIST interrupt completes.

Note: *The PEX 8311 does **not** have an internal BIST.*

13.3.6 DMA Channel *x* Interrupt

A DMA channel can assert a PCI Express message or Local interrupt when done (transfer is complete), or, in DMA Scatter/Gather mode, after a transfer is complete for the current descriptor. The DMA Channel Interrupt Select bit(s) (**LCS DMAMODE*x***[17]) selects the routing of the interrupt, PCI Express or Local Bus (Assert_INTA or LINTo#, respectively). The PCI Express Root Complex or Local Bus Master can read the DMA Channel Interrupt Active bit(s) (**INTCSR**[22 and/or 21]=1) to determine whether a DMA Channel interrupt is pending.

The DMA Channel Done bit(s) (**DMACSR*x***[4]) are used to determine whether an interrupt is one of the following:

- DMA Done interrupt
- Transfer complete for current descriptor interrupt
- DMA Transfer was aborted

The DMA Channel Done Interrupt Enable bit(s) (**DMAMODE*x***[10]=1) enables a Done interrupt. In DMA Scatter/Gather mode, the DMA Channel *x* Descriptor Pointer register Channel Interrupt after the Terminal Count bit(s) (**DMADPR*x***[2]) specifies whether to assert an interrupt at the end of the transfer for the current descriptor.

A DMA Channel interrupt is cleared by writing 1 to the Channel Clear Interrupt bit(s) (**DMACSR*x***[3]=1).

13.4 Root Complex Mode PCI Express Interrupts

In Root Complex mode, the PEX 8311 passes PCI Express Assert_INTA or Deassert_INTA message interrupts as they are received to the Local Bus (LINTo#). The PEX 8311 recognizes only INTA types of PCI Express interrupts received on the PCI Express in Root Complex mode. The internal PCI wire interrupt (INTA#) is asserted and passed to the Local Bus, independently of the **PECS PCI Command** register *Interrupt Disable* bit. The internal PCI wire interrupt signal is asserted only when the PEX 8311 is in power state D0.

13.4.1 Local Interrupt Output (LINTo#)

The PEX 8311 Local Interrupt output (LINTo#) is programmed and asserted, when enabled (**INTCSR**[16]=1), by one of the following:

- **PECS** serial EEPROM transaction performed
- Any GPIO bit that is programmed as an input
- Mailbox registers written
- PCI Express Assert_INTA interrupt message
- PCI Express-to-Local Doorbell register Write access
- PCI Express-to-Local Mailbox register (**MBOX0**, **MBOX1**, **MBOX2**, and/or **MBOX3**) Write access
- Internal Built-In Self-Test interrupt
- DMA Channel x Done or Abort interrupt
- DMA Channel x Terminal Count is reached
- Messaging Inbound Post Queue is not empty
- Power management state change
- Local Data Parity Error for Direct Master Write, Direct Slave Read, and DMA Local-to-PCI Express transactions

LINTo#, or individual sources of an interrupt, are enabled, disabled, or cleared, using the PEX 8311 register bit(s) described in this section. In addition, interrupt status bits for each interrupt source are provided.

Local Parity errors are masked separately from asserting LINTo# using **INTCSR**[6]. The LINTo# signal is a level output that remains asserted when the Interrupt Status or Enable bits are set.

13.4.1.1 Internal INTA# Wire Signals

When an internal interrupt event occurs, it can cause the internal INTA# wire to assert and pass to the Local Bus. Internal PCI Express interrupt sources are masked by the PEX 8311 **PECS PCI Command** register *Interrupt Disable* bit and are routed to the INTA# wire signals, using the **Internal PCI Wire Interrupt** register. The INTA# signal is asserted only when Message Signaled Interrupts (MSI) are disabled.

13.4.1.2 Message Signaled Interrupts

The PEX 8311 does not support Message Signaled Interrupts (MSI) generated by downstream devices on the PCI Express interface. With this mechanism, devices signal an interrupt by writing to a specific memory location. The PEX 8311 uses the 64-bit Message Address version of the MSI capability structure. There are address and data configuration registers associated with the MSI feature – **PECS MSIADDR**, **MSIUPPERADDR**, and **MSIDATA**. When an internal interrupt event occurs, the value in the MSI Data configuration register is written to one of the Local Address Space address-mapped locations (Direct Slave Space 0, Direct Slave Space 1, and/or Expansion ROM) specified by the MSI Address Configuration registers.

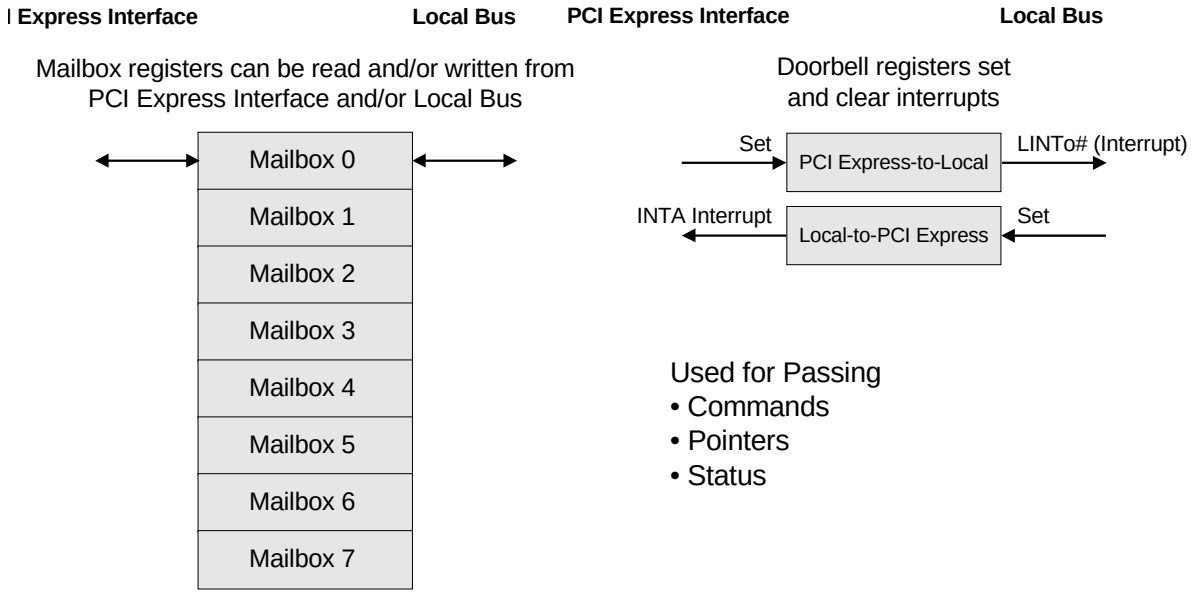
The MSI feature is enabled by the **MSICTL** register *MSI Enable* bit. When MSI is enabled, the internal INTA# wire interrupt signals for internally generated interrupts are disabled. Local Bus interrupt (LINTo#) signal is not asserted. MSI interrupts are generated independently of the PEX 8311 **PECS PCI Command** register *Interrupt Disable* bit. MSI interrupts are gated by the **PCI Command** register *Bus Master Enable* bit.

13.4.2 PCI Express Configuration Space Mailbox Register Interrupts

The PEX 8311 PCI Express interface logic has four, 32-bit Mailbox registers that are written to and read from the PCI Express interface and Local Bus. These registers are used to pass command and status information directly between the PCI Express and Local Bus devices. (Refer to Figure 13-4.) For PCI Express and Local Bus Masters to access Mailbox registers, a Memory- or I/O-Mapped access through **PECS PCIBASE0** register must be performed.

In Root Complex mode, the PEX 8311 is programmed to generate Local interrupts only as a result of the Mailbox Write accesses, when enabled (**PCIIRQENB** register). To pass the interrupt to the Local Bus, **LCS INTCSR**[8, 16] must be enabled. The Mailbox interrupt statuses are located in the **Interrupt Request Status (IRQSTAT)** register. Writing 1 to a Mailbox interrupt status register clears the respective Mailbox interrupt.

Figure 13-4. Mailbox and Doorbell Message Passing



13.4.3 Local Configuration Space Mailbox Register Interrupts

The PEX 8311 Local Bus logic has eight, 32-bit Mailbox registers that are written to and read from the PCI Express interface and Local Bus. These registers are used to pass command and status information directly between the PCI Express and Local Bus devices. (Refer to Figure 13-4.) For PCI Express to access Mailbox registers a Type 1 Configuration access (Type 1 access is internally converted to Type 0) must be performed to Local Configuration space.

A Local interrupt (LINTo#) is asserted, when enabled (**LCS INTCSR**[3, 16]=11b), when the PCI Express Root Complex writes to one of the first four Mailbox registers (**MBOX0**, **MBOX1**, **MBOX2**, or **MBOX3**).

Regardless of whether LINTo# is enabled, a PCI Express write to one of these four Mailbox registers sets a corresponding status bit in **INTCSR**[31:28], provided the Mailbox interrupts are enabled (**INTCSR**[3]=1).

To clear the LINTo# assertion caused by the PCI Express Root Complex write(s) of any of the four Mailbox registers, a Local Bus device must read each Mailbox register that was written.

13.4.4 Doorbell Registers

The PEX 8311 has two 32-bit Doorbell registers. One is assigned to the PCI Express interface; the other to the Local Bus interface.

A PCI Express Root Complex can assert a Local interrupt output (LINTo#) by writing any number other than all zeros (0) to the PCI Express-to-Local Doorbell bits (the PEX 8311 **LCS P2LDBELL**[31:0] register). The Local Interrupt remains asserted until all **P2LDBELL** bits are cleared to 0. A Local processor can cause a PCI Express assert message interrupt generation by writing any number other than all zeros (0) to the *Local-to-PCI Express Doorbell* bits (**LCS L2PDBELL**[31:0]). The PEX 8311 generates a PCI Express de-assert PCI Express message interrupt after all **L2PDBELL** bits are cleared to 0h. (Refer to Figure 13-4.)

13.4.4.1 Local-to-PCI Express Interrupt

A Local Bus Master cannot cause the PEX 8311 to generate a PCI Express message interrupt by writing to the Local-to-PCI Express Doorbell bits (**L2PDBELL**[31:0]). In the PCI Express system interrupts are routed to the Root Complex and can only be generated upstream. When a Local Bus Master (Root Complex device) must pass information to downstream devices by way of the Local-to PCI Express Doorbell register, it can still perform a write to the Doorbell register. Downstream devices can poll the PCI Doorbell Interrupt Active bit (**LCS INTCSR**[13]) by way of a Memory-Mapped transaction, to determine whether a PCI Doorbell interrupt is pending; therefore, if (**INTCSR**[13]=1) read the Local-to-PCI Express Doorbell register by way of a Memory-Mapped transaction.

Each Local-to-PCI Express Doorbell register bit is individually controlled. Local-to-PCI Express Doorbell register bits are set only by the Local Bus. From the Local Bus, writing 1 to any bit position sets that bit and writing 0 has no effect. Local-to-PCI Express Doorbell register bits are cleared only from the PCI Express interface. From the PCI Express interface, writing 1 to any bit position clears that bit and writing 0 has no effect.

To prevent race conditions from occurring when the PCI Express interface is accessing the Local-to-PCI Express Doorbell register (**L2PDBELL**) (or **LCS** registers), the PEX 8311 automatically de-asserts READY# output to prevent Local Bus Configuration accesses.

13.4.4.2 PCI Express-to-Local Interrupt

Downstream devices can assert a Local interrupt output (LINTo#) by writing 1 to any PCI Express-to-Local Doorbell bits (**P2LDBELL**[31:0]). The Local processor can read the Local Doorbell Interrupt Active bit (**INTCSR**[20]) to determine whether a Local Doorbell interrupt is pending; therefore, if (**INTCSR**[20]=1) read the PCI Express-to-Local Doorbell register.

Each PCI Express-to-Local Doorbell register bit is individually controlled. PCI Express-to-Local Doorbell register bits are set only by the PCI Express interface. From the PCI Express interface, writing 1 to any bit position sets that bit and writing 0 has no effect. PCI Express-to-Local Doorbell register bits are cleared only from the Local Bus. From the Local Bus, writing 1 to any bit position clears that bit and writing 0 has no effect.

Note: *When the Local Bus cannot clear a Doorbell interrupt, do **not** use the PCI Express-to-Local Doorbell register.*

The Local interrupt remains set when any PCI Express-to-Local Doorbell register bits are set and the Local Doorbell Interrupt Enable bit is set (**INTCSR**[17]=1).

To prevent race conditions when the Local Bus is accessing the PCI Express-to-Local Doorbell register (or Local Configuration registers), the PEX 8311 automatically issues internal Retry to the PCI Express Address Spaces.

13.4.5 DMA Channel *x* Interrupt

A DMA channel can assert a Local interrupt when done (transfer is complete), or, in DMA Scatter/Gather mode, after a transfer is complete for the current descriptor. The DMA Channel Interrupt Select bit(s) (**LCS DMAMODE*x***[17]) must be set to route the interrupt to Local Bus (LINTo#). In the PCI Express, system interrupts are routed upstream to the Root Complex. The Local Bus Master can read the DMA Channel Interrupt Active bit(s) (**INTCSR**[22 and/or 21]=1) to determine whether a DMA Channel interrupt is pending.

The DMA Channel Done bit(s) (**DMACSR*x***[4]) are used to determine whether an interrupt is one of the following:

- DMA Done interrupt
- Transfer complete for current descriptor interrupt
- DMA Transfer was aborted

The DMA Channel Done Interrupt Enable bit(s) (**DMAMODE*x***[10]=1) enables a Done interrupt. In DMA Scatter/Gather mode, the DMA Channel *x* Descriptor Pointer register Channel Interrupt after Terminal Count bit(s) (**DMADPR*x***[2]) specifies whether to assert an interrupt at the end of the transfer for the current descriptor.

A DMA Channel interrupt is cleared by writing 1 to the Channel Clear Interrupt bit(s) (**DMACSR*x***[3]=1).

13.4.6 Local Interrupt Input (LINTi#)

The PEX 8311 ignores the Local Interrupt Input (LINTi#) signal assertion in Root Complex mode.

Chapter 14 PCI Express Messages

14.1 Endpoint Mode PCI Express Messages

PCI Express defines a set of messages that are for in-band communication of events (*such as* interrupts), generally replacing the need for sideband signals. These messages can also be used for general-purpose messaging. This section describes the PCI Express-to-Local Bus support requirements for these messages.

PCI Express messages are routed explicitly or implicitly, depending on specific bit field encodings in the message request header. An explicitly routed message is routed based on a specific address, or an ID field contained within the message header. The destination of an implicitly routed message is inferred from the message *Type* field.

14.1.1 PCI INTA# Virtual Wire Interrupt Signaling

INTA# Interrupt Signaling messages are used for in-band communication to the Local Bus. (Refer to Section 13.2, "Endpoint Mode PCI Express Interrupts," for details.)

14.1.2 Power Management Messages

Power Management messages support Power Management Events, signaled by sources integrated into the PEX 8311 and for Local Bus devices. (Refer to Section 12.1, "Endpoint Mode Power Management," for details.)

14.1.3 Error Signaling Messages

The PEX 8311 bridge transmits Error Signaling messages on the PCI Express interface, to signal errors for any of the following:

- A particular transaction
- The Link Interface
- Errors internal to the bridge
- Local-related errors detected on the Local Bus interface

The message types include ERR_COR, ERR_FATAL, and ERR_NONFATAL. The relevant Mask bits are located in the PCI Express Capability structure. (Refer to Section 10.1, "Endpoint Mode Error Handling," for details.)

14.1.4 Locked Transactions Support

PCI Express Unlock messages support Locked Transaction sequences in the downstream direction. (Refer to Section 11.1, "Endpoint Mode Exclusive Accesses," for details.)

14.1.5 Slot Power Limit Support

The Root Complex or a switch transmit the Set_Slot_Power_Limit message to endpoints, including bridges. The PEX 8311 supports and complies with these messages. These messages are particularly relevant to devices implemented on add-in boards. (Refer to Section 12.1, "Endpoint Mode Power Management," for details.)

14.1.6 Hot Plug Signaling Messages

The PEX 8311 does ***not support*** Hot Plug signaling, and ignores the associated messages.

14.2 Root Complex Mode PCI Express Messages

In Root Complex mode (ROOT_COMPLEX# pin low), the PEX 8311 provides support for the following message types:

- PCI Express Virtual Wire interrupts
- Power Management interrupts
- Error messages

14.2.1 PCI INTA# Virtual Wire Interrupt Message Support

The PEX 8311 controls the state of the corresponding Local Bus interrupt balls, based on the Assert_INTA and Deassert_INTA messages received. (Refer to Section 13.4, "Root Complex Mode PCI Express Interrupts," for details.)

14.2.2 Power Management Message Support

The PEX 8311 generates a PME_Turn_Off message when placed into power state D3. The PEX 8311 then waits for the PME_TO_Ack message from the downstream device on the PCI Express interface before proceeding with the power-down sequence.

14.2.2.1 PME Handling Requirements

The PEX 8311 asserts PMEOUT# on the Local Bus for the following PCI Express events:

- PCI Express WAKEIN# signal is asserted while the link is in the L2 state
- PCI Express beacon is received while the link is in the L2 state
- PCI Express PM_PME message is received

For compatibility with existing software, the PEX 8311 does not signal PMEOUT# unless PMEOUT# signaling is enabled by the **PECS PWRMSGCSR** register *PME Enable* bit. The PEX 8311 sets the *PME Status* bit when PMEOUT# is signaled and clears PMEOUT# when the *PME Status* or *PME Enable* bit is cleared. PME messages received while the *PME Enable* bit is cleared are ignored and the *PME Status* bit is not set during this time.

14.2.3 Error Signaling Message Support

The PEX 8311 converts ERR_COR, ERR_FATAL, and ERR_NONFATAL messages to LSERR# on the Local Bus. (Refer to Section 10.2, "Root Complex Mode Error Handling," for details.)

14.2.4 Locked Transaction Support

The PEX 8311 is allowed to pass Locked transactions from the Local Bus to the PCI Express interface. The PEX 8311 uses the Memory Read Locked request to initiate a locked sequence when a locked request is transmitted on the Local Bus. Subsequent Locked Read transactions targeting the bridge use the Memory Read Locked request on PCI Express. Subsequent Locked Write transactions use the Memory Write request on the PCI Express interface. The PEX 8311 transmits the Unlock message when the Local Lock sequence is complete. (Refer to Section 11.2, "Root Complex Mode Exclusive Accesses," for details.)

14.2.5 Slot Power Limit Support

The Root Complex transmits the Set Slot Power Limit message to endpoints. The PEX 8311 supports and complies with these messages. These messages are particularly relevant to devices implemented on add-in boards. (Refer to Section 12.2, "Root Complex Mode Power Management," for details.)

Chapter 15 Intelligent I/O (I_2O)

15.1 Introduction

This chapter discusses the I_2O-compatible Messaging Unit.

15.2 I_2O-Compatible Messaging Unit

The I_2O-compatible Messaging Unit supplies two message paths (refer to the *I_2O r1.5* for details):

- Two inbound FIFOs to receive messages from the PCI Express interface
- Two outbound FIFOs to pass messages to the PCI Express interface

I_2O-compatible Messaging Unit Configuration registers are located in Local Configuration space. Accesses to these registers from the PCI Express interface are accomplished by way of Memory-Mapped transactions.

Figure 15-1 and Figure 15-2 illustrate I_2O architecture.

Figure 15-1. Typical I2O Server/Endpoint Board Design

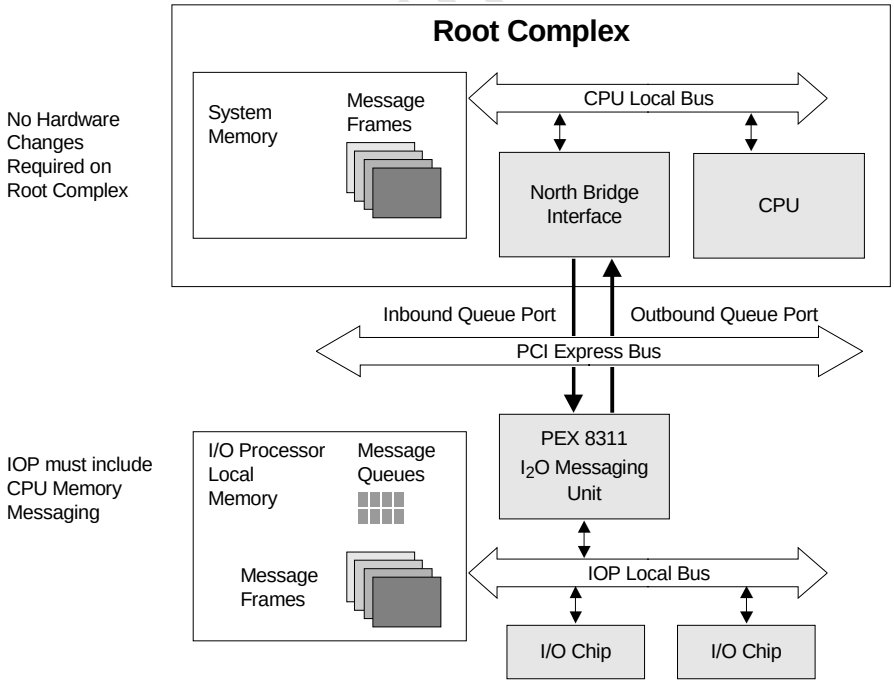
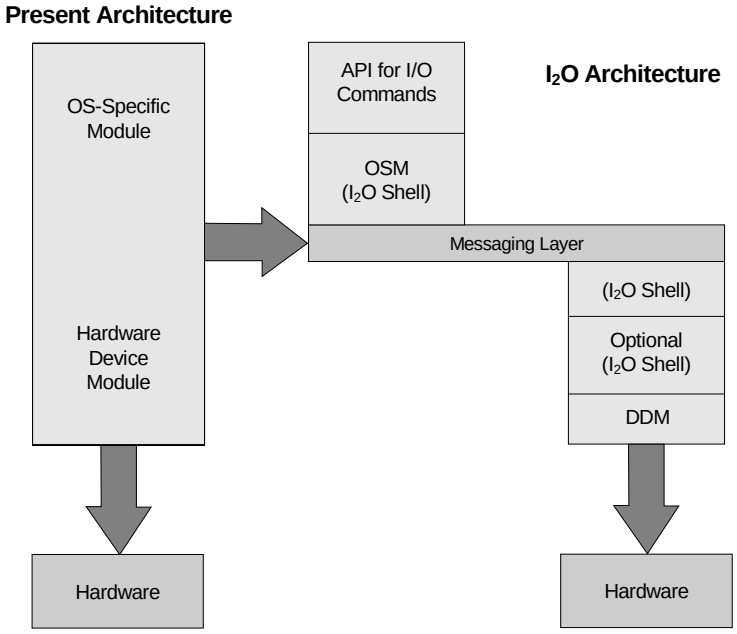


Figure 15-2. Driver Architecture Compared



Note: *The acronyms used in Figure 15-2 are defined as follows:*

- *OS – Operating System*
- *OSM – Operating System Manager*
- *API – Application Programming Interface*
- *DDM – Driver Developing Manager*

15.2.1 Inbound Messages

Inbound messages reside in a pool of message frames (minimum 64-byte frames) allocated in the shared Local Bus I/O Processor (IOP) memory. The inbound message queue is comprised of a pair of rotating FIFOs implemented in Local memory. The Inbound Free List FIFO holds the Message Frame Addresses (MFAs) of available message frames in Local memory. The Inbound Post Queue FIFO holds the MFAs of all currently posted messages in Local Bus IOP memory.

External PCI Express agents, through the Inbound Queue Port location in PCI Express Address space, access the inbound circular FIFOs. (Refer to Table 15-2.) The Inbound Queue Port, when read by an external PCI Express agent, returns an Inbound Free List FIFO MFA. The external PCI Express agent places the MFA into the Inbound Post Queue FIFO by writing its MFA to the Inbound Queue Port location.

15.2.2 Outbound Messages

Outbound messages reside in a pool of message frames (minimum 64-byte frames) allocated in the shared PCI Express interface (System) memory. The Outbound message queue is comprised of a pair of rotating FIFOs implemented in Local memory. The Outbound Free List FIFO holds the MFAs of available message frames in the System memory. The Outbound Post Queue FIFO holds the MFAs of all currently posted messages in the Local Bus (IOP) memory.

External PCI Express agents, through the Outbound Queue Port location in PCI Express Address space, access the outbound circular FIFOs. (Refer to Table 15-2.) The Outbound Queue Port, when read by an external PCI Express agent, returns the Outbound Post Queue FIFO MFA. The External PCI Express agent places free message frames into the Outbound Free List FIFO by writing the free MFA into the Outbound Queue Port location.

Memory for the circular FIFOs must be allocated in Local (IOP) memory. The queue base address is contained in the *Queue Base Address* bits (**QBAR**[31:20]). Each FIFO entry is a 32-bit data value. Each read and write of the queue must be a single 32-bit access.

Circular FIFOs range in size from 4-KB to 64-KB entries. The four FIFOs must be the same size and contiguous. Therefore, the total amount of Local memory needed for circular FIFOs ranges from 64 KB to 1 MB. FIFO size is specified in the *Circular Queue Size* bits (**MQCR**[5:1]).

The starting address of each FIFO is based on the Queue Base Address and the FIFO Size, as delineated in Table 15-1.

Table 15-1. Queue Starting Address

FIFO	Starting Address
Inbound Free List	QBAR
Inbound Post List	QBAR + (1 * FIFO Size)
Outbound Post List	QBAR + (2 * FIFO Size)
Outbound Free List	QBAR + (3 * FIFO Size)

15.2.3 I_2O Pointer Management

The FIFOs always reside in shared Local (IOP) memory and are allocated and initialized by the IOP. Before setting the *Queue Enable* bit (**MQCR**[0]=1), the Local processor must initialize the following registers, with the initial offset according to the configured FIFO size:

- **Inbound Post** and **Free Head Pointer** (**IPHPR** and **IFHPR**, respectively)
- **Inbound Post** and **Free Tail Pointer** (**IPTPR** and **IFTPR**, respectively)
- **Outbound Post** and **Free Head Pointer** (**OPHPR** and **OFHPR**, respectively)
- **Outbound Post** and **Free Tail Pointer** (**OPTPR** and **OFTPR**, respectively)

The PEX 8311 automatically adds the Queue Base Address to the offset in each head and tail pointer register. The software can then enable I_2O. After initialization, ensure that the Local software does ***not*** write to the pointers managed by the PEX 8311 hardware.

Empty flags are set when the queues are disabled (MQCR[0]=0), or the head and tail pointers are equal. This occurs independently of how the head and tail pointers are set.

An empty flag is cleared, signifying not empty, only when the queues are enabled (MQCR[0]=1) and the pointers become not equal.

When an empty flag is cleared and the queues are enabled, the empty flag is set only when the tail pointer is incremented and the head and tail pointers become equal.

Full flags are always cleared when the queues are disabled or the head and tail pointers are not equal.

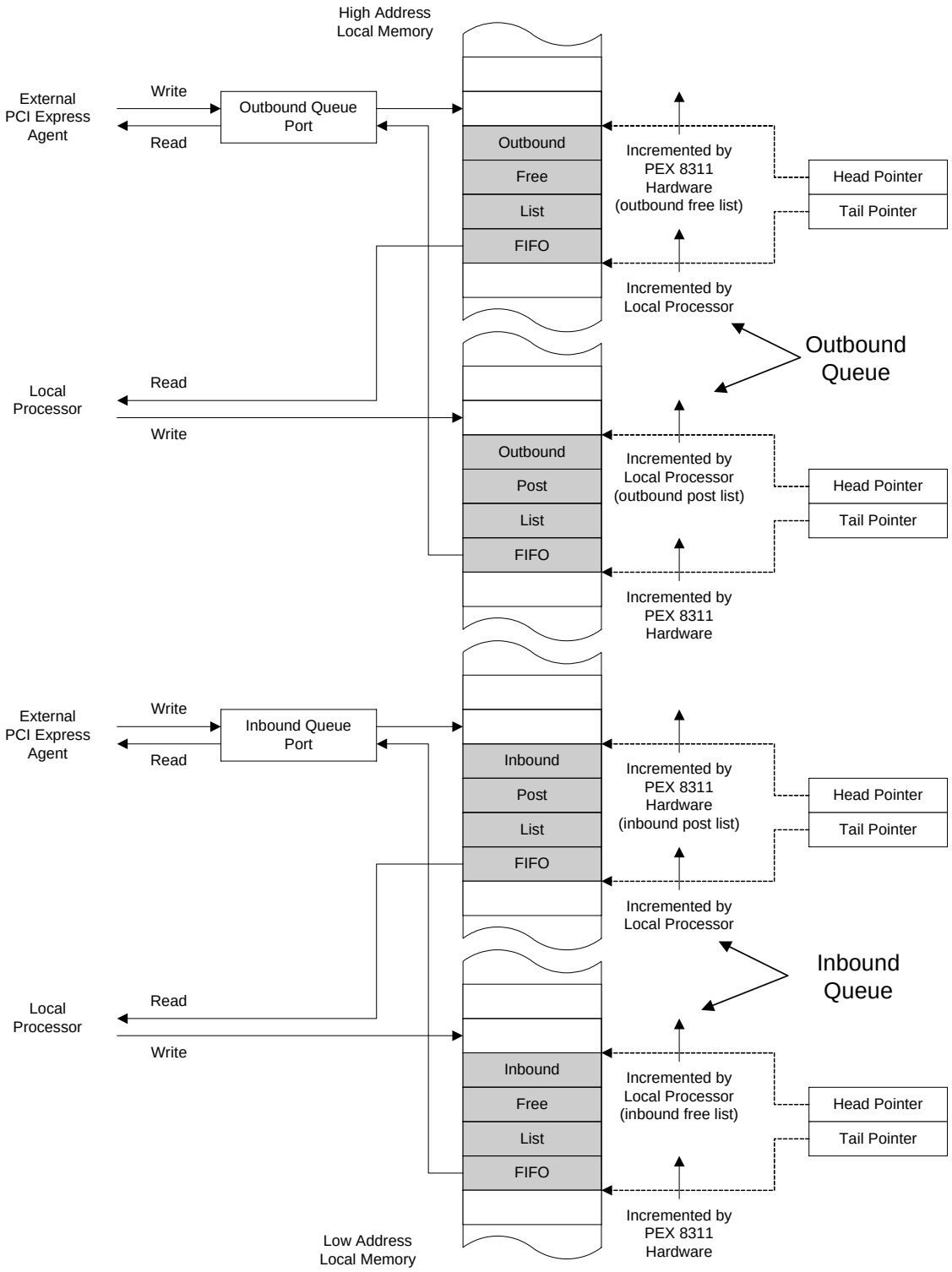
A full flag is set when the queues are enabled, the head pointer is incremented, and the head and tail pointers become equal.

Each circular FIFO has a head pointer and a tail pointer, which are offsets from the Queue Base Address. (Refer to Table 15-2.) Writes to a FIFO occur at the head of the FIFO and reads occur from the tail. Head and tail pointers are incremented by the Local processor or PEX 8311 hardware. The unit that writes to the FIFO also maintains the pointer. Pointers are incremented after a FIFO access. Both pointers wrap around to the first address of the circular FIFO when they reach the FIFO size, allowing the head and tail pointers to continuously "chase" one another in the circular FIFO. The PEX 8311 automatically wraps the pointers that it maintains. The IOP software must wrap the pointers that it maintains. When they are equal, the FIFO is empty. To prevent overflow conditions, I_2O specifies that the number of message frames allocated are to be less than or equal to the number of entries in a FIFO. (Refer to Figure 15-3.)

Each inbound MFA is specified by I_2O as the offset from the start of shared Local (IOP) memory to the start of the message frame. Each outbound MFA is specified as the offset from System memory location 00000000h to the start of the message frame in shared System memory. Because the MFA is an actual address, the message frames need not be contiguous. The IOP allocates and initializes inbound message frames in shared IOP memory, using any suitable memory-allocation technique. The System allocates and initializes outbound message frames in shared System memory using any suitable memory allocation technique. Message frames are a minimum of 64 bytes in length.

I_2O uses a "push" (write-preferred) memory model. That means the IOP writes messages and data to the shared System memory, and the System writes messages and data to shared IOP memory. Ensure that software makes use of Burst and DMA transfers wherever possible to guarantee efficient use of the PCI Express interface for message passing. (Refer to the *I_2O r1.5* for further details about message passing implementation.)

Figure 15-3. Circular FIFO Operation



15.2.4 Inbound Free List FIFO

The Local processor allocates inbound message frames in its shared memory and can place the address of a free (available) message frame into the Inbound Free List FIFO by writing its MFA into the FIFO location pointed to by the **Queue Base** register + Inbound Free Head Pointer register (IFHPR). The Local processor must then increment the **IFHPR** register.

A PCI Express Root Complex or other PCI Express IOP can obtain the MFA of a free message frame by reading the Inbound Queue Port Address (40h). When the FIFO is empty (no free inbound message frames are currently available, head and tail pointers are equal), the PEX 8311 returns 1 (FFFFFFFFh). When the FIFO is not empty (head and tail pointers are not equal), the PEX 8311 reads the MFA pointed to by the **Queue Base** register + **Inbound Free Tail Pointer** register (**IFTPR**), returns its value, and increments the **IFTPR** register. When the Inbound Free Queue is not empty, and the *Inbound Free Queue Prefetch Enable* bit is set (**QSR**[3]=1), the next entry in the FIFO is read from the Local Bus into a prefetch register. The prefetch register then provides the data for the next PCI Express Read request from this queue, thereby reducing the number of potential wait states gathering the data from the Local Bus. (Refer to Figure 15-3.)

15.2.5 Inbound Post Queue FIFO

A PCI Express Root Complex or other PCI Express IOP can write a message into an available message frame in the shared Local (IOP) memory. It can then post that message by writing the MFA to the Inbound Queue Port Address (40h). When the port is written, the PEX 8311 writes the MFA to the Inbound Post Queue FIFO location pointed to by the **Queue Base register** + FIFO Size + Inbound Post **Head Pointer** register (**IPHPR**). After the PEX 8311 writes the MFA to the Inbound Post Queue FIFO, it increments the **IPHPR** register.

The **Inbound Post Tail Pointer** register (**IPTPR**) points to the Inbound Post Queue FIFO location that holds the MFA of the oldest posted message. The Local processor maintains the tail pointer. After a Local processor reads the oldest MFA, it can remove the MFA from the Inbound Post Queue FIFO by incrementing the **IPTPR** register.

The PEX 8311 asserts a Local interrupt when the Inbound Post Queue FIFO is not empty. The *Inbound Post Queue Interrupt Not Empty* bit (**QSR**[5]) indicates the interrupt status. The interrupt clears when the Inbound Post Queue FIFO is empty. The *Inbound Post Queue Interrupt Not Empty Mask* bit can mask the interrupt (**QSR**[4]=1).

From the time a PCI Express Write transaction is received, Direct Slave accesses to the PEX 8311 are issued internal Retry between PCI Express Address and Local Address Spaces (data accumulated in the PCI Express Queue), until the data is written in Local memory and the **Inbound Post Head Pointer** register (**IPHPR**) is incremented.

15.2.6 Outbound Post Queue FIFO

A Local Master (IOP) can write a message into an available message frame in shared Host memory. It can then post that message by writing the MFA to the Outbound Post Queue FIFO location pointed to by the **Queue Base** register + **Outbound Post Head Pointer** register (**OPHPR**) + (2 * FIFO Size). The Local processor then increments the **OPHPR** register.

A PCI master can obtain the MFA of the oldest posted message by reading the Outbound Queue Port Address (44h). When the FIFO is empty (no more outbound messages are posted, head and tail pointers are equal), the PEX 8311 returns -1 (FFFFFFFFh). When the Outbound Post Queue FIFO is not empty (head and tail pointers are not equal), the PEX 8311 reads the MFA pointed to by the **Queue Base** register + (2 * FIFO Size) + **Outbound Post Tail Pointer** register (**OPTPR**), returns its value, and increments the **OPTPR** register.

The PEX 8311 generates a PCI Express message interrupt, when enabled when the **Outbound Post Head Pointer** register (**OPHPR**) is not equal to the **Outbound Post Tail Pointer** register (**OPTPR**). The *Outbound Post Queue Interrupt* bit (**OPQIS**[3]) indicates the interrupt status. When the pointers become equal, both the interrupt and **OPQIS**[3] are automatically cleared. Pointers become equal when a PCI Express Root Complex or other PCI Express IOP reads sufficient FIFO entries to empty the FIFO. The **Outbound Post Queue Interrupt Mask** register can mask the interrupt (**OPQIM**[3]=1).

15.2.7 Outbound Post Queue

To reduce read latency, prefetching from the tail of the queue occurs when the queue is not empty and the tail pointer is incremented (queue has been read from), or when the queue is empty and the head pointer is incremented (queue has been written to). When the PCI Express Root Complex reads the Outbound Post Queue, the data is immediately available.

15.2.8 Inbound Free Queue

To reduce read latency, prefetching from the tail of the queue occurs when the queue is not empty and the tail pointer is incremented (queue has been read from), or when the queue is empty and the head pointer is incremented (queue has been written to). When the PCI Express Root Complex reads the Inbound Free Queue, the data is immediately available.

15.2.9 Outbound Free List FIFO

The PCI Express Root Complex or other PCI Express IOP allocates outbound message frames in its shared memory. The PCI Express Root Complex can place the address of a free (available) message frame into the Outbound Free List FIFO by writing an MFA to the Outbound Queue Port Address (44h). When the port is written, the PEX 8311 writes the MFA to the Outbound Free List FIFO location pointed to by the **Queue Base** register + (3 * FIFO Size) + **Outbound Free Head Pointer** register (**OFHPR**). After the PEX 8311 writes the MFA to the Outbound Free List FIFO, it increments the **OFHPR** register.

When the IOP needs a free outbound message frame, it must first check whether any free frames are available. When the Outbound Free List FIFO is empty (outbound free head and tail pointers are equal), the IOP must wait for the PCI Express Root Complex to place at least one additional outbound free MFA in the Outbound Free List FIFO. When the Outbound Free List FIFO is not empty (head and tail pointers are not equal), the IOP can obtain the MFA of the oldest free outbound message frame by reading the location pointed to by the **Queue Base** register + (3 * FIFO Size) + **Outbound Free Tail Pointer** register (**OFTPR**). After the IOP reads the MFA, it must increment the **OFTPR** register. To prevent overflow conditions, I_2O specifies the number of message frames allocated are to be less than or equal to the number of entries in a FIFO. The PEX 8311 also checks for Outbound Free List FIFO overflows. When the head pointer is incremented and becomes equal to the tail pointer, the Outbound Free List FIFO is full, and the PEX 8311 asserts a Local System Error LSERR# interrupt. The interrupt is recorded in the *Outbound Free Queue Overflow Interrupt Full* bit (**QSR**[7]).

From the time the PCI Express Write transaction is received until the data is written into Local memory and the **Outbound Free Head Pointer** register (OFHPR) is incremented, any Direct Slave access to the PEX 8311 is issued internal Retry between PCI Express Address and Local Address Spaces. The Direct Slave write data is accumulated in the PCI Express Queue.

15.2.10 I_2O Enable Sequence

To enable I_2O, the Local processor performs the following:

- Maps one of the PCI Express Address spaces to Direct Slave Space 1
- Initializes Direct Slave Space 1 address and range (minimum 1,024 bytes)
- Initializes all FIFOs and Message Frame memory
- Sets the **LCS** *PCI Base Class Code* bits (**PCICCR**[23:16]) as an I_2O device with programming interface 01h
- Sets the *I2O Decode Enable* bit (**QSR**[0]=1)
- Sets the *Local Init Status* bit to "done" (**LMISC1**[2]=1)
- Disables all Direct Slave prefetch mechanisms (**LBRD0**[8] for Space 0, **LBRD1**[9] for Space 1, and/or **LBRD0**[9] for Expansion ROM)

Note: *The Local Bus serial EEPROM must **not** set the Local Init Status bit for the PEX 8311 to issue internal Retrys to all PCI Express Configuration Space accesses on the Local Bus until the Local Init Status bit is set to "done" by the Local processor.*

Enabling I_2O Decode causes the remapping of resources for use in I_2O mode (**QSR**[0]=1). When set, all **Memory-Mapped Configuration** registers and Space 1 share the **LCS PCIBAR0** register. The PCI Express Type 1 (Type 1 is internally converted to Type 0) Configuration accesses to **LCS PCIBAR0** offset 00h to FFh result in accesses to the internal **LCS** registers (**Local**, **Runtime**, **DMA**, and **Messaging Queue**).

Accesses above **LCS PCIBAR0** offset FFh result in Local Space accesses, beginning at offset 100h from the internal *Remap PCI Address to Local Address Space 1* into the *Remap PCIBAR3 Base Address to Local Address Space 1 Base Address* bits (**LAS1BA**[31:4]). Therefore, space located at offset 00h to FFh from **LAS1BA** is not addressable from the PCI Express interface using **PCIBAR0**.

Note: *Because PCI Express accesses to **PCIBAR0** offset 00h to FFh result in internal Configuration accesses, the Inbound Free MFA must be greater than FFh.*

Table 15-2. Circular FIFO Summary

FIFO Name	PCI Port	Generate PCI Express Message Interrupt	Generate Local Interrupt	Head Pointer Maintained By	Tail Pointer Maintained By
Inbound Free List FIFO	Inbound Queue Port (PCI Express Root Complex Read Request)	No	No	Local processor	PEX 8311 hardware
Inbound Post List FIFO	Inbound Queue Port (PCI Express Root Complex Write Request)	No	Yes, when Port is written	PEX 8311 hardware	Local processor
Outbound Post List FIFO	Outbound Queue Port (PCI Express Root Complex Read Request)	Yes, when FIFO is not empty	No	Local processor	PEX 8311 hardware
Outbound Free List FIFO	Outbound Queue Port (PCI Express Root Complex Write Request)	No	Yes, (LINTo#/LSERR#) when FIFO is full	PEX 8311 hardware	Local processor

Chapter 16 Vital Product Data (VPD)

16.1 Overview

VPD provides optional bits that are used to identify and track a device. These bits are set to make each device unique. In the original *PCI specification*, Device ID, Vendor ID, Revision ID, Class Code ID, and Subsystem Vendor ID were required in the Configuration Space Header and for basic device identification and configuration. Although this information allows a device to be configured, it is not sufficient to allow each device unique identification. The VPD optional information capability enables new support tools and reduces the cost of computer ownership.

In the *PCI r2.2*, the VPD function defines a storage device and access method for VPD, as well as defining the Read-Only and Read/Write bits. The PEX 8311 stores VPD in a **LCS** serial EEPROM. Access to VPD is through the New Capabilities function of the **LCS PCI Configuration** registers.

16.2 Local Configuration Space VPD Capabilities Registers

The following sections describe the **LCS VPD Capabilities** registers. As delineated in Table 16-1, they include the **VPD Control** and **Data** registers. PCI Express accesses to the **VPD** registers must be Type 1 accesses (which are internally converted to Type 0) to **LCS PCI Extended Capability** registers. Local Bus accesses to the **VPD** registers are accomplished directly by way of Direct Master Memory cycles, with CCS# asserted.

16.2.1 VPD Control Register

The **VPD Control** register is 32 bits wide and is documented as three smaller registers – **VPD ID**, **Next_Cap Pointer**, and **VPD Address** (refer to Table 16-1 and Register 19-33 through Register 19-35):

- **VPD ID** (**PVPDID**[7:0]; PCI:4Ch, LOC:18Ch). PCI-SIG assigned a value of 03h. The VPD ID is hardwired.
- **Next_Cap Pointer** (**PVPD_NEXT**[7:0]; PCI:4Dh, LOC:18Dh).Point to the next New Capability structure. The PEX 8311 defaults to 0h. Because VPD is the last feature of the New Capability structure, this field is cleared to 0h. Bits [1:0] are ***reserved*** by *PCI r2.2*, and are cleared to 00b.
- **VPD Address** (**PVPDAD**[14:0]; PCI:4Eh, LOC:18Eh). Specify the VPD byte address to access. All accesses are 32 bits wide. For VPD writes, the byte address must be Dword-aligned (PVPDAD[1:0]=00b). For VPD reads, the byte address must be word-aligned (**PVPDAD**[0]=0). Bits [14:9] are ignored.
- (**PVPDAD**[15]; PCI:4Eh, LOC:18Eh). The **VPD Address** register *F* bit controls the direction of the next VPD cycle and indicates when the VPD cycle is complete. For Write cycles, the 4 bytes of data are first written into the *VPD Data* bits, after which the VPD Address is written at the same time the *F* bit is set to 1. The *F* bit is cleared when the serial EEPROM Data transfer completes. For Read cycles, the VPD Address is written at the same time the *F* bit is cleared to 0. The *F* bit is set when 4 bytes of data are read from the serial EEPROM.

16.2.2 VPD Data Register

The **VPD Data** register is 32 bits wide and is documented as a single 32-bit register. (Refer to Table 16-1.)

VPD Data (**PVPDATA**[31:0]; PCI:50h, LOC:190h). The **PVPDATA** register is used to read/write data to/from the VPD serial EEPROM. It is not, however, a pure read/write register. The data read from this register is the data read during the last VPD Read operation. The data written to this register is the data written to the serial EEPROM during a VPD Write operation. The register's words are stored in the serial EEPROM, in Big Endian order, beginning at the serial EEPROM word address specified by the *VPD Address* bits (**PVPDAD**[8:1]). Four bytes are always transferred between the register and serial EEPROM.

Table 16-1. VPD Data Register Documentation

Register Bit Range	31	30 16	15 8	7 0
VPD Control Register	F (**PVPDAD**[15])	VPD Address (**PVPDAD**[14:0])	Next_Cap Pointer (0h) (**PVPD_NEXT**[7:0])	VPD ID (03h) (**PVPDID**[7:0])
VPD Data Register	VPD Data (**PVPDATA**[31:0])			

16.3 VPD Serial EEPROM Partitioning

To support VPD, the serial EEPROM is partitioned into Read-Only and Read/Write portions. The boundary between Read-Only and Read/Write is set with the Serial EEPROM Location Starting at Dword Boundary for *VPD Accesses* bits (**PROT_AREA**[6:0]).

16.4 Sequential Read-Only

The first 1,536 bits, 192 bytes of the serial EEPROM contain Read-Only information. After power-on, the Read-Only portion of the serial EEPROM is loaded into the PEX 8311, using the serial EEPROM's Sequential Read protocol. Sequential words are read by holding EECS asserted, following the issuance of a serial EEPROM Read command.

16.5 Random Read and Write

The PEX 8311 can read and write the Read/Write portion of serial EEPROM, using the VPD function. It can also read the Read-Only portion of the serial EEPROM. The writable portion of the serial EEPROM starts at the Dword specified by **PROT_AREA**[6:0] and continues to the top of the serial EEPROM. The *Serial EEPROM Location Starting at Dword Boundary for VPD Accesses* bits (**PROT_AREA**[6:0]) designate this portion. This register is loaded at power-on and can be written with the necessary value, starting at Location 0. This provides the capability of writing the entire serial EEPROM. Writes to serial EEPROM are comprised of the following three commands:

- Write Enable
- Write Data, followed by Write Data (two 16-bit writes)
- Write Disable

This is performed to ensure against accidental writes to the serial EEPROM. Random cycles allow VPD information to be written and read at any time.

To perform a VPD write to the serial EEPROM, the following steps are necessary:

1. Disable EEDO input (**CNTRL**[31]=0, default).
2. Change the write-protected serial EEPROM address in **PROT_AREA**[6:0] to the necessary Dword location. Value of 0h makes the entire serial EEPROM writable.
3. Write necessary data into the **PVPDATA** register.
4. Write the serial EEPROM destination address in the **PVPDAD** register, and the *F* bit to 1 (**PVPDAD**[15]=1). **PVPDAD**[1:0] must be 00b (address is Dword-aligned).
5. Poll the *F* bit until it changes to 0 (**PVPDAD**[15]=0), to ensure that the write completes.

To perform a VPD read from serial EEPROM, the following steps are necessary:

1. Disable EEDO input (**CNTRL**[31]=0, default).
2. Write the serial EEPROM destination address in the **PVPDAD** register, and 0 to the *F* bit (**PVPDAD**[15]=0). **PVPDAD**[0] must be 0 (address is word-aligned).
3. Poll the *F* bit until it changes to 1 (**PVPDAD**[15]=1), to ensure that the Read data is available.
4. Read back the **PVPDATA** register, to obtain the requested data.

Chapter 17 General-Purpose I/Os

17.1 Overview

The PEX 8311 supports one GPI, one GPO, and four GPIO signals.

17.2 USERi and USERo Signals

The PEX 8311 supports user input and output balls, USERi and USERo. Both are multiplexed with other signals. By default, the PEX 8311 configures these balls as USERi and USERo:

- USERi is selected when **LCS** register **CNTRL**[18]=1. User Input data is read from the *General-Purpose Input* bit (**CNTRL**[17]).
- USERo is selected when **CNTRL**[19]=1. User Output data is logged by writing to the *General-Purpose Output* bit (**CNTRL**[16]).

During a software reset, USERo is driven low. USERo behavior is as follows:

- During a hard reset (PERST#=0), USERo is three-stated. On the second rising edge of LCLK after PERST# is de-asserted, LRESET# de-asserts. On the next falling edge of LCLK, USERo is driven to 0 (from three-state). On the next rising edge of LCLK, USERo is driven to the value specified in CNTRL[16] (default value = 1).
- When the *Local Bus Reset* bit is set (**CNTRL**[30]=1), the LRESET# and USERo signals are asserted low (0). When the *Local Bus Reset* bit is cleared (CNTRL[30]=0), USERo reverts to the value specified in CNTRL[16], one LCLK after the LRESET# signal is de-asserted (driven to 1).

17.3 GPIO Signals

The PEX 8311 provides four GPIO balls (GPIO[3:0]) that can be independently programmed as Inputs or Outputs at any given time. Control of these GPIO balls is located in the **PECS GPIOCTL** and **GPIOSTAT** registers.

Chapter 18 PCI Express Configuration Registers

18.1 Introduction

This chapter describes the PCI Express Configuration Space (**PECS**) register set. Local Configuration Space (**LCS**) registers are described in Chapter 19, "Local Configuration Space Registers."

18.2 Register Description

The **PCI-Compatible Configuration** registers are accessed by the PCI Express Root Complex (Endpoint mode) or Local host (Root Complex mode), using the PCI Configuration Address space. **PECS** registers are accessed from the PCI Express interface or Local Bus, using the 64-KB Memory space defined by the **PECS PCI Base Address 0** register. Registers that are written by the PCI Express interface Serial EEPROM Controller are also written using Memory Writes through the **PECS PCI Base Address 0** register.

In Root Complex mode, a Local Bus Master cannot access the **PCI Express Extended Capability** registers by way of PCI Configuration transactions.

When the **Configuration** registers are accessed using Memory transactions to the **PECS Base Address 0** register, the address mapping delineated in Table 18-1 is used.

The PCI Express interface Serial EEPROM Controller can write to any of the Configuration registers. An upper Address bit is used to select one of the two register spaces delineated in Table 18-2.

Each register is 32 bits wide, and accessed one byte, word, or DWORD at a time. These registers utilize Little Endian Byte Ordering, which is consistent with the *PCI r3.0*. The least significant byte in a DWORD is accessed at Address 0. The least significant bit in a DWORD is 0, and the most significant bit is 31.

After the PEX 8311 is powered up or reset, the registers are set to their default values. Writes to unused registers are ignored, and reads from unused registers return a value of 0.

Table 18-1. PCI Base Address 0 Register Address Mapping

Address Offset	Register Space
0000h - 0FFFh	PCI-Compatible Configuration registers
1000h - 1FFFh	Main Configuration registers
2000h - 2FFFh	Memory-Mapped indirect access to downstream PCI Express Endpoint registers (Root Complex mode only)
8000h - 9FFFh	8-KB internal shared memory

Table 18-2. Selecting Register Space

Internal AD12	Register Space
0	PCI-Compatible Configuration registers
1	Main Configuration registers

18.2.1 Indexed Addressing

In addition to Memory-Mapped accesses, the PEX 8311 **Main Configuration** registers are accessed using the **Main Control Register Index** and **Main Control Register Data** registers. This method allows Main Configuration registers to be accessed using Configuration transactions, rather than Memory transactions. First, the **Main Configuration** register offset is written to the **Main Control Register Index** register (offset 84h). Then, the **Main Configuration** register is written or read by accessing the **Main Control Register Data** register (offset 88h).

18.3 PCI Express Configuration Space Configuration Access Types

Table 18-3 delineates the Configuration access types referenced by the registers in this chapter.

Table 18-3. Configuration Access Types

Access Type	Description
CFG	Initiated by PCI Configuration transactions (Type 0 accesses) on the primary interface.
MM	Initiated by PCI Memory transactions on either the primary or secondary interface, using the Address range defined by the **PCI Base Address 0** register.
EE	Initiated by the Serial EEPROM Controller during initialization.

Note: *The primary interface is the PCI Express interface in Endpoint mode, and the Local Bus interface in Root Complex mode.*

The secondary interface is the Local Bus interface in Endpoint mode, and the PCI Express interface in Root Complex mode.

18.4 PCI Express Configuration Space Register Attributes

Table 18-4 delineates the register attributes used to indicate access types provided by each register bit.

Table 18-4. Access Provided by Register Bits

Register Attribute	Description
HwInit	**Hardware Initialized** Hardware initialized register or register bit. The register bits are initialized by a PEX 8311 hardware initialization mechanism or PEX 8311 Serial EEPROM register initialization feature. Register bits are Read-Only after initialization and can only be reset with "Fundamental Reset."
RO	**Read-Only Register** Register bits are Read-Only and cannot be altered by software. Register bits are initialized by a PEX 8311 hardware initialization mechanism or PEX 8311 Serial EEPROM register initialization feature.
RsvdP	***Reserved* and Preserved** ***Reserved*** for future RW implementations. Registers are Read-Only and must return 0 when read. Software must preserve value read for writes to bits.
RsvdZ	***Reserved* and Zero** ***Reserved*** for future RW1C implementations. Registers are Read-Only and must return 0 when read. Software must use 0 for writes to bits.
RW	**Read-Write Register** Register bits are Read-Write and are set or cleared by software to the needed state.
RW1C	**Read-Only Status, Write 1 to Clear Status Register** Register bits indicate status when read; a set bit indicating a status event is cleared by writing 1. Writing 0 to RW1C bits has no effect.
WO	**Write-Only** Used to indicate that a register is written by the Serial EEPROM Controller.

18.5 PCI Express Configuration Space Register Summary

Table 18-5. Register Summary

Register Group	PCI Space	Address Range
PCI Express Configuration Space PCI-Compatible Configuration Registers (Type 1)	PCI Express Configuration (Endpoint mode); PCI Configuration (Root Complex mode)	000h - 0FFh
	Memory-Mapped, BAR0	000h - 0FFh
PCI-Compatible Extended Capability Registers	PCI Express Configuration (Endpoint mode)	100h - 1FFh
	Memory-Mapped, BAR0	100h - 1FFh
Main Control Registers	Memory-Mapped, BAR0; Indexed, by way of the MAINDEX/MAINDATA registers (offsets 84h and 88h, respectively)	1000h - 10FFh
PCI Express Configuration Registers using Enhanced Configuration Access	Memory-Mapped, BAR0	2000h - 2FFFh
8-KB General Purpose Memory	Memory-Mapped, BAR0	8000h - 9FFFh

18.6 PCI Express Configuration Space Register Mapping

18.6.1 PCI Express Configuration Space PCI-Compatible Configuration Registers (Type 1)

Table 18-6. PCI-Compatible Configuration Registers (Type 1)

PCI Configuration Register Address	31 24	23 16	15 8	7 0
00h	PCI Device ID		PCI Vendor ID	
04h	PCI Status		PCI Command	
08h	PCI Class Code			PCI Device Revision ID
0Ch	PCI Built-In Self-Test ***(Not Supported)***	PCI Header Type	Internal PCI Bus Latency Timer	PCI Cache Line Size
10h	PCI Base Address 0			
14h	PCI Base Address 1			
18h	Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number
1Ch	Secondary Status		I/O Limit	I/O Base
20h	Memory Limit		Memory Base	
24h	Prefetchable Memory Limit		Prefetchable Memory Base	
28h	Prefetchable Memory Base Upper 32 Bits			
2Ch	Prefetchable Memory Limit Upper 32 Bits			
30h	I/O Limit Upper 16 Bits		I/O Base Upper 16 Bits	
34h	***Reserved***			PCI Capabilities Pointer
38h	PCI Base Address for Expansion ROM (***Not Supported***)			
3Ch	Bridge Control		Internal PCI Interrupt Wire	Internal PCI Interrupt Line

18.6.2 PCI Express Configuration Space PCI-Compatible Capability Registers

Table 18-7. PCI Express Interface PCI-Compatible Capability Registers

PCI Configuration Register Address	31 24	23 16	15 8	7 0
40h	Power Management Capabilities		Power Management Next Capability Pointer	Power Management Capability ID
44h	Power Management Data	Power Management Bridge Support	Power Management Control/Status	
48h	Device-Specific Control			
4Ch	***Reserved***			
50h	Message Signaled Interrupts Control		Message Signaled Interrupts Next Capability Pointer	Message Signaled Interrupts Capability ID
54h	Message Signaled Interrupts Address			
58h	Message Signaled Interrupts Upper Address			
5Ch	***Reserved***		Message Signaled Interrupts Data	
60h	PCI Express Capabilities		PCI Express Next Capability Pointer	PCI Express Capability ID
64h	Device Capabilities			
68h	PCI Express Device Status		PCI Express Device Control	
6Ch	Link Capabilities			
70h	Link Status		Link Control	
74h	Slot Capabilities			
78h	Slot Status		Slot Control	
7Ch	***Reserved***		Root Control	
80h	Root Status			
84h	Main Control Register Index			
88h	Main Control Register Data			

18.6.3 PCI Express Configuration Space PCI Express Extended Capability Registers

Table 18-8. Power Budgeting Capability and Device Serial Number Registers

PCI Express Configuration Register Offset	3120	1916	158	70
100h	Power Budgeting Next Capability Offset	Power Budgeting Capability Version	Power Budgeting PCI Express Extended Capability ID	
104h	***Reserved***			Power Budgeting Data Select
108h	Power Budgeting Data			
10Ch	***Reserved***			Power Budget Capability
110h	Serial Number Next Capability Offset	Serial Number Capability Version	Serial Number PCI Express Extended Capability ID	
114h	Serial Number Low (Lower DWORD)			
118h	Serial Number Low (Upper DWORD)			

18.6.4 PCI Express Configuration Space Main Control Registers

Table 18-9. Main Control Registers

PCI Express Configuration Register Address	31 0	Page
1000h	Device Initialization	337
1004h	Serial EEPROM Control	338
1008h	Serial EEPROM Clock Frequency	339
100Ch	PCI Control	339
1010h	PCI Express Interrupt Request Enable	341
1014h	PCI Interrupt Request Enable	342
1018h	Interrupt Request Status	343
101Ch	Power (Endpoint Mode Only)	343
1020h	General-Purpose I/O Control	344
1024h	General-Purpose I/O Status	346
1030h	Mailbox 0	347
1034h	Mailbox 1	347
1038h	Mailbox 2	347
103Ch	Mailbox 3	347
1040h	Chip Silicon Revision	348
1044h	Diagnostic Control (Factory Test Only)	348
1048h	TLP Controller Configuration 0	348
104Ch	TLP Controller Configuration 1	350
1050h	TLP Controller Configuration 2	350
1054h	TLP Controller Tag	350
1058h	TLP Controller Time Limit 0	351
105Ch	TLP Controller Time Limit 1	351
1060h	CRS Timer	351
1064h	Enhanced Configuration Address	352

18.7 PCI Express Configuration Space PCI-Compatible Configuration Registers (Type 1)

Register 18-1. (Offset 00h; PCIVENDID) PCI Vendor ID

Bits	Description	CFG	MM	EE	Default
15:0	**PCI Vendor ID** Identifies the device manufacturer. Hardwired to the PLX PCI-SIG-issued Vendor ID, 10B5h.	RO	RW	WO	10B5h

Register 18-2. (Offset 02h; PCIDEVID) PCI Device ID

Bits	Description	CFG	MM	EE	Default
15:0	**PCI Device ID** Identifies the particular device. Defaults to 8111h when the serial EEPROM is blank, or no serial EEPROM is present.	RO	RW	WO	8111h

Register 18-3. (Offset 04h; PCICMD) PCI Command (Endpoint Mode)

Bits	Description	CFG	MM	EE	Default
0	**I/O Access Enable** Enables the PEX 8311 to respond to I/O Space accesses on the PCI Express interface. These accesses must be directed to a target on the Local Bus, because the PEX 8311 does not maintain internal I/O-Mapped resources.	RW	RW	WO	0
1	**Memory Space Enable** Enables the PEX 8311 to respond to Memory Space accesses on the PCI Express interface. These accesses are directed to a target on the Local Bus, or to internal Memory-Mapped registers. When cleared, responds to Memory requests on the PCI Express interface with an Unsupported Request completion.	RW	RW	WO	0
2	**Bus Master Enable** Enables the PEX 8311 to issue Memory and I/O Read/Write requests on the PCI Express interface. Requests other than Memory or I/O requests are not controlled by this bit. When cleared, the bridge must disable response as a target to Memory or I/O transactions on the Local Bus interface (they cannot be forwarded to the PCI Express interface).	RW	RW	WO	0
3	**Special Cycle Enable** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	0

Register 18-3. (Offset 04h; PCICMD) PCI Command (Endpoint Mode) *(Cont.)*

Bits	Description	CFG	MM	EE	Default
4	**Memory Write and Invalidate** When set, enables the PEX 8311 internal PCI Bus master logic to use the Memory Write and Invalidate command. When cleared, the Memory Write command is used instead.	RW	RW	WO	0
5	**VGA Palette Snoop** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	0
6	**Parity Error Response Enable** Controls the response to Data Parity errors forwarded from the PCI Express interface (*such as*, a poisoned TLP). When cleared, the bridge must ignore (but records status, *such as* setting the **PCI Status** register *Detected Parity Error* bit) Data Parity errors detected and continue normal operation. When set, the bridge must take its normal action when a Data Parity error is detected.	RW	RW	WO	0
7	**Address Stepping Enable** The PEX 8311 performs Address Stepping for PCI Configuration cycles; therefore, this bit is read/write with an initial value of 1.	RW	RW	WO	1
8	**Internal SERR# Enable** Enables reporting of Fatal and Non-Fatal errors to the Root Complex. ***Note:*** *Errors are reported when enabled through this bit or through the **PCI Express Device Control** register PCI-Express-specific bits.*	RW	RW	WO	0
9	**Fast Back-to-Back Enable** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	0
10	**Interrupt Disable** When set: • PEX 8311 is prevented from generating INTA# interrupt messages on behalf of functions integrated into the bridge • INTA# emulation interrupts previously asserted must be de-asserted There is no effect on INTA# messages generated on behalf of INTA# inputs associated with the Local Bus interface.	RW	RW	WO	0
15:11	***Reserved***	RsvdP	RsvdP	–	0h

Register 18-4. (Offset 04h; PCICMD) PCI Command (Root Complex Mode)

Bits	Description	CFG	MM	EE	Default
0	**I/O Access Enable** Enables the PEX 8311 to respond to I/O Space accesses on the Local Bus interface. These accesses are directed to a target on the PCI Express interface, because the PEX 8311 does not have internal I/O-Mapped devices. When cleared, PCI I/O accesses to the PEX 8311 result in a Master Abort.	RW	RW	WO	0
1	**Memory Space Enable** Enables the PEX 8311 to respond to Memory Space accesses on the Local Bus interface. These accesses are directed to a target on the PCI Express interface, or to internal Memory-Mapped registers. When cleared, PCI Memory accesses to the PEX 8311 result in a Master Abort.	RW	RW	WO	0
2	**Bus Master Enable** When set, enables the PEX 8311 to perform Memory or I/O transactions on the internal PCI Bus. Configuration transactions are forwarded from the PCI Express interface and performed on the internal PCI Bus independent of this bit. When cleared, the bridge must disable response as a target to Memory or I/O transactions on the PCI Express interface (they cannot be forwarded to the Local Bus interface). In this case, Memory and I/O requests are terminated with an Unsupported Request completion.	RW	RW	WO	0
3	**Special Cycle Enable** A bridge does not respond to special cycle transactions; therefore, forced to 0.	RO	RO	–	0
4	**Memory Write and Invalidate** When set, enables the PEX 8311 internal PCI Bus master logic to use the Memory Write and Invalidate command. When cleared, the Memory Write command is used instead.	RW	RW	WO	0
5	**VGA Palette Snoop** When set, I/O Writes in the first 64 KB of the I/O Address space with Address bits [9:0] equal to 3C6h, 3C8h, and 3C9h (inclusive of ISA aliases – AD[15:10] are not decoded and can be any value) must be positively decoded on the PCI interface and forwarded to the PCI Express interface.	RW	RW	WO	0
6	**Parity Error Response Enable** Enables PCI parity checking.	RW	RW	WO	0
7	***Reserved***	RsvdP	RsvdP	–	0
8	**Internal SERR# Enable** When set, enables the internal SERR# signal to assert.	RW	RW	WO	0
9	**Fast Back-to-Back Enable** ***Not supported.*** The PEX 8311 PCI master interface does not perform Fast Back-to-Back transactions; therefore, forced to 0.	RO	RO	–	0
10	**Interrupt Disable** When set, the PEX 8311 is prevented from asserting INTA# signals on behalf of functions integrated into the bridge. There is no effect on INTA# signals asserted on behalf of INTA# messages associated with the PCI Express interface.	RW	RW	WO	0
15:11	***Reserved***	RsvdP	RsvdP	–	0h

Register 18-5. (Offset 06h; PCISTAT) PCI Status (Endpoint Mode)

Bits	Description	CFG	MM	EE	Default
2:0	***Reserved***	RsvdZ	RsvdZ	–	000b
3	**Interrupt Status** When set, indicates that an INTA# interrupt message is pending on behalf of functions integrated into the bridge. Does not reflect the status of INTA# inputs associated with the Local Bus interface.	RO	RO	–	0
4	**Capabilities List** Indicates whether the **New Capabilities Pointer** at offset 34h is valid. Because PCI Express devices are required to implement the PCI Express capability structure, this bit is hardwired to 1.	RO	RO	–	1
5	**66-MHz Capable (Internal Clock Frequency)** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	0
6	***Reserved***	RsvdZ	RsvdZ	–	0
7	**Fast Back-to-Back Transactions Capable** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	0
8	**Master Data Parity Error** Used to report Data Parity error detection by the bridge. Set when the **PCI Command** register *Parity Error Response Enable* bit is set and either of the following two conditions occur: • Bridge receives a completion marked *poisoned* on PCI Express interface • Bridge poisons a Write request or Read Completion on PCI Express interface Writing 1 clears this bit.	RW1C	RW1C	–	0
10:9	**DEVSEL Timing** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	00b
11	**Signaled Target Abort** Set when the bridge completes a request as a transaction target on the PCI Express interface using Completer Abort completion status. Writing 1 clears this bit.	RW1C	RW1C	–	0
12	**Received Target Abort** Set when the bridge receives a completion with Completer Abort completion status on the PCI Express interface. Writing 1 clears this bit.	RW1C	RW1C	–	0
13	**Received Master Abort** Set when the bridge receives a completion with Unsupported Request completion status on the PCI Express interface. Writing 1 clears this bit.	RW1C	RW1C	–	0
14	**Signaled System Error** Set when the bridge transmits an ERR_FATAL or ERR_NONFATAL message to the Root Complex, and the **PCI Command** register *Internal SERR# Enable* bit is set. Writing 1 clears this bit.	RW1C	RW1C	–	0
15	**Detected Parity Error** Set by the bridge when it receives a poisoned TLP on the PCI Express interface, regardless of the **PCI Command** register *Parity Error Response Enable* bit state. Writing 1 clears this bit.	RW1C	RW1C	–	0

Register 18-6. (Offset 06h; PCISTAT) PCI Status (Root Complex Mode)

Bits	Description	CFG	MM	EE	Default
2:0	***Reserved***	RsvdZ	RsvdZ	–	000b
3	**Interrupt Status** Reflects the state of the PEX 8311 internal PCI interrupt status. INTA# is asserted when this bit is high, the **PCI Command** register *Interrupt Disable* bit is low, and the Power State is D0.	RO	RO	–	0
4	**Capabilities List** Indicates whether the **New Capabilities Pointer** at offset 34h is valid.	RO	RO	–	1
5	**66-MHz Capable (Internal Clock Frequency)** This optional Read-Only bit indicates whether the PEX 8311 is capable of running at 66 MHz. A value of 0 indicates 33 MHz. A value of 1 indicates that the PEX 8311 is 66-MHz capable.	RO	RW	WO	1
6	***Reserved***	RsvdZ	RsvdZ	–	0
7	**Fast Back-to-Back Transactions Capable** ***Not supported.*** The PEX 8311 does not accept Fast Back-to-Back transactions; therefore, forced to 0.	RO	RO	–	0
8	**Master Data Parity Error** Indicates that a Data Parity error occurred when the PEX 8311 was the internal PCI Bus Master. The **PCI Command** register *Parity Error Response Enable* bit must be set for this bit to set. Writing 1 clears this bit.	RW1C	RW1C	–	0
10:9	**DEVSEL Timing** Determines how quickly the PEX 8311 PCI Express bridge responds to a Direct Master transaction on its internal PCI Bus. A value of 01b indicates a medium response.	RO	RO	–	01b
11	**Signaled Target Abort** Set when the PEX 8311 is acting as an internal PCI Bus Target, and terminates its transaction with a Target Abort. A Target Abort occurs when a target detects a Fatal error and is unable to complete the transaction. This never occurs in the PEX 8311; therefore, 0 is always returned.	RsvdZ	RsvdZ	–	0
12	**Received Target Abort** Set when the PEX 8311 is acting as an internal PCI Bus Master, with its transaction terminated with a Target Abort. A Target Abort occurs when a target detects a Fatal error and is unable to complete the transaction. Writing 1 clears this bit.	RW1C	RW1C	–	0
13	**Received Master Abort** Set when the PEX 8311 is acting as an internal PCI Bus Master, with its transaction terminated with a Master Abort. A Master Abort occurs when there is an invalid address on the internal PCI Bus. Writing 1 clears this bit.	RW1C	RW1C	–	0
14	**Signaled System Error** Set when the PEX 8311 asserts the internal SERR# signal. Writing 1 clears this bit.	RW1C	RW1C	–	0
15	**Detected Parity Error** Set when the PEX 8311 detects a Parity error on incoming addresses or data from the internal PCI Bus, regardless of the **PCI Command** register *Parity Error Response Enable* bit state. Writing 1 clears this bit.	RW1C	RW1C	–	0

Register 18-7. (Offset 08h; PCIDEVREV) PCI Device Revision ID

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Express Block Device Revision ID** Identifies the PCI Express block of PEX 8311 silicon revision. Bits [3:0] represent the minor revision number and bits [7:4] represent the major revision number.	RO	RO	–	21h

Register 18-8. (Offset 09h; PCICLASS) PCI Class Code

Bits	Description	CFG	MM	EE	Default
7:0	**Programming Interface**	RO	RW	WO	00h
15:8	**Subclass Code**	RO	RW	WO	04h
23:16	**Base Class Code**	RO	RW	WO	06h

Register 18-9. (Offset 0Ch; PCICACHESIZE) PCI Cache Line Size

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Cache Line Size** Specifies the System Cache Line Size (in units of DWords). The value in this register is used by PCI master devices to determine whether to use Read, Memory Read Line, Memory Read Multiple or Memory Write Invalidate commands to access memory. The PEX 8311 supports Cache Line Sizes of only 2, 4, 8, 16, or 32 DWORDs. Writes of values other than these result in a cache line size of 0; however, the value written is nonetheless returned when this register is read.	RW	RW	WO	0h

Register 18-10. (Offset 0Dh; PCILATENCY) Internal PCI Bus Latency Timer

Bits	Description	CFG	MM	EE	Default
7:0	**Internal PCI Bus Latency Timer** Also referred to as the Primary Latency Timer for Type 1 Configuration Space Header devices. The Primary/Master Latency Timer does not apply to PCI Express (Endpoint mode). In Root Complex mode, specifies (in units of internal clocks) the value of the Latency Timer during Bus Master bursts. When the Latency Timer expires, the PEX 8311 must terminate its tenure on the bus.	RO (E) RW (RC)	RO (E) RW (RC)	– (E) WO (RC)	0h

Note: *In the **CFG**, **MM**, and **EE** columns, "E" indicates Endpoint mode, and "RC" indicates Root Complex mode.*

Register 18-11. (Offset 0Eh; PCIHEADER) PCI Header Type

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Header Type** Specifies the format of the second part of the pre-defined configuration header starting at offset 10h. For PCI bridges, this field is forced to 1.	RO	RO	–	1h

Register 18-12. (Offset 0Fh; PCIBIST) PCI Built-In Self-Test

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Built-In Self-Test** ***Not supported***. Always returns a value of 0h.	RO	RO	–	0h

Register 18-13. (Offset 10h; PCIBASE0) PCI Base Address 0

Bits	Description	CFG	MM	EE	Default
0	**Space Type** When low, this space is accessed as memory. When high, this space is accessed as I/O. ***Note:*** *Hardwired to 0.*	RO	RO	–	0
2:1	**Address Type** Indicates the type of addressing for this space. 00b = Locate anywhere in 32-bit Address space (default) 01b = Locate below 1 MB 10b = Locate anywhere in 64-bit Address space 11b = ***Reserved***	RO	RW	WO	10b
3	**Prefetch Enable** When set, indicates that prefetching has no side effects on reads.	RO	RW	WO	1
15:4	**Base Address** This section of the Base address is ignored for a 64-KB space. ***Note:*** *Hardwired to 0.*	RO	RO	–	0h
31:16	**Base Address** Specifies the upper 16 bits of the 32-bit starting Base address of the 64-KB Address space for the PEX 8311 Configuration registers and shared memory.	RW	RW	WO	0h

Register 18-14. (Offset 14h; PCIBASE1) PCI Base Address 1

Bits	Description	CFG	MM	EE	Default
31:0	**Base Address 1** Determines the upper 32 bits of the address when **PCIBASE0** is configured for 64-bit addressing.	RW	RW	WO	0h

Register 18-15. (Offset 18h; PRIMBUSNUM) Primary Bus Number

Bits	Description	CFG	MM	EE	Default
7:0	**Primary Bus Number** Used to record the Bus Number of the internal PCI Bus segment to which the bridge primary interface is connected. ***Note:*** *The primary interface is the PCI Express interface in Endpoint mode, and the Local Bus interface in Root Complex mode.*	RW	RW	WO	0h

Register 18-16. (Offset 19h; SECBUSNUM) Secondary Bus Number

Bits	Description	CFG	MM	EE	Default
7:0	**Secondary Bus Number** Used to record the Bus Number of the internal PCI Bus segment to which the bridge secondary interface is connected. ***Note:*** *The secondary interface is the Local Bus interface in Endpoint mode, and the PCI Express interface in Root Complex mode.*	RW	RW	WO	0h

Register 18-17. (Offset 1Ah; SUBBUSNUM) Subordinate Bus Number

Bits	Description	CFG	MM	EE	Default
7:0	**Subordinate Bus Number** Used to record the Bus Number of the highest-numbered internal PCI Bus segment behind (or subordinate to) the bridge. ***Note:*** *In Endpoint mode, the Subordinate Bus Number is always equal to the Secondary Bus Number.*	RW	RW	WO	0h

Register 18-18. (Offset 1Bh; SECLATTIMER) Secondary Latency Timer (Endpoint Mode Only)

Bits	Description	CFG	MM	EE	Default
7:0	**Secondary Latency Timer** Valid only in Endpoint mode. Specifies (in units of internal clocks) the Latency Timer value during secondary internal PCI Bus Master bursts. When the Latency Timer expires, the PEX 8311 must terminate its tenure on the bus.	RW	RW	WO	0h

Register 18-19. (Offset 1Ch; IOBASE) I/O Base

Bits	Description	CFG	MM	EE	Default
3:0	**I/O Base Address Capability** Indicates the type of addressing for this space. 0000b = 16-bit I/O address 0001b = 32-bit I/O address All other values = ***Reserved***	RO	RW	WO	0000b
7:4	**I/O Base** Determines the starting address at which I/O transactions on the primary interface are forwarded to the secondary interface. The upper four bits of this register correspond to Address bits AD[15:12]. For address decoding purposes, the bridge assumes that the lower 12 Address bits, AD[11:0], of the I/O Base address are zero (0h). Therefore, the bottom of the defined I/O Address range is aligned to a 4-KB boundary, and the top is one less than a 4-KB boundary. ***Note:*** *The primary interface is the PCI Express interface in Endpoint mode, and the Local Bus interface in Root Complex mode.* *The secondary interface is Local Bus in Endpoint mode, and PCI Express in Root Complex mode.*	RW	RW	WO	0h

Register 18-20. (Offset 1Dh; IOLIMIT) I/O Limit

Bits	Description	CFG	MM	EE	Default
3:0	**I/O Limit Address Capability** Indicates the type of addressing for this space. 0000b = 16-bit I/O address 0001b = 32-bit I/O address All other values = ***Reserved*** The value returned in this field is derived from the **I/O Base (IOBASE)** register *I/O Base Address Capability* field.	RO	RO	–	0000b
7:4	**I/O Limit** Determines the I/O Space range forwarded from the primary interface to the secondary interface. The upper four bits of this register correspond to Address bits AD[15:12]. For address decoding purposes, the bridge assumes that the lower 12 Address bits, AD[11:0], of the I/O Limit address are FFFh. When there are no I/O addresses on the secondary interface, the I/O Limit field is programmed to a value smaller than the I/O Base field. In this case, the bridge does not forward I/O transactions from the primary interface to the secondary interface; however, it does forward all I/O transactions from the secondary interface to the primary interface. ***Note:*** *The primary interface is PCI Express in Endpoint mode, and Local Bus in Root Complex mode.* *The secondary interface is Local Bus in Endpoint mode, and PCI Express in Root Complex mode.*	RW	RW	WO	0h

Register 18-21. (Offset 1Eh; SECSTAT) Secondary Status (Endpoint Mode)

Bits	Description	CFG	MM	EE	Default
4:0	***Reserved***	RsvdZ	RsvdZ	–	0h
5	**Secondary 66-MHz Capable (Internal Clock Frequency)** Indicates whether the Local Bus interface is capable of operating at 66 MHz.	RO	RO	–	0
6	***Reserved***	RsvdZ	RsvdZ	–	0
7	**Secondary Fast Back-to-Back Transactions Capable** ***Not supported.*** Indicates whether the internal PCI Bus is capable of decoding Fast Back-to-Back transactions. The PEX 8311 does ***not support*** Fast Back-to-Back decoding.	RO	RO	–	0
8	**Secondary Master Data Parity Error** Reports Data Parity error detection by the bridge when it is the master of the transaction on the Local Bus interface. Set when the following three conditions are true: • Bridge is the bus master of the transaction on Local Bus interface • Bridge asserted internal PERR# (Read transaction) or detected internal PERR# asserted (Write transaction) • **Bridge Control** register *Secondary Parity Error Response Enable* bit is set Writing 1 clears this bit.	RW1C	RW1C	–	0
10:9	**Secondary DEVSEL Timing** Encodes the internal PCI Bus DEVSEL# timing. Hardwired to a value of 01b, indicating medium DEVSEL# timing.	RO	RO	–	01b
11	**Secondary Signaled Target Abort** Reports Target Abort termination signaling by the bridge when it responds as the transaction target on the internal PCI Bus. Writing 1 clears this bit.	RW1C	RW1C	–	0
12	**Secondary Received Target Abort** Reports Target Abort termination detection by the bridge when it is the transaction master on the internal PCI Bus. Writing 1 clears this bit.	RW1C	RW1C	–	0
13	**Secondary Received Master Abort** Reports Master Abort termination detection by the bridge when it is the transaction master on the internal PCI Bus. Also set for a PCI Express-to-PCI Configuration transaction with an extended address not equal to 0. Writing 1 clears this bit.	RW1C	RW1C	–	0
14	**Secondary Received System Error** Reports internal SERR# assertion detection on the internal PCI Bus. Writing 1 clears this bit.	RW1C	RW1C	–	0
15	**Secondary Detected Parity Error** Reports Address or Data Parity error detection by the bridge on the internal PCI Bus. Set when any of the following three conditions are true: • Bridge detects an Address Parity error as a potential target • Bridge detects a Data Parity error when Write transaction target • Bridge detects a Data Parity error when Read transaction master Set irrespective of the **Bridge Control** register *Secondary Parity Error Response Enable* bit state. Writing 1 clears this bit.	RW1C	RW1C	–	0

Register 18-22. (Offset 1Eh; SECSTAT) Secondary Status (Root Complex Mode)

Bits	Description	CFG	MM	EE	Default
4:0	***Reserved***	RsvdZ	RsvdZ	–	0h
5	**Secondary 66-MHz Capable (Internal Clock Frequency)** Not valid for PCI Express. Indicates whether the PCI Express interface is capable of operating at 66 MHz. Forced to 0.	RO	RO	–	0
6	***Reserved***	RsvdZ	RsvdZ	–	0
7	**Secondary Fast Back-to-Back Transactions Capable** Not valid for PCI Express. Indicates whether the PCI Express interface is capable of decoding Fast Back-to-Back transactions when the transactions are from the same master, but to different targets. Forced to 0.	RO	RO	–	0
8	**Secondary Master Data Parity Error** Used to report Data Parity error detection by the bridge. Set when the **Bridge Control** register *Secondary Parity Error Response Enable* bit is set and either of the following two conditions occur: • Bridge receives a completion marked *poisoned* on the PCI Express interface • Bridge poisons a Write request or Read Completion on the PCI Express interface Writing 1 clears this bit.	RW1C	RW1C	–	0
10:9	**Secondary DEVSEL Timing** Does not apply to PCI Express; therefore, forced to 00b.	RO	RO	–	00b
11	**Secondary Signaled Target Abort** Set when the bridge completes a request as a transaction target on the PCI Express interface using Completer Abort completion status. Writing 1 clears this bit.	RW1C	RW1C	–	0
12	**Secondary Received Target Abort** Set when the bridge receives a completion with Completer Abort completion status on the PCI Express interface. Writing 1 clears this bit.	RW1C	RW1C	–	0
13	**Secondary Received Master Abort** Set when the bridge receives a completion with Unsupported Request completion status on the PCI Express interface. Writing 1 clears this bit.	RW1C	RW1C	–	0
14	**Secondary Received System Error** Set when the PEX 8311 receives an ERR_FATAL or ERR_NONFATAL message from the downstream PCI Express device. Writing 1 clears this bit.	RW1C	RW1C	–	0
15	**Secondary Detected Parity Error** Set by the bridge when it receives a poisoned TLP on the PCI Express interface, regardless of the **Bridge Control** register *Secondary Parity Error Response Enable* bit state. Writing 1 clears this bit.	RW1C	RW1C	–	0

Register 18-23. (Offset 20h; MEMBASE) Memory Base

Bits	Description	CFG	MM	EE	Default
3:0	***Reserved*** ***Note:*** *Hardwired to 0h.*	RsvdP	RsvdP	–	0h
15:4	**Memory Base** Determines the starting address at which Memory transactions on the primary interface are forwarded to the secondary interface. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the bridge assumes that the lower 20 Address bits, AD[19:0], of the Memory Base address are zero (0h). The bottom of the defined Memory Address range is aligned to a 1-MB boundary, and the top is one less than a 1-MB boundary. ***Note:*** *The primary interface is the PCI Express interface in Endpoint mode, and the Local Bus interface in Root Complex mode.* *The secondary interface is the Local Bus interface in Endpoint mode, and the PCI Express interface in Root Complex mode.*	RW	RW	WO	–

Register 18-24. (Offset 22h; MEMLIMIT) Memory Limit

Bits	Description	CFG	MM	EE	Default
3:0	***Reserved*** ***Note:*** *Hardwired to 0h.*	RsvdP	RsvdP	–	0h
15:4	**Memory Limit** Determines the Memory Space range forwarded from the primary interface to the secondary interface. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the bridge assumes that the lower 20 Address bits, AD[19:0], of the Memory Limit address are FFFFFh. When there are no Memory-Mapped I/O addresses on the secondary interface, the Memory Limit field must be programmed to a value smaller than the Memory Base field. When there is no Prefetchable memory, and no Memory-Mapped I/O on the secondary interface, the bridge does not forward Memory transactions from the primary interface to the secondary interface; however, it does forward all Memory transactions from the secondary interface to the primary interface. ***Note:*** *The primary interface is the PCI Express interface in Endpoint mode, and the Local Bus interface in Root Complex mode.* *The secondary interface is the Local Bus interface in Endpoint mode, and the PCI Express interface in Root Complex mode.*	RW	RW	WO	–

Register 18-25. (Offset 24h; PREBASE) Prefetchable Memory Base

Bits	Description	CFG	MM	EE	Default
3:0	**Prefetchable Base Address Capability** Indicates the type of addressing for this space. 0000b = 32-bit I/O address 0001b = 64-bit I/O address All other values = ***Reserved***	RO	RW	WO	0000b
15:4	**Prefetchable Memory Base** Determines the starting address at which Prefetchable Memory transactions on the primary interface are forwarded to the secondary interface. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the bridge assumes that the lower 20 Address bits, AD[19:0], of the Prefetchable Memory Base address are zero (0h). The bottom of the defined Prefetchable Memory Address range is aligned to a 1-MB boundary, and the top is one less than a 1-MB boundary. ***Note:*** *The primary interface is PCI Express in Endpoint mode, and Local Bus in Root Complex mode.* *The secondary interface is Local Bus in Endpoint mode, and PCI Express in Root Complex mode.*	RW	RW	WO	–

Register 18-26. (Offset 26h; PRELIMIT) Prefetchable Memory Limit

Bits	Description	CFG	MM	EE	Default
3:0	**Prefetchable Limit Address Capability** Indicates the type of addressing for this space. 0000b = 32-bit I/O address 0001b = 64-bit I/O address All other values = ***Reserved*** The value returned in this field is derived from the **PREBASE** register *Prefetchable Base Address Capability* field.	RO	RO	–	0000b
15:4	**Prefetchable Memory Limit** Determines the Prefetchable Memory Space range forwarded from the primary interface to the secondary interface. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the bridge assumes that the lower 20 Address bits, AD[19:0], of the Prefetchable Memory Limit address are FFFFFh. When there is no Prefetchable memory on the secondary interface, the *Prefetchable Memory Limit* field must be programmed to a value smaller than the *Prefetchable Memory Base* field. When there is no Prefetchable memory, and no Memory-Mapped I/O on the secondary interface, the bridge does not forward Memory transactions from the primary interface to the secondary interface; however, it does forward all Memory transactions from the secondary interface to the primary interface. ***Note:*** *The primary interface is PCI Express in Endpoint mode, and Local Bus in Root Complex mode.* *The secondary interface is Local Bus in Endpoint mode, and PCI Express in Root Complex mode.*	RW	RW	WO	–

Register 18-27. (Offset 28h; PREBASEUPPER) Prefetchable Memory Base Upper 32 Bits

Bits	Description	CFG	MM	EE	Default
31:0	**Prefetchable Memory Base Upper 32 Bits** When the *Prefetchable Base Address Capability* field indicates 32-bit addressing, this register is Read-Only and returns 0h. When the *Prefetchable Base Address Capability* field indicates 64-bit addressing, this register determines the upper 32 bits of the starting address at which Prefetchable Memory transactions on the primary interface are forwarded to the secondary interface. ***Note:*** *The primary interface is PCI Express in Endpoint mode, and Local Bus in Root Complex mode.* *The secondary interface is Local Bus in Endpoint mode, and PCI Express in Root Complex mode.*	RW	RW	WO	0h

Register 18-28. (Offset 2Ch; PRELIMITUPPER) Prefetchable Memory Limit Upper 32 Bits

Bits	Description	CFG	MM	EE	Default
31:0	**Prefetchable Memory Limit Upper 32 Bits** When the *Prefetchable Base Address Capability* field indicates 32-bit addressing, this register is Read-Only and returns 0h. When the *Prefetchable Base Address Capability* field indicates 64-bit addressing, this register determines the upper 32 bits of the range at which Prefetchable Memory transactions on the primary interface are forwarded to the secondary interface. ***Notes:*** *Refer to Section 5.4.2, "Prefetchable Base and Limit Registers," for further details.* *The primary interface is PCI Express in Endpoint mode, and Local Bus in Root Complex mode.* *The secondary interface is Local Bus in Endpoint mode, and PCI Express in Root Complex mode.*	RW	RW	WO	0h

Register 18-29. (Offset 30h; IOBASEUPPER) I/O Base Upper 16 Bits

Bits	Description	CFG	MM	EE	Default
15:0	**I/O Base Upper 16 Bits** When the *I/O Base Address Capability* field indicates 16-bit addressing, this register is Read-Only and returns 0. When the *I/O Base Address Capability* field indicates 32-bit addressing, this register determines the upper 16 bits of the starting address at which I/O transactions on the primary interface are forwarded to the secondary interface. ***Note:*** *The primary interface is PCI Express in Endpoint mode, and Local Bus in Root Complex mode.* *The secondary interface is Local Bus in Endpoint mode, and PCI Express in Root Complex mode.*	RW	RW	WO	–

Register 18-30. (Offset 32h; IOLIMITUPPER) I/O Limit Upper 16 Bits

Bits	Description	CFG	MM	EE	Default
15:0	**I/O Limit Upper 16 Bits** When the *I/O Base Address Capability* field indicates 16-bit addressing, this register is Read-Only and returns 0. When the *I/O Base Address Capability* field indicates 32-bit addressing, this register determines the upper 16 bits of the range at which I/O transactions on the primary interface are forwarded to the secondary interface. ***Notes:*** *Refer to Section 5.2, "I/O Space," for further details.* *The primary interface is PCI Express in Endpoint mode, and Local Bus in Root Complex mode.* *The secondary interface is Local Bus in Endpoint mode, and PCI Express in Root Complex mode.*	RW	RW	WO	–

Register 18-31. (Offset 34h; PCICAPPTR) PCI Capabilities Pointer

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Capabilities Pointer** Provides the offset location of the first New Capabilities register.	RO	RW	WO	40h
31:8	***Reserved***	RsvdP	RsvdP	–	0h

Register 18-32. (Offset 3Ch; PCIINTLINE) Internal PCI Interrupt Line

Bits	Description	CFG	MM	EE	Default
7:0	**Internal PCI Interrupt Line** Indicates to which system interrupt controller input the device Interrupt pin is connected. Device drivers and operating systems use this field.	RW	RW	WO	0h

Register 18-33. (Offset 3Dh; PCIINTPIN) Internal PCI Wire Interrupt

Bits	Description	CFG	MM	EE	Default
7:0	**Internal PCI Wire Interrupt** For Endpoint mode, this register identifies the legacy interrupt message(s) that the PEX 8311 uses. The only valid value is 1h, which maps to legacy interrupt messages for INTA#. Value of 0 indicates that the PEX 8311 does not use legacy interrupt messages. For Root Complex mode, this register selects the internal PCI INTA# wire interrupt.	RO	RW	WO	1h

Register 18-34. (Offset 3Eh; BRIDGECTL) Bridge Control (Endpoint Mode)

Bits	Description	CFG	MM	EE	Default
0	**Secondary Parity Error Response Enable** Controls the bridge response to Address and Data Parity errors on the Local Bus interface. When cleared, the bridge must ignore Parity errors detected and continue normal operation. A bridge must generate parity, regardless of whether Parity error reporting is disabled. Also, the bridge must always forward Posted Write data with poisoning, from Local-to-PCI Express on a PCI Data Parity error, regardless of this bit's setting. When set, the bridge must take its normal action when a Parity error is detected.	RW	RW	WO	0
1	**Secondary Internal SERR# Enable** Controls forwarding of Local Bus interface internal SERR# assertions to the PCI Express interface. The bridge transmits an ERR_FATAL message on the PCI Express interface when all the following are true: • Internal SERR# is asserted on the Local Bus interface • This bit is set • **PCI Command** register *Internal SERR# Enable* bit is set or **PCI Express Device Control** register *Fatal or Non-Fatal Error Reporting Enable* bits are set	RW	RW	WO	0
2	**ISA Enable** Modifies the bridge response to ISA I/O addresses that are enabled by the **I/O Base** and **I/O Limit** registers and located in the first 64 KB of the PCI I/O Address space. When set, the bridge blocks forwarding of I/O transactions, from the PCI Express interface to the Local Bus interface, that address the last 768 bytes in each 1-KB block. In the opposite direction (Local Bus interface to the PCI Express interface), I/O transactions are forwarded when they address the last 768 bytes in each 1-KB block.	RW	RW	WO	0
3	**VGA Enable** Modifies the bridge response to VGA-compatible addresses. When set, the bridge positively decodes and forwards the following accesses on the PCI Express interface to the Local Bus interface (and, conversely, blocks the forwarding of these addresses from the Local Bus interface to PCI Express interface): • Memory accesses in the range 000A0000h to 000BFFFFh • I/O address in the first 64 KB of the I/O Address space [Address[31:16] for PCI Express are zero (0000h)] and where Address[9:0] is in the range of 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases – Address[15:10] can be any value and is not used in decoding) When the *VGA Enable* bit is set, VGA address forwarding is independent of the **Bridge Control** register *ISA Enable* bit value, and the I/O and Memory Address ranges defined by the **I/O Base** and **Limit**, **Memory Base** and **Limit**, and **Prefetchable Memory Base** and **Limit** registers. VGA address forwarding is qualified by the **PCI Command** register *I/O Access Enable* and *Memory Space Enable* bits. 0 = Do not forward VGA-compatible Memory and I/O addresses from the PCI Express interface to Local Bus interface (addresses defined above), unless they are enabled for forwarding by the defined I/O and Memory Address ranges 1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the PCI Express interface to the Local Bus interface (when the *I/O Access Enable* and *Memory Space Enable* bits are set), independent of the I/O and Memory Address ranges and *ISA Enable* bit	RW	RW	WO	0

Register 18-34. (Offset 3Eh; BRIDGECTL) Bridge Control (Endpoint Mode) *(Cont.)*

Bits	Description	CFG	MM	EE	Default
4	**VGA 16-Bit Decode** Enables the bridge to provide 16-bit decoding of the VGA I/O address, precluding the decoding of alias addresses every 1 KB. Useful only when bit 3 (*VGA Enable)* of this register is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. Enables system configuration software to select between 10- and 16-bit I/O address decoding for VGA I/O register accesses that are forwarded from the PCI Express interface to the Local Bus interface, when the *VGA Enable* bit is set to 1. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses	RW	RW	WO	0
5	**Master Abort Mode** Controls bridge behavior when it receives a Master Abort termination on the internal PCI Bus or an Unsupported Request on PCI Express. 0 = Do not report Master Aborts • When PCI Express UR is received: – Return FFFFFFFFh to internal PCI Bus for reads – Complete Non-Posted Write normally on internal PCI Bus and discard the Write data – Discard posted internal PCI Bus-to-PCI Express Write data • When PCI transaction terminates with Master Abort: – Complete Non-Posted transaction with Unsupported Request – Discard Posted Write data from PCI Express-to-internal PCI Bus 1 = Report Master Aborts • When PCI Express UR is received: – Complete Reads and Non-Posted Writes with PCI Target Abort – Discard posted internal PCI Bus-to-PCI Express Write data • When PCI transaction terminates with Master Abort: – Complete Non-Posted transaction with Unsupported Request – Discard Posted Write data from PCI Express-to-internal PCI Bus – Transmit ERR_NONFATAL message for Posted Writes	RW	RW	WO	0
6	**Local Bridge Full Reset** When set, forces LRESET# assertion on the Local Bus. Additionally, the bridge Local Bus interface, and buffers between the PCI Express and Local Bus interfaces, must be initialized to their default state. The PCI Express interface and Configuration Space registers must not be affected by setting this bit. Because LRESET# is asserted while this bit is set, software must observe proper PCI Reset timing requirements.	RW	RW	WO	0
7	**Fast Back-to-Back Enable** ***Not supported.*** Controls bridge ability to generate Fast Back-to-Back transactions to different devices on the Local Bus interface.	RO	RO	–	0

Register 18-34. (Offset 3Eh; BRIDGECTL) Bridge Control (Endpoint Mode) *(Cont.)*

Bits	Description	CFG	MM	EE	Default
8	**Primary Discard Timer** In Endpoint mode, this bit does not apply and is forced to 0.	RO	RO	–	0
9	**Secondary Discard Timer** Selects the number of internal clocks that the bridge waits for a master on the Local Bus interface to repeat a Delayed Transaction request. The counter starts after the completion (PCI Express Completion associated with the Delayed Transaction request) reaches the head of the bridge downstream queue (*that is*, all ordering requirements are satisfied and the bridge is ready to complete the Delayed Transaction with the originating master on the Local Bus). When the originating master does not repeat the transaction before the counter expires, the bridge deletes the Delayed Transaction from its queue and sets the *Discard Timer Status* bit. 0 = Secondary Discard Timer counts 2^{15} internal clock periods 1 = Secondary Discard Timer counts 2^{10} internal clock periods	RW	RW	WO	0
10	**Discard Timer Status** Set to 1 when the Secondary Discard Timer expires and a Delayed Completion is discarded from a queue within the bridge. Writing 1 clears this bit.	RW1C	RW1C	WO	0
11	**Discard Timer Internal SERR# Enable** When set to 1, enables the bridge to generate an ERR_NONFATAL message on the PCI Express interface when the Secondary Discard Timer expires and a Delayed Transaction is discarded from a queue within the bridge. 0 = Do not generate ERR_NONFATAL message on the PCI Express interface as a result of the Secondary Discard Timer expiration 1 = Generate ERR_NONFATAL message on the PCI Express interface when the Secondary Discard Timer expires and a Delayed Transaction is discarded from a queue within the bridge	RW	RW	WO	0
15:12	***Reserved***	RsvdP	RsvdP	–	0h

Register 18-35. (Offset 3Eh; BRIDGECTL) Bridge Control (Root Complex Mode)

Bits	Description	CFG	MM	EE	Default
0	**Secondary Parity Error Response Enable** Controls the bridge response to Data Parity errors forwarded from the Local Bus interface (*such as*, a poisoned TLP). When cleared, the bridge must ignore Data Parity errors detected and continue normal operation. When set, the bridge must take its normal action when a Data Parity error is detected.	RW	RW	WO	0
1	**Secondary Internal SERR# Enable** No effect in Root Complex mode. PCI Express interface error reporting using internal SERR# is controlled by the **ROOTCTL** register.	RW	RW	WO	0
2	**ISA Enable** Modifies the bridge response to ISA I/O addresses that are enabled by the **I/O Base** and **I/O Limit** registers and located in the first 64 KB of the PCI I/O Address space. When set, the bridge blocks forwarding of I/O transactions, from the Local Bus interface to the PCI Express interface, that address the last 768 bytes in each 1-KB block. In the opposite direction (PCI Express interface to the Local Bus interface), I/O transactions are forwarded when they address the last 768 bytes in each 1-KB block.	RW	RW	WO	0
3	**VGA Enable** Modifies the bridge response to VGA-compatible addresses. When set, the bridge positively decodes and forwards the following accesses on the Local Bus interface to the PCI Express interface (and, conversely, blocks the forwarding of these addresses from the PCI Express interface to the Local Bus interface): • Memory accesses in the range 000A0000h to 000BFFFFh • I/O address in the first 64 KB of the I/O Address space [Address[31:16] for PCI Express are zero (0000h)] and where Address[9:0] is in the range of 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases – Address[15:10] can be any value and is not used in decoding) When the *VGA Enable* bit is set, VGA address forwarding is independent of the **Bridge Control** register *ISA Enable* bit value, and the I/O and Memory Address ranges defined by the **I/O Base** and **Limit**, **Memory Base** and **Limit**, and **Prefetchable Memory Base** and **Limit** registers. VGA address forwarding is qualified by the **PCI Command** register *I/O Access Enable* and *Memory Space Enable* bits. 0 = Do not forward VGA-compatible Memory and I/O addresses from the Local Bus interface to the PCI Express interface (addresses defined above), unless they are enabled for forwarding by the defined I/O and Memory Address ranges 1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the Local Bus interface to the PCI Express interface (when the *I/O Access Enable* and *Memory Space Enable* bits are set), independent of the I/O and Memory Address ranges and *ISA Enable* bit	RW	RW	WO	0

Register 18-35. (Offset 3Eh; BRIDGECTL) Bridge Control (Root Complex Mode) *(Cont.)*

Bits	Description	CFG	MM	EE	Default
4	**VGA 16-Bit Decode** Enables the bridge to provide 16-bit decoding of the VGA I/O address, precluding the decoding of alias addresses every 1 KB. Useful only when bit 3 (*VGA Enable)* of this register is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. Enables system configuration software to select between 10- and 16-bit I/O address decoding for all VGA I/O register accesses that are forwarded from the Local Bus interface to the PCI Express interface, when the *VGA Enable* bit is set to 1. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses	RW	RW	WO	0
5	**Master Abort Mode** Controls bridge behavior when it receives a Master Abort termination on the internal PCI Bus or an Unsupported Request on PCI Express. 0 = Do not report Master Aborts • When PCI Express UR is received: – Return FFFFFFFFh to internal PCI Bus for reads – Complete Non-Posted Write normally on internal PCI Bus (assert TRDY#) and discard the Write data – Discard posted internal PCI Bus-to-PCI Express Write data • When PCI transaction terminates with Master Abort: – Complete Non-Posted transaction with Unsupported Request – Discard Posted Write data from PCI Express-to-internal PCI Bus 1 = Report Master Aborts • When PCI Express UR is received: – Complete Reads and Non-Posted Writes with PCI Target Abort – Discard posted internal PCI Bus-to-PCI Express Write data • When PCI transaction terminates with Master Abort: – Complete Non-Posted transaction with Unsupported Request – Discard Posted Write data from PCI Express-to-internal PCI Bus – Transmit ERR_NONFATAL message for Posted Writes	RW	RW	WO	0
6	**PCI Express Hot Reset** When set, causes a Hot Reset to communicate on the PCI Express interface. The PCI Express interface, and buffers between the Local Bus and PCI Express interfaces, must be returned to their default state. The Local Bus interface and Configuration Space registers are not affected by setting this bit.	RW	RW	WO	0
7	**Fast Back-to-Back Enable** ***Not supported.*** Controls bridge ability to generate Fast Back-to-Back transactions to different devices on the PCI Express interface.	RO	RO	–	0

Register 18-35. (Offset 3Eh; BRIDGECTL) Bridge Control (Root Complex Mode) *(Cont.)*

Bits	Description	CFG	MM	EE	Default
8	**Primary Discard Timer** Selects the number of internal clocks that the bridge waits for a master on the Local Bus interface to repeat a Delayed Transaction request. The counter starts after the completion (PCI Express Completion associated with the Delayed Transaction request) reaches the head of the bridge downstream queue (*that is*, all ordering requirements are satisfied and the bridge is ready to complete the Delayed Transaction with the originating master on the PCI Express interface). When the originating master does not repeat the transaction before the counter expires, the bridge deletes the Delayed Transaction from its queue and sets the *Discard Timer Status* bit. 0 = Secondary Discard Timer counts 2^{15} internal clock periods 1 = Secondary Discard Timer counts 2^{10} internal clock periods	RW	RW	WO	0
9	**Secondary Discard Timer** In Root Complex mode, this bit does not apply and is forced to 0.	RO	RO	–	0
10	**Discard Timer Status** Set to 1 when the Primary Discard Timer expires and a Delayed Completion is discarded from a queue within the bridge.	RW1C	RW1C	–	0
11	**Discard Timer Internal SERR# Enable** When set to 1, enables the bridge to assert internal SERR# on the Local Bus interface when the Primary Discard Timer expires and a Delayed Transaction is discarded from a queue within the bridge. 0 = Do not assert internal SERR# on the Local Bus interface as a result of the Primary Discard Timer expiration 1 = Generate internal SERR# on the Local Bus interface when the Primary Discard Timer expires and a Delayed Transaction is discarded from a queue within the bridge	RW	RW	WO	0
15:12	***Reserved***	RsvdP	RsvdP	–	0h

18.8 PCI-Compatible Extended Capability Registers

Register 18-36. (Offset 40h; PWRMNGID) Power Management Capability ID

Bits	Description	CFG	MM	EE	Default
7:0	**Power Management Capability ID** Specifies the Power Management Capability ID.	RO	RO	–	01h

Register 18-37. (Offset 41h; PWRMNGNEXT) Power Management Next Capability Pointer

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Power Management Next Capability Pointer** Points to the first location of the next item in the New Capabilities Linked List, Message Signaled Interrupts.	RO	RW	WO	50h

Register 18-38. (Offset 42h; PWRMNGCAP) Power Management Capabilities (Endpoint Mode)

Bits	Description	CFG	MM	EE	Default
2:0	**PME Version** Default 010b indicates compliance with the *PCI Power Mgmt. r1.1*.	RO	RW	WO	010b
3	**PME Clock** For Endpoint mode, does not apply to PCI Express; therefore, must always retain a value of 0.	RO	RO	–	0
4	***Reserved***	RsvdP	RsvdP	–	0
5	**Device Specific Initialization** Indicates that the PEX 8311 requires special initialization following a transition to the D0_uninitialized state before the generic class device driver uses it.	RO	RW	WO	0
8:6	**AUX Current** Reports the 3.3Vaux auxiliary current requirements for the PCI function. When PCI backplane PME# generation from D3cold is not supported by the function, must return a value of 000b.	RO	RW	WO	000b
9	**D1 Support** Specifies that the PEX 8311 supports the D1 state.	RO	RW	WO	1
10	**D2 Support** Specifies that the PEX 8311 does ***not support*** the D2 state.	RO	RW	WO	0
15:11	**PME Support** Default 11001b indicates that the corresponding PEX 8311 port forwards PME messages in the D0, D3hot, and D3cold power states. **Value** **Description** XXXX1b Assertable from D0 XXX1Xb Assertable from D1 XX1XXb ***Reserved*** X1XXXb Assertable from D3hot 1XXXXb Assertable from D3cold	RO	RW	WO	11001b

Register 18-39. (Offset 42h; PWRMNGCAP) Power Management Capabilities (Root Complex Mode)

Bits	Description	CFG	MM	EE	Default
2:0	**PME Version** Default 010b indicates compliance with the *PCI Power Mgmt. r1.1*.	RO	RW	WO	010b
3	**PME Clock** When low, indicates that no internal clock is required to generate PME#. When high, indicates that an internal clock is required to generate PME#.	RO	RW	WO	0
4	***Reserved***	RsvdP	RsvdP	–	0
5	**Device-Specific Initialization** Indicates that the PEX 8311 requires special initialization following a transition to the D0_uninitialized state before the generic class device driver uses it.	RO	RW	WO	0
8:6	**AUX Current** Reports the 3.3Vaux auxiliary current requirements for the PCI function. When PME# generation from D3cold is not supported by the function, must return a value of 000b.	RO	RW	WO	000b
9	**D1 Support** Specifies that the PEX 8311 supports the D1 state.	RO	RW	WO	1
10	**D2 Support** Specifies that the PEX 8311 does ***not support*** the D2 state.	RO	RW	WO	0
15:11	**PME Support** Default 11001b indicates that the corresponding PEX 8311 port forwards PME messages in the D0, D3hot, and D3cold power states. **Value** **Description** XXXX1b Assertable from D0 XXX1Xb Assertable from D1 XX1XXb ***Reserved*** X1XXXb Assertable from D3hot 1XXXXb Assertable from D3cold	RO	RW	WO	11001b

Register 18-40. (Offset 44h; PWRMNGCSR) Power Management Control/Status (Endpoint Mode)

Bits	Description	CFG	MM	EE	Default
1:0	**Power State** Used to determine or change the current power state. **Value** **State** 00b D0 01b D1 10b ***Reserved*** 11b D3hot A transition from state D3 to state D0 causes a Soft Reset to occur. In state D1, when the corresponding *D1 Support* bit is set, PCI Memory and I/O accesses are disabled, as well as the PCI interrupt, and only Configuration cycles are allowed. In state D3hot, these functions are also disabled.	RW	RW	WO	00b
7:2	***Reserved***	RsvdP	RsvdP	–	0h
8	**PME Enable** Enables a PME message to transmit upstream.	RW	RW	WO	0
12:9	**Data Select** ***Not supported.*** Always returns a value of 0h.	RO	RO	–	0h
14:13	**Data Scale** ***Not supported.*** Always returns a value of 00b.	RO	RO	–	00b
15	**PME Status** Indicates that a PME message was transmitted upstream. Writing 1 clears this bit.	RW1C	RW1C	–	0

Register 18-41. (Offset 44h; PWRMNGCSR) Power Management Control/Status (Root Complex Mode)

Bits	Description	CFG	MM	EE	Default
1:0	**Power State** Used to determine or change the current power state. **Value** **State** 00b D0 01b D1 10b ***Reserved*** 11b D3hot A transition from state D3 to state D0 causes a Soft Reset. In state D1, when the corresponding *D1 Support* bit is set, PCI Memory and I/O accesses are disabled, as well as the PCI interrupt, and only Configuration cycles are allowed. In state D3hot, these functions are also disabled.	RW	RW	WO	00b
7:2	***Reserved***	RsvdP	RsvdP	–	0h
8	**PME Enable** Enables the PMEOUT# signal to assert.	RW	RW	WO	0
12:9	**Data Select** ***Not supported.*** Always returns a value of 0h.	RO	RO	–	0h
14:13	**Data Scale** ***Not supported.*** Always returns a value of 00b.	RO	RO	–	00b
15	**PME Status** When the *PME Enable* bit is set high, indicates that PMEOUT# is being driven. Writing 1 from the internal PCI Bus clears this bit.	RW1C	RW1C	–	0

Register 18-42. (Offset 46h; PWRMNGBRIDGE) Power Management Bridge Support (Endpoint Mode)

Bits	Description	CFG	MM	EE	Default
5:0	***Reserved***	RsvdP	RsvdP	–	0h
6	**B2/B3 Support** ***Not supported*** in Endpoint mode; therefore, forced to 0.	RO	RO	–	0
7	**Bus Power/Clock Control Enable** ***Not supported*** in Endpoint mode; therefore, forced to 0.	RO	RO	–	0

Register 18-43. (Offset 46h; PWRMNGBRIDGE) Power Management Bridge Support (Root Complex Mode)

Bits	Description	CFG	MM	EE	Default
5:0	***Reserved***	RsvdP	RsvdP	–	0h
6	**B2/B3 Support** When cleared, indicates that, when the bridge function is programmed to D3hot, power is removed (B3) from the PCI Express interface. Useful only when bit 7 is set. When set, indicates that, when the bridge function is programmed to D3hot, the PCI Express interface internal clock is stopped (B2).	RO	RW	WO	0
7	**Bus Power/Clock Control Enable** When set, indicates that the bus power/clock control mechanism (as defined in the *PCI-to-PCI Bridge r1.1*, Section 4.7.1) is enabled.	RO	RW	WO	0

Register 18-44. (Offset 47h; PWRMNGDATA) Power Management Data

Bits	Description	CFG	MM	EE	Default
7:0	**Power Management Data** ***Not supported.*** Always returns a value of 0h.	RO	RO	–	0h

Register 18-45. (Offset 48h; DEVSPECCTL) Device-Specific Control

Bits	Description	CFG	MM	EE	Default
0	**Blind Prefetch Enable** When cleared, a Memory Read command on the internal PCI Bus that targets the PCI Express Memory space causes only 1 word to be read from the PCI Express interface. When set, a Memory Read command on the internal PCI Bus that targets the PCI Express Memory space causes a cache line to be read from the PCI Express interface.	RW	RW	WO	0
1	**PCI Base Address 0 Enable** When set, enables the PCI Base Address 0 space for Memory-Mapped access to the Configuration registers and shared memory. PCI Base Address 0 is also enabled when the BAR0ENB# ball is low.	RW	RW	WO	0
2	**L2 Enable** Valid only in Root Complex mode. When cleared, a power state change to D3 does not cause the PEX 8311 to change the link state to L2. When set, a power state change to D3 causes the PEX 8311 to change the link state to L2.	RW	RW	WO	0
3	**PMU Power Off** When set, the link transitioned to the L2/L3 Ready state, and is ready to power down.	RO	RO	–	0
7:4	**PMU Link State** Indicates the link state. **Value** **State** **Value** **State** 0001b L0 0100b L1 0010b L0s 1000b L2	RO	RO	–	–
9:8	**CRS Retry Control** Determines the PEX 8311 response in Root Complex mode when a PCI-to-PCI Express Configuration transaction is terminated with a Configuration Request Retry Status. **Value** **Response** 00b Retry once after 1s. When another CRS is received, Target Abort on the internal PCI Bus. 01b Retry eight times, once per second. When another CRS is received, Target Abort on the internal PCI Bus. 10b Retry once per second until successful completion. 11b ***Reserved***	RW	RW	WO	00b
10	**WAKE Out Enable** Valid only in Endpoint mode. When set, the WAKEOUT# signal is asserted when the link is in the L2 state.	RW	RW	WO	0
11	**Beacon Generate Enable** Valid only in Endpoint mode. When set, a beacon is generated when the link is in the L2 state.	RW	RW	WO	0
12	**Beacon Detect Enable** Valid only in Root Complex mode. When set, a beacon detected while the link is in the L2 state causes the *PME Status* bit to set.	RW	RW	WO	0
13	**PLL Locked** High when internal PLL is locked.	RO	RO	–	–
15:14	***Reserved***	RsvdP	RsvdP	–	00b
20:16	**Link Training and Status State Machine** ***For internal use only.***	RO	RO	–	–
31:21	***Reserved***	RsvdP	RsvdP	–	0h

Register 18-46. (Offset 50h; MSIID) Message Signaled Interrupts Capability ID

Bits	Description	CFG	MM	EE	Default
7:0	**MSI Capability ID** Specifies the Message Signaled Interrupts Capability ID.	RO	RO	–	5h

Register 18-47. (Offset 51h; MSINEXT) Message Signaled Interrupts Next Capability Pointer

Bits	Description	CFG	MM	EE	Default
7:0	**MSI Next Capability Pointer** Points to the first location of the next item in the New Capabilities Linked List, PCI Express Capability.	RO	RW	WO	60h

Register 18-48. (Offset 52h; MSICTL) Message Signaled Interrupts Control

Bits	Description	CFG	MM	EE	Default
0	**MSI Enable** When set: • Enables the PEX 8311 to use MSI to request service • Virtual interrupt support for internal interrupt sources is disabled for Endpoint mode • INTA# output is disabled in Root Complex mode	RW	RW	WO	0
3:1	**Multiple Message Capable** System software reads this field to determine the number of requested messages. The number of requested messages must be aligned to a power of two (when a function requires three messages, it requests four. The encoding is defined as: **Value** **Number of Messages Requested** 000b 1 001b 2 010b 4 011b 8 100b 16 101b 32 110b, 111b ***Reserved***	RO	RO	–	000b
6:4	**Multiple Message Enable** System software writes to this field to indicate the number of allocated messages (equal to or less than the number of requested messages). The number of allocated messages is aligned to a power of two. The encoding is defined as: **Value** **Number of Messages Requested** 000b 1 001b 2 010b 4 011b 8 100b 16 101b 32 110b, 111b ***Reserved***	RW	RW	WO	000b
7	**MSI 64-Bit Address Capable** When set, the PEX 8311 is capable of generating a 64-bit Message address.	RO	RW	WO	1 (E) 0 (RC)
8	**Per Vector Masking Capable** ***Not supported.*** Forced to 0.	RO	RO	–	0
15:9	***Reserved***	RsvdP	RsvdP	–	0h

Note: *In the **Default** column, "E" indicates Endpoint mode, and "RC" indicates Root Complex mode.*

Register 18-49. (Offset 54h; MSIADDR) Message Signaled Interrupts Address

Bits	Description	CFG	MM	EE	Default
1:0	***Reserved***	RsvdP	RsvdP	–	00b
31:2	**MSI Address** When the **Message Signaled Interrupts Control** register *MSI Enable* bit (bit 0) is set, the register contents specify the DWORD-aligned address for the MSI Memory Write transaction. Address bits [1:0] are driven to zero (00b) during the Address phase.	RW	RW	WO	0h

Register 18-50. (Offset 58h; MSIUPPERADDR) Message Signaled Interrupts Upper Address

Bits	Description	CFG	MM	EE	Default
31:0	**MSI Upper Address** Optionally implemented only when the device supports 64-bit Message addressing (**Message Signaled Interrupts Control** register *64-bit Address Capable* bit is set). When the **Message Signaled Interrupts Control** register *MSI Enable* bit (bit 0) is set, the register contents specify the upper 32 bits of a 64-bit Message address. When the register contents are zero (0h), the PEX 8311 uses the 32-bit address specified by the **Message Signaled Interrupts Address** register.	RW	RW	WO	0h

Register 18-51. (Offset 5Ch; MSIDATA) Message Signaled Interrupts Data

Bits	Description	CFG	MM	EE	Default
15:0	**MSI Data** When the *MSI Enable* bit is set, the message data is driven onto the lower word (AD[15:0]) of the Memory Write transaction Data phase.	RW	RW	WO	0h
31:16	***Reserved***	RsvdP	RsvdP	–	0h

Register 18-52. (Offset 60h; PCIEXID) PCI Express Capability ID

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Express Capability ID** Specifies the PCI Express Capability ID.	RO	RW	–	10h

Register 18-53. (Offset 61h; PCIEXNEXT) PCI Express Next Capability Pointer

Bits	Description	CFG	MM	EE	Default
7:0	**PCI Express Next Capability Pointer** Points to the first location of the next item in the New Capabilities Linked List.	RO	RW	WO	0h

Register 18-54. (Offset 62h; PCIEXCAP) PCI Express Capabilities

Bits	Description	CFG	MM	EE	Default
3:0	**Capability Version** Indicates the PCI Express capability structure version number.	RO	RW	WO	1h
7:4	**Device/Port Type** Indicates the type of PCI Express logical device. Device encodings are as follows: **Value** **Device/Port Type** 0000b PCI Express Endpoint Device 0001b Conventional PCI Express Endpoint Device 0100b Root Port of PCI Express Root Complex 0101b Upstream Port of PCI Express Switch 0110b Downstream Port of PCI Express Switch 0111b PCI Express-to-PCI/PCI-X Bridge 1000b PCI/PCI-X-to-PCI Express Bridge All other values are ***reserved***.	RO	RW	WO	0111b (E) 1000b (RC)
8	**Slot Implemented** When set, indicates that the PCI Express Link associated with this port is connected to a slot.	RO	RW	WO	0
13:9	**Interrupt Message Number** When this function is allocated more than one MSI interrupt number, this field must contain the offset between the Base Message data and the MSI message generated when status bits in the **Slot Status** or **Root Status** register of this capability structure are set. For the field to be correct, hardware must update it when the number of MSI messages assigned to the device changes.	RO	RO	–	0h
15:14	***Reserved***	RsvdP	RsvdP	–	00b

Note: *In the **Default** column, "E" indicates Endpoint mode, and "RC" indicates Root Complex mode.*

Register 18-55. (Offset 64h; DEVCAP) Device Capabilities

Bits	Description	CFG	MM	EE	Default
2:0	**Maximum Payload Size Supported** Indicates the s that the device supports for TLPs. Defined encodings are as follows: **Value** **Maximum Payload Size** 000b 128 bytes 001b 256 bytes 010b 512 bytes 011b 1,024 bytes 100b 2,048 bytes 101b 4,096 bytes 110b, 111b ***Reserved*** ***Note:*** *Because the PEX 8311 only supports a Maximum Payload Size of 128 bytes, this field is hardwired to 000b.*	RO	RO	–	000b
4:3	**Phantom Functions Supported** ***Not supported.*** Hardwired to 00b. This field indicates support for the use of unclaimed Function Numbers to extend the number of outstanding transactions allowed, by logically combining unclaimed Function Numbers (called Phantom Functions) with the Tag identifier.	RO	RO	–	00b
5	**Extended Tag Field Supported** Indicates the maximum supported size of the Tag field. When cleared, a 5-bit Tag field is supported. When set, an 8-bit Tag field is supported. ***Note:*** *8-bit Tag field support must be enabled by the corresponding Control field in the* ***PCI Express Device Control*** *register.*	RO	RW	WO	0
8:6	**Endpoint L0s Acceptable Latency** Indicates the acceptable total latency that an Endpoint withstands due to the transition from the L0s state to the L0 state. It is essentially an indirect measure of the Endpoint internal buffering. Power management software uses the reported L0s Acceptable Latency number to compare against the L0s exit latencies reported by all components comprising the data path from this Endpoint to the Root Complex Root Port to determine whether Active State Link PM L0s entry is used with no loss of performance. Defined encodings are as follows: **Value** **Latency** 000b Less than 64 ns 001b 64 ns to less than 128 ns 010b 128 ns to less than 256 ns 011b 256 ns to less than 512 ns 100b 512 ns to 1 µs 101b 1 µs to less than 2 µs 110b 2 to 4 µs 111b More than 4 µs	RO	RW	WO	000b

Register 18-55. (Offset 64h; DEVCAP) Device Capabilities *(Cont.)*

Bits	Description	CFG	MM	EE	Default
11:9	**Endpoint L1 Acceptable Latency** Indicates the acceptable total latency that an Endpoint withstands due to the transition from the L1 state to the L0 state. It is essentially an indirect measure of the Endpoint internal buffering. Power management software uses the report L1 Acceptable Latency number to compare against the L1 exit latencies reported by all components comprising the data path from this Endpoint to the Root Complex Root Port to determine whether Active State Link PM L1 entry is used with no loss of performance. Defined encodings are as follows: **Value Latency** 000b Less than 1 µs 001b 1 µs to less than 2 µs 010b 2 µs to less than 4 µs 011b 4 µs to less than 8 µs 100b 8 µs to less than 16 µs 101b 16 µs to less than 32 µs 110b 32 to 64 µs 111b More than 64 µs	RO	RW	WO	000b
12	**Attention Button Present** ***Not supported***. Forced to 0.	RO	RO	–	0
13	**Attention Indicator Present** ***Not supported***. Forced to 0.	RO	RO	–	0
14	**Power Indicator Present** ***Not supported***. Forced to 0.	RO	RO	–	0
17:15	***Reserved***	RsvdP	RsvdP	–	000b
25:18	**Captured Slot Power Limit Value** Specifies the upper limit on power supplied by slot in combination with the *Slot Power Limit Scale* value. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the *Slot Power Limit Scale* field. Value is set by the Set Slot Power Limit message.	RO	RW	WO	0h
27:26	**Captured Slot Power Limit Scale** Specifies the scale used for the *Slot Power Limit Value.* Value is set by the Set Slot Power Limit message. Range of values: **Value Scale** 00b 1.0x 01b 0.1x 10b 0.01x 11b 0.001x	RO	RW	WO	00b
31:28	***Reserved***	RsvdP	RsvdP	–	0h

Register 18-56. (Offset 68h; DEVCTL) PCI Express Device Control

Bits	Description	CFG	MM	EE	Default
0	**Correctable Error Reporting Enable** Valid only in Endpoint mode. Controls Correctable error reporting. When a Correctable error is detected in Endpoint mode and this bit is set, an ERR_COR message is transmitted to the Root Complex.	RW	RW	WO	0
1	**Non-Fatal Error Reporting Enable** Valid only in Endpoint mode. Controls Non-Fatal error reporting. When a Non-Fatal error is detected in Endpoint mode and this bit is set, an ERR_NONFATAL message is transmitted to the Root Complex.	RW	RW	WO	0
2	**Fatal Error Reporting Enable** Valid only in Endpoint mode. Controls Fatal error reporting. When a Fatal error is detected in Endpoint mode and this bit is set, an ERR_FATAL message is transmitted to the Root Complex.	RW	RW	WO	0
3	**Unsupported Request Reporting Enable** Valid only in Endpoint mode. Controls Unsupported Request reporting. When an Unsupported Request response is received from the PCI Express in Endpoint mode and this bit is set, a non-ERR_FATAL message is transmitted to the Root Complex.	RW	RW	WO	0
4	**Enable Relaxed Ordering** ***Not supported.*** When set, the device is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require Strong Write ordering. Forced to 0.	RO	RO	–	0
7:5	**Maximum Payload Size** Sets the maximum TLP payload size for the device. As a receiver, the device must handle TLPs as large as the set value. As a transmitter, the device must not generate TLPs exceeding the set value. Permissible values for transmitted TLPs are indicated in the **Device Capabilities** register *Maximum Payload Size Supported* field. Defined encodings are as follows: **Value** — **Maximum Payload Size** 000b — 128 bytes 001b — 256 bytes 010b — 512 bytes 011b — 1,024 bytes 100b — 2,048 bytes 101b — 4,096 bytes 110b, 111b — ***Reserved***	RW	RW	WO	000b

Register 18-56. (Offset 68h; DEVCTL) PCI Express Device Control *(Cont.)*

Bits	Description	CFG	MM	EE	Default
8	**Extended Tag Field Enable** When cleared, the device is restricted to a 5-bit Tag field. Forced to 0 when the **DEVCAP** register *Extended Tag Field Supported* bit is cleared. When set, enables the device to use an 8-bit Tag field as a requester.	RW	RW	WO	0
9	**Phantom Function Enable** ***Not supported.*** Hardwired to 0.	RO	RO	–	0
10	**Auxiliary (AUX) Power PM Enable** ***Not supported.*** Hardwired to 0. When set, enables the PEX 8311 to draw AUX power independent of PME AUX power. Devices that require AUX power on legacy operating systems must continue to indicate PME AUX power requirements. AUX power is allocated as requested in the **Power Management Capabilities** register *AUX Current* field, independent of the **Power Management Control/Status** register *PME Enable* bit.	RO	RO	–	0
11	**Enable No Snoop** ***Not supported.*** Hardwired to 0. When set, the PEX 8311 is permitted to set the *No Snoop* bit in the Requester Attributes of transactions it initiates that do not require hardware-enforced cache coherency. Setting this bit to 1 does not cause a device to blindly set the *No Snoop* attribute on transactions that it initiates. Although this bit is set to 1, a device only sets the *No Snoop* attribute on a transaction when it can guarantee that the transaction address is not stored in a system cache. The PEX 8311 never sets the *No Snoop* attribute; therefore, forced to 0.	RO	RO	–	0
14:12	**Maximum Read Request Size** The value specified in this register is the upper boundary of the **PCI Express Device Control** register *Maximum Read Request Size* field if the **Device-Specific Control** register *Blind Prefetch Enable* bit is set. Sets the maximum Read Request size for the device as a Requester. The device must not generate Read Requests with size exceeding the set value. Defined encodings are as follows: **Value** – **Maximum Payload Size** 000b – 128 bytes 001b – 256 bytes 010b – 512 bytes 011b – 1,024 bytes 100b – 2,048 bytes 101b – 4,096 bytes 110b, 111b – ***Reserved***	RW	RW	WO	010b
15	**Bridge Configuration Retry Enable** When cleared, the PEX 8311 does not generate completions with Completion Retry Status on behalf of PCI Express-to-PCI Configuration transactions. When set, the PEX 8311 generates completions with Completion Retry Status on behalf of PCI Express-to-PCI Configuration transactions. This occurs after a delay determined by the **CRS Timer** register.	RW	RW	WO	0

Register 18-57. (Offset 6Ah; DEVSTAT) PCI Express Device Status

Bits	Description	CFG	MM	EE	Default
0	**Correctable Error Detected** Indicates detected Correctable errors status. Errors are logged in this register, regardless of whether error reporting is enabled in the **PCI Express Device Control** register.	RW1C	RW1C	–	0
1	**Non-Fatal Error Detected** Indicates detected Non-Fatal errors status. Errors are logged in this register, regardless of whether error reporting is enabled in the **PCI Express Device Control** register.	RW1C	RW1C	–	0
2	**Fatal Error Detected** Indicates detected Fatal errors status. Errors are logged in this register, regardless of whether error reporting is enabled in the **PCI Express Device Control** register.	RW1C	RW1C	–	0
3	**Unsupported Request Detected** Indicates that the PEX 8311 received an Unsupported Request. Errors are logged in this register, regardless of whether error reporting is enabled in the **PCI Express Device Control** register.	RW1C	RW1C	–	0
4	**AUX Power Detected** Devices that require AUX power report this bit as set when the device detects AUX power.	RO	RO	–	0
5	**Transactions Pending** Because the PEX 8311 does not internally generate Non-Posted transactions, this bit is forced to 0.	RO	RO	–	0
15:6	***Reserved***	RsvdZ	RsvdZ	–	0h

Register 18-58. (Offset 6Ch; LINKCAP) Link Capabilities

Bits	Description	CFG	MM	EE	Default
3:0	**Maximum Link Speed** Indicates the maximum Link speed of the given PCI Express Link. Set to 0001b for 2.5 Gbps. All other values are ***reserved***.	RO	RO	–	0001b
9:4	**Maximum Link Width** Indicates the maximum width of the given PCI Express Link. By default, the PEX 8311 has an x1 link; therefore, this field is hardwired to 000001b. All other values are ***not supported***.	RO	RO	–	000001b
11:10	**Active State Link PM Support** Indicates the level of active state power management supported on the given PCI Express Link. Defined encodings are as follows: **Value** **Latency** 01b L0s Entry Supported 11b L0s and L1 Supported 00b, 10b ***Reserved***	RO	RW	WO	11b
14:12	**L0s Exit Latency** Indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this port requires to complete the transition from L0s to L0. Defined encodings are as follows: **Value** **Latency** 000b Less than 64 ns 001b 64 ns to less than 128 ns 010b 128 ns to less than 256 ns 011b 256 ns to less than 512 ns 100b 512 ns to 1 µs 101b 1 µs to less than 2 µs 110b 2 to 4 µs 111b More than 4 µs	RO	RW	WO	100b
17:15	**L1 Exit Latency** Indicates the L1 exit latency for the given PCI Express Link. The value reported indicates the length of time this port requires to complete the transition from L1 to L0. Defined encodings are as follows: **Value** **Latency** 000b Less than 1 µs 001b 1 µs to less than 2 µs 010b 2 µs to less than 4 µs 011b 4 µs to less than 8 µs 100b 8 µs to less than 16 µs 101b 16 µs to less than 32 µs 110b 32 to 64 µs 111b More than 64 µs	RO	RW	WO	100b
23:18	***Reserved***	RsvdP	RsvdP	–	0h
31:24	**Port Number** Indicates the PCI Express port number for the given PCI Express Link.	RO	RW	WO	0h

Register 18-59. (Offset 70h; LINKCTL) Link Control

Bits	Description	CFG	MM	EE	Default
1:0	**Active State Link PM Control** Controls the level of active state PM supported on the given PCI Express Link. Defined encodings are as follows: **Value PM Control** 00b Disabled 01b L0s Entry Supported 10b ***Reserved*** 11b L0s and L1 Entry Supported ***Note:*** *"L0s Entry Enabled" indicates the Transmitter entering L0s.*	RW	RW	WO	00b
2	***Reserved***	RsvdP	RsvdP	–	0
3	**Read Completion Boundary (RCB) Control** When cleared, the Read Completion boundary is 64 bytes. When set, the Read Completion boundary is 128 bytes.	RW (E) RO (RC)	RW	WO	0
4	**Link Disable** Valid only in Root Complex mode. When set to 1, this bit disables the link. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state.	RO (E) RW (RC)	RO (E) RW (RC)	– (E) WO (RC)	0
5	**Retrain Link** Valid only in Root Complex mode. When set, initiates link retraining. Always returns 0 when read.	RO (E) RW (RC)	RO (E) RW (RC)	– (E) WO (RC)	0
6	**Common Clock Configuration** When set, indicates that this component and the component at the opposite end of this link are operating with a distributed common reference clock. Value of 0 indicates that this component and the component at the opposite end of this link are operating with asynchronous reference clock. Components utilize this common clock configuration information to report the correct L0s and L1 Exit Latencies.	RW	RW	WO	0
7	**Extended Sync** When set, this bit forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from the L1 state prior to entering the L0 state. This mode provides external devices monitoring the link sufficient time to achieve bit and symbol lock before the link enters the L0 state and resumes communication.	RW	RW	WO	0
15:8	***Reserved***	RsvdP	RsvdP	–	0h

Note: *In the **CFG**, **MM**, and **EE** columns, "E" indicates Endpoint mode, and "RC" indicates Root Complex mode.*

Register 18-60. (Offset 72h; LINKSTAT) Link Status

Bits	Description	CFG	MM	EE	Default
3:0	**Link Speed** Indicates the negotiated Link speed of the given PCI Express Link. Set to 0001b for 2.5 Gbps. All other values are ***reserved***.	RO	RO	–	0001b
9:4	**Negotiated Link Width** Indicates the negotiated width of the given PCI Express Link. By default, the PEX 8311 has an x1 link; therefore, this field is hardwired to 000001b. All other values are ***not supported***.	RO	RO	–	000001b
10	**Link Training Error** Valid only in Root Complex mode. Indicates that a Link Training error occurred. Cleared by hardware upon successful training of the link to the L0 state.	RO	RO	–	0
11	**Link Training** Valid only in Root Complex mode. Indicates that Link training is in progress; hardware clears this bit after Link training is complete.	RO	RO	–	0
12	**Slot Clock Configuration** Indicates that the component uses the same physical reference clock that the platform provides on the connector. When the device uses an independent clock irrespective of the presence of a reference on the connector, this bit must be cleared.	HwInit	RW	WO	0
15:13	***Reserved***	RsvdZ	RsvdZ	–	000b

Register 18-61. (Offset 74h; SLOTCAP) Slot Capabilities

Bits	Description	CFG	MM	EE	Default
0	**Attention Button Present** ***Not supported***. Forced to 0.	RO	RO	–	0
1	**Power Controller Present** ***Not supported***. Forced to 0.	RO	RO	–	0
2	**MRL Sensor Present** ***Not supported***. Forced to 0.	RO	RO	–	0
3	**Attention Indicator Present** ***Not supported***. Forced to 0.	RO	RO	–	0
4	**Power Indicator Present** ***Not supported***. Forced to 0.	RO	RO	–	0
5	**Hot Plug Surprise** ***Not supported***. Forced to 0.	RO	RO	–	0
6	**Hot Plug Capable** ***Not supported***. Forced to 0.	RO	RO	–	0
14:7	**Slot Power Limit Value** Valid only in Root Complex mode. In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by the slot. The Power limit (in Watts) is calculated by multiplying the value in this field by the value in the *Slot Power Limit Scale* field. Writes to this register cause the PEX 8311 to transmit the Set Slot Power Limit message downstream.	RO	RW	WO	25d
16:15	**Slot Power Limit Scale** Valid only in Root Complex mode. Specifies the scale used for the *Slot Power Limit Value*. Writes to this register cause the PEX 8311 to transmit the Set Slot Power Limit message downstream. Defined encodings are as follows: **Value** **Scale** 00b 1.0x 01b 0.1x 10b 0.01x 11b 0.001x	RO	RW	WO	00b
18:17	***Reserved***	RsvdP	RsvdP	–	00b
31:19	**Physical Slot Number** ***Not supported***. Forced to 0h.	RO	RO	–	0h

Register 18-62. (Offset 78h; SLOTCTL) Slot Control

Bits	Description	CFG	MM	EE	Default
0	**Attention Button Pressed Enable** ***Not supported***. Forced to 0.	RW	RW	WO	0
1	**Power Fault Detected Enable** ***Not supported***. Forced to 0.	RW	RW	WO	0
2	**MRL Sensor Changed Enable** ***Not supported***. Forced to 0.	RW	RW	WO	0
3	**Presence Detect Changed Enable** ***Not supported***. Forced to 0.	RW	RW	WO	0
4	**Command Completed Interrupt Enable** ***Not supported***. Forced to 0.	RW	RW	WO	0
5	**Hot Plug Interrupt Enable** ***Not supported***. Forced to 0.	RW	RW	WO	0
7:6	**Attention Indicator Control** ***Not supported***. Forced to 00b.	RW	RW	WO	00b
9:8	**Power Indicator Control** ***Not supported***. Forced to 00b.	RW	RW	WO	00b
10	**Power Controller Control** ***Not supported***. Forced to 0.	RW	RW	WO	0
15:11	***Reserved***	RsvdP	RsvdP	–	0h

Register 18-63. (Offset 7Ah; SLOTSTAT) Slot Status

Bits	Description	CFG	MM	EE	Default
0	**Attention Button Pressed** ***Not supported***. Forced to 0.	RO	RO	–	0
1	**Power Fault Detected** ***Not supported***. Forced to 0.	RO	RO	–	0
2	**MRL Sensor Changed** ***Not supported***. Forced to 0.	RO	RO	–	0
3	**Presence Detect Changed** ***Not supported***. Forced to 0.	RO	RO	–	0
4	**Command Completed** ***Not supported***. Forced to 0.	RO	RO	–	0
5	**MRL Sensor State** ***Not supported***. Forced to 0.	RO	RO	–	0
6	**Presence Detect State** ***Not supported***. Forced to 1.	RO	RO	–	1
15:7	***Reserved***	RsvdP	RsvdP	–	0h

Register 18-64. (Offset 7Ch; ROOTCTL) Root Control (Root Complex Mode Only)

Bits	Description	CFG	MM	EE	Default
0	**System Error on Correctable Error Enable** When set, a System error (internal SERR#) is generated when an ERR_COR error is reported by devices in the hierarchy associated with this Root Port, or by the Root Port itself.	RW	RW	WO	0
1	**System Error on Non-Fatal Error Enable** When set, a System error (internal SERR#) is generated when an ERR_NONFATAL error is reported by devices in the hierarchy associated with this Root Port, or by the Root Port itself.	RW	RW	WO	0
2	**System Error on Fatal Error Enable** When set, a System error (internal SERR#) is generated when an ERR_FATAL error is reported by devices in the hierarchy associated with this Root Port, or by the Root Port itself.	RW	RW	WO	0
3	**PME Interrupt Enable** When set, enables PME interrupt generation upon PME message receipt as reflected in the *PME Status* bit. A PME interrupt is also generated when the *PME Status* bit is set when this bit is set from a cleared state.	RW	RW	WO	0
31:4	***Reserved***	RsvdP	RsvdP	–	0h

Register 18-65. (Offset 80h; ROOTSTAT) Root Status (Root Complex Mode Only)

Bits	Description	CFG	MM	EE	Default
15:0	**PME Requester ID** Indicates the PCI Requester ID of the last PME requester.	RO	RO	–	–
16	**PME Status** Indicates that PME was asserted by the Requester ID indicated in the *PME Requester ID* field. Subsequent PMEs remain pending until this bit is cleared by software, by writing 1.	RW1C	RW1C	–	0
17	**PME Pending** Indicates that another PME is pending when the *PME Status* bit is set. When the *PME Status* bit is cleared by software, the PME is delivered by hardware by setting the *PME Status* bit again and updating the Requester ID appropriately. Cleared by hardware when no other PMEs are pending.	RO	RO	–	–
31:18	***Reserved***	RsvdP	RsvdP	–	0h

Register 18-66. (Offset 84h; MAININDEX) Main Control Register Index

Bits	Description	CFG	MM	EE	Default
11:0	**Main Control Register Index** Selects a **Main Control** register that is accessed by way of the **MAINDATA** register.	RW	RW	WO	0h
31:12	***Reserved***	RsvdP	RsvdP	–	0h

Register 18-67. (Offset 88h; MAINDATA) Main Control Register Data

Bits	Description	CFG	MM	EE	Default
31:0	**Main Control Register Data** Writes to and reads from this register are mapped to a **Main Control** register selected by the **MAININDEX** register.	RW	RW	WO	0h

18.9 PCI Express Extended Capability Registers

18.9.1 PCI Express Power Budgeting Registers

Register 18-68. (Offset 100h; PWRCAPHDR) Power Budgeting Capability Header

Bits	Description	CFG	MM	EE	Default
15:0	**PCI Express Extended Capability ID** PCI-SIG-defined ID Number that indicates the nature and format of the extended capability.	RO	RW	WO	4h
19:16	**Capability Version** PCI-SIG-defined Version Number that indicates the version of the capability structure present.	RO	RW	WO	1h
31:20	**Next Capability Offset** Contains the offset to the next PCI Express capability structure, or 000h when no other items exist in the New Capabilities Linked List. Set to 110h when Serial Number Capability must be enabled.	RO	RW	WO	000h

Register 18-69. (Offset 104h; PWRDATASEL) Power Budgeting Data Select

Bits	Description	CFG	MM	EE	Default
7:0	**Data Select Register** Indexes the Power Budgeting Data reported through the **Power Budgeting Data** register. Selects the DWORD of Power Budgeting Data that is to appear in the **Power Budgeting Data** register. The PEX 8311 supports values from 0 to 31 for this field. For values greater than 31, a value of 0h is returned when the **Power Budgeting Data** register is read.	RW	RW	WO	0h
31:8	***Reserved***	RsvdP	RsvdP	–	0h

Register 18-70 returns the DWORD of Power Budgeting Data selected by the **Power Budgeting Data Select** register. When the **Power Budgeting Data Select** register contains a value greater than or equal to the number of operating conditions for which the PEX 8311 provides power information, this register returns all zeros (0h). The PEX 8311 supports 32 operating conditions.

Register 18-70. (Offset 108h; PWRDATA) Power Budgeting Data

Bits	Description	CFG	MM	EE	Default
7:0	**Base Power** Specifies (in Watts) the base power value in the given operating condition. This value must be multiplied by the data scale to produce the actual power consumption value.	RO	RW	WO	0h
9:8	**Data Scale** Specifies the scale to apply to the Base Power value. The PEX 8311 power consumption is determined by multiplying the *Base Power* field contents with the value corresponding to the encoding returned by this field. Defined encodings are as follows: **Value** **Scale Factor** **Value** **Scale Factor** 00b 1.0x 10b 0.01x 01b 0.1x 11b 0.001x	RO	RW	WO	00b
12:10	**PM Sub-State** Specifies the power management sub-state of the operating condition being described. Defined encodings are as follows: **Value** **Sub-State** 000b Default Sub-State All other values Device-Specific Sub-State	RO	RW	WO	000b
14:13	**PM State** Specifies the power management state of the operating condition being described. A device returns 11b in this field and Aux or PME Aux in the *PM Type* field to specify the D3cold PM state. An encoding of 11b along with any other *PM Type* field value specifies the D3hot state. Defined encodings are as follows: **Value** **PM State** **Value** **PM State** 00b D0 10b ***Reserved*** 01b D1 11b D3	RO	RW	WO	00b
17:15	**PM Type** Specifies the type of the operating condition being described. Defined encodings are as follows: **Value** **PM Type** **Value** **PM Type** 000b PME Aux 011b Sustained 001b Auxiliary 111b Maximum 010b Idle All other values ***Reserved***	RO	RW	WO	000b
20:18	**Power Rail** Specifies the power rail of the operating condition being described. Defined encodings are as follows: **Value** **Power Rail** **Value** **Power Rail** 000b Power (12V) 111b Thermal 001b Power (3.3V) All other values ***Reserved*** 010b Power (1.8V)	RO	RW	WO	000b
31:21	***Reserved***	RsvdP	RsvdP	–	0h

Register 18-71. (Offset 10Ch; PWRBUDCAP) Power Budget Capability

Bits	Description	CFG	MM	EE	Default
0	**System Allocated** When set, indicates that the device power budget is included within the system power budget. When set, software to ignore Reported Power Budgeting Data for power budgeting decisions.	RO	RW	WO	0
31:1	***Reserved***	RsvdP	RsvdP	–	0h

18.9.2 PCI Express Serial Number Registers

Register 18-72. (Offset 110h; SERCAPHDR) Serial Number Capability Header

Bits	Description	CFG	MM	EE	Default
15:0	**PCI Express Extended Capability ID** PCI-SIG-defined ID Number that indicates the nature and format of the extended capability. Forced to 0 when Serial Number Capability is disabled.	RO	RO	–	3h
19:16	**Capability Version** PCI-SIG-defined Version Number that indicates the version of the capability structure present. Forced to 0 when Serial Number Capability is disabled.	RO	RO	–	1h
31:20	**Next Capability Offset** Contains the offset to the next PCI Express capability structure or 000h when no other items exist in the New Capabilities Linked List.	RO	RO	–	000h

Register 18-73. (Offset 114h; SERNUMLOW) Serial Number Low (Lower DWORD)

Bits	Description	CFG	MM	EE	Default
31:0	**PCI Express Device Serial Number** Contains the lower DWORD of the IEEE-defined 64-bit extended unique identifier. Includes a 24-bit Company ID value assigned by the IEEE registration authority and a 40-bit extension identifier assigned by the manufacturer. Forced to 0 when Serial Number Capability is disabled.	RO	RW	WO	0h

Register 18-74. (Offset 118h; SERNUMHI) Serial Number Hi (Upper DWord)

Bits	Description	CFG	MM	EE	Default
31:0	**PCI Express Device Serial Number** Contains the upper DWORD of the IEEE-defined 64-bit extended unique identifier. This identifier includes a 24-bit Company ID value assigned by the IEEE registration authority and a 40-bit extension identifier assigned by the manufacturer. Forced to 0 when Serial Number Capability is disabled.	RO	RW	WO	0h

18.10 Main Control Registers

Register 18-75. (Offset 1000h; DEVINIT) Device Initialization

Bits	Description	Access	Default
3:0	**PCLKO Clock Frequency** Controls the PCLKO ball frequency. When cleared to 0000b, the clock is stopped and remains at a logic low. Non-zero values represent divisors of the 100-MHz REFCLK. The default value is 0011b, representing a frequency of 66 MHz. **Value** **Frequency (MHz)** 0000b 0 0001b 100 0010b 50 0011b 33.3/66 (PCLKO frequency is 66 MHz) 0100b 25 0101b 20 0110b 16.7 0111b 14.3 1000b 12.5 1001b 11.1 1010b 10 1011b 9.1 1100b 8.3 1101b 7.7 1110b 7.1 1111b 6.7	RW	0011b
4	**PCI Express Enable** When cleared, Configuration accesses to the PEX 8311 result in a completion status of Configuration Request Retry Status. When set, the PEX 8311 responds normally to PCI Express Configuration accesses. Automatically set when a valid serial EEPROM is not detected.	RW	0
5	**PCI Enable** When cleared, PCI accesses to the PEX 8311 result in a Target Retry response. When set, the PEX 8311 responds normally to PCI accesses. Automatically set when a valid serial EEPROM is not detected.	RW	0
31:6	***Reserved***	RsvdP	0h

Register 18-76. (Offset 1004h; EECTL) Serial EEPROM Control

Bits	Description	Access	Default
7:0	**Serial EEPROM Write Data** Determines the byte written to the serial EEPROM when the *Serial EEPROM Byte Write Start* bit is set. Represents an opcode, address, or data being written to the serial EEPROM.	RW	0h
15:8	**Serial EEPROM Read Data** Determines the byte read from the serial EEPROM when the *Serial EEPROM Byte Read Start* bit is set.	RO	–
16	**Serial EEPROM Byte Write Start** When set, the value in the *Serial EEPROM Write Data* field is written to the serial EEPROM. Automatically cleared when the Write operation is complete.	RW	0
17	**Serial EEPROM Byte Read Start** When set, a byte is read from the serial EEPROM, and is accessed using the *Serial EEPROM Read Data* field. Automatically cleared when the Read operation is complete.	RW	0
18	**Serial EEPROM Chip Select Enable** When set, the serial EEPROM Chip Select is enabled.	RW	0
19	**Serial EEPROM Busy** When set, the Serial EEPROM Controller is busy performing a Byte Read or Write operation. An interrupt can be generated when this bit goes false.	RO	0
20	**Serial EEPROM Valid** A serial EEPROM with 5Ah in the first byte is detected.	RO	–
21	**Serial EEPROM Present** Set when the Serial EEPROM Controller determines that a serial EEPROM is connected to the PEX 8311.	RO	–
22	**Serial EEPROM Chip Select Active** Set when the EECS# ball to the serial EEPROM is active. The Chip Select can be active across multiple byte operations.	RO	–
24:23	**Serial EEPROM Address Width** Reports the addressing width of the installed serial EEPROM. A non-zero value is reported only when the validation signature (5Ah) is successfully read from the first serial EEPROM location. If there is no serial EEPROM present, or if the first byte read is not a valid signature byte (5Ah), 0 is returned. ***Note: Programs that reference this value to determine the address width used for Serial EEPROM Writes do not function when a 0 value is read. To program a blank or corrupted serial EEPROM, programs must use either a user-entered or hardwired value.*** **Value** **Address Width** 00b Undetermined 01b 1 byte 10b 2 bytes 11b 3 bytes	RO	–
30:25	***Reserved***	RsvdP	0h
31	**Serial EEPROM Reload** Writing 1 to this bit causes the Serial EEPROM Controller to perform an initialization sequence. Configuration registers and shared memory are loaded from the serial EEPROM. Reading this bit returns 0 while the initialization is in progress, and 1 when initialization is complete.	RW	0

Register 18-77. (Offset 1008h; EECLKFREQ) Serial EEPROM Clock Frequency

Bits	Description	Access	Default
2:0	**Serial EEPROM Clock Frequency** Controls the EECLK ball frequency. **Value** **Frequency** 000b 2 MHz 001b 5 MHz 010b 8.3 MHz 011b 10 MHz 100b 12.5 MHz 101b 16.7 MHz 110b 25 MHz 111b ***Reserved***	RW	000b
31:3	***Reserved***	RsvdP	0h

Register 18-78. (Offset 100Ch; PCICTL) PCI Control

Bits	Description	Access	Default
0	**PCI Multi-Level Arbiter** When cleared, PCI requesters are placed into a single-level Round-Robin arbiter, each with equal access to the internal PCI Bus. When set, a two-level arbiter is selected.	RW	0
3:1	**Internal Arbiter Park Select** Determines which PCI master controller is granted the internal PCI Bus when there are no pending requests. **Value** **Park** 000b Last Grantee 001b PCI Express Interface 010b, 011b ***Reserved*** 100b External Requester 0 101b External Requester 1 110b External Requester 2 111b External Requester 3	RW	000b
4	**Bridge Mode** Reflects the ROOT_COMPLEX# ball status. When low, the PEX 8311 operates in Root Complex mode (Local-to-PCI Express). When high, the device operates in Endpoint mode (PCI Express-to-Local).	RO	–
5	***Reserved***	RO	0
6	**Locked Transaction Enable** When cleared, PCI Express Memory Read Locked requests are completed with UR status, and the internal LOCK# signal is not driven in Endpoint mode. In Root Complex mode, the internal LOCK# signal is ignored. When set, Locked transactions are propagated through the PEX 8311, from the Local Bus interface to the PCI Express interface.	RW	0
7	***Reserved***	RO	0

Register 18-78. (Offset 100Ch; PCICTL) PCI Control *(Cont.)*

Bits	Description	Access	Default
15:8	**PCI-to-PCI Express Retry Count** Valid only in Root Complex mode when the PCI Express link is down. Determines the number of times to Retry a PCI Type 1 Configuration transaction to PCI Express before aborting the transfer (in units of 2^{14} Retries). A value of 0h indicates that the transaction is Retried forever. A value of 255 selects a Retry count of 2^{24}. When the timer times out, a Master Abort is returned to the internal PCI Bus.	RW	80h
23:16	**PCI Express-to-PCI Retry Count** Determines the number of times to Retry a PCI Express-to-PCI transaction before aborting the transfer (in units of 2^{4} Retries). A value of 0h indicates that the transaction is Retried forever. A value of 255 selects a Retry count of 2^{24}.	RW	0h
24	**Memory Read Line Enable** When cleared, the PEX 8311 issues a Memory Read command for transactions that do not start on a cache boundary. When set, a Memory Read Line command is issued when a transaction is not aligned to a cache boundary, and the burst transfer size is at least one cache line of data. The PCI burst is stopped at the cache line boundary when the burst transfer size is less than one cache line of data or when a Memory Read Multiple command is started.	RW	1
25	**Memory Read Multiple Enable** When cleared, the PEX 8311 issues a Memory Read command for transactions that start on a cache boundary. When set, a Memory Read Multiple command is issued when a transaction is aligned to a cache boundary, and the burst transfer size is at least one cache line of data. The PCI burst continues when the Burst Transfer size remains greater than or equal to one cache line of data.	RW	1
26	**Early Byte Enables Expected** When cleared, the PEX 8311 accepts PCI Byte Enables that are not valid until IRDY# is asserted. When set, the PEX 8311 expects the PCI Byte Enables to be valid in the clock tick following the Address phase. For maximum compatibility with non-compliant PCI devices, clear this bit to 0. For maximum performance, set this bit to 1.	RW	0
29:27	**Programmed Prefetch Size** Valid only for Memory Read Line and Memory Read Multiple transactions, or Memory Read transactions with the **DEVSPECCTL** register *Blind Prefetch Enable* bit set. Determines the number of bytes requested from the PCI Express interface as a result of a PCI-to-PCI Express read. Enable feature only when the PCI initiator reads all requested data without disconnecting. Otherwise, performance is impacted. The Prefetch Size is limited by the **DEVCTL** register *Maximum Read Request Size* field. **Value** **Prefetch Size** 000b Disabled 001b 64 bytes 010b 128 bytes 011b 256 bytes 100b 512 bytes 101b 1,024 bytes 110b 2,048 bytes 111b 4,096 bytes (refer to Note) ***Note:*** *If the Programmed Prefetch Size is 4 KB, the* **TLP Controller Configuration 0** *register Limit Completion Flow Control Credit bit must be set.*	RW	000b
31:30	***Reserved***	RsvdP	00b

Register 18-79. (Offset 1010h; PCIEIRQENB) PCI Express Interrupt Request Enable

Bits	Description	Access	Default
0	**Serial EEPROM Done Interrupt Enable** When set, enables a PCI Express interrupt to generate when a serial EEPROM Read or Write transaction completes.	RW	0
1	**GPIO Interrupt Enable** When set, enables a PCI Express interrupt to generate when an interrupt is active from one of the GPIO balls.	RW	0
2	***Reserved***	RsvdP	0
3	**PCI Express-to-PCI Retry Interrupt Enable** When set, enables a PCI Express interrupt to generate when the PCI Express-to-PCI Retry Count is reached.	RW	0
4	**Mailbox 0 Interrupt Enable** When set, enables a PCI Express interrupt to generate when Mailbox 0 is written.	RW	0
5	**Mailbox 1 Interrupt Enable** When set, enables a PCI Express interrupt to generate when Mailbox 1 is written.	RW	0
6	**Mailbox 2 Interrupt Enable** When set, enables a PCI Express interrupt to generate when Mailbox 2 is written.	RW	0
7	**Mailbox 3 Interrupt Enable** When set, enables a PCI Express interrupt to generate when Mailbox 3 is written.	RW	0
30:8	***Reserved***	RsvdP	0h
31	**PCI Express Internal Interrupt Enable** When set, enables a PCI Express interrupt to generate as a result of an internal PEX 8311 interrupt source. The internal interrupt is serviced as either a Message Signaled Interrupt (MSI) or virtual wire interrupt.	RW	1 (E) 0 (RC)

Note: *In the **Default** column, "E" indicates Endpoint mode, and "RC" indicates Root Complex mode.*

Register 18-80. (Offset 1014h; PCIIRQENB) PCI Interrupt Request Enable

Bits	Description	Access	Default
0	**Serial EEPROM Done Interrupt Enable** When set, enables a PCI interrupt to generate when a serial EEPROM Read or Write transaction completes.	RW	0
1	**GPIO Interrupt Enable** When set, enables a PCI interrupt to generate when an interrupt is active from one of the GPIO balls.	RW	0
2	***Reserved***	RsvdP	0
3	**PCI Express-to-PCI Retry Interrupt Enable** When set, enables a PCI interrupt to generate when the PCI Express-to-PCI Retry Count is reached.	RW	0
4	**Mailbox 0 Interrupt Enable** When set, enables a PCI interrupt to generate when Mailbox 0 is written.	RW	0
5	**Mailbox 1 Interrupt Enable** When set, enables a PCI interrupt to generate when Mailbox 1 is written.	RW	0
6	**Mailbox 2 Interrupt Enable** When set, enables a PCI interrupt to generate when Mailbox 2 is written.	RW	0
7	**Mailbox 3 Interrupt Enable** When set, enables a PCI interrupt to generate when Mailbox 3 is written.	RW	0
8	**Unsupported Request Interrupt Enable** When set, enables a PCI interrupt to generate when an Unsupported Request Completion response is received from the PCI Express.	RW	0
30:9	***Reserved***	RsvdP	0h
31	**PCI Internal Interrupt Enable** When set, enables a PCI interrupt to generate as a result of an internal PEX 8311 interrupt source.	RW	0 (E) 1 (RC)

Note: *In the **Default** column, "E" indicates Endpoint mode, and "RC" indicates Root Complex mode.*

Register 18-81. (Offset 1018h; IRQSTAT) Interrupt Request Status

Bits	Description	Access	Default
0	**Serial EEPROM Done Interrupt** Set when a serial EEPROM Read or Write transaction completes. Writing 1 clears this status bit.	RW1C	0
1	**GPIO Interrupt** Conveys the interrupt status for the four GPIO balls. When set, the GPIO Status register is read to determine the cause of the interrupt. Set independently of the interrupt enable bit.	RO	0
2	***Reserved***	RsvdP	0
3	**PCI Express-to-PCI Retry Interrupt** Set when the PCI Express-to-PCI Retry Count is reached. Writing 1 clears this status bit.	RW1C	0
4	**Mailbox 0 Interrupt** Set when Mailbox 0 is written. Writing 1 clears this bit.	RW1C	0
5	**Mailbox 1 Interrupt** Set when Mailbox 1 is written. Writing 1 clears this bit.	RW1C	0
6	**Mailbox 2 Interrupt** Set when Mailbox 2 is written. Writing 1 clears this bit.	RW1C	0
7	**Mailbox 3 Interrupt** Set when Mailbox 3 is written. Writing 1 clears this bit.	RW1C	0
8	**Unsupported Request Interrupt** Set when an Unsupported Request Completion is received from the PCI Express. Writing 1 clears this bit	RW1C	0
31:9	***Reserved***	RsvdZ	0h

Register 18-82. (Offset 101Ch; POWER) Power (Endpoint Mode Only)

Bits	Description	Access	Default
7:0	**Power Compare 0** Specifies the power required for the PEX 8311 and downstream PCI devices in Endpoint mode. It is compared with the **DEVCAP** register *Captured Slot Power Limit Value* field. When the *Captured Slot Power Limit Value* is greater than or equal to this field, the PWR_OK signal is asserted. Used when the *Captured Slot Power Limit Scale* field is 00b (scale = 1.0x).	RW	0h
15:8	**Power Compare 1** Specifies the power required for the PEX 8311 and downstream PCI devices in Endpoint mode. It is compared with the **DEVCAP** register *Captured Slot Power Limit Value* field. When the *Captured Slot Power Limit Value* is greater than or equal to this field, the PWR_OK signal is asserted. Used when the *Captured Slot Power Limit Scale* field is 01b (scale = 0.1x).	RW	0h
23:16	**Power Compare 2** Specifies the power required for the PEX 8311 and downstream PCI devices in Endpoint mode. It is compared with the **DEVCAP** register *Captured Slot Power Limit Value* field. When the *Captured Slot Power Limit Value* is greater than or equal to this field, the PWR_OK signal is asserted. Used when the *Captured Slot Power Limit Scale* field is 10b (scale = 0.01x).	RW	0h
31:24	**Power Compare 3** Specifies the power required for the PEX 8311 and downstream PCI devices in Endpoint mode. It is compared with the **DEVCAP** register *Captured Slot Power Limit Value* field. When the *Captured Slot Power Limit Value* is greater than or equal to this field, the PWR_OK signal is asserted. Used when the *Captured Slot Power Limit Scale* field is 11b (scale = 0.001x).	RW	0h

Register 18-83. (Offset 1020h; GPIOCTL) General Purpose I/O Control

Bits	Description	Access	Default
0	**GPIO0 Data** When programmed as an output, values written to this bit appear on the GPIO0 ball. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO0 ball.	RW	0
1	**GPIO1 Data** When programmed as an output, values written to this bit appear on the GPIO1 ball. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO1 ball.	RW	0
2	**GPIO2 Data** When programmed as an output, values written to this bit appear on the GPIO2 ball. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO2 ball.	RW	0
3	**GPIO3 Data** When programmed as an output, values written to this bit appear on the GPIO3 ball. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO3 ball.	RW	0
4	**GPIO0 Output Enable** When cleared, the GPIO0 ball is an input. When set, the GPIO0 ball is an output. The *GPIO Diagnostic Select* field overrides this bit when a diagnostic output is selected.	RW	1
5	**GPIO1 Output Enable** When cleared, the GPIO1 ball is an input. When set, the GPIO1 ball is an output. The *GPIO Diagnostic Select* field overrides this bit when a diagnostic output is selected.	RW	0
6	**GPIO2 Output Enable** When cleared, the GPIO2 ball is an input. When set, the GPIO2 ball is an output. The *GPIO Diagnostic Select* field overrides this bit when a diagnostic output is selected.	RW	0
7	**GPIO3 Output Enable** When cleared, the GPIO3 ball is an input. When set, the GPIO3 ball is an output. The *GPIO Diagnostic Select* field overrides this bit when a diagnostic output is selected.	RW	0
8	**GPIO0 Interrupt Enable** When set, changes on the GPIO0 ball (when programmed as an input) are enabled to generate an interrupt.	RW	0
9	**GPIO1 Interrupt Enable** When set, changes on the GPIO1 ball (when programmed as an input) are enabled to generate an interrupt.	RW	0
10	**GPIO2 Interrupt Enable** When set, changes on the GPIO2 ball (when programmed as an input) are enabled to generate an interrupt.	RW	0
11	**GPIO3 Interrupt Enable** When set, changes on the GPIO3 ball (when programmed as an input) are enabled to generate an interrupt.	RW	0

Register 18-83. (Offset 1020h; GPIOCTL) General Purpose I/O Control *(Cont.)*

Bits	Description	Access	Default
13:12	**GPIO Diagnostic Select** Selects diagnostic signals that are output on the GPIO balls. **Value** **Description** 00b Normal GPIO operation 01b GPIO0 driven high when Link is up. GPIO[3:1] operate normally 10b GPIO[3:0] are driven with the lower four bits of the LTSSM state machine for 2s, alternating with GPIO[1:0] driven with the upper two bits of the LTSSM state machine for 1s 11b GPIO[3:0] driven with PMU Linkstate (L2, L1, L0s, and L0) **LTSSM Codes** 00h – L3_L2 (Fundamental Reset) 01h – Detect 02h – Polling.Active 03h – Polling.Configuration 04h – Polling.Compliance 05h – Configuration.Linkwidth.Start & Accept (Root Complex mode) 06h – Configuration.Lanenum.Wait & Accept (Root Complex mode) 07h – Configuration.Complete (Root Complex mode) 08h – Configuration.Idle (Root Complex mode) 09h – Configuration.Linkwidth.Start (Endpoint mode) 0Ah – Configuration.Linkwidth.Accept (Endpoint mode) 0Bh – Configuration.Lanenum.Wait & Accept (Endpoint mode) 0Ch – Configuration.Complete (Endpoint mode) 0Dh – Configuration.Idle (Endpoint mode) 0Eh – L0 0Fh – L0 (Transmit E.I.Ordered-set) 10h – L0 (Wait E.I.Ordered-set) 12h – L1.Idle 14h – L2.Idle 15h – Recovery.Rcvrlock (Extended Sync enabled) 16h – Recovery.Rcvrlock 17h – Recovery.RcvrCfg 18h – Recovery.Idle 19h – Disabled (Transmit TS1) 1Ah – Disabled (Transmit E.I.Ordered-set) 1Dh – Disabled (Wait Electrical Idle) 1Eh – Disabled (Disable) 1Fh – Loopback.Entry 20h – Loopback.Active 21h – Loopback.Exit 22h – Hot Reset (Wait TS1 with Hot Reset, Root Complex mode) 23h – Hot Reset (Reset Active) 24h – Loopback.Actice (Transmit E.I.Ordered-set) 25h – Loopback.Active (Wait Electrical Idle)	RW	01b
31:14	***Reserved***	RsvdP	0h

Register 18-84. (Offset 1024h; GPIOSTAT) General Purpose I/O Status

Bits	Description	Access	Default
0	**GPIO0 Interrupt** Set when the state of the GPIO0 ball changes and the ball is programmed as an input. Writing 1 clears this bit.	RW1C	0
1	**GPIO1 Interrupt** Set when the state of the GPIO1 ball changes and the ball is programmed as an input. Writing 1 clears this bit.	RW1C	0
2	**GPIO2 Interrupt** Set when the state of the GPIO2 ball changes and the ball is programmed as an input. Writing 1 clears this bit.	RW1C	0
3	**GPIO3 Interrupt** Set when the state of the GPIO3 ball changes and the ball is programmed as an input. Writing 1 clears this bit.	RW1C	0
31:4	***Reserved***	RsvdZ	0h

Register 18-85. (Offset 1030h; MAILBOX 0) Mailbox 0

Bits	Description	Access	Default
31:0	**Mailbox Data** Written or read from the PCI Express interface or Local Bus. Interrupts are generated to either interface when this register is written.	RW	FEEDFACEh

Register 18-86. (Offset 1034h; MAILBOX 1) Mailbox 1

Bits	Description	Access	Default
31:0	**Mailbox Data** Written or read from the PCI Express interface or Local Bus. Interrupts are generated to either interface when this register is written.	RW	0h

Register 18-87. (Offset 1038h; MAILBOX 2) Mailbox 2

Bits	Description	Access	Default
31:0	**Mailbox Data** Written or read from the PCI Express interface or Local Bus. Interrupts are generated to either interface when this register is written.	RW	0h

Register 18-88. (Offset 103Ch; MAILBOX 3) Mailbox 3

Bits	Description	Access	Default
31:0	**Mailbox Data** Written or read from the PCI Express interface or Local Bus. Interrupts are generated to either interface when this register is written.	RW	0h

Register 18-89. (Offset 1040h; CHIPREV) Chip Silicon Revision

Bits	Description	Access	Default
15:0	**Chip Revision** Returns the current PEX 8311 silicon revision number.	RO	Current Revision
31:16	***Reserved***	RsvdP	0h

Note: *CHIPREV is the silicon revision, encoded as a 4-digit BCD value. The value of CHIPREV for the first release of the bridge (Rev. AA) is 0201h. The least-significant digit is incremented for mask changes, and the most-significant digit is incremented for major revisions.*

Register 18-90. (Offset 1044h; DIAG) Diagnostic Control *(Factory Test Only)*

Bits	Description	Access	Default
0	**Fast Times** When set, internal timers and counters operate at a fast speed for factory testing.	RW	0
1	**Force PCI Interrupt** When set, this bit forces the PCI INTA# interrupt signal to assert. Effective only when the **PCI Command** register *Interrupt Disable* bit is low.	RW	0
2	**Force Internal SERR#** When set, this bit forces the internal SERR# interrupt signal to assert when the **PCI Command** register *Internal SERR# Enable* bit is set (Root Complex mode). In Endpoint mode, the **Bridge Control** register *Secondary Internal SERR# Enable* bit must be set.	RW	0
3	**Force PCI Express Interrupt** When set, this bit forces an interrupt to the PCI Express Root Complex using Message Signaled Interrupts or virtual wire INTA# interrupts.	RW	0
31:4	***Reserved***	RsvdP	0h

Register 18-91. (Offset 1048h; TLPCFG0) TLP Controller Configuration 0

Bits	Description	Access	Default
7:0	**CFG_NUM_FTS** Forced NUM_FTS signal. [*NUM_FTS* is the number of Fast Training sequence (0 to 255)]. For detailed information, refer to the *PCI Express Base 1.0a*, Section 4.2.4.3.	RW	20h
8	**CFG_ACK_FMODE** PCI Express core ACK_DLLP transmitting interval mode. 0 = Core hardware uses own interval value 1 = Core hardware uses *CFG_ACK_COUNT* as interval value	RW	0
9	**CFG_TO_FMODE** PCI Express core Timeout detection mode for Replay Timer. 0 = Core hardware uses own timer value 1 = Core hardware uses *CFG_TO_COUNT* as timer value	RW	0
10	**CFG_PORT_DISABLE** When set, the PCI Express interface is disabled. This allows the endpoint to disable the PCI Express connection when powered up or before the configuration is complete.	RW	0
11	**CFG_RCV_DETECT** Asserted when the PCI Express core establishes the PCI Express connection.	RO	0

Register 18-91. (Offset 1048h; TLPCFG0) TLP Controller Configuration 0 *(Cont.)*

Bits	Description	Access	Default
12	**CFG_LPB_MODE** Link Loop-Back mode.	RW	0
13	**CFG_PORT_MODE** When cleared, Link core is configured as an upstream port (Endpoint mode). When set, Link core is configured as a downstream port (Root Complex mode).	RW	0 (E) 1 (RC)
14	***Reserved***	RsvdP	0
15	**CFG_ECRC_GEN_ENABLE** ***Not supported.*** When set, link is allowed generate End-to-end Cyclic Redundancy Check (ECRC). The PEX 8311 does not support ECRC; therefore, clear this bit to 0.	RW	0
16	**TLB_CPLD_NOSUCCESS_MALFORM_ENABLE** When cleared, received completion is retained. When set, completion received when completion timeout expired is treated as a malformed TLB and is discarded.	RW	1
17	**Scrambler Disable** When cleared, data scrambling is enabled. When set, data scrambling is disabled. Only set for testing and debugging.	RW	0
18	**Delay Link Training** When cleared, link training is allowed to commence immediately after reset is de-asserted. When set, link training is delayed for 12 ms after reset is de-asserted. Automatically set when GPIO3 is low during reset.	RW	0
19	**Decode Primary Bus Number** When cleared, the PEX 8311 ignores the Primary Bus Number in a PCI Express Type 0 Configuration Request. When set, the PEX 8311 compares the Primary Bus Number in a PCI Express Type 0 Configuration Request with the **Primary Bus Number** register. When they match, the request is accepted. Otherwise, an Unsupported Request is returned. This comparison occurs only after the first Type 0 Configuration write occurs.	RW	0
20	**Ignore Function Number** When cleared, the PEX 8311 only responds to Function Number 0 during a Type 0 Configuration transaction. Accesses to other function numbers result in an Unsupported Request (PCI Express) or Master Abort (PCI). When set, the PEX 8311 ignores the Function Number in a PCI or PCI Express Type 0 Configuration Request, and responds to all eight functions.	RW	0
21	**Check RCB Boundary** When cleared, the PEX 8311 ignores Read Completion Boundary (RCB) violations. When set, the PEX 8311 checks for RCB violations. When detected, the PEX 8311 treats it as a malformed TLP (packet is dropped and a Non-Fatal Error message is transmitted).	RW	0
22	**Limit Completion Flow Control Credit** When cleared, the PEX 8311 advertises infinite flow control credits for completions. When set, the PEX 8311advertises completion flow control credits, based on available FIFO storage. This bit must be set when the **PCI Control** register *Programmed Prefetch Size* field is set to 4 KB. When GPIO2 is low during reset, this bit is automatically set. Because this bit is used during link training, it must be set by driving GPIO2 low during reset.	RW	0
23	**L2 Secondary Bus Reset** When clear and the PEX 8311 is in the L2/L3 Ready state in Root Complex mode, PCI-to-PCI Express Configuration transactions are Retried until the P2PE_RETRY_COUNT expires. The PEX 8311 then responds with a Master Abort. When set, and the PEX 8311 is in the L2/L3 Ready state in Root Complex mode, PCI-to-PCI Express Configuration transactions result in a Local Bus interface reset (Endpoint mode) or PCI Express interface reset (Root Complex mode). After the link training completes, the PCI-to-PCI Express Configuration transaction completes normally.	RW	1
31:24	***Reserved***	RsvdP	0h

Note: *In the **Default** column, "E" indicates Endpoint mode, and "RC" indicates Root Complex mode.*

Register 18-92. (Offset 104Ch; TLPCFG1) TLP Controller Configuration 1

Bits	Description	Access	Default
20:0	**CFG_TO_COUNT** PCI Express core replay timer timeout value when *CFG_TO_FMODE* is set to 1.	RW	D4h
30:21	**CFG_ACK_COUNT** PCI Express core ACK DLLP transmitting interval value when *CFG_ACK_MODE* is set to 1.	RW	0h
31	***Reserved***	RsvdP	0

Register 18-93. (Offset 1050h; TLPCFG2) TLP Controller Configuration 2

Bits	Description	Access	Default
15:0	**CFG_COMPLETER_ID0** Bits [15:8] – Bus number Bits [7:3] – Device number Bits [2:0] – Function number When TLB0_TRANS is asserted with a Type 0 Configuration Cycle, this signal latches CFG_TLB0_BUS_NUMBER[7:0] and CFG_TLB0_DEV_NUMBER[4:0] into the corresponding bits.	RW	0h
26:16	**Update Credit FC** Controls a counter that determines the gap between UpdateFC DLLPs (in units of 62.5 MHz clocks = 16 ns = 4 symbol times). When data or headers are read from the TLP Controller, the Credit Allocation Manager transmits a set of UpdateFC DLLPs; posted, non-posted, and completion when the **TLPCFG0** register *Limit Completion Flow Control Credit* bit is set. While transmitting the set of DLLPs, the Credit Allocation Manager uses the counter value to insert gaps between the DLLPs.	RW	1h
31:27	***Reserved***	RsvdP	0h

Register 18-94. (Offset 1054h; TLPTAG) TLP Controller Tag

Bits	Description	Access	Default
7:0	**TAG BME1** Message Request tag field.	RW	0h
15:8	**TAG ERM** Error Manager tag field.	RW	0h
23:16	**TAG PME** Power Manager tag field.	RW	0h
31:24	***Reserved***	RsvdP	0h

Register 18-95. (Offset 1058h; TLPTIMELIMIT0) TLP Controller Time Limit 0

Bits	Description	Access	Default
23:0	**BME_COMPLETION_TIMEOUT_LIMIT** Bus master engine completion timeout (in units of internal clocks). The default value produces a 10-ms timeout.	RW	A2C2Ah
27:24	**L2L3_PWR_REMOVAL_TIME_LIMIT** This value determines the amount of time before power is removed after entering the L2 state (in units of internal clocks). Enter this value as at least 100 ns.	RW	8h
31:28	***Reserved***	RsvdP	0h

Register 18-96. (Offset 105Ch; TLPTIMELIMIT1) TLP Controller Time Limit 1

Bits	Description	Access	Default
10:0	**ASPM_LI_DLLP_INTERVAL_TIME_LIMIT** Determines the time interval between two consecutive PM_ACTIVE_STATE_REQUEST_L1 DLLP transmissions (in units of internal clocks). Allow at least 10 µs spent in LTSSM L0 and L0s state before the next PM_ACTIVE_STATE_REQUEST_L1 DLLP is transmitted. Detailed information is in the *PCI Express Base 1.0a Errata*, page 19.	RW	29Ah
31:11	***Reserved***	RsvdP	0h

Register 18-97. (Offset 1060h; CRSTIMER) CRS Timer

Bits	Description	Access	Default
15:0	**CRS Timer** Valid only in Endpoint mode when the **DEVCTL** register *Bridge Configuration Retry Enable* bit is set. Determines the amount of microseconds to wait before returning a completion with CRS status in response to a PCI Express-to-PCI Configuration transaction. When the timer times out and the completion with CRS status is returned, the transaction is discarded from the Non-Posted Transaction queue.	RW	25d
31:16	***Reserved***	RsvdP	0h

Register 18-98. (Offset 1064h; ECFGADDR) Enhanced Configuration Address

Bits	Description	Access	Default
11:0	***Reserved***	RsvdP	0h
14:12	**Configuration Function Number** Provides the Function Number for an enhanced Configuration transaction.	RW	000b
19:15	**Configuration Device Number** Provides the Device Number for an enhanced Configuration transaction.	RW	0h
27:20	**Configuration Bus Number** Provides the Bus Number for an enhanced Configuration transaction.	RW	0h
30:28	***Reserved***	RsvdP	0h
31	**Enhanced Configuration Enable** When cleared, accesses to Base Address 0 register, offset 2000h, are not responded to by the PEX 8311. When set, accesses to Base Address 0 register, offset 2000h, are forwarded to the PCI Express interface as a Configuration Request. Used only in Root Complex mode.	RW	0

Chapter 19 Local Configuration Space Registers

19.1 Introduction

This chapter describes the Local Configuration Space (**LCS**) register set. PCI Express Configuration Space (**PECS**) registers are described in Chapter 18, "PCI Express Configuration Registers."

19.2 Register Description

The **LCS PCI** registers are accessed from the PCI Express interface, using Type 1 Configuration accesses (PCI Express Type 1 accesses are internally converted to Type 0). The remainder of the **LCS Local**, **Runtime**, **DMA**, and **Messaging Queue** registers are accessed from the PCI Express interface, using Memory- or I/O-Mapped accesses through the **LCS PCIBAR0** or **PCIBAR1** registers, respectively. **LCS** registers are accessed directly by the Local Bus Master in Endpoint or Root Complex mode, by way of Direct Master accesses.

In Root Complex mode, a Local Bus Master cannot access the **PCI Express Extended Capability** registers by way of PCI Configuration transactions.

When the **Configuration** registers are accessed using Memory transactions to the **PECS Base Address 0** register, the address mapping delineated in Table 19-1 is used.

The PCI Express interface Serial EEPROM Controller can write to any of the Configuration registers. An upper Address bit is used to select one of the two register spaces delineated in Table 19-2.

Each register is 32 bits wide, and accessed one byte, word, or DWORD at a time. These registers utilize Little Endian Byte Ordering, which is consistent with the *PCI r2.2*. The least significant byte in a DWORD is accessed at Address 0. The least significant bit in a DWORD is 0, and the most significant bit is 31.

After the PEX 8311 is powered up or reset, the registers are set to their default values. Writes to unused registers are ignored, and reads from unused registers return a value of 0.

PCI Express Configuration Space (**PECS**) registers are described in Chapter 18, "PCI Express Configuration Registers."

Table 19-1. PCI Base Address 0 Register Address Mapping

Address Offset	Register Space
0000h - 0FFFh	PCI-Compatible Configuration registers
1000h - 1FFFh	Main Configuration registers
2000h - 2FFFh	Memory-Mapped indirect access to downstream PCI Express Endpoint registers (Root Complex mode only)
8000h - 9FFFh	8-KB internal shared memory

Table 19-2. Selecting Register Space

Internal AD12	Register Space
0	PCI-Compatible Configuration registers
1	Main Configuration registers

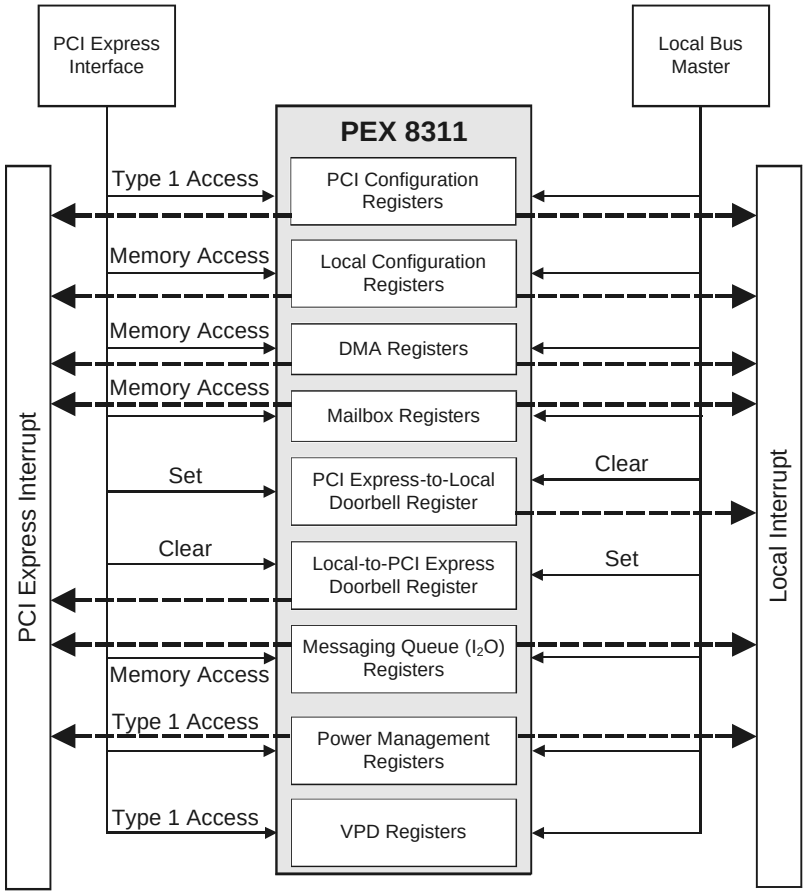
19.3 PEX 8311 Local Configuration Space

19.3.1 Local Configuration Space Access

The PEX 8311 **LCS** internal registers provide maximum flexibility in bus-interface control and performance. These registers are accessible from the PCI Express interface and Local Bus (refer to Figure 19-1) and include the following:

- PCI Configuration
- Local Configuration
- DMA
- Mailbox
- PCI-to-Local and Local-to-PCI Doorbell
- Messaging Queue (I_2O)
- Power Management
- Hot Swap (***Reserved***)
- VPD

Figure 19-1. PEX 8311 Internal Local Configuration Space Register Accesses



19.3.2 New Capabilities Function Support

The New Capabilities Function Support includes PCI Power Management, Hot Swap, and VPD features, as delineated in Table 19-3.

Note: *Although the PEX 8311 provides Hot Swap configuration registers, the Hot Swap feature is* ***not supported****.*

When a New Capabilities Function is not used and passed over in the Capability Pointer's linked list, the unused New Capabilities Function registers are set to default values.

Table 19-3. New Capabilities Function Support Features in Local Configuration Space PCI Registers

New Capability Function	PCI Register Offset Location
First (Power Management)	40h, when the New Capabilities Function Support bit is enabled (PCISR[4]=1; default). (Refer to Chapter 12, "Power Management," for details about this feature.)
Second (Hot Swap)	***Not supported.*** 48h, which is pointed to from PMNEXT[7:0].
Third (VPD)	4Ch, which is pointed to from HS_NEXT[7:0]. Because PVPD_NEXT[7:0] defaults to 0h, this indicates that VPD is the last New Capability Function Support feature of the PEX 8311. [Refer to Chapter 16, "Vital Product Data (VPD)," for details about this feature.]

19.3.3 Local Bus Access to Local Configuration Space Registers

The Local Bus Master can access PEX 8311 internal **LCS** registers through an external Chip Select. The PEX 8311 responds to a Local Bus access when the PEX 8311 Configuration Chip Select input (CCS#) is asserted low during the Address phase.

Local Read or Write accesses to the PEX 8311 internal registers are Byte, Word, or DWord accesses. Local accesses to the PEX 8311 internal registers are Burst or Non-Burst accesses.

The READY# signal indicates that the Data transfer is complete.

19.4 Local Configuration Space Register Address Mapping

Table 19-4. PCI Configuration Register Address Mapping

PCI Configuration Register Address	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PEX 8311 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 30 24 23 16 15 8 7 0				PCI/Local Writable	Serial EEPROM Writable
00h	00h	PCI Device ID		PCI Vendor ID		Local	Yes
04h	04h	PCI Status		PCI Command		Yes	No
08h	08h	PCI Class Code			PCI Revision ID	Local	Yes
0Ch	0Ch	PCI Built-In Self-Test	PCI Header Type	Internal PCI Bus Latency Timer	PCI Cache Line Size	Yes	No
10h	10h	PCI Base Address for Memory Accesses to Local, Runtime, DMA, and Messaging Queue Registers (PCIBAR0)				Yes	No
14h	14h	PCI Base Address for I/O Accesses to Local, Runtime, DMA, and Messaging Queue Registers (PCIBAR1)				Yes	No
18h	18h	PCI Base Address for Accesses to Local Address Space 0 (PCIBAR2)				Yes	No
1Ch	1Ch	PCI Base Address for Accesses to Local Address Space 1 (PCIBAR3)				Yes	No
20h	20h	PCI Base Address 4 ***(Reserved)***				No	No
24h	24h	PCI Base Address 5 ***(Reserved)***				No	No
28h	28h	PCI Cardbus Information Structure (CIS) Pointer ***(Not Supported)***				No	No
2Ch	2Ch	PCI Subsystem ID		PCI Subsystem Vendor ID		Local	Yes
30h	30h	PCI Base Address for Local Expansion ROM				Yes	No
34h	34h	***Reserved***			New Capability Pointer	Local	No
38h	38h	***Reserved***				No	No
3Ch	3Ch	PCI Maximum Latency	PCI Minimum Grant	Internal PCI Interrupt Wire	Internal PCI Interrupt Line	Yes	Yes
40h	180h	Power Management Capabilities		Power Management Next Capability Pointer	Power Management Capability ID	Local [31:21, 19:8]	Yes [31:25, 18:16]
44h	184h	Power Management Data	PMCSR Bridge Support Extensions ***(Reserved)***	Power Management Control/ Status		PCI [15, 12:8, 1:0], Local [31:24, 15:8, 1:0]	Yes [31:24, 14:8]
48h	188h	***Reserved***	Hot Swap Control/Status ***(Not Supported)***	Hot Swap Next Capability Pointer ***(Not Supported)***	Hot Swap Control (Capability ID) ***(Not Supported)***	PCI [23:22, 19, 17], Local [23:22, 17, 15:0]	Yes [15:0]

Table 19-4. PCI Configuration Register Address Mapping *(Cont.)*

PCI Configuration Register Address	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PEX 8311 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 30 24 23 16 15 8 7 0				PCI/Local Writable	Serial EEPROM Writable
4Ch	18Ch	F	PCI VPD Address	PCI VPD Next Capability Pointer	PCI VPD Capability ID	PCI [31:16], Local [31:8]	No
50h	190h	PCI VPD Data				Yes	No

Notes: *Refer to PCI r2.2 for definitions of the registers listed in this table.*

Where Writable bit numbers are not listed, refer to the individual register descriptions to determine which bits are writable.

Table 19-5. Local Configuration Register Address Mapping

PCI (Offset from Base Address)	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PEX 8311 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 24 23 16 15 8 7 0	PCI/Local Writable	Serial EEPROM Writable
00h	80h	Direct Slave Local Address Space 0 Range	Yes	Yes
04h	84h	Direct Slave Local Address Space 0 Local Base Address (Remap)	Yes	Yes
08h	88h	Mode/DMA Arbitration	Yes	Yes
0Ch	8Ch	Local Miscellaneous Control 2 | Serial EEPROM Write-Protected Address Boundary | Local Miscellaneous Control 1 | Big/Little Endian Descriptor	Yes	Yes
10h	90h	Direct Slave Expansion ROM Range	Yes	Yes
14h	94h	Direct Slave Expansion ROM Local Base Address (Remap) and BREQo Control	Yes	Yes
18h	98h	Local Address Space 0/Expansion ROM Bus Region Descriptor	Yes	Yes
1Ch	9Ch	Local Range for Direct Master-to-PCI	Yes	Yes
20h	A0h	Local Base Address for Direct Master-to-PCI Memory	Yes	Yes
24h	A4h	Local Base Address for Direct Master-to-PCI I/O Configuration	Yes	Yes
28h	A8h	PCI Base Address (Remap) for Direct Master-to-PCI Memory	Yes	Yes
2Ch	ACh	PCI Configuration Address for Direct Master-to-PCI I/O Configuration	Yes	Yes
F0h	170h	Direct Slave Local Address Space 1 Range	Yes	Yes
F4h	174h	Direct Slave Local Address Space 1 Local Base Address (Remap)	Yes	Yes
F8h	178h	Local Address Space 1 Bus Region Descriptor	Yes	Yes
FCh	17Ch	Direct Master PCI Dual Address Cycles Upper Address	Yes	No
100h	1A0h	Internal Arbiter Control	Yes	Yes
104h	1A4h	PCI Abort Address	No	No

Notes: *PCI offset registers 100h and 104h are accessible only by way of the PCIBAR0 register.*

Refer to the individual register descriptions to determine which bits are writable.

Table 19-6. Runtime Register Address Mapping

PCI (Offset from Base Address)	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PEX 8311 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 16 15 8 7 0	PCI/Local Writable	Serial EEPROM Writable
40h	C0h	Mailbox 0 (refer to Notes)	Yes	Yes
44h	C4h	Mailbox 1 (refer to Notes)	Yes	Yes
48h	C8h	Mailbox 2	Yes	No
4Ch	CCh	Mailbox 3	Yes	No
50h	D0h	Mailbox 4	Yes	No
54h	D4h	Mailbox 5	Yes	No
58h	D8h	Mailbox 6	Yes	No
5Ch	DCh	Mailbox 7	Yes	No
60h	E0h	PCI-to-Local Doorbell	Yes	No
64h	E4h	Local-to-PCI Doorbell	Yes	No
68h	E8h	Interrupt Control/Status	Yes	No
6Ch	ECh	Serial EEPROM Control, PCI Command Codes, User I/O Control, and Init Control	Yes	No
70h	F0h	Device ID | Vendor ID	No	No
74h	F4h	***Reserved*** | Revision ID	No	No
78h	C0h	Mailbox 0 (refer to Notes)	Yes	Yes
7Ch	C4h	Mailbox 1 (refer to Notes)	Yes	Yes

Notes: *The Mailbox 0 register (MBOX0) is always accessible at PCI address 78h, Local address C0h. The Mailbox 1 register (MBOX1) is always accessible at PCI address 7Ch, Local address C4h.*

When I_2O Decode is disabled (QSR[0]=0), MBOX0 and MBOX1 are also accessible at PCI addresses 40h and 44h for PCI 9054 compatibility. When I_2O Decode is enabled (QSR[0]=1), the Inbound and Outbound Queue pointers are accessed at PCI addresses 40h and 44h, replacing MBOX0 and MBOX1 in PCI Address space.

Refer to the individual register descriptions to determine which bits are writable.

Table 19-7. DMA Register Address Mapping

PCI (Offset from Base Address)	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PEX 8311 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 16 15 8 7 0	PCI/Local Writable	Serial EEPROM Writable
80h	100h	DMA Channel 0 Mode	Yes	No
84h/88h‡	104h/108h‡	DMA Channel 0 PCI Address	Yes	No
88h/8Ch‡	108h/10Ch‡	DMA Channel 0 Local Address	Yes	No
8Ch/84h‡	10Ch/104h‡	DMA Channel 0 Transfer Size (Bytes)	Yes	No
90h	110h	DMA Channel 0 Descriptor Pointer	Yes	No
94h	114h	DMA Channel 1 Mode	Yes	No
98h/9Ch‡	118h/11Ch‡	DMA Channel 1 PCI Address	Yes	No
9Ch/A0h‡	11Ch/120h‡	DMA Channel 1 Local Address	Yes	No
A0h/98h‡	120h/118h‡	DMA Channel 1 Transfer Size (Bytes)	Yes	No
A4h	124h	DMA Channel 1 Descriptor Pointer	Yes	No
A8h	128h	***Reserved*** | DMA Channel 1 Command/ Status | DMA Channel 0 Command/ Status	Yes	No
ACh	12Ch	DMA Arbitration	Yes	Yes
B0h	130h	DMA Threshold	Yes	No
B4h	134h	DMA Channel 0 PCI Dual Address Cycles Upper Address	Yes	No
B8h	138h	DMA Channel 1 PCI Dual Address Cycles Upper Address	Yes	No

Notes: *‡ PCI and Local Configuration offset depends upon the DMAMODEx[20] setting(s).*

Refer to the individual register descriptions to determine which bits are writable.

Table 19-8. Messaging Queue (I_2O) Register Address Mapping

PCI (Offset from Base Address)	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PEX 8311 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 0	PCI/Local Writable	Serial EEPROM Writable
30h	B0h	Outbound Post Queue Interrupt Status	No	No
34h	B4h	Outbound Post Queue Interrupt Mask	Yes	No
40h	–	Inbound Queue Port	PCI	No
44h	–	Outbound Queue Port	PCI	No
C0h	140h	Messaging Queue Configuration	Yes	No
C4h	144h	Queue Base Address	Yes	No
C8h	148h	Inbound Free Head Pointer	Yes	No
CCh	14Ch	Inbound Free Tail Pointer	Yes	No
D0h	150h	Inbound Post Head Pointer	Yes	No
D4h	154h	Inbound Post Tail Pointer	Yes	No
D8h	158h	Outbound Free Head Pointer	Yes	No
DCh	15Ch	Outbound Free Tail Pointer	Yes	No
E0h	160h	Outbound Post Head Pointer	Yes	No
E4h	164h	Outbound Post Tail Pointer	Yes	No
E8h	168h	Queue Status/Control	Yes	No

Notes: *When I_2O Decode is enabled (**QSR**[0]=1), the PCI Express Root Complex or other IOP uses the Inbound Queue Port to read Message Frame Addresses (MFAs) from the Inbound Free List FIFO and to write MFAs to the Inbound Post Queue FIFO. The Outbound Queue Port reads MFAs from the Outbound Post Queue FIFO and writes MFAs to the Outbound Free List FIFO.*

*Each Inbound MFA is specified by I_2O as an offset from the PCI Memory Base Address (programmed in **LCS PCIBAR0**) to the start of the message frame. That is, all inbound message frames reside in **PCIBAR0** Memory space.*

Each Outbound MFA is specified by I_2O as an offset from system address 00000000h. Outbound MFA is a physical 32-bit address of the frame in shared PCI Express system memory.

The Inbound and Outbound Queues can reside in Local Address Space 0 or Space 1 by programming QSR. The queues need not be in shared memory.

Refer to the individual register descriptions to determine which bits are writable.

19.5 Local Configuration Space PCI Configuration Registers

Notes: *All registers can be written to or read from in Byte, Word, or Dword accesses.*

"Yes" in the register Read and Write columns indicates the register is writable by the PCI Express interface and Local Bus.

Register 19-1. (PCIIDR; PCI:00h, LOC:00h) PCI Configuration ID

Bits	Description	Read	Write	Default
15:0	**Vendor ID** Identifies the device manufacturer. Defaults to the PLX PCI-SIG-issued Vendor ID, 10B5h, when the serial EEPROM is blank, or no serial EEPROM is present.	Yes	Local/ Serial EEPROM	10B5h
31:16	**Device ID** Identifies the particular device. Defaults to 9056h when the serial EEPROM is blank, or no serial EEPROM is present.	Yes	Local/ Serial EEPROM	9056h

Register 19-2. (PCICR; PCI:04h, LOC:04h) PCI Command

Bits	Description	Read	Write	Default
0	**I/O Space** Writing 0 disables the PEX 8311 from responding to I/O Space accesses. Writing 1 allows the PEX 8311 to respond to I/O Space accesses.	Yes	Yes	0
1	**Memory Space** Writing 0 disables the PEX 8311 from responding to Memory Space accesses. Writing 1 allows the PEX 8311 to respond to Memory Space accesses.	Yes	Yes	0
2	**Master Enable** Writing 0 disables the PEX 8311 from generating Bus Master accesses. Writing 1 allows the PEX 8311 to behave as a Bus Master.	Yes	Yes	0
3	**Special Cycle** ***Not supported.***	Yes	No	0
4	**Memory Write and Invalidate Enable** Writing 1 enables the Memory Write and Invalidate mode for Direct Master and DMA. ***Note:*** *Refer to DMPBAM[9] for Direct Master and DMAMODEx[13] for DMA.*	Yes	Yes	0
5	**VGA Palette Snoop** ***Not supported.***	Yes	No	0
6	**Parity Error Response** Writing 0 disables internal PERR# from being asserted when a Parity error is detected. Writing 1 enables internal PERR# to assert when a Parity error is detected. Parity error status is reported in PCISR[15], regardless of this bit's value.	Yes	Yes	0
7	**Stepping Control** Controls whether the PEX 8311 does address/data stepping. Writing 0 indicates the PEX 8311 never does stepping. Writing 1 indicates the PEX 8311 always does stepping. ***Note:*** *Hardwired to 0.*	Yes	No	0
8	**Internal SERR# Enable** Writing 0 disables the internal SERR# driver. Writing 1 enables the internal SERR# driver.	Yes	Yes	0
9	**Fast Back-to-Back Enable** Indicates what type of fast back-to-back transfers a Master can perform on the bus. Writing 0 indicates fast back-to-back transfers can occur only to the same agent as in the previous cycle. Writing 1 indicates fast back-to-back transfers can occur to any agent on the bus. ***Note:*** *Hardwired to 0.*	Yes	No	0
15:10	***Reserved***	Yes	No	0h

Register 19-3. (PCISR; PCI:06h, LOC:06h) PCI Status

Bits	Description	Read	Write	Default
3:0	***Reserved***	Yes	No	0h
4	**New Capability Functions Support** Writing 1 supports New Capabilities Functions. When enabled, the first New Capability Function ID is located at the PCI Configuration Space offset determined by the New Capabilities linked list pointer value at offset 34h. Can be written only from the Local Bus. Read-Only from the internal PCI Bus.	Yes	Local	1
5	**66 MHz-Capable** When set to 1, the PEX 8311 supports a 66-MHz internal clock environment.	Yes	Local	1
6	***Reserved***	Yes	No	0
7	**Fast Back-to-Back Capable** Writing 1 indicates an adapter can accept Fast Back-to-Back transactions. ***Note:*** *Hardwired to 1.*	Yes	No	1
8	**Master Data Parity Error** Set to 1 when the following three conditions are met: • Internal PERR# is asserted; • PEX 8311 was internal Bus Master for operation in which error occurred; and • *Parity Error Response* bit is set (PCICR[6]=1). Writing 1 clears this bit to 0.	Yes	Yes/Clr	0
10:9	**DEVSEL Timing** Indicates timing for DEVSEL# assertion. Writing 01b sets these bits to medium. ***Note:*** *Hardwired to 01b.*	Yes	No	01b
11	**Signaled Target Abort** When set to 1, indicates the PEX 8311 signaled an internal Target Abort. Writing 1 clears this bit to 0.	Yes	Yes/Clr	0
12	**Received Target Abort** When set to 1, indicates the PEX 8311 received an internal Target Abort signal. Writing 1 clears this bit to 0.	Yes	Yes/Clr	0
13	**Received Master Abort** When set to 1, indicates the PEX 8311 received an internal Master Abort signal. Writing 1 clears this bit to 0.	Yes	Yes/Clr	0
14	**Signaled System Error (Internal SERR# Status)** When set to 1, indicates the PEX 8311 reported an internal System error on internal SERR#. Writing 1 clears this bit to 0.	Yes	Yes/Clr	0
15	**Detected Parity Error** When set to 1, indicates the PEX 8311 has detected an internal PCI Bus Parity error internally, regardless of whether Parity error handling is disabled [the *Parity Error Response* bit in the **Command** register is clear (PCICR[6]=0)]. One of three conditions can cause this bit to be set when the PEX 8311 detects a Parity error during: • PCI Address phase • PCI Data phase when the PEX 8311 is the Target of a write • Direct Master or DMA Read operation Writing 1 clears this bit to 0.	Yes	Yes/Clr	0

Register 19-4. (PCIREV; PCI:08h, LOC:08h) PCI Revision ID

Bits	Description	Read	Write	Default
7:0	**Revision ID** Silicon revision of the PEX 8311 Local Bus Logic.	Yes	Local/ Serial EEPROM	Current Rev # (AAh)

Register 19-5. (PCICCR; PCI:09-0Bh, LOC:09-0Bh) PCI Class Code

Bits	Description	Read	Write	Default
7:0	**Register Level Programming Interface** None defined.	Yes	Local/ Serial EEPROM	0h
15:8	**Subclass Code (Other Bridge Device)**	Yes	Local/ Serial EEPROM	80h
23:16	**Base Class Code (Bridge Device)**	Yes	Local/ Serial EEPROM	06h

Register 116. (PCICLSR; PCI:0Ch, LOC:0Ch) PCI Cache Line Size

Bits	Description	Read	Write	Default
7:0	**System Cache Line Size** Specifies (in units of 32-bit words – 8 or 16 Dwords) the System Cache Line Size. When a size other than 8 or 16 is specified, the PEX 8311 performs Write transfers rather than Memory Write and Invalidate transfers.	Yes	Yes	0h

Register 19-6. (PCILTR; PCI:0Dh, LOC:0Dh) Internal PCI Bus Latency Timer

Bits	Description	Read	Write	Default
7:0	**Internal PCI Bus Latency Timer** Specifies length of time (in units of internal PCI Bus clocks) the PEX 8311, as a Bus Master, can burst data on the internal PCI Bus.	Yes	Yes	0h

Register 19-7. (PCIHTR; PCI:0Eh, LOC:0Eh) PCI Header Type

Bits	Description	Read	Write	Default
6:0	**Configuration Layout Type** Specifies layout of registers 10h through 3Fh in configuration space. Header Type 0 is defined for all PCI devices other than PCI-to-PCI bridges (Header Type 1) and Cardbus bridges (Header Type 2).	Yes	Local	0h
7	**Multi-Function Device** ***Not supported. Local processors should never write 1 to this bit.*** Value of 1 indicates multiple (up to eight) functions (logical devices) each containing its own, individually addressable configuration space, 64 Dwords in size.	Yes	Local	0

Register 19-8. (PCIBISTR; PCI:0Fh, LOC:0Fh) PCI Built-In Self-Test (BIST)

Bits	Description	Read	Write	Default
3:0	**Built-In Self-Test Pass/Fail** Writing 0h indicates the PEX 8311 passed its test. Non-0h values indicate the PEX 8311 failed its test. Device-specific failure codes are encoded in a non-0h value.	Yes	Local	0h
5:4	***Reserved***	Yes	No	00b
6	**PCI Built-In Self-Test Interrupt Enable** The internal PCI Bus writes 1 to enable BIST interrupts. Generates a BIST interrupt to the Local Bus. Reset by the Local Bus when BIST is complete. Software fails the PEX 8311 when BIST is not complete after 2s. ***Note:*** *Refer to INTCSR[23] for BIST interrupt status.*	Yes	Yes	0
7	**Built-In Self-Test Support** Returns 1 when the PEX 8311 supports BIST. Returns 0 when the PEX 8311 is not BIST-compatible.	Yes	Local	0

Register 19-9. (PCIBAR0; PCI:10h, LOC:10h) PCI Base Address for Memory Accesses to Local, Runtime, DMA, and Messaging Queue Registers

Bits	Description	Read	Write	Default
0	**Memory Space Indicator** Value of 0 indicates this register maps into Memory space. ***Note:*** *Hardwired to 0.*	Yes	No	0
2:1	**Register Location** Value of 00b locates anywhere in 32-bit Memory Address space. ***Note:*** *Hardwired to 00b.*	Yes	No	00b
3	**Prefetchable** Writing 1 indicates there are no side effects on reads. Does not affect PEX 8311 operation. ***Note:*** *Hardwired to 0.*	Yes	No	0
8:4	**Memory Base Address** Memory Base address for access to Local, Runtime, DMA, and Messaging Queue registers (requires 512 bytes). ***Note:*** *Hardwired to 0h.*	Yes	No	0h
31:9	**Memory Base Address** Memory Base address for access to Local, Runtime, DMA, and Messaging Queue registers.	Yes	Yes	0h

Note: *For I_2O, the Inbound message frame pool must reside in the Address space pointed to by PCIBAR0. Message Frame Address (MFA) is defined by I_2O as an offset from this Base address to the start of the message frame.*

Register 19-10. (PCIBAR1; PCI:14h, LOC:14h) PCI Base Address for I/O Accesses to Local, Runtime, DMA, and Messaging Queue Registers

Bits	Description	Read	Write	Default
0	**I/O Space Indicator** Value of 1 indicates this register maps into I/O space. ***Note:*** *Hardwired to 1.*	Yes	No	1
1	***Reserved***	Yes	No	0
7:2	**I/O Base Address** Base Address for I/O access to Local, Runtime, DMA, and Messaging Queue registers (requires 256 bytes). ***Note:*** *Hardwired to 0h.*	Yes	No	0h
31:8	**I/O Base Address** Base Address for I/O access to Local, Runtime, DMA, and Messaging Queue registers.	Yes	Yes	0h

Note: *PCIBAR1 is enabled or disabled by setting or clearing the I/O Base Address Register Enable bit (LMISC1[0]).*

Register 19-11. (PCIBAR2; PCI:18h, LOC:18h) PCI Base Address for Accesses to Local Address Space 0

Bits	Description	Read	Write	Default
0	**Memory Space Indicator** Writing 0 indicates the register maps into Memory space. Writing 1 indicates the register maps into I/O space. (Bit is writable by way of the LAS0RR register.)	Yes	No	0
2:1	**Register Location (If Memory Space)** Values: 00b = Locate anywhere in 32-bit Memory Address space 01b = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, ***Reserved*** 10b or 11b = ***Reserved*** (Specified in the LAS0RR register.) When mapped into I/O space (PCIBAR2[0]=1), bit 1 is always 0 and bit 2 is included in the Base Address (PCIBAR2[31:4]).	Yes	PCIBAR2[0]=0: No PCIBAR2[0]=1: Bit 1 No, Bit 2 Yes	00b
3	**Prefetchable (If Memory Space)** Writing 1 indicates there are no side effects on reads. Reflects value of LAS0RR[3] and provides only status to the system. Does not affect PEX 8311 operation. The associated Bus Region Descriptor register (LBRD0) controls prefetching functions of this Address space. When mapped into I/O space (PCIBAR2[0]=1), bit 3 is included in the Base Address (PCIBAR2[31:4]).	Yes	Memory: No I/O: Yes	0
31:4	**Base Address** Base Address for access to Local Address Space 0.	Yes	Yes	0h

Note: *Configure LAS0RR before configuring PCIBAR2.*

When allocated, Local Address Space 0 is enabled or disabled by setting or clearing LAS0BA[0].

Register 19-12. (PCIBAR3; PCI:1Ch, LOC:1Ch) PCI Base Address for Accesses to Local Address Space 1

Bits	Description	Read	Write	Default
0	**Memory Space Indicator** Writing 0 indicates the register maps into Memory space. Writing 1 indicates the register maps into I/O space. (Bit is writable by way of the LAS1RR register.)	Yes	No	0
2:1	**Register Location** Values: 00b = Locate anywhere in 32-bit Memory Address space 01b = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, ***Reserved*** 10b or 11b = ***Reserved*** (Specified in the LAS1RR register.) When mapped into I/O space (PCIBAR3[0]=1), bit 1 is always 0 and bit 2 is included in the Base Address (PCIBAR3[31:4]).	Yes	PCIBAR3[0]=0: No PCIBAR3[0]=1: Bit 1 No, Bit 2 Yes	00b
3	**Prefetchable (If Memory Space)** Writing 1 indicates there are no side effects on reads. Reflects value of LAS1RR[3] and provides only status to the system. Does not affect PEX 8311 operation. The associated Bus Region Descriptor register (LBRD1) controls prefetching functions of this Address space. When mapped into I/O space (PCIBAR3[0]=1), bit 3 is included in the Base Address (PCIBAR3[31:4]).	Yes	Memory: No I/O: Yes	0
31:4	**Base Address** Base address for access to Local Address Space 1. When I_2O Decode is enabled (QSR[0]=1), PCIBAR3[31:4] return 0h.	Yes	Yes	0h

Note: *Configure LAS1RR before configuring PCIBAR3.*

When allocated, Local Address Space 1 is enabled or disabled by setting or clearing LAS1BA[0].

Register 19-13. (PCIBAR4; PCI:20h, LOC:20h) PCI Base Address

Bits	Description	Read	Write	Default
31:0	***Reserved***	Yes	No	0h

Register 19-14. (PCIBAR5; PCI:24h, LOC:24h) PCI Base Address

Bits	Description	Read	Write	Default
31:0	***Reserved***	Yes	No	0h

Register 19-15. (PCICIS; PCI:28h, LOC:28h) PCI Cardbus Information Structure Pointer

Bits	Description	Read	Write	Default
31:0	**Cardbus Information Structure (CIS) Pointer for PC Cards** ***Not supported.***	Yes	No	0h

Register 19-16. (PCISVID; PCI:2Ch, LOC:2Ch) PCI Subsystem Vendor ID

Bits	Description	Read	Write	Default
15:0	**Subsystem Vendor ID (Unique Add-In Board Vendor ID)** The PLX PCI-SIG-issued Vendor ID is 10B5h.	Yes	Local/ Serial EEPROM	10B5h

Register 19-17. (PCISID; PCI:2Eh, LOC:2Eh) PCI Subsystem ID

Bits	Description	Read	Write	Default
15:0	**Subsystem ID (Unique Add-In Board Device ID)**	Yes	Local/ Serial EEPROM	9056h

Register 19-18. (PCIERBAR; PCI:30h, LOC:30h) PCI Base Address for Local Expansion ROM

Bits	Description	Read	Write	Default
0	**Address Decode Enable** Works in conjunction with EROMRR[0]. Writing 0 indicates the PEX 8311 does not accept accesses to Expansion ROM address. Clear to 0 when there is no Expansion ROM. Writing 1 indicates the PEX 8311 accepts Memory accesses to the Expansion ROM address.	Yes	Yes	0
10:1	***Reserved***	Yes	No	0h
31:11	**Expansion ROM Base Address (Upper 21 Bits).**	Yes	Yes	0h

Register 19-19. (CAP_PTR; PCI:34h, LOC:34h) New Capability Pointer

Bits	Description	Read	Write	Default
7:0	**New Capability Pointer** Provides an offset into PCI Configuration Space for location of the Power Management capability in the New Capabilities Linked List. ***Note:*** *For the New Capability Pointer features, this field must always contain the default value of 40h.*	Yes	Local	40h
31:8	***Reserved***	Yes	No	0h

Register 19-20. (PCIILR; PCI:3Ch, LOC:3Ch) Internal PCI Interrupt Line

Bits	Description	Read	Write	Default
7:0	**Internal PCI Interrupt Line Routing Value** Value indicates which input of the System Interrupt Controller(s) is connected to the PEX 8311 INTA# output.	Yes	Yes/Serial EEPROM	0h

Register 19-21. (PCIIPR; PCI:3Dh, LOC:3Dh) Internal PCI Wire Interrupt

Bits	Description	Read	Write	Default
7:0	**Internal PCI Wire Interrupt** Indicates which wire interrupt the PEX 8311 uses. The following values are valid: 0h = No wire interrupt 1h = INTA#	Yes	Local/ Serial EEPROM	1h

Register 19-22. (PCIMGR; PCI:3Eh, LOC:3Eh) PCI Minimum Grant

Bits	Description	Read	Write	Default
7:0	**Minimum Grant** Specifies how long a burst period the PEX 8311 needs, assuming a clock rate of 33 MHz. Value is a multiple of 1/4 µs increments.	Yes	Local/ Serial EEPROM	0h

Register 19-23. (PCIMLR; PCI:3Fh, LOC:3Fh) PCI Maximum Latency

Bits	Description	Read	Write	Default
7:0	**Maximum Latency** Specifies how often the PEX 8311 must gain access to the internal PCI Bus. Value is a multiple of 1/4 µs increments.	Yes	Local/ Serial EEPROM	0h

Register 19-24. (PMCAPID; PCI:40h, LOC:180h) Power Management Capability ID

Bits	Description	Read	Write	Default
7:0	**Power Management Capability ID** The PCI-SIG-issued Capability ID for Power Management is 01h.	Yes	No	01h

Register 19-25. (PMNEXT; PCI:41h, LOC:181h) Power Management Next Capability Pointer

Bits	Description	Read	Write	Default
7:0	**Next_Cap Pointer** Provides an offset into PCI Configuration space for location of the Hot Swap capability in the New Capabilities Linked List. When Power Management is the last capability in the list, clear to 0h. Otherwise, these bits must contain the default value of 48h. ***Note:*** *48h, Hot Swap, is not supported. The next supported capability is at offset 4Ch.*	Yes	Local	48h

Register 19-26. (PMC; PCI:42h, LOC:182h) Power Management Capabilities

Bits	Description	Read	Write	Default
2:0	**Version** Reading value of 010b indicates this function complies with *PCI Power Mgmt. r1.1*.	Yes	Local/Serial EEPROM	010b
3	**Internal Clock Required for PME# Signal** When set to 1, indicates a function relies on the presence of the internal clock for PME# operation. Because the PEX 8311 does not require the internal clock for PME#, clear to 0 in the serial EEPROM.	Yes	Local	0
4	***Reserved***	Yes	No	0
5	**Device-Specific Implementation (DSI)** When set to 1, the PEX 8311 requires special initialization following a transition to a D0_uninitialized state before a generic class device driver is able to use the PEX 8311.	Yes	Local	0
8:6	**AUX Current** Refer to the *PCI Power Mgmt. r1.1*.	Yes	Local	000b
9	**D1 Support** When set to 1, the PEX 8311 supports the D1 power state.	Yes	Local/Serial EEPROM	0
10	**D2 Support** Specifies that the PEX 8311 does ***not support*** the D2 state.	Yes	Local/Serial EEPROM	0
15:11	**PME Support** Indicates power states in which the PEX 8311 can assert PME#. Values: XXXX1b = PME# asserted from D0 XXX1Xb = PME# asserted from D1 XX1XXb = ***Reserved*** X1XXXb = PME# asserted from D3hot ***Note:*** *"X" is "Don't Care."*	Yes	Local/Serial EEPROM	00000b

Register 19-27. (PMCSR; PCI:44h, LOC:184h) Power Management Control/Status

Bits	Description	Read	Write	Default
1:0	**Power State** Determines or changes the current power state. Values: 00b = D0 10b = ***Reserved*** 01b = D1 11b = D3hot In a D3hot power state, PCI Memory and I/O accesses are disabled, as well as internal interrupts, and only configuration or PME# assertion is allowed. The same is true for the D1 power state, when the corresponding *D1 Support* bit is set (PMC[9]=1). Transition from a D3hot to a D0 power state causes a Soft Reset.	Yes	Yes	00b
7:2	***Reserved***	Yes	No	0h
8	**PME_En** Writing 1 enables generation of PM PME messages to PCI Express Space. ***Notes:*** *Value after reset is indeterminate (either 1 or 0) at time of initial operating system boot when the internal PRESENT_DET signal is connected to power (D3cold power state support).* *Value after reset is 0 when the internal PRESENT_DET signal is connected to ground (no D3cold power state support).*	Yes	Yes/Serial EEPROM	Sticky bit, refer to Note
12:9	**Data_Select** Selects which data to report through the PMDATA register and Data_Scale (PMCSR[14:13] bits.	Yes	Yes/Serial EEPROM	0h
14:13	**Data_Scale** Indicates the scaling factor to use when interpreting the value of the Data register. Bit values and definitions depend on the data value selected by the Data_Select bits (PMCSR[12:9]). When the Local CPU initializes the Data_Scale values, the Data_Select bits must be used to determine which Data_Scale value the Local CPU is writing. For Power Consumed and Power Dissipated data, the following scale factors are used. Unit values are in watts. **Value** **Scale** 00b Unknown 01b 0.1x 10b 0.01x 11b 0.001x	Yes	Local/Serial EEPROM	00b
15	**PME_Status** Indicates PME# is being driven when the PME_En bit is set (PMCSR[8]=1). Writing 1 from the Local Bus sets this bit; writing 1 from the internal PCI Bus clears this bit to 0. Depending on the current power state, set only when the appropriate *PME Support* bit(s) is set (*for example*, PMC[15:11]=1h). ***Note:*** *Value after reset is indeterminate (either 1 or 0) at time of initial operating system boot when the internal PRESENT_DET signal is connected to power (D3cold power state support). Value after reset is 0 when the internal PRESENT_DET signal is connected to ground (no D3cold power state support).*	Yes	Local/Set, PCI/Clr	Sticky bit, refer to Note

Register 19-28. (PMCSR_BSE; PCI:46h, LOC:186h) PMCSR Bridge Support Extensions

Bits	Description	Read	Write	Default
7:0	***Reserved***	Yes	No	0h

Register 19-29. (PMDATA; PCI:47h, LOC:187h) Power Management Data

Bits	Description	Read	Write	Default
7:0	**Power Management Data** Provides operating data, *such as* power consumed or heat dissipation. Data returned is selected by the Data_Select bit(s) (PMCSR[12:9]) and scaled by the Data_Scale bit(s) (PMCSR[14:13]). Values: **Data_Select** **Description** 0 D0 Power Consumed 1 D1 Power Consumed 2 ***Reserved*** 3 D3 Power Consumed 4 D0 Power Dissipated 5 D1 Power Dissipated 6 ***Reserved*** 7 D3 Power Dissipated	Yes	Local/Serial EEPROM	0h

Register 19-30. (HS_CNTL; PCI:48h, LOC:188h) Hot Swap Control *(Not Supported)*

Bits	Description	Read	Write	Default
7:0	**Hot Swap ID** ***Not supported.*** The Hot Swap Capability ID is 06h. To disable Hot Swap capabilities, clear this register to 0h.	Yes	Local/ Serial EEPROM	06h

Register 19-31. (HS_NEXT; PCI:49h, LOC:189h) Hot Swap Next Capability Pointer *(Not Supported)*

Bits	Description	Read	Write	Default
7:0	**Next_Cap Pointer** ***Not supported.*** Provides an offset into PCI Configuration space for location of the VPD capability in the New Capabilities Linked List. When Hot Swap is the last capability in the list, clear to 0h. Otherwise, this field must contain the default value of 4Ch.	Yes	Local/ Serial EEPROM	4Ch

Register 19-32. (HS_CSR; PCI:4Ah, LOC:18Ah) Hot Swap Control/Status *(Not Supported)*

Bits	Description	Read	Write	Default
0	***Reserved***	Yes	No	0
1	**ENUM# Interrupt Mask (EIM)** ***Not supported.*** Writing 0 enables interrupt assertion. Writing 1 masks interrupt assertion.	Yes	Yes/Clr	0
2	***Reserved***	Yes	No	0
3	**LED Software On/Off Switch** ***Not supported.*** Writing 1 asserts the LEDon# signal. Writing 0 de-asserts the LEDon# signal.	Yes	PCI	0
5:4	**Programming Interface 0 (PI = 0)** ***Not supported.***	Yes	No	00b
6	**ENUM# Status – Extraction** ***Not supported.*** Writing 1 reports the ENUM# assertion for removal process.	Yes	Yes/Clr	0
7	**ENUM# Status – Insertion** ***Not supported.*** Writing 1 reports the ENUM# assertion for insertion process.	Yes	Yes/Clr	0
15:8	***Reserved***	Yes	No	0h

Register 19-33. (PVPDID; PCI:4Ch, LOC:18Ch) PCI Vital Product Identification

Bits	Description	Read	Write	Default
7:0	**VPD ID** The PCI-SIG-issued Capability ID for VPD is 03h.	Yes	No	03h

Register 19-34. (PVPD_NEXT; PCI:4Dh, LOC:18Dh) PCI Vital Product Data Next Capability Pointer

Bits	Description	Read	Write	Default
7:0	**Next_Cap Pointer** Because VPD is the last capability in the list, cleared to 0h.	Yes	Local	0h

Register 19-35. (PVPDAD; PCI:4Eh, LOC:18Eh) PCI Vital Product Data Address

Bits	Description	Read	Write	Default
14:0	**VPD Address** VPD byte address to be accessed. All accesses are 32 bits wide. For VPD writes, the byte address must be Dword-aligned (bits [1:0]=00b). For VPD reads, the byte address must be word-aligned (bit 0 = 0). PVPDAD[14:9] are ignored.	Yes	Yes	0h
15	**F** Controls the direction of the next VPD cycle and indicates when the VPD cycle is complete. Writing 0 along with the VPD address causes a read of VPD information into PVPDATA. The hardware sets this bit to 1 when the VPD Data transfer is complete. Writing 1 along with the VPD address causes a write of VPD information from PVPDATA into a storage component. The hardware clears this bit to 0 after the Write operation is complete.	Yes	Yes	0

Register 19-36. (PVPDATA; PCI:50h, LOC:190h) PCI VPD Data

Bits	Description	Read	Write	Default
31:0	**VPD Data** Refer to Section 16.2.2, "VPD Data Register," for details.	Yes	Yes	0h

19.6 Local Configuration Space Local Configuration Registers

Note: *"Yes" in the register Read and Write columns indicates the register is writable by the PCI Express interface and Local Bus.*

Register 19-37. (LAS0RR; PCI:00h, LOC:80h) Direct Slave Local Address Space 0 Range

Bits	Description	Read	Write	Default
0	**Memory Space Indicator** Writing 0 indicates Local Address Space 0 maps into PCI Memory space. Writing 1 indicates Local Address Space 0 maps into PCI I/O space.	Yes	Yes/Serial EEPROM	0
2:1	When mapped into Memory space (LAS0RR[0]=0), the only valid value is 00b. Locate anywhere in PCI Address space. When mapped into I/O space (LAS0RR[0]=1), bit 1 must be cleared to 0. Bit 2 is included with LAS0RR[31:3] to indicate the decoding range.	Yes	Yes/Serial EEPROM	00b
3	When mapped into Memory space (LAS0RR[0]=0), writing 1 indicates reads are prefetchable (does not affect PEX 8311 operation, but is used for system status). When mapped into I/O space (LAS0RR[0]=1), this bit is included with LAS0RR[31:4, 2] to indicate the decoding range.	Yes	Yes/Serial EEPROM	0
31:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Address Space 0. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to Address bit 31. Write 1 to all bits that must be included in decode and 0 to all others (used in conjunction with PCIBAR2). Default is 1 MB. ***Notes:*** *LAS0RR range (**not** the Range register) must be power of 2. "Range register value" is two's complement of the range.* *Per PCI r2.2, limit I/O-Mapped spaces to 256 bytes per space.*	Yes	Yes/Serial EEPROM	FFF0000h

Register 19-38. (LAS0BA; PCI:04h, LOC:84h) Direct Slave Local Address Space 0 Local Base Address (Remap)

Bits	Description	Read	Write	Default
0	**Local Address Space 0 Enable** Writing 1 enables decoding of PCI addresses for Direct Slave access to Local Address Space 0. Writing 0 disables decoding.	Yes	Yes/Serial EEPROM	0
1	***Reserved***	Yes	No	0
3:2	When Local Address Space 0 is mapped into Memory space (LAS0RR[0]=0), LAS0BA[3:2] must be 00b. When mapped into I/O space (LAS0RR[0]=1), included with LAS0BA[31:4] for remapping.	Yes	Yes/Serial EEPROM	00b
31:4	**Remap PCIBAR2 Base Address to Local Address Space 0 Base Address** The PCIBAR2 Base address translates to the Local Address Space 0 Base Address programmed in this register. A Direct Slave access to an offset from PCIBAR2 maps to the same offset from this Local Base Address. ***Notes:*** *Remap Address value must be a multiple of the LAS0RR range (**not** the Range register).*	Yes	Yes/Serial EEPROM	0h

Register 19-39. (MARBR; PCI:08h or ACh, LOC:88h or 12Ch) Mode/DMA Arbitration

Bits	Description	Read	Write	Default
7:0	**Local Bus Latency Timer** Number of Local Bus clock cycles to occur before de-asserting LHOLD and releasing the Local Bus. The Local Bus Latency Timer starts counting upon LHOLDA assertion.	Yes	Yes/Serial EEPROM	0h
15:8	**Local Bus Pause Timer** Valid only during DMA transfers. Number of Local Bus Clock cycles to occur before reasserting LHOLD after releasing the Local Bus.	Yes	Yes/Serial EEPROM	0h
16	**Local Bus Latency Timer Enable** Writing 0 disables the Latency Timer. Writing 1 enables the Latency Timer.	Yes	Yes/Serial EEPROM	0
17	**Local Bus Pause Timer Enable** Writing 0 disables the Pause Timer. Writing 1 enables the Pause Timer.	Yes	Yes/Serial EEPROM	0
18	**Local Bus BREQi Enable** Writing 1 enables the Local Bus BREQi. When BREQi is asserted, the PEX 8311 de-asserts LHOLD and releases the Local Bus.	Yes	Yes/Serial EEPROM	0
20:19	**DMA Channel Priority** Writing 00b indicates a rotational priority scheme. Writing 01b indicates Channel 0 has priority. Writing 10b indicates Channel 1 has priority. Value of 11b is ***reserved***.	Yes	Yes/Serial EEPROM	00b
21	**Local Bus Direct Slave Release Bus Mode** When set to 1, the PEX 8311 de-asserts LHOLD and releases the Local Bus when either of the following occur: • Direct Slave Write FIFO becomes empty during a Direct Slave write • Direct Slave Read FIFO becomes full during a Direct Slave read	Yes	Yes/Serial EEPROM	1
22	**Direct Slave Internal LOCK# Input Enable** Writing 0 disables Direct Slave locked sequences. Writing 1 enables Direct Slave locked sequences.	Yes	Yes/Serial EEPROM	0
23	**PCI Request Mode** Writing 0 causes the PEX 8311 to hold REQ# asserted for the entire Bus Master cycle. Writing 1 causes the PEX 8311 to de-assert REQ# when the PEX 8311 internally asserts FRAME# during a Master cycle.	Yes	Yes/Serial EEPROM	0

Register 19-39. (MARBR; PCI:08h or ACh, LOC:88h or 12Ch) Mode/DMA Arbitration *(Cont.)*

Bits	Description	Read	Write	Default
24	**PCI Compliance Enable** When set to 1, the PEX 8311 internally performs PCI Read and Write transactions in compliance with the *PCI r2.2*. Setting this bit enables Direct Slave Delayed Reads, 2^{15} internal clock timeout on Retrys, 16- and 8-clock PCI latency rules, and enables the option to select PCI Read No Write mode (Retries for writes) (MARBR[25]). Value of 0 causes TRDY# to remain de-asserted on reads until Read data is available. ***Note:*** *Refer to Section 8.3.4, "PCI Compliance Enable," for further details.*	Yes	Yes/Serial EEPROM	0
25	**PCI Read No Write Mode (PCI Retries for Writes)** When PCI Compliance is enabled (MARBR[24]=1), value of 1 forces a PCI Retry on writes when a Delayed Read is pending. Value of 0 (or MARBR[24]=0) allows writes to occur while a Delayed Read is pending.	Yes	Yes/Serial EEPROM	0
26	**PCI Read with Write Flush Mode** Value of 0 does not affect a pending Delayed Read when a Write cycle occurs. Value of 1 flushes a pending Delayed Read cycle when a Write cycle is detected.	Yes	Yes/Serial EEPROM	0
27	**Gate Local Bus Latency Timer with BREQi** The Local Bus Latency Timer counts only while BREQi is asserted (BREQi=1) and this bit is set to 1. The Local Bus Latency Timer does not timeout until the number of Local clocks programmed into MARBR[7:0] is reached. When cleared to 0, or when the Local Bus Latency Timer is disabled (MARBR[16]=0), BREQi assertion causes the PEX 8311 to release the Local Bus. ***Note:*** *Refer to Section 6.2, "Local Bus Arbitration and BREQi," for further details.*	Yes	Yes/Serial EEPROM	0
28	**PCI Read No Flush Mode** Writing 0 submits a request to flush the Direct Slave Read FIFO when a PCI Read cycle completes. Writing 1 submits a request to not flush the Direct Slave Read FIFO when a PCI Read cycle completes (Direct Slave Read Ahead mode).	Yes	Yes/Serial EEPROM	0
29	**Device and Vendor ID Select** When cleared to 0, reads from the PCI Configuration register address 00h return the Device and Vendor IDs. When set to 1, reads from the PCI Configuration register address 00h return the Subsystem and Subsystem Vendor IDs.	Yes	Yes/Serial EEPROM	0
30	**Direct Master Write FIFO Full Status Flag** When set to 1, the Direct Master Write FIFO is almost full. Reflects the DMPAF ball value, as determined by the Programmable Almost Full Flag value in DMPBAM[10, 8:5].	Yes	No	0
31	***Reserved***	Yes	No	0

Register 19-40. (BIGEND; PCI:0Ch, LOC:8Ch) Big/Little Endian Descriptor

Bits	Description	Read	Write	Default
0	**Configuration Register Big Endian Mode (Address Invariance)** Writing 0 specifies use of Little Endian data ordering for Local accesses to the Configuration registers. Writing 1 specifies Big Endian ordering.	Yes	Yes/Serial EEPROM	0
1	**Direct Master Big Endian Mode (Address Invariance)** Writing 0 specifies use of Little Endian data ordering for Direct Master accesses. Writing 1 specifies Big Endian ordering.	Yes	Yes/Serial EEPROM	0
2	**Direct Slave Local Address Space 0 Big Endian Mode (Address Invariance)** Writing 0 specifies use of Little Endian data ordering for Direct Slave accesses to Local Address Space 0. Writing 1 specifies Big Endian ordering.	Yes	Yes/Serial EEPROM	0
3	**Direct Slave Expansion ROM Space Big Endian Mode (Address Invariance)** Writing 0 specifies use of Little Endian data ordering for Direct Slave accesses to Expansion ROM. Writing 1 specifies Big Endian ordering.	Yes	Yes/Serial EEPROM	0
4	**Big Endian Byte Lane Mode** Writing 0 specifies that in any Endian mode, use the following byte lanes for the modes listed: • [15:0] for a 16-bit Local Bus • [7:0] for an 8-bit Local Bus Writing 1 specifies that in any Endian mode, use the following byte lanes for the modes listed: • [31:16] for a 16-bit Local Bus • [31:24] for an 8-bit Local Bus	Yes	Yes/Serial EEPROM	0
5	**Direct Slave Local Address Space 1 Big Endian Mode (Address Invariance)** Writing 0 specifies use of Little Endian data ordering for Direct Slave accesses to Local Address Space 1. Writing 1 specifies Big Endian ordering.	Yes	Yes/Serial EEPROM	0
6	**DMA Channel 1 Big Endian Mode (Address Invariance)** Writing 0 specifies use of Little Endian data ordering for DMA Channel 1 accesses to the Local Bus. Writing 1 specifies Big Endian ordering.	Yes	Yes/Serial EEPROM	0
7	**DMA Channel 0 Big Endian Mode (Address Invariance)** Writing 0 specifies use of Little Endian data ordering for DMA Channel 0 accesses to the Local Bus. Writing 1 specifies Big Endian ordering.	Yes	Yes/Serial EEPROM	0

Register 19-41. (LMISC1; PCI:0Dh, LOC:8Dh) Local Miscellaneous Control

Bits	Description	Read	Write	Default
0	**I/O Base Address Register Enable** When set to 1, the PCI Base Address for I/O accesses to Local, Runtime, DMA, and Messaging Queue Registers register (PCIBAR1) is enabled. When cleared to 0, PCIBAR1 is disabled. This option is intended for embedded systems only. Set this bit to 1 for PC platforms.	Yes	Yes/Serial EEPROM	1
1	**I/O Base Address Register Shift** When the I/O Base Address register is disabled and this bit is cleared to 0 (LMISC1[1:0]=00b), then PCIBAR2 and PCIBAR3 remain at PCI Configuration addresses 18h and 1Ch. When the I/O Base Address register is disabled and this bit is set to 1 (LMISC1[1:0]=10b), then PCIBAR2 (Local Address Space 0) and PCIBAR3 (Local Address Space 1) are shifted to become PCIBAR1 and PCIBAR2 at PCI Configuration addresses 14h and 18h. Set when a blank region in I/O Base Address register space cannot be accepted by the system BIOS.	Yes	Yes/Serial EEPROM	0
2	**Local Init Status** Reading 1 indicates Local Init is done. Responses to PCI accesses prior to this bit being set are determined by the USERi state when the PEX 8311 receives an external reset at PERST# de-assertion in Endpoint mode (ROOT_COMPLEX#=1), or LRESET# input de-assertion in Root Complex mode (ROOT_COMPLEX#=0). ***Note:*** *Refer to Section 4.3.2, "Local Initialization and PCI Express Interface Behavior," for further details.*	Yes	Local/ Serial EEPROM	0
3	**Direct Master (PCI Initiator) Write FIFO Flush during PCI Master Abort** When cleared to 0, the PEX 8311 flushes the Direct Master Write FIFO each time a PCI Master/Target Abort or Retry timeout occurs. When set to 1, the PEX 8311 retains data in the Direct Master Write FIFO.	Yes	Yes/Serial EEPROM	0
6:4	***Reserved***	Yes	No	000b
7	**Disconnect with Flush Read FIFO** When PCI Compliance is enabled (MARBR[24]=1), value of 1 causes acceptance of a new Read request with flushing of the Read FIFO when a Direct Slave Read request does not match an existing, pending Delayed Read in the Read FIFO. Value of 0, or clearing of the PCI Compliance Enable bit (MARBR[24]=0), causes a new Direct Slave Read request to Retry when a Delayed Read is pending in the Read FIFO.	Yes	Yes/Serial EEPROM	0

Register 19-42. (PROT_AREA; PCI:0Eh, LOC:8Eh) Serial EEPROM Write-Protected Address Boundary

Bits	Description	Read	Write	Default
6:0	**Serial EEPROM Location Starting at Dword Boundary (48 Dwords = 192 Bytes) for VPD Accesses** Value is the number of Dwords that are VPD write-protected (starting from serial EEPROM byte address 00h). The corresponding serial EEPROM byte (VPD) address is this value multiplied by 4. Default value of 30h sets the boundary at serial EEPROM byte (VPD) address C0h. Value of 40h write protects a 2K-bit serial EEPROM. A maximum value of 7Fh write-protects all but 2 words in a 4K-bit serial EEPROM. Serial EEPROM addresses below this boundary are Read-Only. ***Note:*** *PEX 8311 configuration data is stored below Dword address 19h.*	Yes	Yes/Serial EEPROM	30h
7	***Reserved***	Yes	No	0

Register 19-43. (LMISC2; PCI:0Fh, LOC:8Fh) Local Miscellaneous Control 2

Bits	Description	Read	Write	Default
0	**READY# Timeout Enable** Value of 1 enables READY# timeout.	Yes	Yes/Serial EEPROM	0
1	**READY# Timeout Select** Values: 0 = 32 clocks 1 = 1,024 clocks	Yes	Yes/Serial EEPROM	0
4:2	**Direct Slave Delayed Write Mode** Delay in LCLK of LHOLD assertion for PCI Burst writes. Values: 0 = 0 LCLK 2 = 8 LCLK 4 = 20 LCLK 6 = 28 LCLK 1 = 4 LCLK 3 = 16 LCLK 5 = 24 LCLK 7 = 32 LCLK	Yes	Yes/Serial EEPROM	000b
5	**Direct Slave Write FIFO Full Condition.** Value of 1 guarantees that when the Direct Slave Write FIFO is full with Direct Slave Write data, there is always one location remaining empty for the Direct Slave Read address to be accepted by the PEX 8311. Value of 0 Retries Direct Slave Read accesses when the Direct Slave Write FIFO is full with Direct Slave Write data.	Yes	Yes/Serial EEPROM	0
7:6	***Reserved***	Yes	No	00b

Register 19-44. (EROMRR; PCI:10h, LOC:90h) Direct Slave Expansion ROM Range

Bits	Description	Read	Write	Default
0	**Address Decode Enable** Bit 0 is enabled only from the serial EEPROM. To disable, clear the PCI Expansion ROM Address Decode Enable bit to 0 (PCIERBAR[0]=0).	Yes	Serial EEPROM Only	0
10:1	***Reserved***	Yes	No	0h
31:11	Specifies which PCI Address bits to use for decoding a PCI-to-Local Bus Expansion ROM. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to Address bit 31. Write 1 to all bits that must be included in decode and 0 to all others (used in conjunction with PCIERBAR). The minimum range, when enabled, is 2 KB, and maximum range allowed by *PCI r2.2* is 16 MB. ***Notes:*** *EROMRR range (**not** the Range register) must be power of 2. "Range register value" is two's complement of the range.* *Program EROMRR by way of the serial EEPROM to a value of 0h, unless Expansion ROM is present on the Local Bus. When the value is not 0h, system BIOS can attempt to allocate Expansion ROM Address space and then access it at the Local Address space specified in EROMBA[31:11] (default value is 0h) to determine whether the Expansion ROM image is valid. When the image is not valid, as defined in the PCI r2.2, Section 6.3.1.1 (PCI Expansion ROM Header Format), the system BIOS unmaps the Expansion ROM Address space that it initially allocated, by writing 0h to PCIERBAR.*	Yes	Yes/Serial EEPROM	0h

Register 19-45. (EROMBA; PCI:14h, LOC:94h) Direct Slave Expansion ROM Local Base Address (Remap) and BREQo Control

Bits	Description	Read	Write	Default
3:0	**Backoff Request Delay Clocks** Number of Local Bus clocks in which a Direct Slave LHOLD request is pending and a Local Direct Master access is in progress and not being granted the bus (LHOLDA) before asserting BREQo. BREQo remains asserted until the PEX 8311 receives LHOLDA (LSB is 8 or 64 clocks).	Yes	Yes/Serial EEPROM	0h
4	**Local Bus Backoff Enable** Writing 1 enables the PEX 8311 to assert BREQo.	Yes	Yes/Serial EEPROM	0
5	**Backoff Timer Resolution** Writing 1 changes the LSB of the Backoff Timer from 8 to 64 clocks.	Yes	Yes/Serial EEPROM	0
10:6	***Reserved***	Yes	No	0h
31:11	**Remap PCI Expansion ROM into Local Address Space** Bits in this register remap (replace) the PCI Address bits used in decode as Local Address bits. ***Note:*** *Remap Address value must be a multiple of the EROMRR range (**not** the Range register).*	Yes	Yes/Serial EEPROM	0h

Register 19-46. (LBRD0; PCI:18h, LOC:98h) Local Address Space 0/Expansion ROM Bus Region Descriptor

Bits	Description	Read	Write	Default
1:0	**Local Address Space 0 Local Bus Data Width** Writing the following values indicates the associated bus data width: 00b = 8 bit 01b = 16 bit 10b or 11b = 32 bit	Yes	Yes/Serial EEPROM	11b
5:2	**Local Address Space 0 Internal Wait State Counter** Address-to-Data; Data-to-Data; 0 to 15 Wait States.	Yes	Yes/Serial EEPROM	0h
6	**Local Address Space 0 READY# Input Enable** Writing 1 enables READY# input. Writing 0 disables READY# input.	Yes	Yes/Serial EEPROM	1
7	**Local Address Space 0 Continuous Burst Enable** When bursting is enabled (LBRD0[24]=1), writing 1 enables Continuous Burst mode and writing 0 enables Burst-4 mode. Writing 1 additionally enables BTERM# input, which when asserted overrides the READY# input state (when READY# is enabled, LBRD0[6]=1). ***Note:*** *Refer to Section 8.4.2, "Local Bus Direct Slave Data Transfer Modes," for further details.*	Yes	Yes/Serial EEPROM	0
8	**Local Address Space 0 Prefetch Disable** When mapped into Memory space (LAS0RR[0]=0), writing 0 enables Read prefetching. Writing 1 disables prefetching. When prefetching is disabled, the PEX 8311 disconnects after each Memory read.	Yes	Yes/Serial EEPROM	0
9	**Expansion ROM Space Prefetch Disable** Writing 0 enables Read prefetching. Writing 1 disables prefetching. When prefetching is disabled, the PEX 8311 disconnects after each Memory read.	Yes	Yes/Serial EEPROM	0
10	**Local Address Space 0/Expansion ROM Space Prefetch Counter Enable** When cleared to 0, the PEX 8311 ignores the count and continues prefetching as follows: • **If PCI Read No Flush mode is enabled (MARBR[28]=1)** – Continues prefetching until the Direct Slave Read FIFO is full, or • **If PCI Read No Flush mode is disabled (MARBR[28]=0)** – Continues prefetching until PCI Read Completion, at which time the Direct Slave Read FIFO is flushed. When set to 1 and Memory prefetching is enabled, the PEX 8311 prefetches up to the number of Dwords specified in the Prefetch Counter (LBRD0[14:11]).	Yes	Yes/Serial EEPROM	0
14:11	**Local Address Space 0/Expansion ROM Space Prefetch Counter** Number of Dwords to prefetch during Memory Read cycles (0 to 15). A count of zero selects a prefetch of 16 Dwords.	Yes	Yes/Serial EEPROM	0h
15	***Reserved***	Yes	No	0

Register 19-46. (LBRD0; PCI:18h, LOC:98h) Local Address Space 0/Expansion ROM Bus Region Descriptor *(Cont.)*

Bits	Description	Read	Write	Default
17:16	**Expansion ROM Space Local Bus Data Width** Writing the following values indicates the associated bus data width: 00b = 8 bit 01b = 16 bit 10b or 11b = 32 bit	Yes	Yes/Serial EEPROM	11b
21:18	**Expansion ROM Space Internal Wait State Counter** Address-to-Data; Data-to-Data; 0 to 15 Wait States.	Yes	Yes/Serial EEPROM	0h
22	**Expansion ROM Space READY# Input Enable** Writing 1 enables READY# input. Writing 0 disables READY# input.	Yes	Yes/Serial EEPROM	1
23	**Expansion ROM Space Continuous Burst Enable** When bursting is enabled (LBRD0[26]=1), writing 1 enables Continuous Burst mode and writing 0 enables Burst-4 mode. Writing 1 additionally enables BTERM# input, which when asserted overrides the READY# input state (when READY# is enabled, LBRD0[22]=1). ***Note:*** *Refer to Section 8.4.2, "Local Bus Direct Slave Data Transfer Modes," for further details.*	Yes	Yes/Serial EEPROM	0
24	**Local Address Space 0 Burst Enable** Writing 1 enables bursting. Writing 0 disables bursting.	Yes	Yes/Serial EEPROM	0
25	**Extra Long Load from Serial EEPROM** Writing 1 loads the Subsystem ID, Local Address Space 1 registers, and Internal Arbiter register values. Writing 0 indicates not to load them.	Yes	Serial EEPROM Only	0
26	**Expansion ROM Space Burst Enable** Writing 1 enables bursting. Writing 0 disables bursting.	Yes	Yes/Serial EEPROM	0
27	**Direct Slave PCI Write Mode** Writing 0 indicates the PEX 8311 disconnects from the internal PCI Bus when the Direct Slave Write FIFO is full. Writing 1 indicates the PEX 8311 de-asserts TRDY# when the Direct Slave Write FIFO is full. ***Note:*** *Used for all three Local Address spaces – Space 0, Space 1, and Expansion ROM.*	Yes	Yes/Serial EEPROM	0
31:28	**Direct Slave Retry Delay Clocks** Number of internal clocks (multiplied by 8) from the beginning of a Direct Slave access until a PCI Retry is issued, when the transfer was not completed. Valid for Read cycles only when MARBR[24]=0. Valid for Write cycles only when LBRD0[27]=1. ***Note:*** *Used for all three Local Address spaces – Space 0, Space 1, and Expansion ROM.*	Yes	Yes/Serial EEPROM	4h (32 clocks)

Register 19-47. (DMRR; PCI:1Ch, LOC:9Ch) Local Range for Direct Master-to-PCI

Bits	Description	Read	Write	Default
15:0	***Reserved*** (64-KB increments).	Yes	No	0h
31:16	Specifies which Local Address bits to use for decoding a Local-to-internal PCI Bus access. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to Address bit 31. Write 1 to all bits that must be included in decode and 0h to all others. ***Note:*** *DMRR range (**not** the Range register) must be power of 2. "Range register value" is two's complement of the range.*	Yes	Yes/Serial EEPROM	0h

Register 19-48. (DMLBAM; PCI:20h, LOC:A0h) Local Base Address for Direct Master-to-PCI Memory

Bits	Description	Read	Write	Default
15:0	***Reserved***	Yes	No	0h
31:16	Assigns a value to bits to use for decoding Local-to-PCI Memory accesses. ***Note:*** *Local Base Address value must be a multiple of the DMRR range (**not** the Range register).*	Yes	Yes/Serial EEPROM	0h

Register 19-49. (DMLBAI; PCI:24h, LOC:A4h) Local Base Address for Direct Master-to-PCI I/O Configuration

Bits	Description	Read	Write	Default
15:0	***Reserved***	Yes	No	0h
31:16	Assigns a value to bits to use for decoding Local-to-PCI I/O or PCI Configuration Space accesses. ***Notes:*** *Local Base Address value must be a multiple of the DMRR range (**not** the Range register). I/O Address space is 64 KB.* *Refer to DMPBAM[13] for the I/O Remap Address option.*	Yes	Yes/Serial EEPROM	0h

Register 19-50. (DMPBAM; PCI:28h, LOC:A8h) PCI Base Address (Remap) for Direct Master-to-PCI Memory

Bits	Description	Read	Write	Default
0	**Direct Master Memory Access Enable** Writing 0 disables decode of Direct Master Memory accesses. Writing 1 enables decode of Direct Master Memory accesses within the Address space defined by the DMLBAM and DMRR registers.	Yes	Yes/Serial EEPROM	0
1	**Direct Master I/O Access Enable** Writing 0 disables decode of Direct Master I/O accesses. Writing 1 enables decode of Direct Master I/O accesses within the 64 KB Address space beginning at the DMLBAI Base address.	Yes	Yes/Serial EEPROM	0
2	**Direct Master Read Ahead Mode** Valid only when DMPBAM[12, 3]=00b. Writing 0 submits a request to flush the Read FIFO when a Local Read cycle completes. Writing 1 submits a request to not flush the Read FIFO when the Local Read cycle completes (Direct Master Read Ahead mode). ***Caution: To prevent constant locking of the internal PCI Bus, do not simultaneously enable this bit and Direct Master PCI Read mode (DMPBAM[2, 4]≠11b).***	Yes	Yes/Serial EEPROM	0
12, 3	**Direct Master Read Prefetch Size Control** Values: 00b = The PEX 8311 continues to prefetch Read data from the internal PCI Bus until the Direct Master Read access is finished. This can result in an additional four unneeded Dwords being prefetched from the internal PCI Bus. 01b = Prefetch up to 4 Dwords from the internal PCI Bus. 10b = Prefetch up to 8 Dwords from the internal PCI Bus. 11b = Prefetch up to 16 Dwords from the internal PCI Bus. ***Caution: Direct Master Burst reads must not exceed the programmed limit.***	Yes	Yes/Serial EEPROM	00b
4	**Direct Master PCI Read Mode** Writing 0 indicates the PEX 8311 releases the internal PCI Bus when the Read FIFO becomes full. Writing 1 indicates the PEX 8311 retains the internal PCI Bus and de-assert IRDY# when the Read FIFO becomes full. ***Caution: To prevent constant locking of the internal PCI Bus, do not simultaneously enable this bit and Direct Master Read Ahead mode (DMPBAM[2, 4]≠11b).***	Yes	Yes/Serial EEPROM	0
10, 8:5	**Programmable Almost Full Flag** When the number of entries in the 64 Dword Direct Master Write FIFO exceeds a (programmed value +1, times 2), DMPAF is asserted high.	Yes	Yes/Serial EEPROM	00000b
9	**Memory Write and Invalidate Mode** When set to 1, the PEX 8311 waits for 8 or 16 Dwords to be written from the Local Bus before starting a PCI access. Memory Write and Invalidate cycles to the internal PCI Bus must be 8 or 16 Dword bursts.	Yes	Yes/Serial EEPROM	0
11	**Direct Master Prefetch Limit** Writing 0 results in continuous prefetch over the boundary space. Writing 1 causes the PEX 8311 to terminate a prefetch at 4-KB boundaries and restart when the boundary is crossed.	Yes	Yes/Serial EEPROM	0

Register 19-50. (DMPBAM; PCI:28h, LOC:A8h) PCI Base Address (Remap) for Direct Master-to-PCI Memory *(Cont.)*

Bits	Description	Read	Write	Default
13	**I/O Remap Select** Writing 0 uses DMPBAM[31:16] as PCI Address bits [31:16] for PCI I/O Direct Master transactions. Writing 1 forces PCI Address bits [31:16] to all zeros (0) for PCI I/O Direct Master transactions.	Yes	Yes/Serial EEPROM	0
15:14	**Direct Master Delayed Write Mode** Delays internal PCI Bus request after Direct Master Burst Write cycle has started. Values: 00b = No delay; immediately start cycle 01b = Delay 4 internal clocks 10b = Delay 8 internal clocks 11b = Delay 16 internal clocks	Yes	Yes/Serial EEPROM	00b
31:16	**Remap Local-to-PCI Space into PCI Address Space** Bits in this register remap (replace) Local Address bits used in decode as the PCI Address bits. ***Note:*** *Remap Address value must be a multiple of the DMRR range (**not** the Range register).*	Yes	Yes/Serial EEPROM	0h

Register 19-51. (DMCFGA; PCI:2Ch, LOC:ACh) PCI Configuration Address for Direct Master-to-PCI I/O Configuration

Bits	Description	Read	Write	Default
1:0	**Configuration Cycle Type** 00b = Type 0 01b = Type 1	Yes	Yes/Serial EEPROM	00b
7:2	**Register Number**	Yes	Yes/Serial EEPROM	0h
10:8	**Function Number**	Yes	Yes/Serial EEPROM	000b
15:11	**Device Number**	Yes	Yes/Serial EEPROM	0h
23:16	**Bus Number**	Yes	Yes/Serial EEPROM	0h
30:24	***Reserved***	Yes	No	0h
31	**Conversion Enable** When set, I/O accesses are converted to a Type 0 or Type 1 **LCS** PCI Configuration Space access. Fundamental for configuring the PCI Express bridge in Root Complex mode. ***Note:*** *Refer to the Direct Master Type 0 Configuration Cycle Example in Section 9.4.2.1, "Direct Master Configuration (PCI Type 0 or Type 1 Configuration Cycles)," for further details.*	Yes	Yes/Serial EEPROM	0

Register 19-52. (LAS1RR; PCI:F0h, LOC:170h) Direct Slave Local Address Space 1 Range

Bits	Description	Read	Write	Default
0	**Memory Space Indicator** Writing 0 indicates Local Address Space 1 maps into PCI Memory space. Writing 1 indicates Local Address Space 1 maps into PCI I/O space.	Yes	Yes/Serial EEPROM	0
2:1	When mapped into Memory space (LAS1RR[0]=0), the only valid value is 00b. Locate anywhere in PCI Address space. When mapped into I/O space (LAS1RR[0]=1), bit 1 must be cleared to 0. Bit 2 is included with LAS1RR[31:3] to indicate the decoding range.	Yes	Yes/Serial EEPROM	00b
3	When mapped into Memory space (LAS1RR[0]=0), writing 1 indicates reads are prefetchable (does not affect PEX 8311 operation, but is used for system status). When mapped into I/O space (LAS1RR[0]=1), included with LAS1RR[31:4, 2] to indicate the decoding range.	Yes	Yes/Serial EEPROM	0
31:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Address Space 1. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to Address bit 31. Write 1 to all bits that must be included in decode and 0 to all others. (Used in conjunction with PCIBAR3.) Default is 1 MB. When I_2O Decode is enabled (QSR[0]=1), defines PCIBAR0 (minimum range is 1,024 bytes). ***Notes:*** *LAS1RR range (**not** the Range register) must be power of 2. "Range register value" is two's complement of the range.* *Per PCI r2.2, limit I/O-Mapped spaces to 256 bytes per space.*	Yes	Yes/Serial EEPROM	FFF0000h

Register 19-53. (LAS1BA; PCI:F4h, LOC:174h) Direct Slave Local Address Space 1 Local Base Address (Remap)

Bits	Description	Read	Write	Default
0	**Local Address Space 1 Enable** Writing 1 enables decoding of PCI addresses for Direct Slave access to Local Address Space 1. Writing 0 disables decoding.	Yes	Yes/Serial EEPROM	0
1	***Reserved***	Yes	No	0
3:2	When Local Address Space 1 is mapped into Memory space (LAS1RR[0]=0), LAS1BA[3:2] must be 00b. When mapped into I/O space (LAS1RR[0]=1), included with LAS1BA[31:4] for remapping.	Yes	Yes/Serial EEPROM	00b
31:4	**Remap PCIBAR3 Base Address to Local Address Space 1 Base Address** The PCIBAR3 Base address translates to the Local Address Space 1 Base Address programmed in this register. A Direct Slave access to an offset from PCIBAR3 maps to the same offset from this Local Base Address. ***Note:*** *Remap Address value must be a multiple of the LAS1RR range (not the Range register).*	Yes	Yes/Serial EEPROM	0h

Register 19-54. (LBRD1; PCI:F8h, LOC:178h) Local Address Space 1 Bus Region Descriptor

Bits	Description	Read	Write	Default
1:0	**Local Address Space 1 Local Bus Data Width** Writing the following values indicates the associated bus data width: 00b = 8 bit 01b = 16 bit 10b or 11b = 32 bit	Yes	Yes/Serial EEPROM	11b
5:2	**Local Address Space 1 Internal Wait State Counter** Address-to-Data; Data-to-Data; 0 to 15 Wait States.	Yes	Yes/Serial EEPROM	0h
6	**Local Address Space 1 READY# Input Enable** Writing 1 enables READY# input. Writing 0 disables READY# input.	Yes	Yes/Serial EEPROM	1
7	**Local Address Space 1 Continuous Burst Enable** When bursting is enabled (LBRD1[8]=1), writing 1 enables Continuous Burst mode and writing 0 enables Burst-4 mode. Writing 1 additionally enables BTERM# input, which when asserted overrides the READY# input state (when READY# is enabled, LBRD1[6]=1). ***Note:*** *Refer to Section 8.4.2, "Local Bus Direct Slave Data Transfer Modes," for further details.*	Yes	Yes/Serial EEPROM	0
8	**Local Address Space 1 Burst Enable** Writing 1 enables bursting. Writing 0 disables bursting.	Yes	Yes/Serial EEPROM	0
9	**Local Address Space 1 Prefetch Disable** When mapped into Memory space (LAS1RR[0]=0), writing 0 enables Read prefetching. Writing 1 disables prefetching. When prefetching is disabled, the PEX 8311 disconnects after each Memory read.	Yes	Yes/Serial EEPROM	0
10	**Local Address Space 1 Prefetch Counter Enable** When cleared to 0, the PEX 8311 ignores the count and continues prefetching as follows: • **If PCI Read No Flush mode is enabled (MARBR[28]=1)** – Continues prefetching until the Direct Slave Read FIFO is full, or • **If PCI Read No Flush mode is disabled (MARBR[28]=0)** – Continues prefetching until PCI Read Completion, at which time the Direct Slave Read FIFO is flushed. When set to 1 and Memory prefetching is enabled, the PEX 8311 prefetches up to the number of Dwords specified in the Prefetch Counter (LBRD1[14:11]).	Yes	Yes/Serial EEPROM	0
14:11	**Local Address Space 1 Prefetch Counter** Number of Dwords to prefetch during Memory Read cycles (0 to 15). A count of zero selects a prefetch of 16 Dwords.	Yes	Yes/Serial EEPROM	0h
31:15	***Reserved***	Yes	No	0h

Register 19-55. (DMDAC; PCI:FCh, LOC:17Ch) Direct Master PCI Dual Address Cycles Upper Address

Bits	Description	Read	Write	Default
31:0	**Upper 32 Bits of PCI Dual Address Cycle PCI Address during Direct Master Cycles** When cleared to 0h, the PEX 8311 performs 32-bit address Direct Master access.	Yes	Yes	0h

Register 19-56. (PCIARB; PCI:100h, LOC:1A0h) Internal Arbiter Control

Bits	Description	Read	Write	Default
3:0	***Reserved***	Yes	Local/ Serial EEPROM	0h
31:4	***Reserved***	Yes	No	0h

Notes: *PCIARB registers must stay to their default values during normal operation.*

*PCIARB **cannot** be accessed from the internal PCI Bus by an I/O access, because of the PCI r2.2 PCI I/O space 256-byte limitation.*

Serial EEPROMs should load only zeros (0) to the PCIARB register.

Register 19-57. (PABTADR; PCI:104h, LOC:1A4h) PCI Abort Address

Bits	Description	Read	Write	Default
31:0	**PCI Abort Address** When a PCI Master/Target Abort occurs, the PCI address wherein the abort occurred is written to this register.	Yes	No	0h

Note: *PABTADR **cannot** be accessed from the internal PCI Bus by an I/O access, because of the PCI r2.2 PCI I/O space 256-byte limitation.*

19.7 Local Configuration Space Runtime Registers

Note: *"Yes" in the register Read and Write columns indicates the register is writable by the PCI Express interface and Local Bus.*

Register 19-58. (MBOX0; PCI:40h or 78h, LOC:C0h) Mailbox 0

Bits	Description	Read	Write	Default
31:0	**32-Bit Mailbox Register** ***Note:*** *The Inbound Queue Port register (IQP) replaces this register at PCI:40h when I2O Decode is enabled (QSR[0]=1). MBOX0 is always accessible at PCI address 78h and Local address C0h. Refer to Section 15.2.10, "I2O Enable Sequence," for further details.*	Yes	Yes/Serial EEPROM	0h

Register 19-59. (MBOX1; PCI:44h or 7Ch, LOC:C4h) Mailbox 1

Bits	Description	Read	Write	Default
31:0	**32-Bit Mailbox Register** ***Note:*** *The Outbound Queue Port register (OQP) replaces this register at PCI:44h when I2O Decode is enabled (QSR[0]=1). MBOX1 is always accessible at PCI address 7Ch and Local address C4h. Refer to Section 15.2.10, "I2O Enable Sequence," for further details.*	Yes	Yes/Serial EEPROM	0h

Register 19-60. (MBOX2; PCI:48h, LOC:C8h) Mailbox 2

Bits	Description	Read	Write	Default
31:0	**32-Bit Mailbox Register**	Yes	Yes	0h

Register 19-61. (MBOX3; PCI:4Ch, LOC:CCh) Mailbox 3

Bits	Description	Read	Write	Default
31:0	**32-Bit Mailbox Register**	Yes	Yes	0h

Register 19-62. (MBOX4; PCI:50h, LOC:D0h) Mailbox 4

Bits	Description	Read	Write	Default
31:0	**32-Bit Mailbox Register**	Yes	Yes	0h

Register 19-63. (MBOX5; PCI:54h, LOC:D4h) Mailbox 5

Bits	Description	Read	Write	Default
31:0	**32-Bit Mailbox Register**	Yes	Yes	0h

Register 19-64. (MBOX6; PCI:58h, LOC:D8h) Mailbox 6

Bits	Description	Read	Write	Default
31:0	**32-Bit Mailbox Register**	Yes	Yes	0h

Register 19-65. (MBOX7; PCI:5Ch, LOC:DCh) Mailbox 7

Bits	Description	Read	Write	Default
31:0	**32-Bit Mailbox Register**	Yes	Yes	0h

Register 19-66. (P2LDBELL; PCI:60h, LOC:E0h) PCI-to-Local Doorbell

Bits	Description	Read	Write	Default
31:0	**Doorbell Register** The internal PCI Bus Master can write to this register and assert a Local interrupt output (LINTo#) to the Local processor. The Local processor can then read this register to determine which Doorbell bit was set. The internal PCI Bus Master sets the doorbell by writing 1 to a particular bit. The Local processor can clear a Doorbell bit by writing 1 to that bit position.	Yes	Yes/Clr	0h

Register 19-67. (L2PDBELL; PCI:64h, LOC:E4h) Local-to-PCI Doorbell

Bit	Description	Read	Write	Default
31:0	**Doorbell Register** The Local processor can write to this register and assert the internal PCI wire interrupt (INTA#). The internal PCI Bus Master can then read this register to determine which Doorbell bit was set. The Local processor sets the doorbell by writing 1 to a particular bit. The internal PCI Bus Master can clear a Doorbell bit by writing 1 to that bit position.	Yes	Yes/Clr	0h

Register 19-68. (INTCSR; PCI:68h, LOC:E8h) Interrupt Control/Status

Bits	Description	Read	Write	Default
0	**Enable Interrupt Sources (Bit 0)** Writing 1 enables LSERR# to assert upon detection of a Local Parity error or PCI Abort. ***Note:*** *Refer to Figure 13-2, "Local Interrupt and Error Sources," for further details.*	Yes	Yes	0
1	**Enable Interrupt Sources (Bit 1)** Writing 1 enables LSERR# to assert upon detection of an internal SERR# assertion in Root Complex mode, or detection of a PCI Parity error or a messaging queue outbound overflow. ***Note:*** *Refer to Figure 13-2, "Local Interrupt and Error Sources," for further details.*	Yes	Yes	0
2	**Generate Internal PCI Bus Internal SERR# Interrupt** When cleared to 0, writing 1 asserts the internal SERR# interrupt.	Yes	Yes	0
3	**Mailbox Interrupt Enable** Writing 1 enables a Local interrupt output (LINTo#) to assert when the internal PCI Bus writes to MBOX0 through MBOX3. To clear a LINTo# interrupt, the Local Bus Master must read the Mailbox. Used in conjunction with the Local Interrupt Output Enable bit (INTCSR[16]).	Yes	Yes	0
4	**Power Management Interrupt Enable** Writing 1 enables a Local interrupt output (LINTo#) to assert when the Power Management Power State changes.	Yes	Yes	0
5	**Power Management Interrupt** When set to 1, indicates a Power Management interrupt is pending. A Power Management interrupt is caused by a change in the Power Management Control/Status register Power State bits (PMCSR[1:0]). Writing 1 clears the interrupt. Writable from the internal PCI Bus only in the D0 power state.	Yes	Yes/Clr	0
6	**Direct Master Write/Direct Slave Read Local Data Parity Check Error Enable** Writing 1 enables a Local Bus Data Parity Error signal to assert through the LSERR# ball. INTCSR[0] must be enabled for this to have an effect.	Yes	Yes	0
7	**Direct Master Write/Direct Slave Read Local Data Parity Check Error Status** When set to 1, indicates the PEX 8311 detected a Local Data Parity Check error, regardless of whether the *Parity Check Error* bit is disabled (INTCSR[6]=0). Writing 1 clears this bit to 0.	Yes	Yes/Clr	0

Register 19-68. (INTCSR; PCI:68h, LOC:E8h) Interrupt Control/Status *(Cont.)*

Bits	Description	Read	Write	Default
8	**Internal PCI Wire Interrupt Enable** Writing 1 enables internal PCI wire interrupts (INTA#).	Yes	Yes	1
9	**PCI Doorbell Interrupt Enable** Writing 1 enables Local-to-PCI Doorbell interrupts. Used in conjunction with the *Internal PCI Wire Interrupt Enable* bit (INTCSR[8]). Clearing the L2PDBELL register bits that caused the interrupt also clears the interrupt.	Yes	Yes	0
10	**PCI Abort Interrupt Enable** Value of 1 enables a Master Abort or Master detection of a Target Abort to assert the internal PCI wire interrupt (INTA#). Used in conjunction with the *Internal PCI Wire Interrupt Enable* bit (INTCSR[8]). Clearing the Received Master and Target Abort bits (PCISR[13:12]) also clears the PCI interrupt.	Yes	Yes	0
11	**Local Interrupt Input Enable** Writing 1 enables a Local interrupt input (LINTi#) assertion to assert the internal PCI wire interrupt (INTA#). Used in conjunction with the *Internal PCI Wire Interrupt Enable* bit (INTCSR[8]). De-asserting LINTi# also clears the interrupt.	Yes	Yes	0
12	**Retry Abort Enable** Writing 1 enables the PEX 8311 to treat 256 consecutive internal Master Retrys to a Target (PCI Express Address space) as a Target Abort. Writing 0 enables the PEX 8311 to attempt Master Retrys indefinitely.	Yes	Yes	0
13	**PCI Doorbell Interrupt Active** When set to 1, indicates the PCI Doorbell interrupt is active.	Yes	No	0
14	**PCI Abort Interrupt Active** When set to 1, indicates the PCI Master or Target Abort interrupt is active.	Yes	No	0
15	**Local Interrupt Input Active** When set to 1, indicates the Local interrupt input (LINTi#) is active.	Yes	No	0

Register 19-68. (INTCSR; PCI:68h, LOC:E8h) Interrupt Control/Status *(Cont.)*

Bits	Description	Read	Write	Default
16	**Local Interrupt Output Enable** Writing 1 enables Local interrupt output (LINTo#).	Yes	Yes	1
17	**Local Doorbell Interrupt Enable** Writing 1 enables PCI-to-Local Doorbell interrupts. Used in conjunction with the Local Interrupt Output Enable bit (INTCSR[16]). Clearing the P2LDBELL register bits that caused the interrupt also clears the interrupt.	Yes	Yes	0
18	**DMA Channel 0 Interrupt Enable** Writing 1 enables DMA Channel 0 interrupts. Used in conjunction with the DMA Channel 0 Interrupt Select bit (DMAMODE0[17]). Setting the DMA Channel 0 Clear Interrupt bit (DMACSR0[3]=1) also clears the interrupt.	Yes	Yes	0
19	**DMA Channel 1 Interrupt Enable** Writing 1 enables DMA Channel 1 interrupts. Used in conjunction with the DMA Channel 1 Interrupt Select bit (DMAMODE1[17]). Setting the DMA Channel 1 Clear Interrupt bit (DMACSR1[3]=1) also clears the interrupt.	Yes	Yes	0
20	**Local Doorbell Interrupt Active** Reading 1 indicates the Local Doorbell interrupt is active.	Yes	No	0
21	**DMA Channel 0 Interrupt Active** Reading 1 indicates the DMA Channel 0 interrupt is active.	Yes	No	0
22	**DMA Channel 1 Interrupt Active** Reading 1 indicates the DMA Channel 1 interrupt is active.	Yes	No	0
23	**Built-In Self-Test (BIST) Interrupt Active** Reading 1 indicates the BIST interrupt is active. The BIST interrupt is enabled by writing 1 to the PCI Built-In Self-Test Interrupt Enable bit (PCIBISTR[6]=1). Clearing the Enable bit (PCIBISTR[6]=0) also clears the interrupt. ***Note:*** *Refer to the PCIBISTR register for a description of the self-test.*	Yes	No	0
24	Reading 0 indicates the Direct Master was the Bus Master during a Master or Target Abort.	Yes	No	1
25	Reading 0 indicates that DMA Channel 0 was the Bus Master during a Master or Target Abort.	Yes	No	1
26	Reading 0 indicates that DMA Channel 1 was the Bus Master during a Master or Target Abort.	Yes	No	1
27	Reading 0 indicates that the PEX 8311 asserted a Target Abort after internal 256 consecutive Master Retrys to a Target (PCI Express Address Spaces).	Yes	No	1
28	Reading 1 indicates that the internal PCI Bus wrote data to MBOX0. Enabled only when the Mailbox Interrupt Enable bit is set (INTCSR[3]=1).	Yes	No	0
29	Reading 1 indicates that the internal PCI Bus wrote data to MBOX1. Enabled only when the Mailbox Interrupt Enable bit is set (INTCSR[3]=1).	Yes	No	0
30	Reading 1 indicates that the internal PCI Bus wrote data to MBOX2. Enabled only when the Mailbox Interrupt Enable bit is set (INTCSR[3]=1).	Yes	No	0
31	Reading 1 indicates that the internal PCI Bus wrote data to MBOX3. Enabled only when the Mailbox Interrupt Enable bit is set (INTCSR[3]=1).	Yes	No	0

Register 19-69. (CNTRL; PCI:6Ch, LOC:ECh) Serial EEPROM Control, PCI Command Codes, User I/O Control, and Init Control

Bits	Description	Read	Write	Default
3:0	**PCI Read Command Code for DMA**	Yes	Yes	1110b
7:4	**PCI Write Command Code for DMA**	Yes	Yes	0111b
11:8	**PCI Memory Read Command Code for Direct Master**	Yes	Yes	0110b
15:12	**PCI Memory Write Command Code for Direct Master**	Yes	Yes	0111b
16	**General-Purpose Output** Writing 1 causes USERo output to go high. Writing 0 causes USERo output to go low.	Yes	Yes	1
17	**General-Purpose Input** Reading 1 indicates the USERi ball is high. Reading 0 indicates the USERi ball is low.	Yes	No	–
18	**USERi or LLOCKi# Pin Select** Writing 1 selects USERi as an input to the PEX 8311. Writing 0 selects LLOCKi# as an input to the PEX 8311.	Yes	Yes	1
19	**USERo or LLOCKo# Pin Select** Writing 1 selects USERo as an output from the PEX 8311. Writing 0 selects LLOCKo# as an output from the PEX 8311.	Yes	Yes	1
20	**LINTo# Interrupt Status** When ROOT_COMPLEX# is enabled, reading 1 indicates the LINTo# interrupt is active by way of the internal PCI wire interrupt (INTA#). Writing 1 clears this bit to 0.	Yes	Yes/Clr	0
21	**LSERR# Interrupt Status** When ROOT_COMPLEX# is enabled, reading 1 indicates the LSERR# interrupt is active by way of the internal SERR# System error. Writing 1 clears this bit to 0.	Yes	Yes/Clr	0
23:22	***Reserved***	Yes	No	00b
24	**Serial EEPROM Clock for PCI or Local Bus Reads or Writes to Serial EEPROM (EESK)** Toggling this bit toggles the serial EEPROM clock output.	Yes	Yes	0
25	**Serial EEPROM Chip Select (EECS).** For PCI or Local Bus reads or writes to the serial EEPROM, setting this bit to 1 provides the serial EEPROM Chip Select output.	Yes	Yes	0
26	**Write Bit to Serial EEPROM (EEDI)** For writes, the EEDI output signal is input to the serial EEPROM. Clocked into the serial EEPROM by the serial EEPROM clock. ***Note:*** *Refer to Section 4.3.3, "Serial EEPROM Access," for further details.*	Yes	Yes	0
27	**Read Bit from Serial EEPROM (EEDO)** ***Note:*** *Refer to Section 4.3.3, "Serial EEPROM Access," for further details.*	Yes	No	–

Register 19-69. (CNTRL; PCI:6Ch, LOC:ECh) Serial EEPROM Control, PCI Command Codes, User I/O Control, and Init Control *(Cont.)*

Bits	Description	Read	Write	Default
28	**Serial EEPROM Present** When set to 1, indicates that a blank or programmed serial EEPROM is present (*Serial EEPROM Start* bit detected).	Yes	No	0
29	**Reload Configuration Registers** When cleared to 0, writing 1 causes the PEX 8311 to reload the **LCS Configuration** registers from the serial EEPROM. ***Note:*** *Not self-clearing.*	Yes	Yes	0
30	**Local Bus Reset (Endpoint Mode)** Writing 1 holds the PEX 8311 Local Bus logic in a reset state, and asserts LRESET# output. Contents of the **PCI Configuration** and **Runtime** registers are not reset. A Local Bus Reset is cleared only from the internal PCI Bus. **PCI Express Bridge Reset (Root Complex Mode)** Writing 1 holds the PEX 8311 internal PCI Bus logic and DMA Configuration registers in a reset state, and asserts PERST# output. Contents of the **LCS Configuration**, **Runtime**, and **Messaging Queue** registers are not reset. A PCI Express Bridge Reset is cleared only from the Local Bus.	Yes	Yes	0
31	**EEDO Input Enable** When set to 1, the EEDI/EEDO I/O buffer is placed in a bus high-impedance state, enabling the serial EEPROM data to be read. The serial EEPROM data resides in CNTRL[27]. Cleared to 0 to allow VPD cycles to occur.	Yes	Yes	0

Register 19-70. (PCIHIDR; PCI:70h, LOC:F0h) PCI Hardwired Configuration ID

Bits	Description	Read	Write	Default
15:0	**Vendor ID** Identifies the device manufacturer. Hardwired to the PLX PCI-SIG-issued Vendor ID, 10B5h.	Yes	No	10B5h
31:16	**Device ID** Identifies the particular device. Hardwired to 9056h.	Yes	No	9056h

Register 19-71. (PCIHREV; PCI:74h, LOC:F4h) PCI Hardwired Revision ID

Bits	Description	Read	Write	Default
7:0	**Revision ID** Hardwired silicon revision of the PEX 8311 Local Bus logic.	Yes	No	Current Rev # (AAh)

19.8 Local Configuration Space DMA Registers

Note: *"Yes" in the register Read and Write columns indicates the register is writable by the PCI Express interface and Local Bus.*

Register 19-72. (DMAMODE0; PCI:80h, LOC:100h) DMA Channel 0 Mode

Bits	Description	Read	Write	Value after Reset
1:0	**DMA Channel 0 Local Bus Data Width** Writing the following values indicates the associated bus data width: 00b = 8 bit 01b = 16 bit 10b or 11b = 32 bit	Yes	Yes	11b
5:2	**DMA Channel 0 Internal Wait State Counter** Address-to-Data; Data-to-Data; 0 to 15 Wait States.	Yes	Yes	0h
6	**DMA Channel 0 READY# Input Enable** Writing 1 enables READY# input. Writing 0 disables READY# input.	Yes	Yes	1
7	**DMA Channel 0 Continuous Burst Enable** When bursting is enabled (DMAMODE0[8]=1), writing 1 enables Continuous Burst mode and writing 0 enables Burst-4 mode. Writing 1 additionally enables BTERM# input, which when asserted overrides the READY# input state (when READY# is enabled, DMAMODE0[6]=1). ***Note:*** *Refer to Section 8.5.18, "Local Bus DMA Data Transfer Modes," for further details.*	Yes	Yes	0
8	**DMA Channel 0 Local Burst Enable** Writing 1 enables Local bursting. Writing 0 disables Local bursting.	Yes	Yes	0
9	**DMA Channel 0 Scatter/Gather Mode.** Writing 1 indicates DMA Scatter/Gather mode is enabled. For Scatter/Gather mode, the DMA source and destination addresses and byte count are loaded from memory in PCI or Local Address spaces. Writing 0 indicates DMA Block mode is enabled.	Yes	Yes	0
10	**DMA Channel 0 Done Interrupt Enable** Writing 1 enables an interrupt when done. Writing 0 disables an interrupt when done. When DMA Clear Count mode is enabled (DMAMODE0[16]=1), the interrupt does not occur until the Byte Count is cleared.	Yes	Yes	0
11	**DMA Channel 0 Local Addressing Mode** Writing 1 holds the Local Address Bus constant. Writing 0 indicates the Local Address is incremented.	Yes	Yes	0

Register 19-72. (DMAMODE0; PCI:80h, LOC:100h) DMA Channel 0 Mode *(Cont.)*

Bits	Description	Read	Write	Value after Reset
12	**DMA Channel 0 Demand Mode** Writing 1 causes the DMA Channel 0 DMA Controller to operate in Demand mode. In Demand mode, the DMA Controller transfers data when its DREQ0# input is asserted. Asserts DACK0# to indicate the current Local Bus transfer is in response to DREQ0# input. The DMA Controller transfers Dwords (32 bits) of data. This could result in multiple transfers for an 8- or 16-bit bus.	Yes	Yes	0
13	**DMA Channel 0 Memory Write and Invalidate Mode for DMA Transfers** When set to 1, the PEX 8311 performs Memory Write and Invalidate cycles to the internal PCI Bus. The PEX 8311 supports Memory Write and Invalidate sizes of 8 or 16 Dwords. The size is specified in the System Cache Line Size bits (PCICLSR[7:0]). When a size other than 8 or 16 is specified, the PEX 8311 performs Write transfers, rather than Memory Write and Invalidate transfers. Transfers must start and end at cache line boundaries. PCICR[4] must be set to 1.	Yes	Yes	0
14	**DMA Channel 0 EOT# Enable** Writing 1 enables the EOT# input ball. Writing 0 disables the EOT# input ball. When DMAMODE0[14] and DMAMODE1[14]=00b, the EOT# ball becomes the DMPAF ball.	Yes	Yes	0
15	**DMA Channel 0 Fast/Slow Terminate Mode Select** Writing 0 sets the PEX 8311 into Slow Terminate mode. As a result, BLAST# is asserted on the last Data transfer to terminate the DMA transfer. Writing 1 sets the PEX 8311 into Fast Terminate mode, and indicates the PEX 8311 DMA transfer terminates immediately when EOT# (when enabled) is asserted, or during DMA Demand mode when DREQ0# is de-asserted.	Yes	Yes	0

Register 19-72. (DMAMODE0; PCI:80h, LOC:100h) DMA Channel 0 Mode *(Cont.)*

Bits	Description	Read	Write	Value after Reset
16	**DMA Channel 0 Clear Count Mode** Writing 1 clears the Byte Count in each Scatter/Gather descriptor when the corresponding DMA transfer is complete.	Yes	Yes	0
17	**DMA Channel 0 Interrupt Select** Writing 1 routes the DMA Channel 0 interrupt to the internal PCI wire interrupt (INTA#). Writing 0 routes the DMA Channel 0 interrupt to the Local interrupt output (LINTo#).	Yes	Yes	0
18	**DMA Channel 0 DAC Chain Load** When set to 1, enables the descriptor to load the PCI Dual Address Cycles value. Otherwise, the descriptor loads the DMADAC0 register contents.	Yes	Yes	0
19	**DMA Channel 0 EOT# End Link** Used only for DMA Scatter/Gather transfers. Value of 1 indicates that when EOT# is asserted, the DMA transfer ends the current Scatter/Gather link and continues with the remaining Scatter/Gather transfers. Value of 0 indicates that when EOT# is asserted, the DMA transfer ends the current Scatter/Gather transfer and does not continue with the remaining Scatter/Gather transfers.	Yes	Yes	0
20	**DMA Channel 0 Ring Management Valid Mode Enable** Value of 0 indicates the Ring Management Valid bit (DMASIZ0[31]) is ignored. Value of 1 indicates the DMA descriptors are processed only when the Ring Management Valid bit is set (DMASIZ0[31]=1). When the Valid bit is set, the transfer count is 0, and the descriptor is not the last descriptor in the chain. The DMA Channel 0 DMA Controller then moves to the next descriptor in the chain. ***Note:*** *Descriptor Memory fields are re-ordered when this bit is set.*	Yes	Yes	0
21	**DMA Channel 0 Ring Management Valid Stop Control** Value of 0 indicates the DMA Scatter/Gather controller continuously polls a descriptor with the Valid bit cleared to 0 (invalid descriptor) when Ring Management Valid Mode is enabled (DMAMODE0[20]=1). Value of 1 indicates the Scatter/Gather controller stops polling when the Ring Management Valid bit with a value of 0 is detected (DMASIZ0[31]=0). In this case, the CPU must restart the DMA Channel 0 DMA Controller by setting the Start bit (DMACSR0[1]=1). A pause clearing the Start bit (DMACSR0[1]=0) sets the DMA Done bit (DMACSR0[4]=1).	Yes	Yes	0
31:22	***Reserved***	Yes	No	0h

Register 19-73. (DMAPADR0; (PCI:84h, LOC:104h when DMAMODE0[20]=0 or PCI:88h, LOC:108h when DMAMODE0[20]=1) DMA Channel 0 PCI Address

Bits	Description	Read	Write	Default
31:0	**DMA Channel 0 PCI Address** Indicates from where in PCI Memory space DMA transfers (reads or writes) start. Value is a physical address.	Yes	Yes	0h

Register 19-74. (DMALADR0; PCI:88h, LOC:108h when DMAMODE0[20]=0 or PCI:8Ch, LOC:10Ch when DMAMODE0[20]=1) DMA Channel 0 Local Address

Bits	Description	Read	Write	Default
31:0	**DMA Channel 0 Local Address** Indicates from where in Local Memory space DMA transfers (reads or writes) start.	Yes	Yes	0h

Register 19-75. (DMASIZ0; PCI:8Ch, LOC:10Ch when DMAMODE0[20]=0 or PCI:84h, LOC:104h when DMAMODE0[20]=1) DMA Channel 0 Transfer Size (Bytes)

Bits	Description	Read	Write	Default
22:0	**DMA Channel 0 Transfer Size (Bytes)** Indicates the number of bytes to transfer during a DMA operation.	Yes	Yes	0h
30:23	***Reserved***	Yes	No	0h
31	**DMA Channel 0 Ring Management Valid** When Ring Management Valid Mode is enabled (DMAMODE0[20]=1), indicates the validity of this DMA descriptor.	Yes	Yes	0

Register 19-76. (DMADPR0; PCI:90h, LOC:110h) DMA Channel 0 Descriptor Pointer

Bits	Description	Read	Write	Default
0	**DMA Channel 0 Descriptor Location** Writing 1 indicates PCI Address space. Writing 0 indicates Local Address space.	Yes	Yes	0
1	**DMA Channel 0 End of Chain** Writing 1 indicates end of chain. Writing 0 indicates not end of chain descriptor. (Same as DMA Block mode.)	Yes	Yes	0
2	**DMA Channel 0 Interrupt after Terminal Count** Writing 1 causes an interrupt to assert after the terminal count for this descriptor is reached. Writing 0 disables interrupts from being asserted.	Yes	Yes	0
3	**DMA Channel 0 Direction of Transfer** Writing 1 indicates transfers from the Local Bus to the internal PCI Bus. Writing 0 indicates transfers from the internal PCI Bus to the Local Bus.	Yes	Yes	0
31:4	**DMA Channel 0 Next Descriptor Address** X0h-aligned (DMADPR0[3:0]=0h).	Yes	Yes	0h

Register 19-77. (DMAMODE1; PCI:94h, LOC:114h) DMA Channel 1 Mode

Bits	Description	Read	Write	Default
1:0	**DMA Channel 1 Local Bus Data Width** Writing the following values indicates the associated bus data width: 00b = 8 bit 01b = 16 bit 10b or 11b = 32 bit	Yes	Yes	11b
5:2	**DMA Channel 1 Internal Wait State Counter** Address-to-Data; Data-to-Data; 0 to 15 Wait States.	Yes	Yes	0h
6	**DMA Channel 1 READY# Input Enable** Writing 1 enables READY# input. Writing 0 disables READY# input.	Yes	Yes	1
7	**DMA Channel 0 Continuous Burst Enable** When bursting is enabled (DMAMODE1[8]=1), writing 1 enables Continuous Burst mode and writing 0 enables Burst-4 mode. Writing 1 additionally enables BTERM# input, which when asserted overrides the READY# input state (when READY# is enabled, DMAMODE1[6]=1). ***Note:*** *Refer to Section 8.5.18, "Local Bus DMA Data Transfer Modes," for further details.*	Yes	Yes	0
8	**DMA Channel 1 Local Burst Enable** Writing 1 enables Local bursting. Writing 0 disables Local bursting.	Yes	Yes	0
9	**DMA Channel 1 Scatter/Gather Mode.** Writing 1 indicates DMA Scatter/Gather mode is enabled. For Scatter/Gather mode, the DMA source and destination addresses and byte count are loaded from memory in PCI or Local Address spaces. Writing 0 indicates DMA Block mode is enabled.	Yes	Yes	0
10	**DMA Channel 1 Done Interrupt Enable** Writing 1 enables an interrupt when done. Writing 0 disables an interrupt when done. When DMA Clear Count mode is enabled (DMAMODE1[16]=1), the interrupt does not occur until the Byte Count is cleared.	Yes	Yes	0
11	**DMA Channel 1 Local Addressing Mode** Writing 1 holds the Local Address Bus constant. Writing 0 indicates the Local Address is incremented.	Yes	Yes	0

Register 19-77. (DMAMODE1; PCI:94h, LOC:114h) DMA Channel 1 Mode *(Cont.)*

Bits	Description	Read	Write	Default
12	**DMA Channel 1 Demand Mode** Writing 1 causes the DMA Channel 1 DMA Controller to operate in Demand mode. In Demand mode, the DMA Controller transfers data when its DREQ1# input is asserted. Asserts DACK1# to indicate the current Local Bus transfer is in response to DREQ1# input. The DMA Controller transfers Dwords (32 bits) of data. This could result in multiple transfers for an 8- or 16-bit bus.	Yes	Yes	0
13	**DMA Channel 1 Memory Write and Invalidate Mode for DMA Transfers** When set to 1, the PEX 8311 performs Memory Write and Invalidate cycles to the internal PCI Bus. The PEX 8311 supports Memory Write and Invalidate sizes of 8 or 16 Dwords. The size is specified in the System Cache Line Size bits (PCICLSR[7:0]). When a size other than 8 or 16 is specified, the PEX 8311 performs Write transfers, rather than Memory Write and Invalidate transfers. Transfers must start and end at cache line boundaries. PCICR[4] must be set to 1.	Yes	Yes	0
14	**DMA Channel 1 EOT# Enable** Writing 1 enables the EOT# input ball. Writing 0 disables the EOT# input ball. When DMAMODE0[14] and DMAMODE1[14]=00b, the EOT# ball becomes the DMPAF ball.	Yes	Yes	0
15	**DMA Channel 1 Fast/Slow Terminate Mode Select** Writing 0 sets the PEX 8311 into Slow Terminate mode. As a result, BLAST# is asserted on the last Data transfer to terminate the DMA transfer. Writing 1 sets the PEX 8311 into Fast Terminate mode, and indicates the PEX 8311 DMA transfer terminates immediately when EOT# (when enabled) is asserted, or during DMA Demand mode when DREQ1# is de-asserted.	Yes	Yes	0

Register 19-77. (DMAMODE1; PCI:94h, LOC:114h) DMA Channel 1 Mode *(Cont.)*

Bits	Description	Read	Write	Default
16	**DMA Channel 1 Clear Count Mode** Writing 1 clears the Byte Count in each Scatter/Gather descriptor when the corresponding DMA transfer is complete.	Yes	Yes	0
17	**DMA Channel 1 Interrupt Select** Writing 0 routes the DMA Channel 1 interrupt to the Local interrupt output (LINTo#). Writing 1 routes the DMA Channel 1 interrupt to the internal PCI wire interrupt (INTA#).	Yes	Yes	0
18	**DMA Channel 1 DAC Chain Load** When set to 1, enables the descriptor to load the PCI Dual Address Cycles value. Otherwise, the descriptor loads the DMADAC1 register contents.	Yes	Yes	0
19	**DMA Channel 1 EOT# End Link** Used only for DMA Scatter/Gather transfers. Value of 1 indicates that when EOT# is asserted, the DMA transfer ends the current Scatter/Gather link and continues with the remaining Scatter/Gather transfers. Value of 0 indicates that when EOT# is asserted, the DMA transfer ends the current Scatter/Gather transfer and does not continue with the remaining Scatter/Gather transfers.	Yes	Yes	0
20	**DMA Channel 1 Ring Management Valid Mode Enable** Value of 0 indicates the Ring Management Valid bit (DMASIZ1[31]) is ignored. Value of 1 indicates the DMA descriptors are processed only when the Ring Management Valid bit is set (DMASIZ1[31]=1). When the Valid bit is set, the transfer count is 0, and the descriptor is not the last descriptor in the chain. The DMA Channel 1 DMA Controller then moves to the next descriptor in the chain. ***Note:*** *Descriptor Memory fields are re-ordered when this bit is set.*	Yes	Yes	0
21	**DMA Channel 1 Ring Management Valid Stop Control** Value of 0 indicates the DMA Scatter/Gather controller continuously polls a descriptor with the Valid bit cleared to 0 (invalid descriptor) when Ring Management Valid Mode is enabled (DMAMODE1[20]=1). Value of 1 indicates the Scatter/Gather controller stops polling when the Ring Management Valid bit with a value of 0 is detected (DMASIZ1[31]=0). In this case, the CPU must restart the DMA Channel 1 DMA Controller by setting the Start bit (DMACSR1[1]=1). A pause clearing the Start bit (DMACSR1[1]=0) sets the DMA Done bit (DMACSR1[4]=1).	Yes	Yes	0
31:22	***Reserved***	Yes	No	0h

Register 19-78. (DMAPADR1;PCI:98h, LOC:118h when DMAMODE1[20]=0 or PCI:9Ch, LOC:11Ch when DMAMODE1[20]=1) DMA Channel 1 PCI Address

Bits	Description	Read	Write	Default
31:0	**DMA Channel 1 PCI Address** Indicates from where in PCI Memory space DMA transfers (reads or writes) start. Value is a physical address.	Yes	Yes	0h

Register 19-79. (DMALADR1;PCI:9Ch, LOC:11Ch when DMAMODE1[20]=0 or PCI:A0h, LOC:120h when DMAMODE1[20]=1) DMA Channel 1 Local Address

Bits	Description	Read	Write	Default
31:0	**DMA Channel 1 Local Address** Indicates from where in Local Memory space DMA transfers (reads or writes) start.	Yes	Yes	0h

Register 19-80. (DMASIZ1; PCI:A0h, LOC:120h when DMAMODE1[20]=0 or PCI:98h, LOC:118h when DMAMODE1[20]=1) DMA Channel 1 Transfer Size (Bytes)

Bits	Description	Read	Write	Default
22:0	**DMA Channel 1 Transfer Size (Bytes)** Indicates the number of bytes to transfer during a DMA operation.	Yes	Yes	0h
30:23	***Reserved***	Yes	No	0h
31	**DMA Channel 1 Ring Management Valid** When Ring Management Valid Mode is enabled (DMAMODE1[20]=1), indicates the validity of this DMA descriptor.	Yes	Yes	0

Register 19-81. (DMADPR1; PCI:A4h, LOC:124h) DMA Channel 1 Descriptor Pointer

Bits	Description	Read	Write	Default
0	**DMA Channel 1 Descriptor Location** Writing 1 indicates PCI Address space. Writing 0 indicates Local Address space.	Yes	Yes	0
1	**DMA Channel 1 End of Chain** Writing 1 indicates end of chain. Writing 0 indicates not end of chain descriptor. (Same as DMA Block mode.)	Yes	Yes	0
2	**DMA Channel 1 Interrupt after Terminal Count** Writing 1 causes an interrupt to assert after the terminal count for this descriptor is reached. Writing 0 disables interrupts from being asserted.	Yes	Yes	0
3	**DMA Channel 1 Direction of Transfer.** Writing 1 indicates transfers from the Local Bus to the internal PCI Bus. Writing 0 indicates transfers from the internal PCI Bus to the Local Bus.	Yes	Yes	0
31:4	**DMA Channel 1 Next Descriptor Address** X0h-aligned (DMADPR1[3:0]=0h).	Yes	Yes	0h

Register 19-82. (DMACSR0; PCI:A8h, LOC:128h) DMA Channel 0 Command/Status

Bits	Description	Read	Write	Default
0	**DMA Channel 0 Enable** Writing 1 enables the channel to transfer data. Writing 0 disables the channel from starting a DMA transfer, and when in the process of transferring data, suspends the transfer (pause).	Yes	Yes	0
1	**DMA Channel 0 Start** Writing 1 causes the channel to start transferring data when the channel is enabled.	No	Yes/Set	0
2	**DMA Channel 0 Abort** Writing 1 causes the channel to abort the current transfer. The DMA Channel 0 Enable bit must be cleared (DMACSR0[0]=0). Sets the DMA Channel 0 Done bit (DMACSR0[4]=1) when the abort is complete.	No	Yes/Set	0
3	**DMA Channel 0 Clear Interrupt** Writing 1 clears DMA Channel 0 interrupts.	No	Yes/Clr	0
4	**DMA Channel 0 Done** Reading 1 indicates the transfer is complete. The transfer is complete because the DMA transfer finished successfully, or the DMA transfer was aborted when software set the Abort bit (DMACSR0[2]=1). Reading 0 indicates the Channel transfer is not complete.	Yes	No	1
7:5	***Reserved***	Yes	No	000b

Register 19-83. (DMACSR1; PCI:A9h, LOC:129h) DMA Channel 1 Command/Status

Bits	Description	Read	Write	Default
0	**DMA Channel 1 Enable** Writing 1 enables the channel to transfer data. Writing 0 disables the channel from starting a DMA transfer, and when in the process of transferring data, suspends the transfer (pause).	Yes	Yes	0
1	**DMA Channel 1 Start** Writing 1 causes channel to start transferring data when the channel is enabled.	No	Yes/Set	0
2	**DMA Channel 1 Abort** Writing 1 causes the channel to abort the current transfer. The DMA Channel 1 Enable bit must be cleared (DMACSR1[0]=0). Sets the DMA Channel 1 Done bit (DMACSR1[4]=1) when the abort is complete.	No	Yes/Set	0
3	**DMA Channel 1 Clear Interrupt** Writing 1 clears DMA Channel 1 interrupts.	No	Yes/Clr	0
4	**DMA Channel 1 Done** Reading 1 indicates the transfer is complete. The transfer is complete because the DMA transfer finished successfully, or the DMA transfer was aborted when software set the Abort bit (DMACSR1[2]=1). Reading 0 indicates the Channel transfer is not complete.	Yes	No	1
7:5	***Reserved***	Yes	No	000b

Register 19-84. (DMAARB; PCI:ACh, LOC:12Ch) DMA Arbitration

Same as Register 19-39 (MARBR; PCI:08h or ACh, LOC:88h or 12Ch) Mode/DMA Arbitration.

Register 19-85. (DMATHR; PCI:B0h, LOC:130h) DMA Threshold

Bits	Description	Read	Write	Default
3:0	**DMA Channel 0 PCI-to-Local Almost Full (C0PLAF)** Number of full (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the Local Bus for writes. Nybble values 0h through Eh are used. (Refer to Table 19-9.) (15 - C0PLAF) > C0LPAE.	Yes	Yes	0h
7:4	**DMA Channel 0 Local-to-PCI Almost Empty (C0LPAE)** Number of empty (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the Local Bus for reads. Nybble values 0h through Eh are used. (Refer to Table 19-9.) (15 - C0PLAF) > C0LPAE.	Yes	Yes	0h
11:8	**DMA Channel 0 Local-to-PCI Almost Full (C0LPAF)** Number of full (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the internal PCI Bus for writes. Nybble values 0h through Eh are used. (Refer to Table 19-9.)	Yes	Yes	0h
15:12	**DMA Channel 0 PCI-to-Local Almost Empty (C0PLAE)** Number of empty (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the internal PCI Bus for reads. Nybble values 0h through Eh are used. (Refer to Table 19-9.)	Yes	Yes	0h
19:16	**DMA Channel 1 PCI-to-Local Almost Full (C1PLAF)** Number of full (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the Local Bus for writes. Nybble values 0h through Eh are used. (Refer to Table 19-9.) (15 - C1PLAF) > C1LPAE.	Yes	Yes	0h
23:20	**DMA Channel 1 Local-to-PCI Almost Empty (C1LPAE)** Number of empty (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the Local Bus for reads. Nybble values 0h through Eh are used. (Refer to Table 19-9.) (15 - C1PLAF) > C1LPAE.	Yes	Yes	0h
27:24	**DMA Channel 1 Local-to-PCI Almost Full (C1LPAF)** Number of full (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the internal PCI Bus for writes. Nybble values 0h through Eh are used. (Refer to Table 19-9.)	Yes	Yes	0h
31:28	**DMA Channel 1 PCI-to-Local Almost Empty (C1PLAE)** Number of empty (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the internal PCI Bus for reads. Nybble values 0h through Eh are used. (Refer to Table 19-9.)	Yes	Yes	0h

Note: *For all DMATHR 4-bit fields, value of Fh is* ***reserved****.*

Nybble values 0h through Eh are used to set the number of full or empty Dword entries for each 4-bit field of the DMATHR register, as listed in Table 19-9.

Table 19-9. DMA Threshold Nybble Values

Nybble Value	Setting	Nybble Value	Setting	Nybble Value	Setting
0h	4 Dwords	5h	24 Dwords	Ah	44 Dwords
1h	8 Dwords	6h	28 Dwords	Bh	48 Dwords
2h	12 Dwords	7h	32 Dwords	Ch	52 Dwords
3h	16 Dwords	8h	38 Dwords	Dh	58 Dwords
4h	20 Dwords	9h	40 Dwords	Eh	60 Dwords

Register 19-86. (DMADAC0; PCI:B4h, LOC:134h) DMA Channel 0 PCI Dual Address Cycles Upper Address

Bits	Description	Read	Write	Default
31:0	**Upper 32 Bits of the PCI Dual Address Cycle PCI Address during DMA Channel 0 Cycles** When cleared to 0h, the PEX 8311 performs a 32-bit address DMA Channel 0 access.	Yes	Yes	0h

Register 19-87. (DMADAC1; PCI:B8h, LOC:138h) DMA Channel 1 PCI Dual Address Cycle Upper Address

Bits	Description	Read	Write	Default
31:0	**Upper 32 Bits of the PCI Dual Address Cycle PCI Address during DMA Channel 1 Cycles** When cleared to 0h, the PEX 8311 performs a 32-bit address DMA Channel 1 access.	Yes	Yes	0h

19.9 Local Configuration Space Messaging Queue (I_2O) Registers

Note: *"Yes" in the register Read and Write columns indicates the register is writable by the PCI Express interface and Local Bus.*

Register 19-88. (OPQIS; PCI:30h, LOC:B0h) Outbound Post Queue Interrupt Status

Bits	Description	Read	Write	Default
2:0	***Reserved***	Yes	No	000b
3	**Outbound Post Queue Interrupt** Set when the Outbound Post Queue is not empty. Not affected by the Interrupt Mask bit (OPQIM[3]) state.	Yes	No	0
31:4	***Reserved***	Yes	No	0h

Register 19-89. (OPQIM; PCI:34h, LOC:B4h) Outbound Post Queue Interrupt Mask

Bits	Description	Read	Write	Default
2:0	***Reserved***	Yes	No	000b
3	**Outbound Post Queue Interrupt Mask** Writing 1 masks the Outbound Post Queue interrupt.	Yes	Yes	1
31:4	***Reserved***	Yes	No	0h

Register 19-90. (IQP; PCI:40h) Inbound Queue Port

Bits	Description	Read	Write	Default
31:0	Value written by the PCI Master is stored into the Inbound Post Queue, which is located in Local memory at the address pointed to by the Queue Base Address + Queue Size + Inbound Post Head Pointer. From the time of the PCI write until the Local Memory write and update of the Inbound Post Queue Head Pointer, further accesses to this register result in a Retry. A Local interrupt output (LINTo#) is asserted when the Inbound Post Queue is not empty. When the port is read by the PCI Master, the value is read from the Inbound Free Queue, which is located in Local memory at the address pointed to by the Queue Base Address + Inbound Free Tail Pointer. When the queue is empty, FFFFFFFFh is returned.	PCI	PCI	0h

Register 19-91. (OQP; PCI:44h) Outbound Queue Port

Bits	Description	Read	Write	Default
31:0	Value written by the PCI Master is stored into the Outbound Free Queue, which is located in Local memory at the address pointed to by the Queue Base Address + 3*Queue Size + Outbound Free Head Pointer. From the time of the PCI write until the Local Memory write and update of the Outbound Free Queue Head Pointer, further accesses to this register result in a Retry. When the queue fills, Local interrupt LSERR# is asserted. When the port is read by the PCI Master, the value is read from the Outbound Post Queue, which is located in Local memory at the address pointed to by the Queue Base Address + 2*Queue Size + Outbound Post Tail Pointer. When the queue is empty, FFFFFFFFh is returned. The internal PCI wire interrupt (INTA#) is asserted when the Outbound Post Queue is not empty.	PCI	PCI	0h

Register 19-92. (MQCR; PCI:C0h, LOC:140h) Messaging Queue Configuration

Bits	Description	Read	Write	Default
0	**Queue Enable** Writing 1 allows accesses to the Inbound and Outbound Queue ports. When cleared to 0, writes are accepted but ignored and reads return FFFFFFFFh.	Yes	Yes	0
5:1	**Circular Queue Size** Contains the size of one of the circular FIFO queues. Each of the four queues are the same size. Queue Size encoding values: **MQCR[5:1] — Number of Entries — Total Size** 00001b — 4-KB entries — 64 KB 00010b — 8-KB entries — 128 KB 00100b — 16-KB entries — 256 KB 01000b — 32-KB entries — 512 KB 10000b — 64-KB entries — 1 MB	Yes	Yes	00001b
31:6	***Reserved***	Yes	No	0h

Register 19-93. (QBAR; PCI:C4h, LOC:144h) Queue Base Address

Bits	Description	Read	Write	Default
19:0	***Reserved***	Yes	No	0h
31:20	**Queue Base Address** Local Memory Base address of circular queues. Queues must be aligned on a 1-MB boundary.	Yes	Yes	0h

Register 19-94. (IFHPR; PCI:C8h, LOC:148h) Inbound Free Head Pointer

Bits	Description	Read	Write	Default
1:0	***Reserved***	Yes	No	00b
19:2	**Inbound Free Head Pointer** Local Memory Offset for the Inbound Free Queue. Maintained by the Local CPU software.	Yes	Yes	0h
31:20	**Queue Base Address**	Yes	No	0h

Register 19-95. (IFTPR; PCI:CCh, LOC:14Ch) Inbound Free Tail Pointer

Bits	Description	Read	Write	Default
1:0	***Reserved***	Yes	No	00b
19:2	**Inbound Free Tail Pointer** Local Memory offset for the Inbound Free Queue. Maintained by the hardware and incremented by the modulo of the queue size.	Yes	Yes	0h
31:20	**Queue Base Address**	Yes	No	0h

Register 19-96. (IPHPR; PCI:D0h, LOC:150h) Inbound Post Head Pointer

Bits	Description	Read	Write	Default
1:0	***Reserved***	Yes	No	00b
19:2	**Inbound Post Head Pointer** Local Memory offset for the Inbound Post Queue. Maintained by the hardware and incremented by the modulo of the queue size.	Yes	Yes	0h
31:20	**Queue Base Address**	Yes	No	0h

Register 19-97. (IPTPR; PCI:D4h, LOC:154h) Inbound Post Tail Pointer

Bits	Description	Read	Write	Default
1:0	***Reserved***	Yes	No	00b
19:2	**Inbound Post Tail Pointer** Local Memory offset for the Inbound Post Queue. Maintained by the Local CPU software.	Yes	Yes	0h
31:20	**Queue Base Address**	Yes	No	0h

Register 19-98. (OFHPR; PCI:D8h, LOC:158h) Outbound Free Head Pointer

Bits	Description	Read	Write	Default
1:0	***Reserved***	Yes	No	00b
19:2	**Outbound Free Head Pointer** Local Memory offset for the Outbound Free Queue. Maintained by the hardware and incremented by the modulo of the queue size.	Yes	Yes	0h
31:20	**Queue Base Address**	Yes	No	0h

Register 19-99. (OFTPR; PCI:DCh, LOC:15Ch) Outbound Free Tail Pointer

Bits	Description	Read	Write	Default
1:0	***Reserved***	Yes	No	00b
19:2	**Outbound Free Tail Pointer** Local Memory offset for the Outbound Free Queue. Maintained by the Local CPU software.	Yes	Yes	0h
31:20	**Queue Base Address**	Yes	No	0h

Register 19-100. (OPHPR; PCI:E0h, LOC:160h) Outbound Post Head Pointer

Bits	Description	Read	Write	Default
1:0	***Reserved***	Yes	No	00b
19:2	**Outbound Post Head Pointer** Local Memory offset for the Outbound Post Queue. Maintained by the Local CPU software.	Yes	Yes	0h
31:20	**Queue Base Address**	Yes	No	0h

Register 19-101. (OPTPR; PCI:E4h, LOC:164h) Outbound Post Tail Pointer

Bits	Description	Read	Write	Default
1:0	***Reserved***	Yes	No	00b
19:2	**Outbound Post Tail Pointer** Local Memory offset for the Outbound Post Queue. Maintained by the hardware and incremented by the modulo of the queue size.	Yes	Yes	0h
31:20	**Queue Base Address**	Yes	No	0h

Register 19-102. (QSR; PCI:E8h, LOC:168h) Queue Status/Control

Bits	Description	Read	Write	Default
0	**I_2O Decode Enable** When set to 1, replaces the MBOX0 and MBOX1 registers with the Inbound and Outbound Queue Port registers and redefines Space 1 as the PCI Memory Base Address to be accessed by PCIBAR0. Program former Space 1 registers – LAS1RR, LAS1BA, and LBRD1 – to configure their shared I_2O Memory space, defined as the PCI Memory Base Address.	Yes	Yes	0
1	**Queue Local Space Select** When cleared to 0, use the Local Address Space 0 Bus Region descriptor for Queue accesses. When set to 1, use the Local Address Space 1 Bus Region Descriptor for Queue accesses.	Yes	Yes	0
2	**Outbound Post Queue Prefetch Enable** Writing 1 causes prefetching to occur from the Outbound Post Queue when the queue is not empty.	Yes	Yes	0
3	**Inbound Free Queue Prefetch Enable** Writing 1 causes prefetching to occur from the Inbound Free Queue when the queue is not empty.	Yes	Yes	0
4	**Inbound Post Queue Interrupt Not Empty Mask** Writing 1 masks the Inbound Post Queue Not Empty Interrupt from generating a Local interrupt. Value of 0 clears the mask.	Yes	Yes	1
5	**Inbound Post Queue Interrupt Not Empty** Set when the Inbound Post Queue is not empty. Not affected by the Interrupt Mask bit (QSR[4]) state.	Yes	No	0
6	**Outbound Free Queue Overflow Interrupt Full Mask** When set to 1, masks the Local LSERR# (NMI) interrupt. Value of 0 clears the mask.	Yes	Yes	1
7	**Outbound Free Queue Overflow Interrupt Full** Set when the Outbound Free Queue becomes full. A Local LSERR# interrupt is asserted. Writing 1 clears the interrupt.	Yes	Yes/Clr	0
31:8	***Reserved***	Yes	No	0h

Chapter 20 Testability and Debug

20.1 JTAG Interface

The PEX 8311 provides a Joint Test Action Group (JTAG) Boundary Scan interface, which is utilized to debug board connectivity for each ball. Due to the two-die designs, the PEX 8311 JTAG Boundary Scan is serially interconnected. The PEX 8311 provides two individual BSDL files for each die.

20.1.1 *IEEE Standard 1149.1* Test Access Port

The *IEEE Standard 1149.1* Test Access Port (TAP), commonly referred to as the *JTAG* debug port, is an architectural standard described in the *IEEE Standard 1149.1-1990 IEEE Standard Test Access Port and Boundary-Scan Architecture*. This standard describes a method for accessing internal bridge facilities, using a four- or five-signal interface.

The JTAG debug port, originally designed to support scan-based board testing, is enhanced to support the attachment of debug tools. The enhancements, which comply with the *IEEE Standard 1149.1b-1994 Specifications for Vendor-Specific Extensions*, are compatible with standard JTAG hardware for boundary-scan system testing.

- JTAG Signals – JTAG debug port implements the four required JTAG signals (TCK, TDI, TDO, TMS) and the optional TRST# signal
- JTAG Clock Requirements – TCK signal frequency can range from DC to 10 MHz
- JTAG Reset Requirements – Refer to Section 20.1.4, "JTAG Reset Input TRST#"

20.1.2 JTAG Instructions

The JTAG debug port provides the *IEEE standard 1149.1* EXTEST, IDCODE, SAMPLE/PRELOAD, BYPASS, and PRIVATE instructions, as listed in Table 20-1. ***PRIVATE instructions are for PLX use only.*** Invalid instructions behave as the BYPASS instruction.

Table 20-1 delineates the PCI Express JTAG instructions, along with their input codes. The PEX 8311 returns the PCI Express IDCODE values listed in Table 20-2.

Table 20-1. PEX 8311 PCI Express Die EXTEST, IDCODE, SAMPLE/PRELOAD, BYPASS, and PRIVATE Instructions

Instruction	Input Code	Comments
EXTEST	00000b	*IEEE Standard 1149.1-1990*
IDCODE	00001b	
SAMPLE/PRELOAD	00011b	
BYPASS	11111b	
PRIVATE[a]	00011b	
	00100b	
	00101b	
	00110b	
	00111b	
	01000b	
	01001b	
	01010b	

*a. **Warning: Non-PLX use of PRIVATE instructions can cause a component to operate in a hazardous manner.***

Table 20-2. PEX 8311 PCI Express Die JTAG IDCODE Values

PEX 8311	Version	Part Number	PLX Manufacturer Identity	Least Significant Bit
Bits	0010b	1000_0001_1101_0010b	000_0001_0000b	1
Hex	2h	81D2h	10h	1h
Decimal	2	33234	16	1

The PEX 8311 returns the Local Bus IDCODE values delineated in Table 20-3. Table 20-4 delineates the JTAG instructions, with their input codes.

Table 20-3. PEX 8311 Local Bus Die JTAG IDCODE Value

MSB																													LSB
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Version				Part Number (PCI 9056 when converted to decimal)																PLX Manufacturer Identity											
0	0	0	1	0	0	1	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	1	1	1	0	0	1	1	0	1	1

Table 20-4. PEX 8311 Local Bus Die JTAG Instructions

Instruction	Input Code	Comments
EXTEST	00b	*IEEE Standard 1149.1-1990*
IDCODE	01b	
SAMPLE/PRELOAD	10b	
BYPASS	11b	

20.1.3 JTAG Boundary Scan

Scan Description Language (BSDL), IEEE 1149.1b-1994, is a supplement to *IEEE Standard 1149.1-1990* and *IEEE 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture. BSDL*, a subset of the *IEEE 1076-1993 Standard VHSIC Hardware Description Language (VHDL)*, which allows a rigorous description of testability features in components which comply with the standard. It is used by automated test pattern generation tools for package interconnect tests and Electronic Design Automation (EDA) tools for synthesized test logic and verification. *BSDL* supports robust extensions that are used for internal test generation and to write software for hardware debug and diagnostics.

The primary components of *BSDL* include the logical port description, physical ball map, instruction set, and boundary register description.

The logical port description assigns symbolic names to the PEX 8311 balls. Each ball contains a logical type of In, Out, In Out, Buffer, or Linkage that defines the logical direction of signal flow.

The physical ball map correlates the bridge logical ports to the physical balls of a specific package. A *BSDL* description maintains several physical ball maps; each map is assigned a unique name.

Instruction set statements describe the bit patterns that must be shifted into the Instruction register to place the bridge in the various test modes defined by the standard. Instruction set statements also support descriptions of instructions that are unique to the bridge.

The boundary register description lists each cell or shift stage of the Boundary register. Each cell contains a unique number; the cell numbered 0 is the closest to the Test Data Out (TDO) ball and the cell with the highest number is closest to the Test Data In (TDI) ball. Each cell contains additional information, including:

- Cell type
- Logical port associated with the cell
- Logical function of the cell
- Safe value
- Control cell number
- Disable value
- Result value

20.1.4 JTAG Reset Input TRST#

The TRST# input ball is the asynchronous JTAG logic reset. TRST# assertion causes the PEX 8311 TAP Controller to initialize. In addition, when the TAP Controller is initialized, it selects the PEX 8311 normal logic path (PCI Express interface-to-I/O). It is recommended that the following be taken into consideration when implementing the asynchronous JTAG logic reset on a board:

- When JTAG functionality is required, consider one of the following:
  - TRST# input signal uses a low-to-high transition one time during the PEX 8311 boot-up, along with the RST# signal
  - Hold the PEX 8311 TMS ball high while transitioning the PEX 8311 TCK ball five times
- When JTAG functionality is not required, the TRST# signal must be directly connected to ground

Chapter 21 Shared Memory

21.1 Overview

The PEX 8311 contains a 2K x 32-bit (8-KB) memory block that is accessed from the PCI Express interface serial EEPROM, PCI Express interface, or Local Bus.

21.2 PCI Express Configuration Serial EEPROM Accesses

When the *Shared Memory Load* bit in the Serial EEPROM Format byte is set, the shared memory is loaded from the serial EEPROM starting at location REG BYTE COUNT + 6. The number of bytes to load is determined by the value in EEPROM locations REG BYTE COUNT + 4 and REG BYTE COUNT + 5. The serial EEPROM data is always loaded into the shared memory, starting at Address 0. Data is transferred from the serial EEPROM to the shared memory (in units of DWORDs). (Refer to Chapter 4, "Serial EEPROM Controllers," for details.)

21.3 PCI Express Accesses

The shared memory is accessed from PCI Express Space, using the 64-KB Address space defined by the **PECS Base Address 0** register. The shared memory is located at address offset 8000h in this space. PCI Express Posted Writes are used to write data to the shared memory. Single or Burst Writes are accepted, and PCI Express first and last Byte Enables are supported. When shared Memory Write data is poisoned, the data is discarded and an ERR_NONFATAL message is generated, when enabled. PCI Express Non-Posted Reads are used to read data from the shared memory. Either Single or Burst Reads are accepted. When the 8-KB boundary of the shared memory is reached during a Burst Write or Read, the address wraps around to the beginning of the memory.

21.4 Local Bus Accesses

Local Bus Masters access the PEX 8311's shared memory by way of Memory-Mapped Direct Master transaction, using the 64-KB Address space defined by the **PECS Base Address 0** register. The shared memory is located at offset 8000h in this space. Local Bus Single or Burst Writes are used to write data to the shared memory. Local Bus Byte Enables are supported for each DWORD transferred. Local Bus Single or Burst Reads are used to read data from the shared memory. When the 8-KB boundary of the shared memory is reached during a Burst Write or Read, an internal Disconnect is generated to the Local Address space during the transaction.

21.5 DMA Scatter/Gather Descriptors

The DMA descriptors can be stored in the shared memory for ease of access and to overcome bus latency on the PCI Express interface. The PEX 8311 accesses the PCI Express shared memory as a Memory-Mapped transaction during the descriptor load access. For further details, refer to Section 8.5.4, "DMA Scatter/Gather Mode."

Chapter 22 Electrical Specifications

22.1 Power-Up Sequence

As in all multiple power supply devices, ensure proper power-on procedures for the PEX 8311.

The PEX 8311 maintains four power supplies, requiring voltages of 3.3V, 2.5V, 1.5V and 1.5V (filtered), respectively. The only sequencing requirement is that the 2.5V and 1.5V supplies must reach nominal operating voltage no later than 10 ms after power is applied to the 3.3V I/O supply pins. This delay allows the 2.5V and 1.5V supplies to be regulated from 3.3V, without need for load switching or power sequencing circuitry.

Caution: ***Never apply power only to the 3.3V supply balls, as the un-powered core logic presents a low-resistance path to ground, and high current flow results. Maintaining this condition for more than 10 ms damages or shortens the life of the device.***

Table 22-1. Supply Voltages

Supply Voltage	Supply Balls	Description	Maximum Delay from 3.3V
3.3V	VDD3.3	3.3V I/O Buffers	–
2.5V	VDD2.5	Local Bus core logic	+10 ms
1.5V	VDD1.5, AVDD, VDD_T, VDD_R	PCI Express core logic, analog, and differential signals	
1.5V (filtered)	VDD_P	PLL Supply	

22.2 Power-Down Sequence

The 3.3V, 2.5V, and 1.5V power supply is powered down in any order.

22.3 3.3V and 5V Mixed-Voltage Devices

The PEX 8311 I/O buffers are 3.3V-based, but 5V tolerant. They are capable of receiving 5V signals and their output levels meet 5V TTL specifications.

22.4 Absolute Maximum Ratings

Caution: Conditions that exceed the Absolute Maximum limits can destroy the PEX 8311.

Table 22-2. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
VDD1.5, VDD_P, VDD_R, VDD_T, AVDD	1.5V Supply Voltages	With Respect to Ground	-0.5	+1.8	V
VDD3.3	3.3V Supply Voltages		-0.5	+4.6	V
VDD2.5	2.5V Supply Voltage		-0.5	+3.6	V
V_{IN}	DC Input Voltage	3.3V buffer	-0.5	+4.6	V
		5V Tolerant buffer (Local)	-0.5	+6.5	V
I_{OUT}	DC Output Current, Per Ball	3 mA Buffer	-10	+10	mA
		6 mA Buffer	-20	+20	mA
		12 mA Buffer	-40	+40	mA
		24 mA Buffer	-70	+70	mA
T_{STG}	Storage Temperature	No bias	-65	+150	°C
T_{AMB}	Ambient Temperature	Under bias	0	+70	°C
V_{ESD}	ESD Rating	R = 1.5K Ohm, C = 100 pF		2	KV
V_{OUT}	DC Output Voltage	3.3V, 5V Tolerant buffer (Local)	V_{SS} -0.5V	VDD3.3 +0.5	V
Maximum Power Consumption	Power			500	mW
Maximum Package Power Dissipation	Power			TBD	W

22.5 Recommended Operating Conditions

Caution: Conditions that exceed the Operating limits can cause the PEX 8311 to malfunction.

Junction-to-Ambient Package Thermal Resistance – $Theta_{j-a}$ = 23.28 °C/W, at 0 m/s Linear Air Flow.

Table 22-3. Recommended Operating Conditions

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
VDD1.5, VDD_P, VDD_R, VDD_T, AVDD	1.5V Supply Voltages		1.4	1.6	V
VDD3.3	3.3V Supply Voltages		3.0	3.6	V
VDD2.5	2.5V Supply Voltage		2.3	2.7	V
V_N	Negative Trigger Voltage	3.3V buffer	0.8	1.7	V
		5V tolerant buffer	0.8	1.7	V
V_P	Positive Trigger Voltage	3.3V buffer	1.3	2.4	V
		5V tolerant buffer	1.3	2.4	V
V_{IL}	Low Level Input Voltage	3.3V buffer	0	0.7	V
		5V tolerant buffer	0	0.8	V
V_{IH}	High Level Input Voltage	3.3V buffer	1.7	VDD3.3	V
		5V tolerant buffer	2.0	VDD3.3 + 0.5	V
I_{OL}	Low Level Output Current	3 mA buffer (V_{OL} = 0.4)		3	mA
		6 mA buffer (V_{OL} = 0.4)		6	mA
		12 mA buffer (V_{OL} = 0.4)		12	mA
		24 mA buffer (V_{OL} = 0.4)		24	mA
I_{OH}	High Level Output Current	3 mA buffer (V_{OH} = 2.4)		-3	mA
		6 mA buffer (V_{OH} = 2.4)		-6	mA
		12 mA buffer (V_{OH} = 2.4)		-12	mA
		24 mA buffer (V_{OH} = 2.4)		-24	mA
T_A	Operating Temperature		0	70	°C
t_R	Input Rise Times	Normal input	0	200	ns
t_F	Input Fall Time		0	200	ns
t_R	Input Rise Times	Schmitt input	0	10	ms
t_F	Input Fall Time		0	10	ms

Table 22-4. Capacitance (Sample Tested Only)

Parameter	Test Conditions	Ball Type	Value		Units
			Typical	Maximum	
C_{IN}	V_{IN} = 0V	Input	4	6	pF
C_{OUT}	V_{OUT} = 0V	Output	6	10	pF

Table 22-5. Electrical Characteristics over Operating Range

Parameter	Description	Test Conditions		Minimum	Maximum	Units	Buffer Type
V_{OH}[1]	Output High Voltage	V_{DD} = Minimum V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12.0 mA	2.4	–	V	Local
V_{OL}[1]	Output Low Voltage		I_{OL} = +12 mA	–	0.4	V	
V_{OH}[2]	Output High Voltage		I_{OH} = -24.0 mA	2.4	–	V	
V_{OL}[2]	Output Low Voltage		I_{OL} = +24 mA	–	0.4	V	
V_{IH}	Input High Level	–	–	2.0	VDD3.3 + 0.5	V	
V_{IL}	Input Low Level	–	–	-0.5	+0.8	V	

1. *For 12 mA I/O or output cells (Local Bus).*
2. *For 24 mA I/O or output cells (Local Bus).*

22.6 Local Bus Inputs

Figure 22-1 illustrates the PEX 8311 Local input setup and hold timing. Table 22-6 and Table 22-7 delineate the Local Bus Worst Case TSETUP and THOLD values for each Local Bus mode. TSETUP is the setup time, the time that an input signal is stable before the rising edge of LCLK. THOLD is the time that an input signal is stable after the rising edge of LCLK.

Figure 22-1. PEX 8311 Local Input Setup and Hold Timing

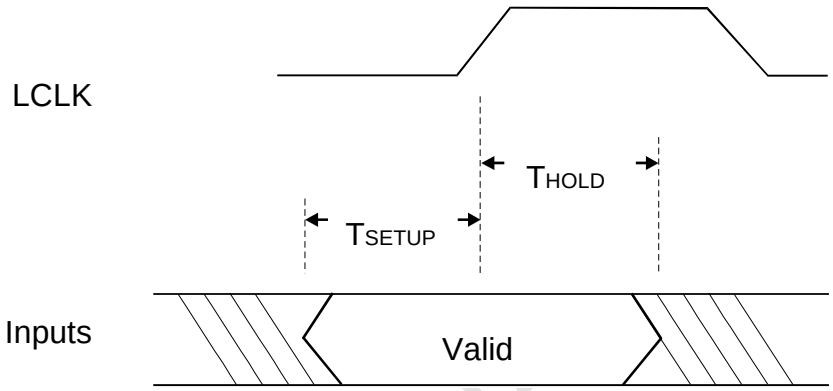


Table 22-6. C Mode Local Bus Worst Case Input AC Timing Specifications

Signals (Synchronous Inputs)	T_{SETUP}	T_{HOLD}	Signals (Synchronous Inputs)	T_{SETUP}	T_{HOLD}
	V_{CC} = 3.0V, T_A = 85 °C			V_{CC} = 3.0V, T_A = 85 °C	
ADS#	2.1 ns	1 ns	LA[31:2]	3.4 ns	1 ns
BIGEND#	4.0 ns	1 ns	LBE[3:0]#	3.6 ns	1 ns
BLAST#	3.4 ns	1 ns	LD[31:0]	3.1 ns	1 ns
BREQi	3.0 ns	1 ns	LHOLDA	2.5 ns	1 ns
BTERM#	4.0 ns	1 ns	LW/R#	3.5 ns	1 ns
CCS#	2.9 ns	1 ns	READY#	4.0 ns	1 ns
DMPAF/EOT#	4.2 ns	1 ns	USERi/LLOCKi#	2.9 ns	1 ns
DP[3:0]	2.9 ns	1 ns	WAIT#	4.0 ns	1 ns
DREQ[1:0]#	3.3 ns	1 ns			

Clock Input Frequency	Minimum	Maximum
Local	0 MHz	66 MHz
Internal PCI		

Table 22-7. J Mode Local Bus Worst Case Input AC Timing Specifications

Signals (Synchronous Inputs)	T_{SETUP}	T_{HOLD}	Signals (Synchronous Inputs)	T_{SETUP}	T_{HOLD}
	V_{CC} = 3.0V, T_A = 85 °C			V_{CC} = 3.0V, T_A = 85 °C	
ADS#	2.1 ns	1 ns	DREQ[1:0]#	3.3 ns	1 ns
ALE	1.7 ns	1 ns	LA[28:2]	3.4 ns	1 ns
BIGEND#	4.0 ns	1 ns	LAD[31:0]	3.1 ns	1 ns
BLAST#	3.4 ns	1 ns	LBE[3:0]#	3.6 ns	1 ns
BREQi	3.0 ns	1 ns	LHOLDA	2.5 ns	1 ns
BTERM#	4.2 ns	1 ns	LW/R#	3.5 ns	1 ns
CCS#	2.9 ns	1 ns	READY#	4.2 ns	1 ns
DMPAF/EOT#	4.2 ns	1 ns	USERi/LLOCKi#	2.9 ns	1 ns
DP[3:0]	2.9 ns	1 ns	WAIT#	4.0 ns	1 ns

Clock Input Frequency	Minimum	Maximum
Local	0 MHz	66 MHz
Internal PCI		

22.7 Local Bus Outputs

Figure 22-2 illustrates the PEX 8311 Local output delay timing. Table 22-8 and Table 22-9 delineate the T_{VALID} (MAX) values for the C and J Local Bus modes. T_{VALID} is output valid (clock-to-out), the time after the rising edge of LCLK until the output is stable. T_{VALID} (MIN) is no less than 2.2 ns for each signal for the C and J Local Bus modes.

Figure 22-2. PEX 8311 Local Output Delay

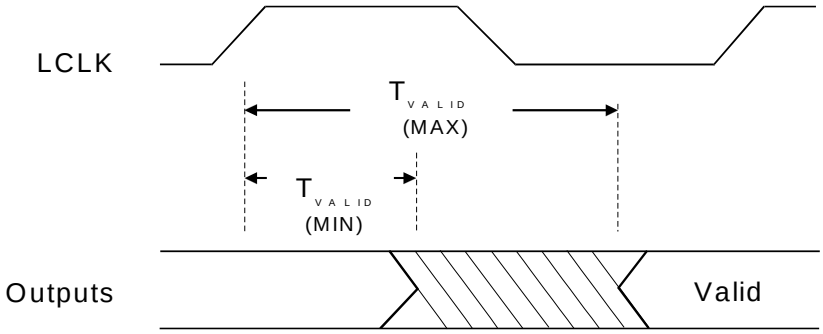


Table 22-8. C Mode Local Bus T_{VALID} (MAX) Output AC Timing Specifications

Signals (Synchronous Outputs)	Output T_{VALID} C_L = 50 pF, V_{CC} = 3.0V, T_aA = 85 °C	Signals (Synchronous Outputs)	Output T_{VALID} C_L = 50 pF, V_{CC} = 3.0V, T_A = 85 °C
ADS#	6.3 ns	LBE[3:0]#	6.3 ns
BLAST#	6.3 ns	LD[31:0]	6.4 ns
BREQo	6.8 ns	LHOLD	6.8 ns
BTERM#	6.8 ns	LSERR#	7.5 ns
DACK[1:0]#	6.3 ns	LW/R#	6.3 ns
DMPAF/EOT#	6.6 ns	READY#	7.2 ns
DP[3:0]	6.8 ns	USERo/LLOCKo#	6.3 ns
LA[31:2]	6.8 ns	WAIT#	6.4 ns

Notes: *On high-to-low transitions, output T_{VALID} values increase/decrease by 16 ps for each increase/decrease of 1 pF.*

On low-to-high transitions, output T_{VALID} values increase/decrease by 20 ps for each increase/decrease of 1 pF.

On high-to-low transitions, the slew rate at 50 pF loading is 1.93V/ns typical; 0.94V/ns worst case.

On low-to-high transitions, the slew rate at 50 pF loading is 1.15V/ns typical; 0.70V/ns worst case.

Table 22-9. J Mode Local Bus T_{VALID} (MAX) Output AC Timing Specifications

Signals (Synchronous Outputs)	Output T_{VALID} C_L = 50 pF, V_{CC} = 3.0V, T_A = 85 °C	Signals (Synchronous Outputs)	Output T_{VALID} C_L = 50 pF, V_{CC} = 3.0V, T_A = 85 °C
ADS#	6.3 ns	LA[28:2]	6.4 ns
ALE	Refer to Figure 22-3	LAD[31:0]	6.4 ns
BLAST#	6.3 ns	LBE[3:0]#	6.3 ns
BREQo	6.8 ns	LHOLD	6.8 ns
BTERM#	6.8 ns	LSERR#	7.5 ns
DACK[1:0]#	6.3 ns	LW/R#	6.3 ns
DEN#	6.4 ns	READY#	7.2 ns
DMPAF/EOT#	6.6 ns	USERo/LLOCKo#	6.3 ns
DP[3:0]	6.8 ns	WAIT#	6.4 ns
DT/R#	6.3 ns		

Notes: *On high-to-low transitions, output T_{VALID} values increase/decrease by 16 ps for each increase/decrease of 1 pF.*

On low-to-high transitions, output T_{VALID} values increase/decrease by 20 ps for each increase/decrease of 1 pF.

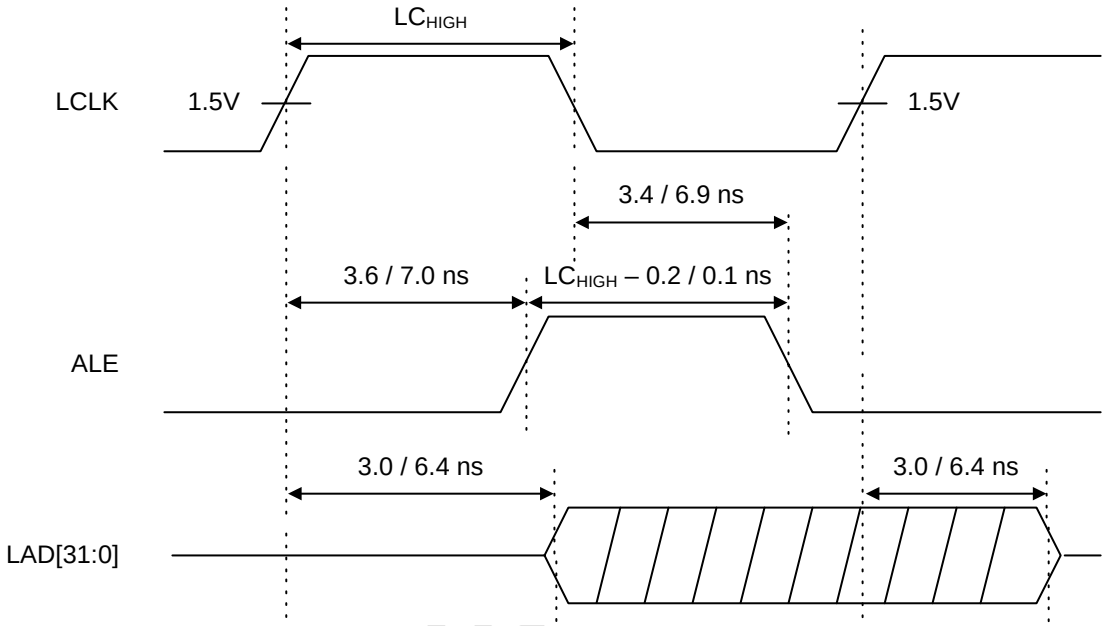
On high-to-low transitions, the slew rate at 50 pF loading is 1.93V/ns typical; 0.94V/ns worst case.

On low-to-high transitions, the slew rate at 50 pF loading is 1.15V/ns typical; 0.70V/ns worst case.

22.8 ALE Output Delay Timing for Local Bus Clock Rates

Figure 22-3 illustrates the PEX 8311 ALE output delay timing for any processor/Local Bus clock rate.

Figure 22-3. PEX 8311 ALE Output Delay to Local Clock



Notes: *LC_{HIGH} is the time, in ns, that the processor/Local Bus clock is high.*

Times listed in Figure 22-3 are "minimum/maximum" values.

Chapter 23 Physical Specifications

23.1 PEX 8311 Package Specifications

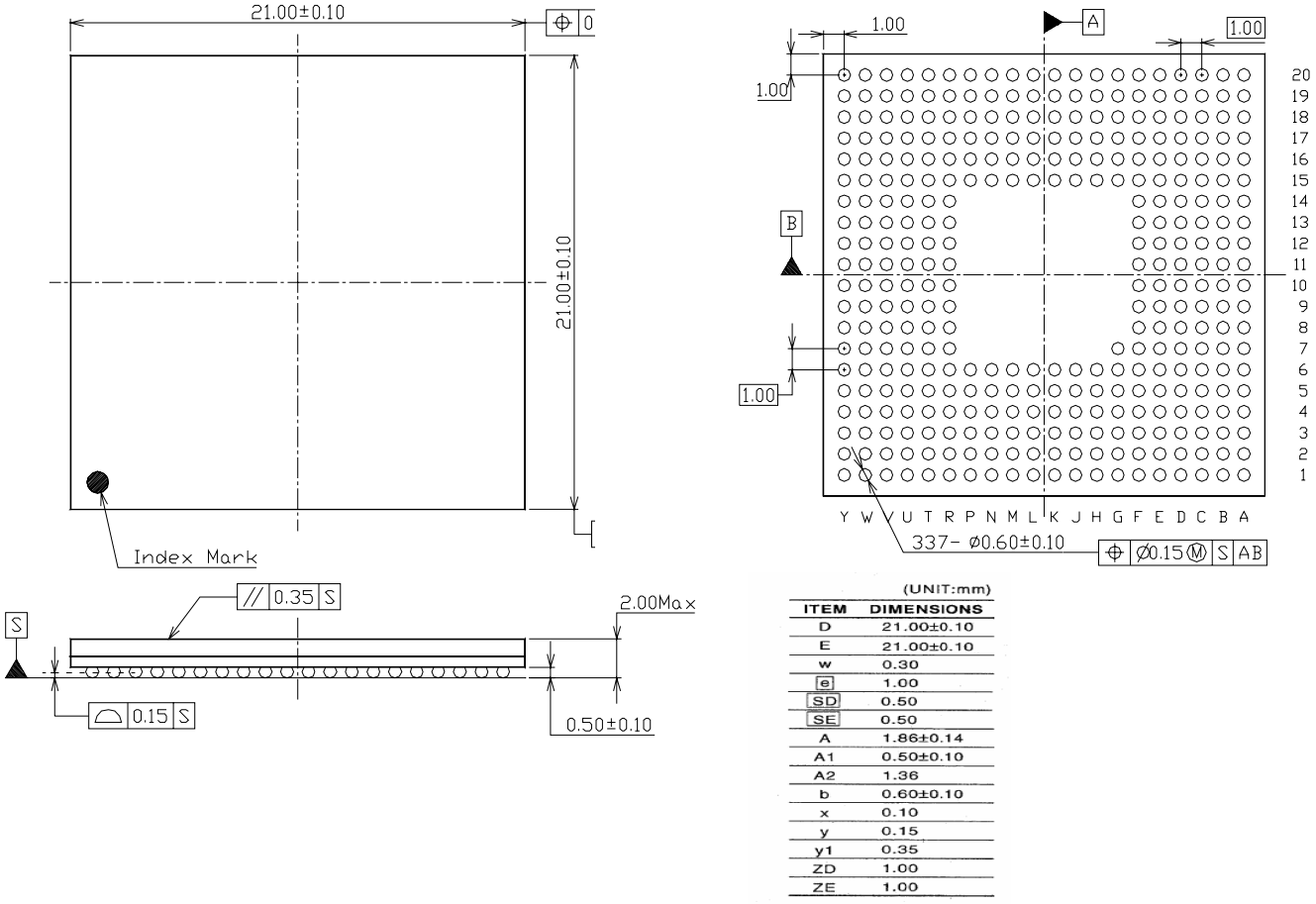
The PEX 8311 is offered as a 21-mm square, 337-ball PBGA (Plastic BGA) package. Package specifications are delineated in Table 23-1.

Table 23-1. PEX 8311 337-Ball PBGA Package Specifications

Parameter	Specification
Package Type	Plastic Ball Grid Array
Package Dimensions	21 x 21 mm (approximately 1.83 ±0.017 mm high)
Ball Matrix Pattern	20 x 20 mm (refer to Figure 23-1)
Ball Pitch	1.00 mm
Ball Diameter	0.60 ±0.15 mm
Ball Spacing	0.40 mm

23.2 Mechanical Drawing

Figure 23-1. PEX 8311 Mechanical Drawing



(UNIT:mm)

ITEM	DIMENSIONS
D	21.00±0.10
E	21.00±0.10
w	0.30
e	1.00
SD	0.50
SE	0.50
A	1.86±0.14
A1	0.50±0.10
A2	1.36
b	0.60±0.10
x	0.10
y	0.15
y1	0.35
ZD	1.00
ZE	1.00

Appendix A General Information

A.1 Product Ordering Information

Contact your local PLX sales representative for ordering information.

Table A-1. Product Ordering Information

Part Number	Description
PEX8311-AA66BC F	PCI Express-to-Generic Local Bus Bridge, Standard PBGA Package (337-Ball, 21 x 21 mm), Lead Free
PEX8311-AA66BC F F – Lead Free C – Case Temperature I = Industrial Temperature C = Commercial Temperature ES = Engineering Sample B – Package Type B = Plastic Ball Grid Array AA – Part Revision Code 66 – Speed Grade (66 MHz Local Bus) 8311 – Part Number PEX – PCI Express product family	
PEX8311RDK	Endpoint Reference Design Kit

A.2 United States and International Representatives and Distributors

PLX Technology, Inc., representatives and distributors are listed at www.plxtech.com.

A.3 Technical Support

PLX Technology, Inc., technical support information is listed at www.plxtech.com/support/, or call 408 774-9060 or 800 759-3735.