DUAL J-K FLIP-FLOP   **MTTL III MC3100/3000 series**

MC3161F · MC3061F
MC3161L · MC3061L,P

This dual JK flip-flop triggers on the negative edge of clock. Each flip-flop is provided with a separate direct SET input in addition to the common direct RESET input. These direct inputs provide a means of resetting a group of flip-flops such as a register which may be followed by the presetting of a data pattern. The clock input for this device is common for both flip-flops, making it particularly useful in registers or other common clock applications.

Data may be applied to or changed at, the clocked inputs at any time during the clock cycle, except during the time interval between the Setup and Hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between the Set-up and Hold time is stored in the flip-flop when the clock falls. Each flip-flop may be set at any time without regard to the clock state by applying a low level to the SET input. In addition, both flip-flops may be reset simultaneously by using the common RESET in a similar manner.

LOGIC DIAGRAM

1/2 OF DEVICE SHOWN,
RESET AND CLOCK COMMON TO BOTH

Input Loading Factors:
SET = 1.75
RESET, CLOCK = 3.7
J, K = 0.75

Output Loading Factor = 10

J-K TRUTH TABLE

J	K	Qⁿ	Qⁿ⁺¹
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Typical Characteristics
(V_{CC} = 5.0 V; T_A = 25°C)

Total Power Dissipation = 100 mW/pkg
Toggle Frequency = 50 MHz typ
Logical "1" Setup Time = 8.0 ns
Logical "0" Setup Time = 8.0 ns
Logical "1" and "0" Hold Times = 0 ns
t_{pd-} = 12 ns
t_{pd+} = 12 ns

1/2 OF CIRCUIT
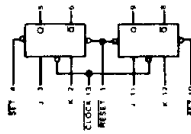SHOWN (RESET AND CLOCK
COMMON TO BOTH)
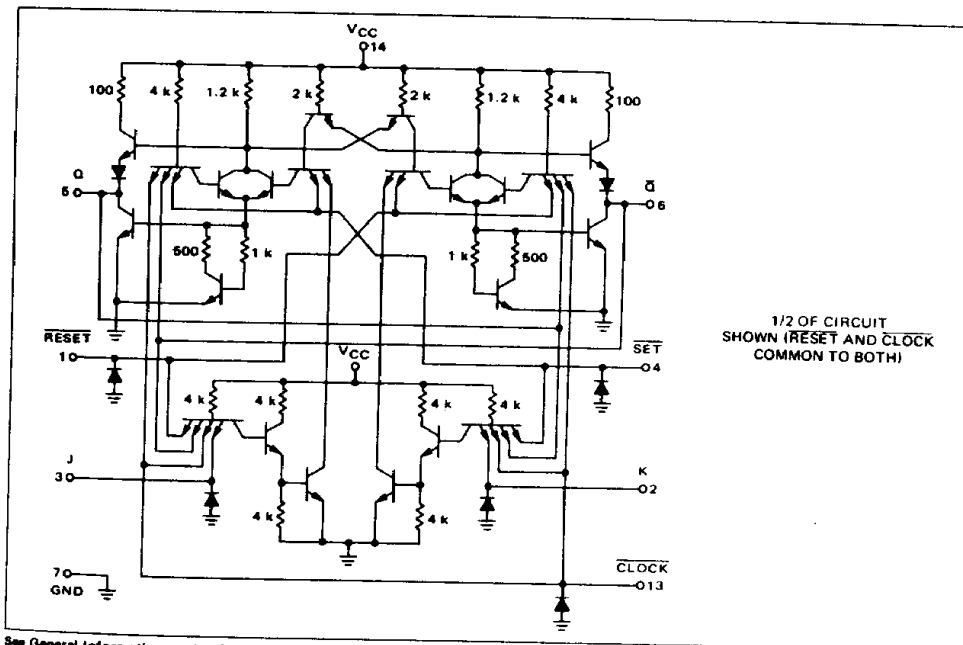
See General Information section for packaging.

MC3161F, MC3061F/MC3161L, MC3061L,P (continued)

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop plus the inputs common to both flip-flops. To complete testing, sequence through the remaining inputs in the same manner.
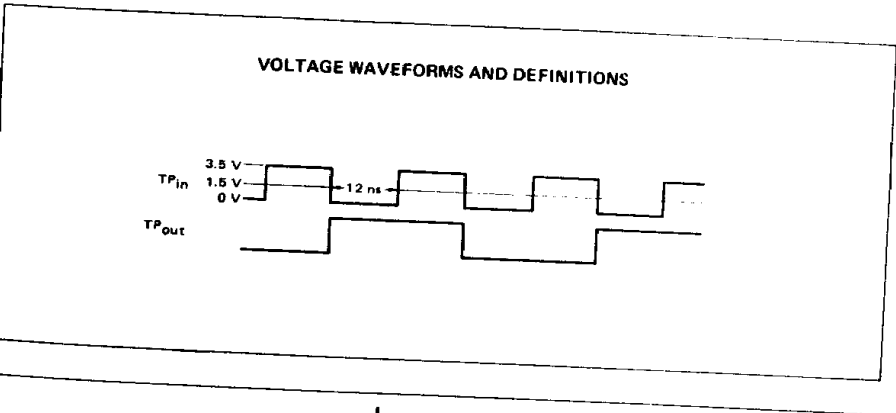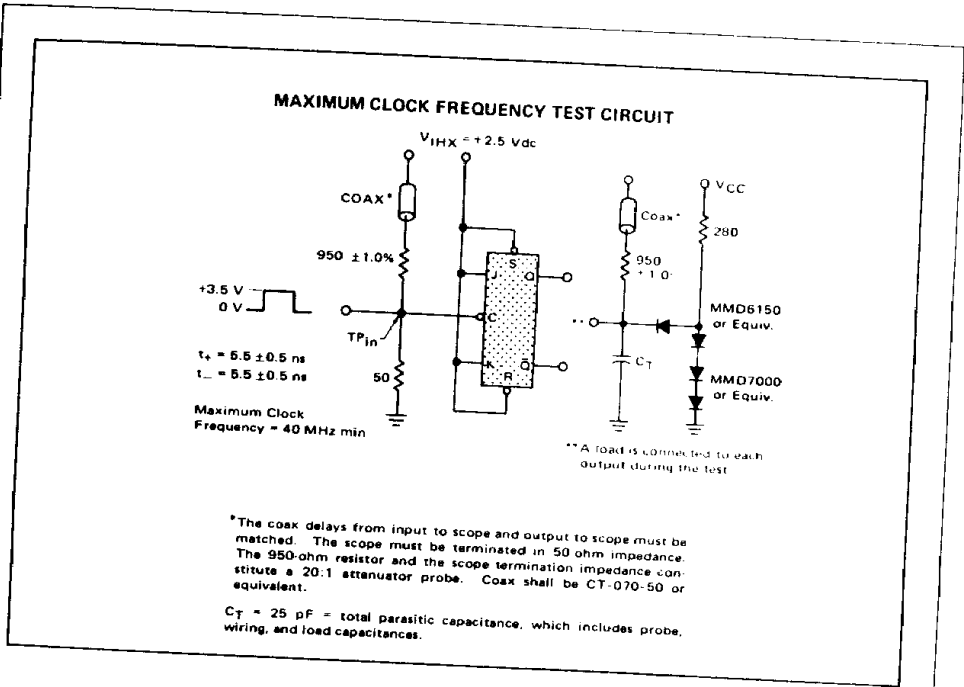
Characteristic	Symbol	Pin Under Test	MC3161 Test Limits −55°C Min	Max	+25°C Min	Max	+125°C Min	Max	MC3061 Test Limits 0°C Min	Max	+25°C Min	Max	+75°C Min	Max	Unit
Input Forward Current	I_{FJ}	3		−1.5		−1.5		−1.5		−1.5		−1.5		−1.5	mAdc
	I_{FK}	2		−1.5		−1.5		−1.5		−1.5		−1.5		−1.5	mAdc
	I_{FR}	1		−6.4		−6.4		−6.4		−6.4		−6.4		−6.4	mAdc
	I_{FS}	4		−4.0		−4.0		−4.0		−4.0		−4.0		−4.0	mAdc
	I_{FC}	13		−9.2		−9.2		−9.2		−9.2		−9.2		−9.2	µAdc
Leakage Current	I_{RJ}	3		50		50		50		50		50		50	µAdc
	I_{RK}	2		50		50		50		50		50		50	µAdc
	I_{RR}	1		200		200		200		200		200		200	µAdc
	I_{RS}	4		150		150		150		150		150		150	µAdc
	I_{RC}	13		300		300		300		300		300		300	µAdc
Breakdown Voltage	BV_{in}	3 / 2 / 1 / 4 / 13	5.5		5.5				5.5		5.5				Vdc
Clamp Voltage	V_D			−1.5		−1.5		−1.5		−1.5		−1.5		−1.5	Vdc
Output Output Voltage	V_{OL}	5 / 6		0.4		0.4		0.4		0.4		0.4		0.4	Vdc
	V_{OH}	5 / 6	2.4		2.4		2.4		2.5		2.5		2.5		Vdc
Short-Circuit Current	I_{SC}	5 / 6	−20	−65	−20	−65	−20	−65	−20	−65	−20	−65	−20	−65	mAdc
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14				42						42			mAdc
Power Supply Drain	I_{PD}	14		30		30		30		30		30		30	mAdc

*Momentarily ground pin prior to taking measurement. (If pin is also in another column, the pin must be returned to that voltage or current for measurement.)

MC3161F, MC3061F/MC3161L, MC3061L,P (continued)

OPERATING CHARACTERISTICS

High state data must be present 12 ns prior to the fall of the clock and remain until 0 ns after the clock falls.

The direct SET (individual) inputs and RESET (common) inputs may be used at any time without regard to the clock state. The flip-flop is set to the Q = 1 state by applying a low level to the SET input or reset to the Q = 0 state by applying a low level to the RESET input. If these inputs are not used they should be returned to a volt-

age between 2.0 and 5.5 Vdc.

Negative edge triggering   The input state during the time interval between the Setup and Hold times is stored in the flip-flop when the clock goes low.

Unused clocked inputs should be tied to the clock, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc.

MAXIMUM CLOCK FREQUENCY TEST CIRCUIT

V_{IHX} = +2.5 Vdc

COAX*

950 ±1.0%

+3.5 V
0 V

TP_{in}

t_+ = 5.5 ±0.5 ns
t_- = 5.5 ±0.5 ns

50

Maximum Clock
Frequency = 40 MHz min

Coax*

950
+ 1.0

V_{CC}

280

MMD6150
or Equiv.

C_T

MMD7000
or Equiv.

**A load is connected to each
output during the test

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50 ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS

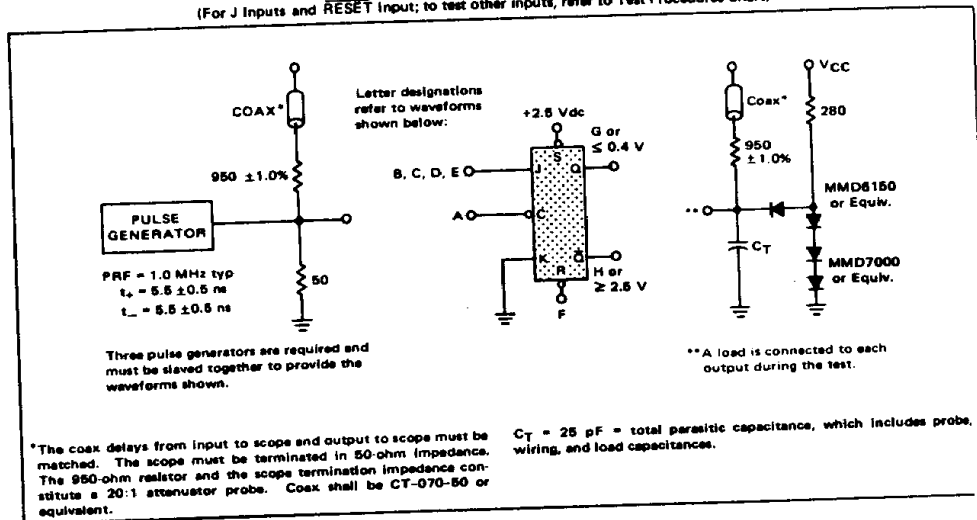TP_{in} 3.5 V
         1.5 V
         0 V

12 ns

TP_{out}

74

MC3161F, MC3061F/MC3161L, MC3061L,P (continued)

OPERATING CHARACTERISTICS (continued)

SWITCHING TIME TEST CIRCUIT
(For J Inputs and $\overline{RESET}$ Input; to test other inputs, refer to Test Procedures Chart)

Letter designations refer to waveforms shown below:
B, C, D, E
A

COAX*
950 ±1.0%
PULSE GENERATOR
PRF = 1.0 MHz typ
t_+ = 5.5 ±0.5 ns
t_- = 5.5 ±0.5 ns
50

Three pulse generators are required and must be slaved together to provide the waveforms shown.

+2.5 Vdc
G or ≤ 0.4 V
S
J Q
C
A
Q
K
R Q
F
H or ≥ 2.5 V

V_{CC}
Coax*
280
950 ±1.0%
MMD6150 or Equiv.
C_T
MMD7000 or Equiv.

**A load is connected to each output during the test.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS

A 3.5 V / 0 V — |30 ns| 1.5 V — CLOCK (Must be used on all tests)
B 3.5 V / 0 V — |30 ns| 1.5 V — t_{Setup} "1"
C 3.5 V / 0 V — |30 ns| 1.5 V — t_{Hold} "1"
D 3.5 V / 0 V — |30 ns| 1.5 V — t_{Setup} "0"
E 3.5 V / 0 V — |30 ns| 1.5 V — t_{Hold} "0"
F 3.5 V / 0 V — 500 ns — 30 ns — 1.5 V
G 3.5 V / 0 V — t_{pd+} 1.5 V — t_{sd-}
H 3.5 V / 0 V — 1.5 V — t_{pd-} — t_{sd+}

TEST PROCEDURES CHART

| TEST | INPUT | | | | | | LIMITS (ns) |
	J*	SET*	RESET*	K*	Q*	Q̄*	Max
t_{Setup} "1" J	B	2.5 V	F	Gnd	Q	H	18
t_{Hold} "1" J	C	2.5 V	F	Gnd	Q	H	0**
t_{Setup} "0" J	D	2.5 V	F	Gnd	≤0.4 V	≥2.5 V	18
t_{Hold} "0" J	E	2.5 V	F	Gnd	≤0.4 V	≥2.5 V	0**
t_{Setup} "1" K	Gnd	F	2.5 V	B	H	Q	18
t_{Hold} "1" K	Gnd	F	2.5 V	C	H	Q	0**
t_{Setup} "0" K	Gnd	F	2.5 V	D	≥2.5 V	≤0.4 V	18
t_{Hold} "0" K	Gnd	F	2.5 V	E	≥2.5 V	≤0.4 V	0**
t_{pd+}	Delay from CLOCK to Q during t_{Setup} "1" J test. Delay from CLOCK to Q̄ during t_{Setup} "1" K test.						18
t_{pd-}	Delay from CLOCK to Q̄ during t_{Setup} "1" J test. Delay from CLOCK to Q during t_{Setup} "1" K test.						18
t_{sd+}	Delay from SET to Q during t_{Setup} "1" J test. Delay from RESET to Q̄ during t_{Setup} "1" J test.						18
t_{sd-}	Delay from SET to Q̄ during t_{Setup} "1" K test. Delay from RESET to Q during t_{Setup} "1" J test.						18

*Letters shown in these columns refer to waveforms shown at the left.
**Hold is typically a negative number.

AC ELECTRICAL CHARACTERISTICS

The timing waveforms in the AC Electrical Characteristics are tested with a V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all pins, except EXTAL, $\overline{RESET}$, MODA, MODB, and MODC. These pins are tested using the input levels set forth in the DC Electrical Characteristics. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56002 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively.
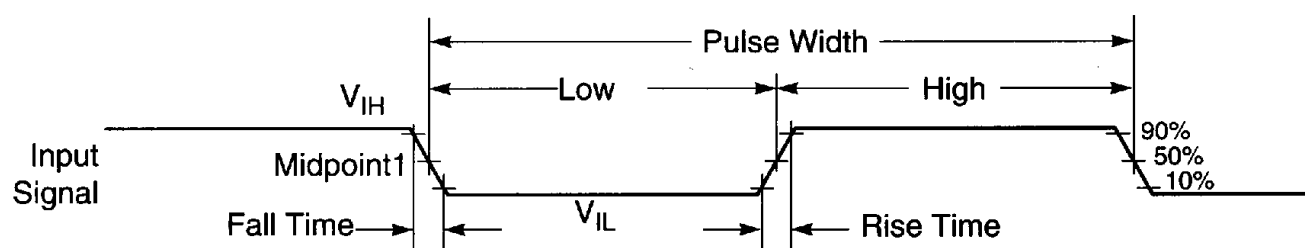
Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

AA0179

Figure 2-1 Signal Measurement Reference