

# LINEAR POWER TRANSISTOR CHIP

HXTR-5001

## Features

**HIGH P<sub>1dB</sub> LINEAR POWER**  
23 dBm Typical at 2 GHz  
22 dBm Typical at 4 GHz

**HIGH P<sub>1dB</sub> GAIN**  
13.5 dB Typical at 2 GHz  
8.0 dB Typical at 4 GHz

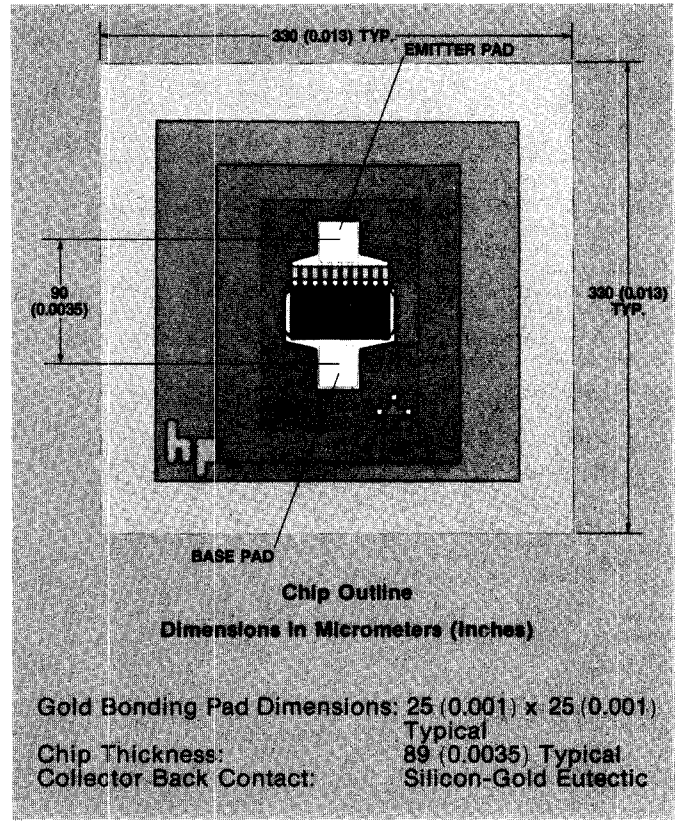
**LOW DISTORTION**

**HIGH POWER-ADDED EFFICIENCY**

## Description/Applications

The HXTR-5001 is an NPN bipolar transistor chip designed for high output power and gain to 5 GHz. To achieve excellent uniformity and reliability, the manufacturing process utilizes ion implantation, self-alignment techniques and Ti/Pt/Au metallization. The chip has a dielectric scratch protection over its active area and Ta<sub>2</sub>N ballast resistors for ruggedness.

The superior power, gain and distortion performance of the HXTR-5001 commend it for use in broad and narrow band commercial and military communications, radar, and ECM hybrid applications. Programs requiring hermetically packaged devices with similar performance should employ the HXTR-5101 and the HXTR-5103 which utilize this chip.



## Electrical Specifications at T<sub>A</sub> = 25°C

Symbol	Parameters and Test Conditions	Test MIL-STD-750	Units	Min.	Typ.	Max.
BV <sub>CB0</sub>	Collector-Base Breakdown Voltage at I <sub>C</sub> = 3 mA	3001.1*	V	40		
BV <sub>CE0</sub>	Collector-Emitter Breakdown Voltage at I <sub>C</sub> = 15 mA	3011.1*	V	24		
BV <sub>EB0</sub>	Emitter-Base Breakdown Voltage at I <sub>B</sub> = 30 μA	3026.1*	V	3.3		
I <sub>EB0</sub>	Emitter-Base Leakage Current at V <sub>EB</sub> = 2 V	3061.1	μA			2
I <sub>CE0</sub>	Collector-Emitter Leakage Current at V <sub>CE</sub> = 32 V	3041.1**	nA			200
I <sub>CB0</sub>	Collector-Base Leakage Current at V <sub>CB</sub> = 20 V	3036.1**	nA			100
h <sub>FE</sub>	Forward Current Transfer Ratio at V <sub>CE</sub> = 18 V, I <sub>C</sub> = 30 mA	3076.1*		15	40	75
P <sub>1dB</sub>	Power Output at 1 dB Gain Compression		dBm		23	
					22	
					13.5	
					8	
G <sub>1dB</sub>	Associated 1 dB Compressed Gain		dB		13.5	
					8	
P <sub>SAT</sub>	Saturated Power Output (8 dB Gain) (3 dB Gain)		dBm		25.5	
					25	
η	Power-Added Efficiency at 1 dB Compression		%		35	
					25	
IMD	Third Order Intermodulation Distortion (Reference to either tone), at P <sub>O</sub> (PEP) = 22 dBm Tuned for Maximum Output Power at 1dB Compression V <sub>CE</sub> = 18 V, I <sub>C</sub> = 30 mA, θ <sub>JA</sub> = 210°C/W		dB			-30

\*300 μs wide pulse measurement at ≤2% duty cycle.  
\*\*Measured under low ambient light conditions.

DEVICES FOR HYBRID INTEGRATED CIRCUITS



# Recommended Maximum Continuous Operating Conditions<sup>[1]</sup>

Symbol	Parameter	Value
V <sub>CB0</sub>	Collector to Base Voltage	40V
V <sub>CE0</sub>	Collector to Emitter Voltage	22V
V <sub>EB0</sub>	Emitter to Base Voltage	3.3V
I <sub>C</sub>	DC Collector Current	50 mA
P <sub>T</sub>	Total Device Dissipation <sup>[2]</sup>	700 mW
T <sub>J</sub>	Junction Temperature	200°C
T <sub>STG</sub>	Storage Temperature	-65°C to +200°C

**Notes:**

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1 x 10<sup>7</sup> hours at T<sub>J</sub> = 175°C assumed Activation Energy = 1.5 eV.
2. Power dissipation derating should include a  $\theta_{JB}$  (Junction-to-Back contact thermal resistance) of 150°C/W.

Total  $\theta_{JA}$  (Junction-to-Ambient) will be dependent upon the heat sinking provided in the individual application.

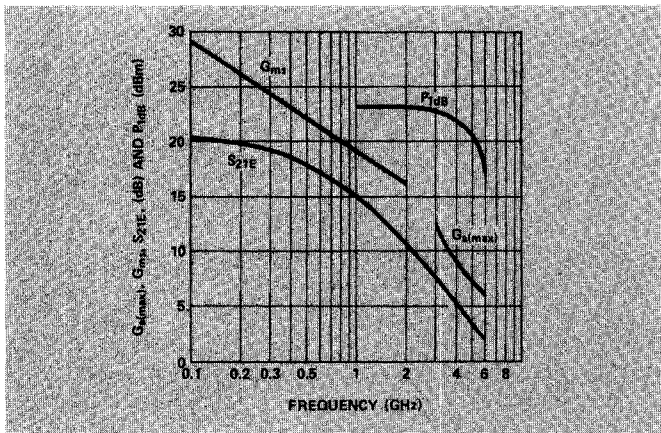


Figure 1. Typical  $G_{a(max)}$ , Maximum Stable Gain ( $G_{ms}$ ),  $S_{21E}$ , and  $P_{1dB}$  Linear Power vs. Frequency at  $V_{CE} = 18V$ ,  $I_C = 30 mA$ .

# Absolute Maximum Ratings\*

Symbol	Parameter	Limit
V <sub>CB0</sub>	Collector to Base Voltage	45V
V <sub>CE0</sub>	Collector to Emitter Voltage	27V
V <sub>EB0</sub>	Emitter to Base Voltage	4.0V
I <sub>C</sub>	DC Collector Current	100 mA
P <sub>T</sub>	Total Device Dissipation	1.4W
T <sub>J</sub>	Junction Temperature	300°C
T <sub>STG(MAX)</sub>	Maximum Storage Temperature	300°C

\*Operation in excess of any one of these conditions may result in permanent damage to this device.

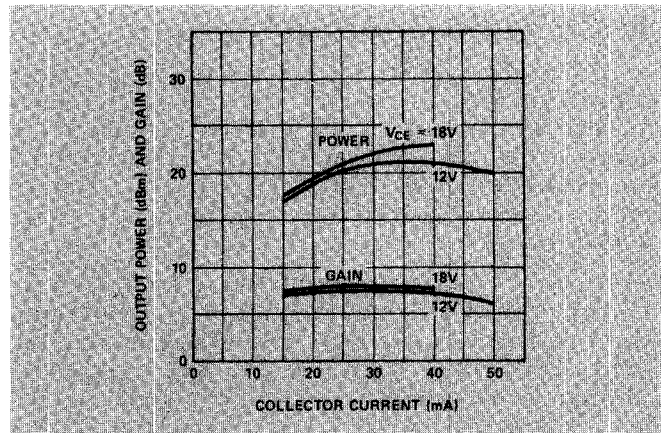


Figure 2. Typical  $P_{1dB}$  Linear Power and Associated 1 dB Compressed Gain vs. Current at  $V_{CE} = 12V$  and  $18V$  at 4 GHz.

# Typical S-Parameters\* $V_{CE} = 18V$ , $I_C = 30 mA$

Freq. (GHz)	S <sub>11</sub>		S <sub>21</sub>			S <sub>12</sub>			S <sub>22</sub>	
	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.100	0.74	-15	20.2	10.2	171	-38	0.01	83	0.99	-5
0.200	0.73	-30	19.9	9.88	162	-33	0.02	75	0.97	-10
0.300	0.72	-44	19.5	9.42	154	-30	0.03	69	0.93	-15
0.400	0.71	-57	19.0	8.87	146	-28	0.04	63	0.89	-19
0.500	0.70	-68	18.4	8.28	140	-26	0.05	58	0.85	-22
0.600	0.69	-78	17.7	7.71	134	-25	0.06	54	0.80	-24
0.700	0.67	-87	17.1	7.16	129	-25	0.06	50	0.76	-26
0.800	0.67	-94	16.5	6.65	124	-24	0.06	47	0.73	-28
0.900	0.66	-101	15.8	6.19	120	-24	0.07	44	0.70	-29
1.000	0.65	-107	15.2	5.78	117	-23	0.07	42	0.67	-30
1.500	0.63	-128	12.6	4.25	103	-22	0.08	37	0.58	-32
2.000	0.62	-140	10.5	3.33	94	-22	0.08	35	0.53	-32
2.500	0.61	-148	8.7	2.73	87	-21	0.09	35	0.51	-33
3.000	0.61	-154	7.3	2.32	81	-21	0.09	35	0.50	-35
3.500	0.61	-158	6.1	2.02	76	-20	0.10	36	0.49	-36
4.000	0.60	-161	5.8	1.79	71	-20	0.10	37	0.49	-38
4.500	0.60	-164	4.1	1.61	66	-19	0.11	38	0.49	-40
5.000	0.60	-166	3.3	1.47	62	-19	0.11	39	0.49	-43
5.500	0.59	-168	2.6	1.35	58	-19	0.12	40	0.49	-45
6.000	0.59	-169	2.0	1.25	55	-18	0.12	40	0.49	-47

\*Values do not include any parasitic bonding inductances and were generated by use of a computer model.