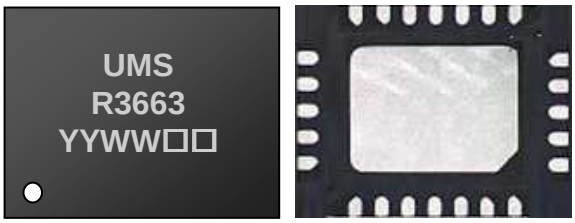
Preliminary

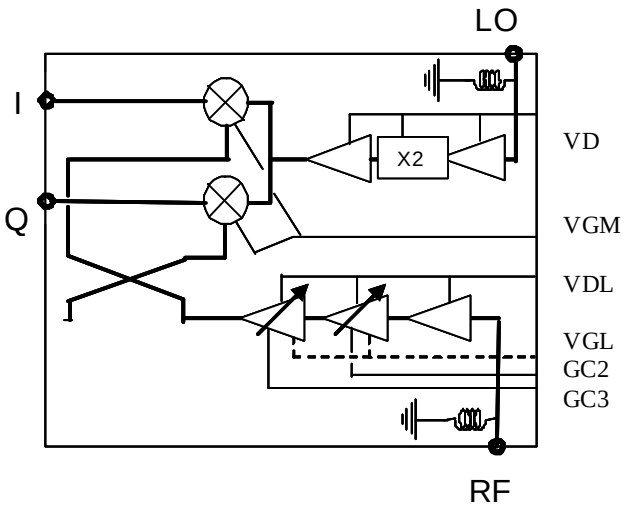
17-24GHz Integrated Down Converter

GaAs Monolithic Microwave IC in SMD package

Description

The CHR3663-QEG is a multifunction part, which integrates a balanced cold FET mixer, a multiplier by two, and a RF LNA including gain control.
It is designed for a wide range of applications, typically commercial communication systems.
The circuit is manufactured with a pHEMT process, 0.25µm gate length.
It is available in lead-free SMD package.





Main Features

- Broadband RF performance 17-24GHz
- 11dB conversion gain
- 15 dBc Image Rejection
- 3 dBm Input IP3
- 15dB Gain control
- 24LQFN4x5
- ESD protected

Main Characteristics

Tamb = +25°C, Vd= 4.5V

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	17		24.0	GHz
F_{LO}	LO frequency range	7		14.0	GHz
F_{IF}	IF frequency range	DC		3.5	GHz
G_c	Conversion gain		11		dB

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

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Electrical Characteristics

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Tamb = +25℃, VD=VDL= 4.5V

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	17		24.0	GHz
F_{LO}	LO frequency range	7		14.0	GHz
F_{IF}	IF frequency range	DC		3.5	GHz
G_c	Conversion gain@ min. attenuation (1)		11		dB
ΔG	Gain control range		15		dB
NF	Noise Figure@ min. attenuation		3.5		dB
Im_rej	Image rejection (1)		15		dBc
P_{LO}	LO Input power		0		dBm
IIP3	Input IP3@ all gain range (ΔG)		3		dBm
2LO/RF	2LO leakage at RF port @ max. gain		-40		dBm
VD, VDL	DC drain voltage		4.5		V
Id	Drain current		380		mA
VGL	LNA DC gate voltage		-0.4		V
GC2, GC3	Gain control DC voltage	-2		+0,6	V
VGM	Mixer DC gate voltage		-0.7		V

These values are representative of onboard measurements as defined on the drawing at page 15 (paragprah "Evaluation mother board").
(1) An external combiner 90°is required on I / Q.
Note : Id not affected by GC2, GC3.

Absolute Maximum Ratings (1)

Tamb = +25℃

Symbol	Parameter	Values	Unit
Vd	Maximum drain bias voltage	5	V
Id	Maximum drain bias current	450	mA
VGL	LNA DC gate voltage	-2.0 to +0.4	V
VGM	Mixer DC gate voltage	-2.0 to +0.4	V
GC1, GC2	Gain control voltage	-2.5 to + 0.8	V
P_RF	Maximum peak input power overdrive	10	dBm
P_LO	Maximum LO input power	10	dBm
Tch	Maximum channel temperature (1)	175	℃
Ta	Operating temperature range	-40 to +85	℃
Tstg	Storage temperature range	-55 to +125	℃

(1) Operation of this device above anyone of these paramaters may cause permanent damage.

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Device thermal performances

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All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

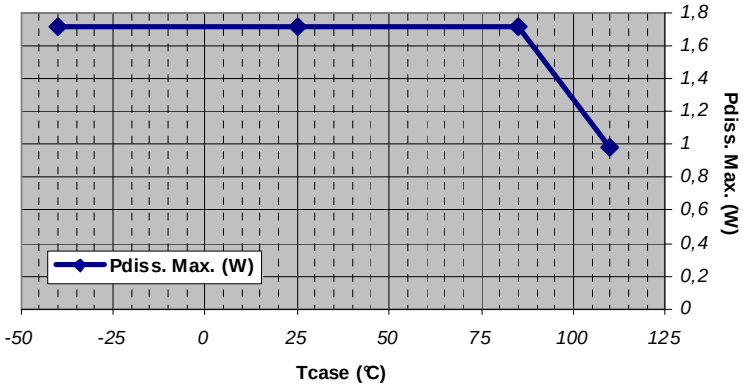
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

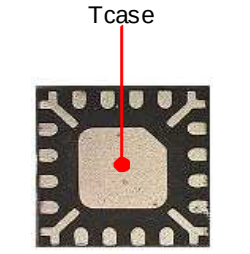
DEVICE THERMAL SPECIFICATION : CHR3663-QEG			
Recommanded max. junction temperature (Tj max)		:	143 °C
Junction temperature absolute maximum rating		:	175 °C
Max. continuous dissipated power @ Tcase=	85 °C	:	1,71 W
=> Pdiss derating above Tcase(1)=	85 °C	:	29 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)		:	<34 °C/W
Min. package back side operating temperature(3)		:	-40 °C
Max. package back side operating temperature(3)		:	85 °C
Min. storage temperature		:	-55 °C
Max. storage temperature		:	125 °C

(1) Derating at junction temperature constant = Tj max

*(2) Rth J-C is calculated for a worst case where the **hotter junction** of the MMIC is considered.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example of QFN 16L 3x3 back-side view, temperature reference point (Tcase) location.

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Typical Measured Performances

Tamb = +25°C, VD = VDL = 4.5V, VGL=-0.4V, VGM = -0. 7V, P_LO = 0 dBm

These values are representative of onboard measurements (on connector access planes) as defined on the drawing 97625 page 16. The board losses are estimated from 1.5 to 2dB in the frequency range.

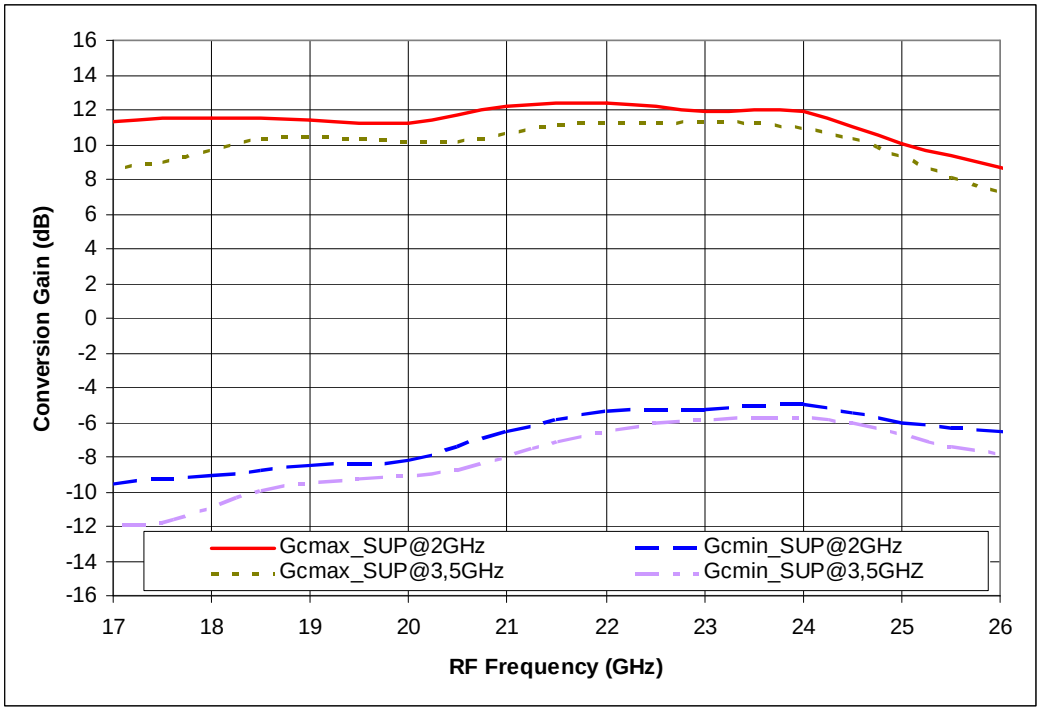

Figure 1 : Conversion Gain in Supradyne Mode versus Frequency F_RF=2xF_LO+F_IF, F_IF=2 & 3.5GHz, GC2=GC3=-1.5 & 0.5V

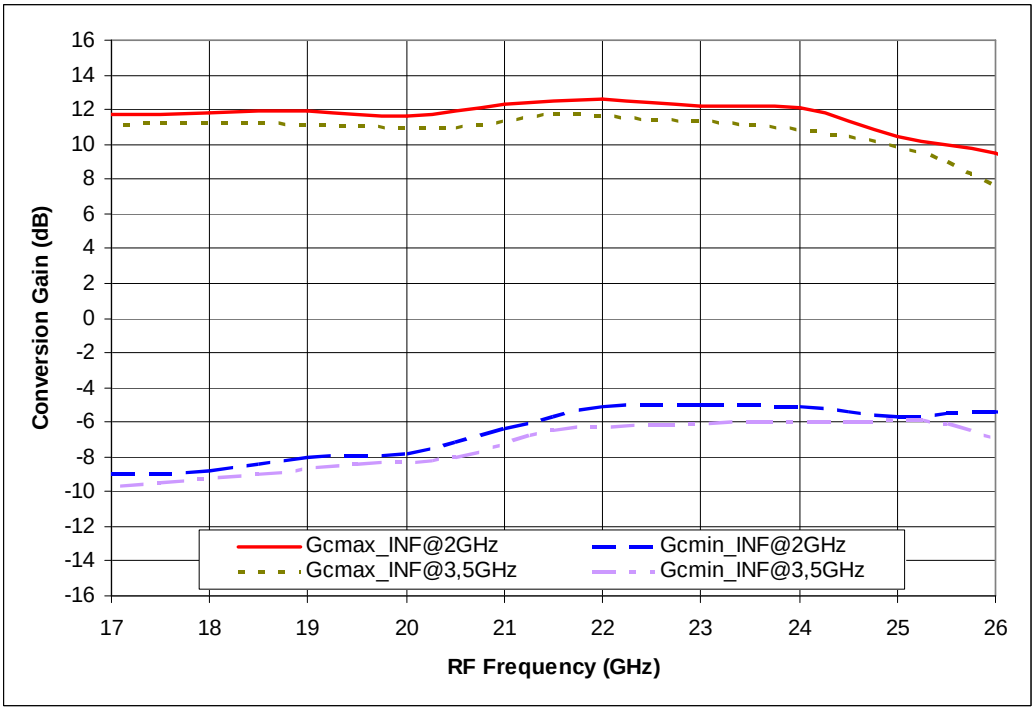

Figure 2 : Conversion Gain in Infradyne Mode versus Frequency F_RF=2xF_LO-F_IF, F_IF=2 & 3.5GHz, GC2=GC3=-1.5 & 0.5V

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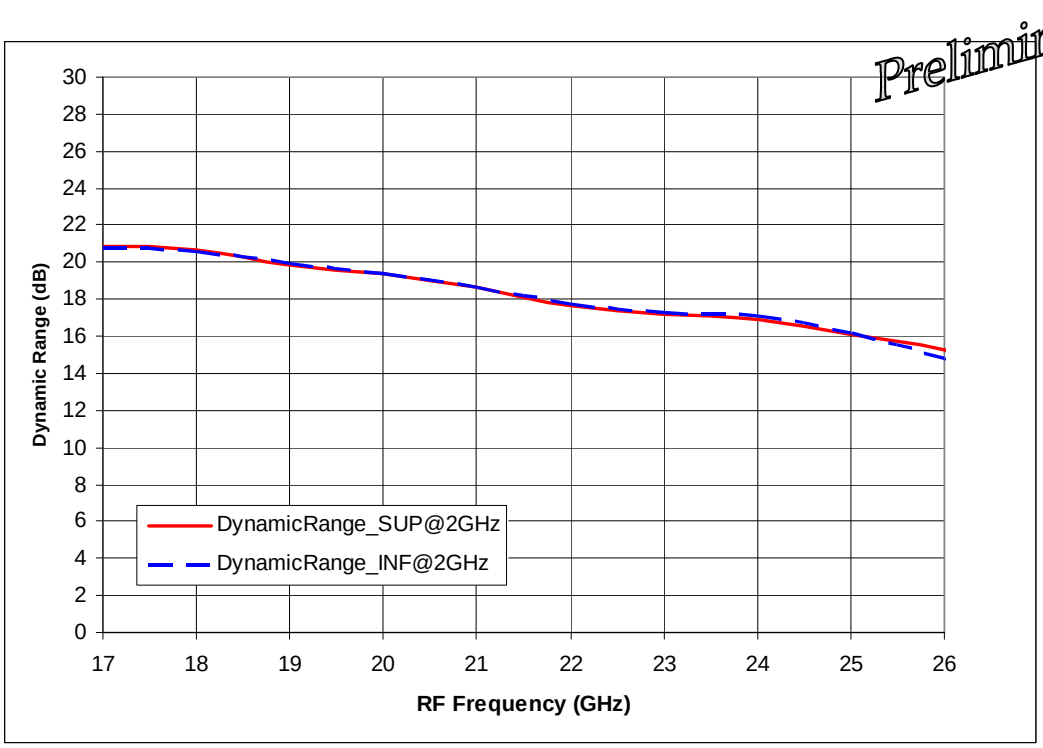

Figure 3 : Dynamic Range (Gcmax – Gcmin) versus Frequency
F_RF=2xF_LO-F_IF & F_RF=2xF_LO+F_IF, F_IF=2GHz

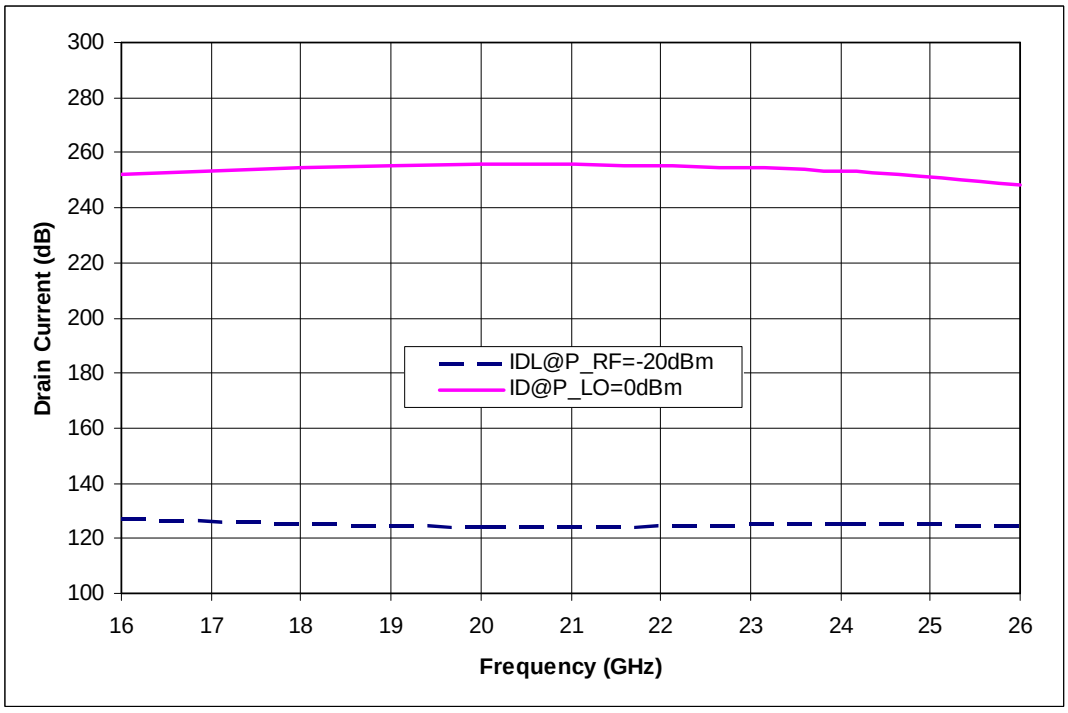

Figure 4 : Drain Currents versus Frequency
F_RF=2xF_LO-F_IF, Freq_IF=2GHz, GC2=GC3=-1.5V

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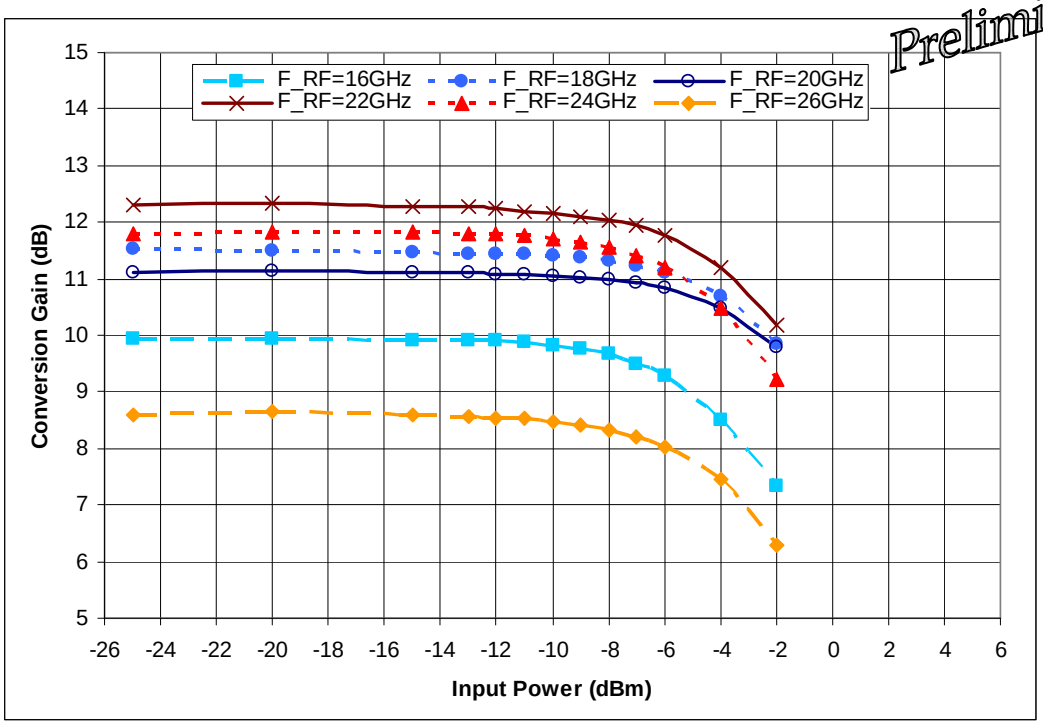

Figure 5 : Conversion Gain versus RF Power
F_RF=2xF_LO+F_IF, F_IF=2 GHz, GC2=GC3=-1.5V

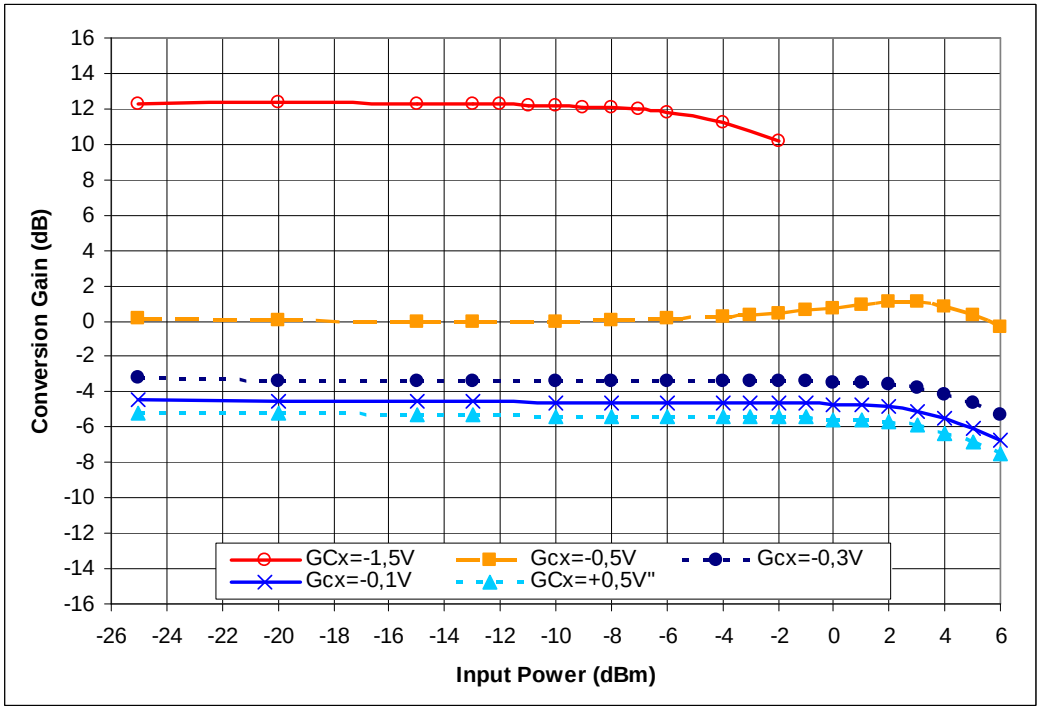

Figure 6: : Conversion Gain versus RF Power
F_RF=2xF_LO+F_IF, F_RF=20 GHz, F_IF=2 GHz

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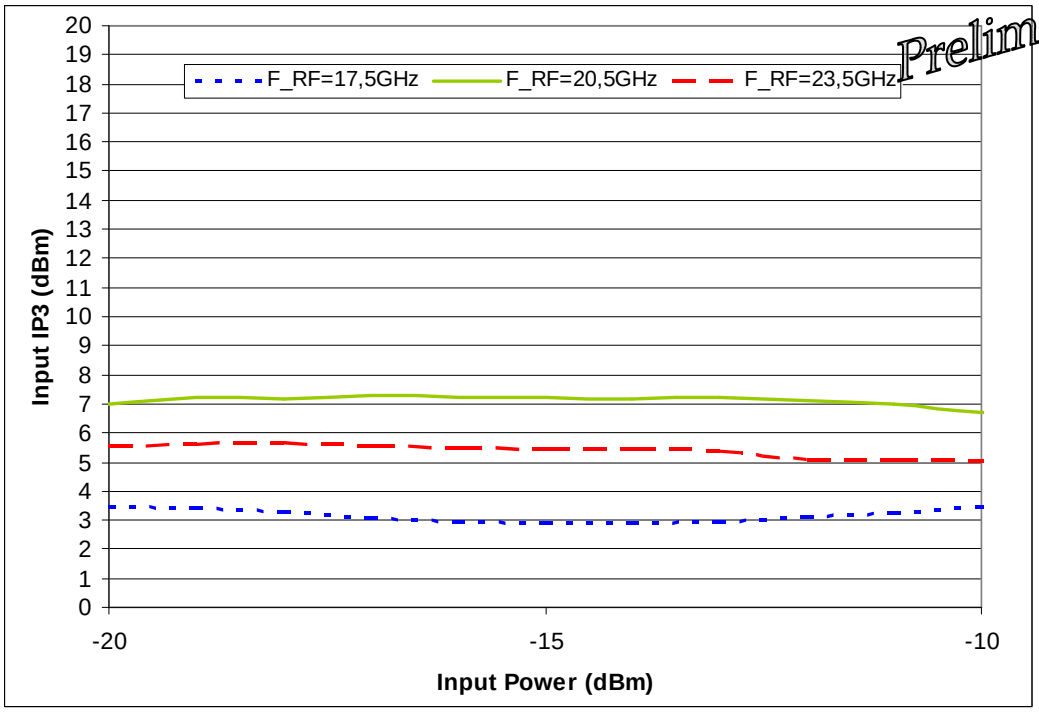

Figure 7 : Input IP3 versus RF Frequency & RF Power (Double Carrier)
F_RF=2xF_LO-F_IF, F_IF=3.5 GHz, GC2=GC3=-1.5V

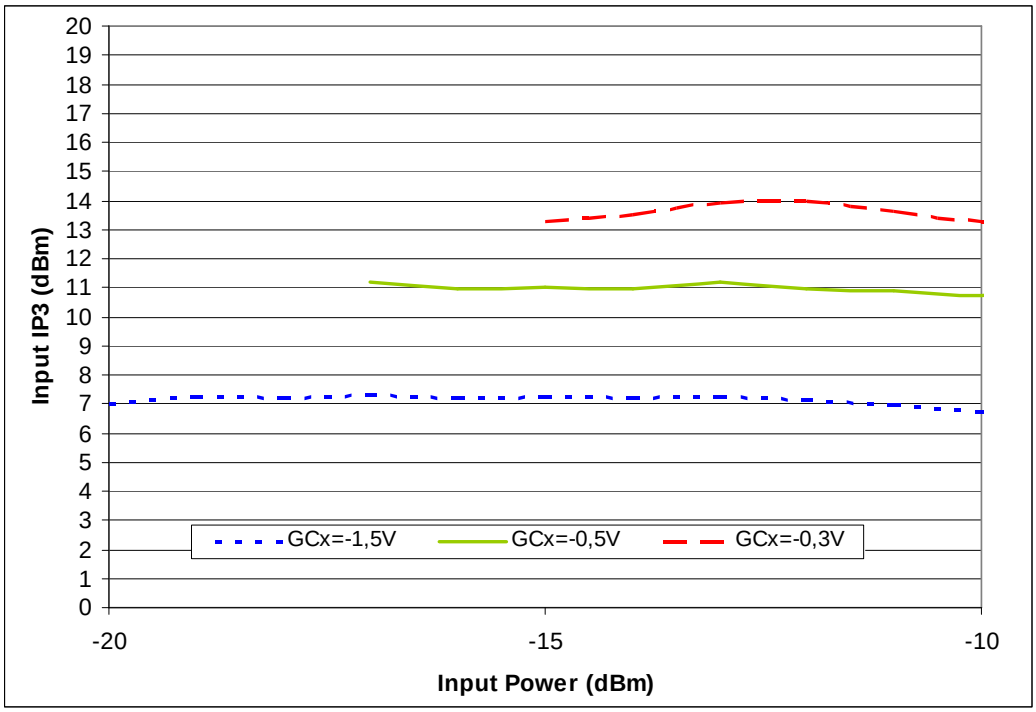

Figure 8 : Input IP3 versus Gain Control & RF Power (Double Carrier)
F_RF=2xF_LO-F_IF, F_RF=20.5 GHz, F_IF=3.5 GHz

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Temperature Measurements

T = [-40, +25, 85] ℃, VD = VDL = 4.5V, VGL=-0.4V, VGM = -0.7V, P_LO = 0 dBm

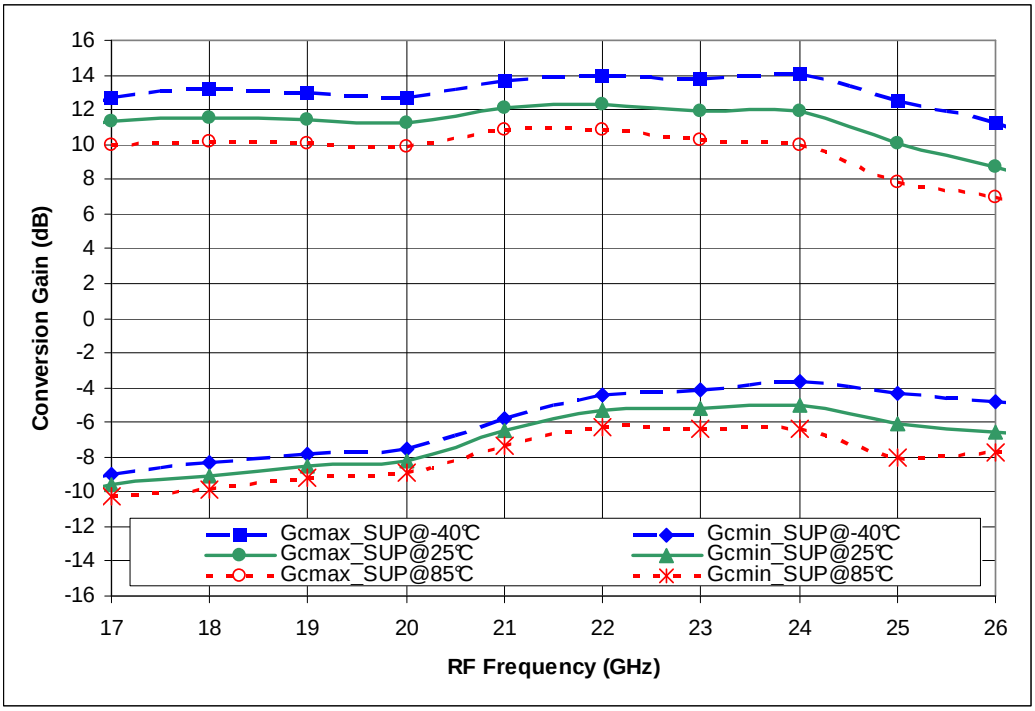

Figure 9: Conversion Gain in Supradyne Mode versus Temperature & Frequency F_RF=2xF_LO+F_IF, F_IF=2GHz, GC2=GC3=-1.5 & 0.5V

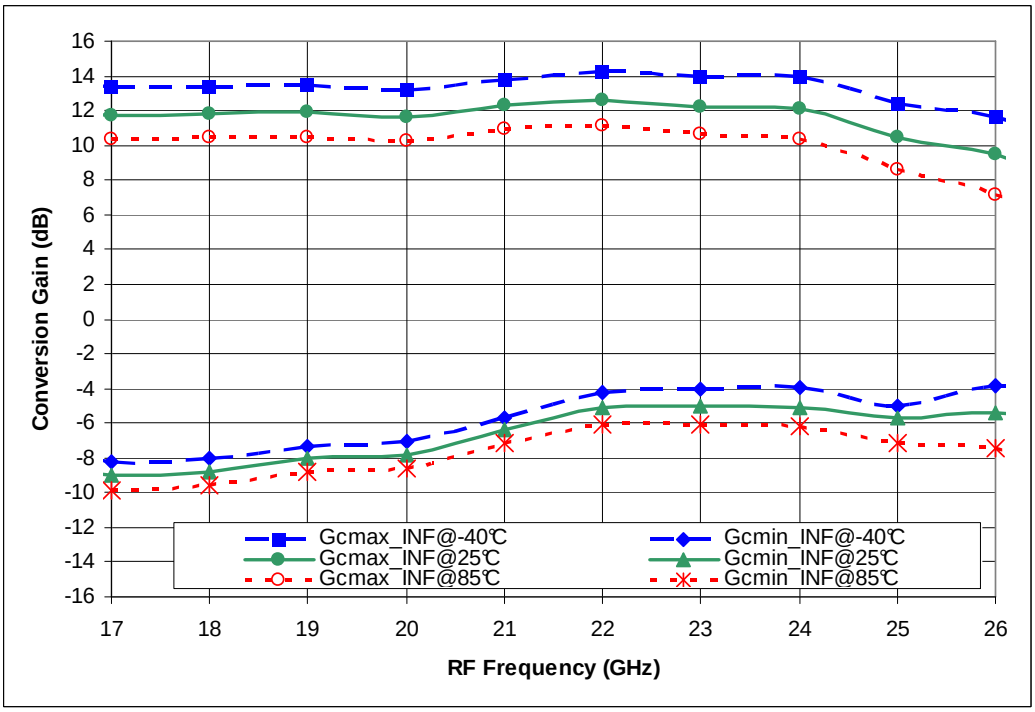

Figure 10 : Conversion Gain in Infradyne Mode versus Temperature & Frequency F_RF=2xF_LO-F_IF, F_IF=2GHz, GC2=GC3=-1.5 & 0.5V

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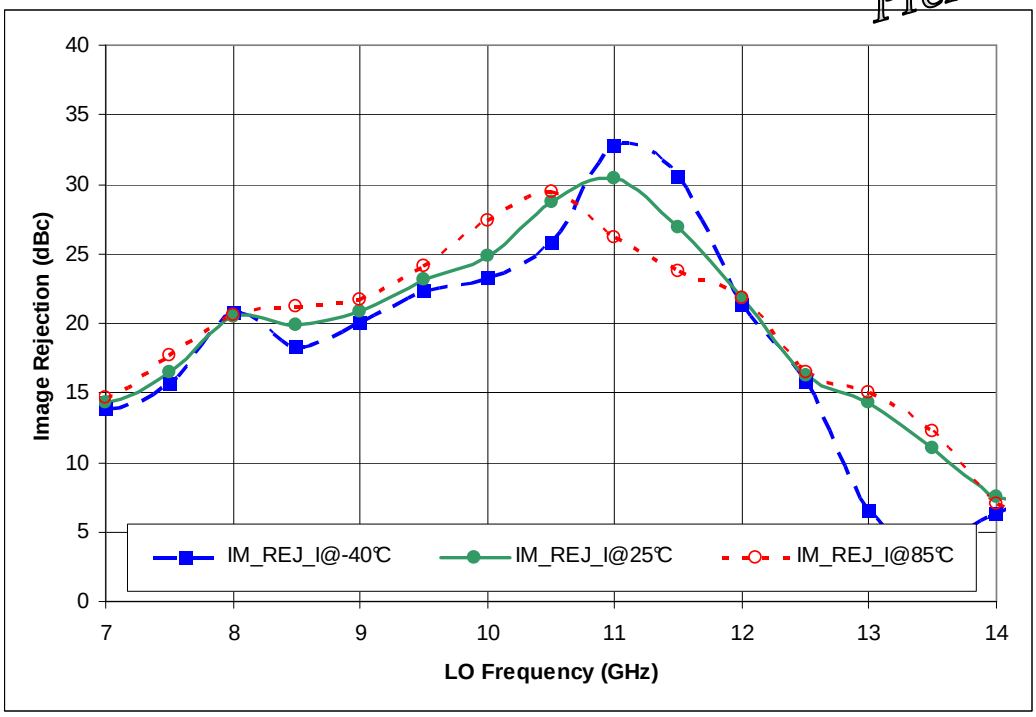

Figure 11 : Image Rejection on Output I
F_IF=2GHz, GC2=GC3=-1.5V

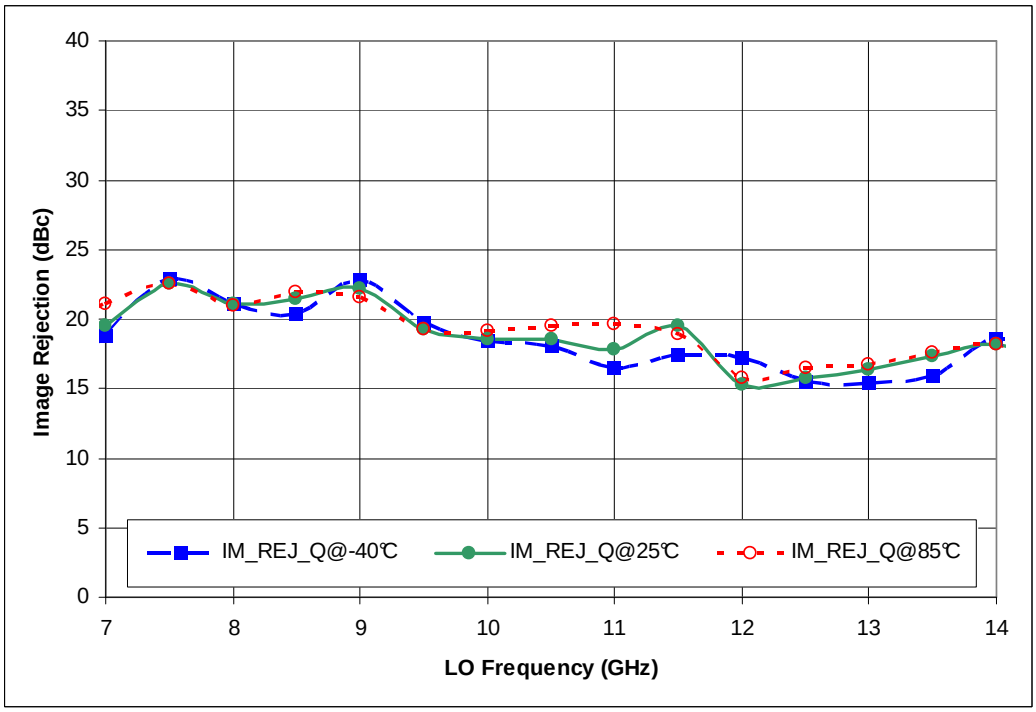

Figure 12 : Image Rejection on Output Q
F_IF=2GHz, GC2=GC3=-1.5V

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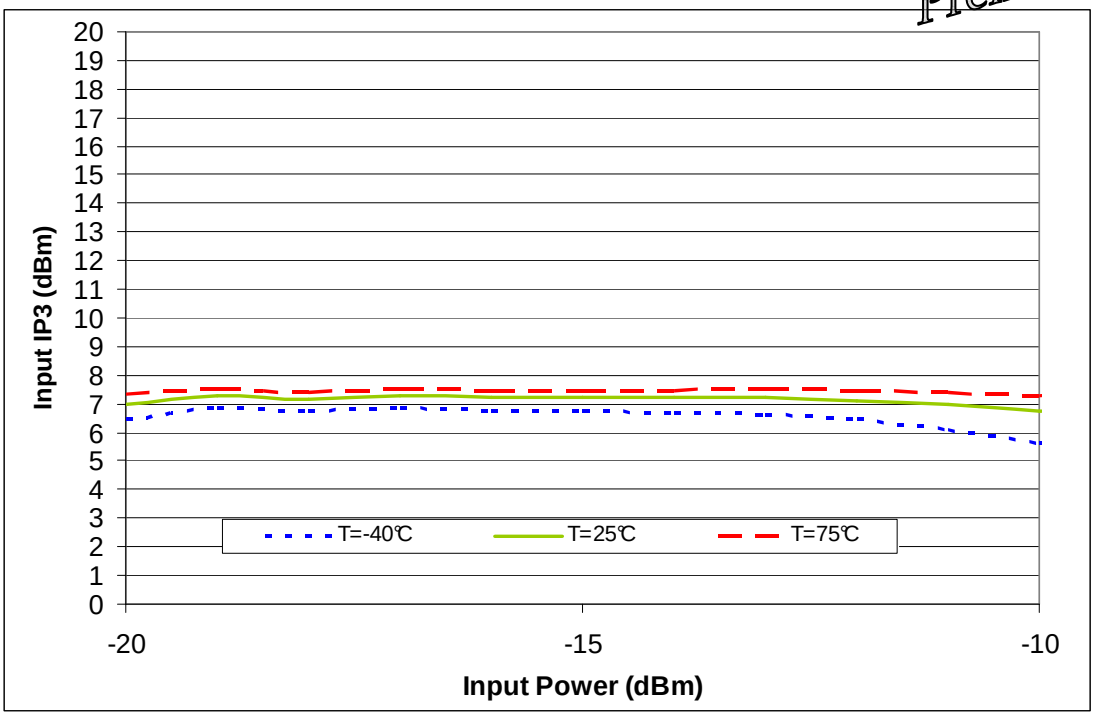

Figure 13 : Input IP3 versus Temperature & RF Power (Double Carrier)
F_RF=2xF_LO-F_IF, F_RF = 20.5 GHz, F_IF = 3.5 GHz, GC2=GC3=-1.5V

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The following values are representative of onboard measurements of the Noise Figure where board losses have been deembedded (result given on package access planes).

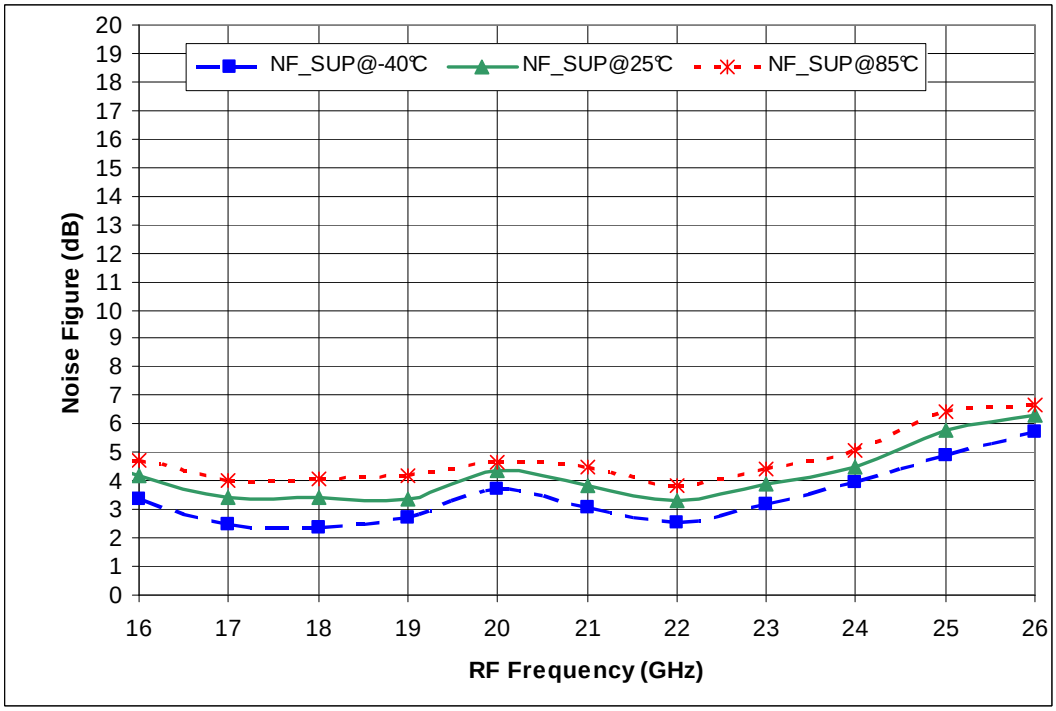

Figure 14 : Noise Figure in Surpradyne Mode vs Temperature & Frequency
F_RF=2xF_LO+F_IF, F_IF=2GHz, GC2=GC3=-1.5V

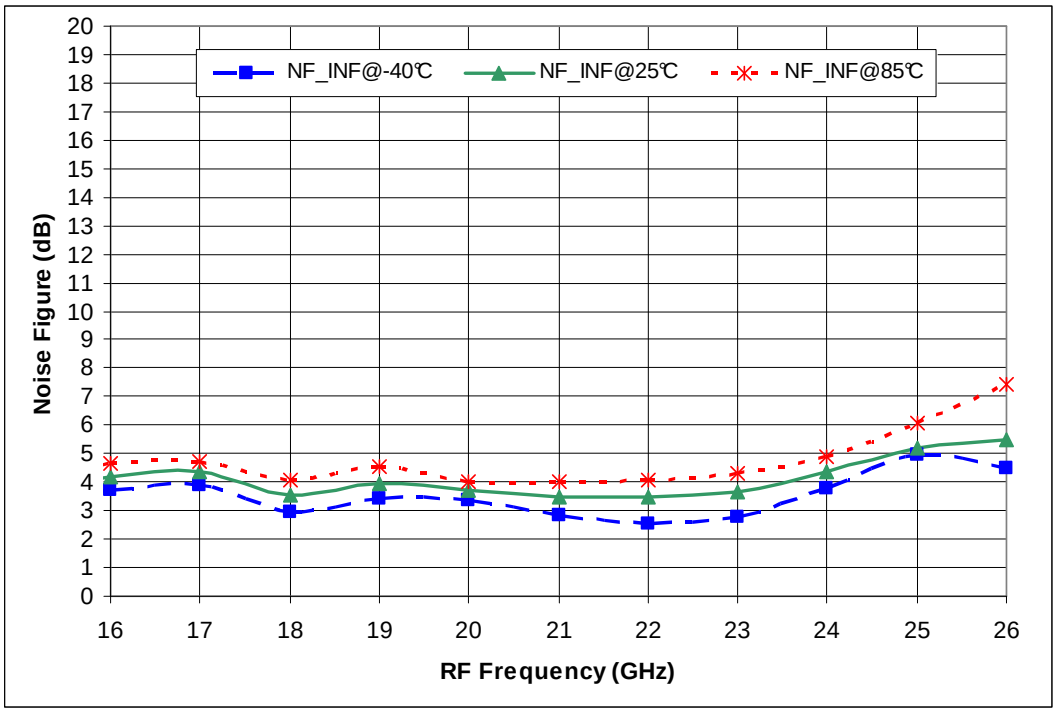

Figure 15 : Noise Figure in Infradyne Mode vs Temperature & Frequency
F_RF=2xF_LO-F_IF, F_IF=2GHz, GC2=GC3=-1.5V

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Package outline (1)

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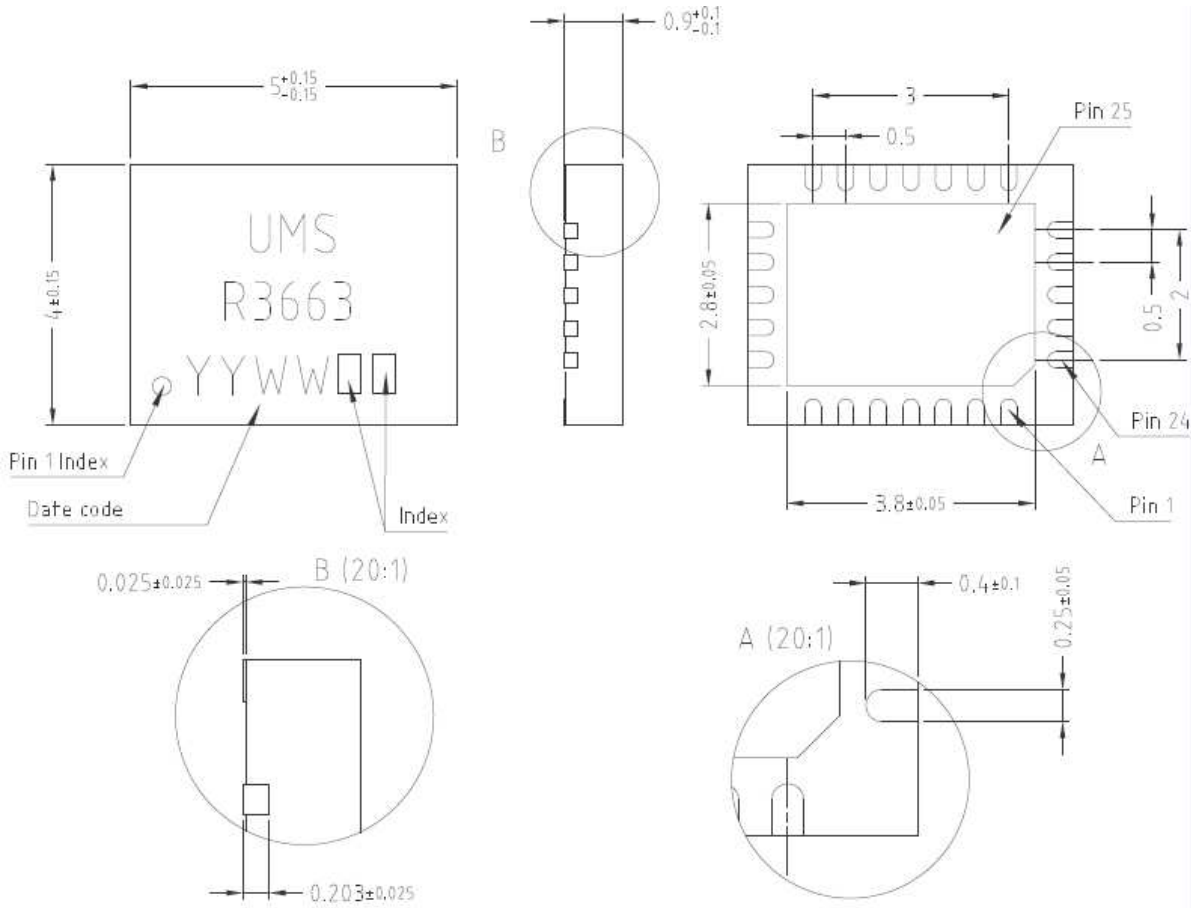

1- Nc	9- VGL	17- Nc	25- GND Exposed Pad
2- Nc	10- VDL	18- Nc	
3- Nc	11- VGM	19- Nc	
4- Gnd	12- VD	20- I	
5- RF	13- Nc	21- Gnd	
6- Gnd	14- Gnd	22- O	
7- GC3	15- LO	23- Nc	
8- GC2	16- Gnd	24- Nc	

(1)The package outline drawing included to this data-sheet is given for indication. Refere to the application note AN0017 available at http://www.ums-gaas.com for exact package dimensions.

(2)It is strongly recommended to ground on the PCB board all the pins referenced as GND.

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Definition of the Sij reference planes

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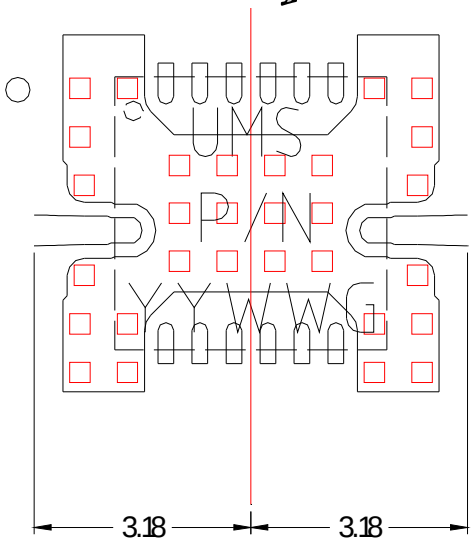
The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended at the page 15.



Recommanded package footprint

Refere to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommandations.

SMD mounting procedure

The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawings above.

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

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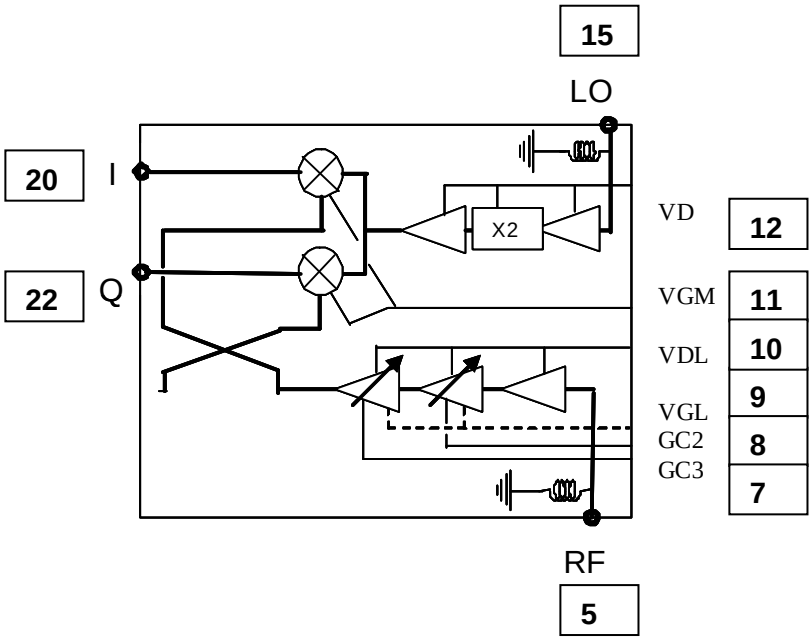
Due to ESD protection circuits on RF and LO inputs, an external capacitance might be requested to isolate the product from external voltage that could be present on these accesses in the application.



ESD protections are also implemented on gate accesses.
The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

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Evaluation mother board

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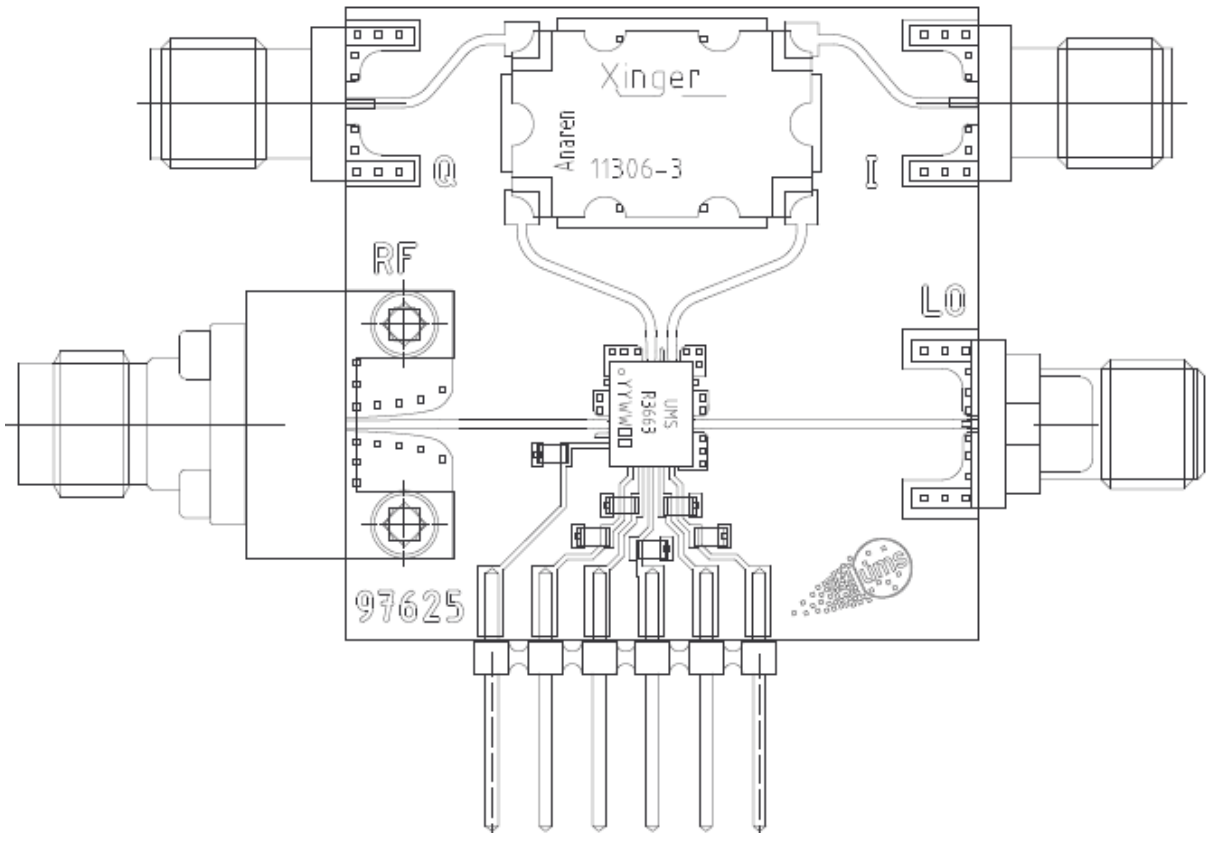
- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- (See application note AN0017 for details).



Decoupling Capacitors = 10nF
Hybrid coupler Anaren 90°2-4GHz

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Ordering Information

QFN 4x5 RoHS compliant package : CHR3663-QEG/XY
Stick: XY = 20 Tape & reel: XY = 21

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