Features

- **Dual ADC, 8-bit Resolution**
- **1 Gsps Sampling Rate per Channel, 2 Gsps in Interlaced Mode**
- **Single or 1:2 Demultiplexed Output**
- **LVDS Output Format (100Ω)**
- **500 mVpp Analog Input (Differential Only)**
- **Differential or Single-ended 50Ω PECL/LVDS Compatible Clock Inputs**
- **Power Supply: 3.3V (Analog), 3.3V (Digital), 2.25V (Output)**
- **LQFP144 Package**
- **Temperature Range:**
  - **0°C<TA<70°C (Commercial Grade)**
  - **-40°C<TA<85°C (Industrial Grade)**

Smart Features

- **3-wire Serial Interface**
- **16-bit Data, 3-bit Address**
- **1:2 or 1:1 Output Demultiplexer Ratio Selection**
- **Full or Partial Standby Mode**
- **Analog Gain (± 1.5 dB) Digital Control**
- **Input Clock Selection**
- **Analog Input Switch Selection**
- **Binary or Gray Logical Outputs**
- **Asynchronous Data Ready Reset**
- **Data Ready Delay Adjustable on Both Channels**
- **Interlacing Functions:**
  - **Offset and Gain (Channel to Channel) Calibration**
  - **Digital Fine SDA (Fine Sampling Delay Adjust) on One Channel**
- **Internal Static or Dynamic Built-In Test (BIT)**

Performance

- Low Power Consumption: 1.4W
- Power Consumption in Standby Mode: 120 mW
- 1.5 GHz Full Power Input Bandwidth (-3 dB)
- SNR = 47 dB Typ (7.3 ENOB), THD = -56 db, SFDR = - 58 dBc at Fs = 1 Gsps Fin = 500 MHz
- 2-tone IMD: -56 dBc Min (499 MHz, 501 MHz) at 1 Gsps
- DNL = 0.25 LSB, INL = 0.5 LSB
- Channel to Channel Input Offset Error: 0.5 LSB Max (After Calibration)
- Gain Matching (Channel to Channel): 0.5 LSB Max (After Calibration)
- Low Bit Error Rate (10^{-13}) at 1 Gsps

Application

- Instrumentation
- Satellite Receiver
- Direct RF Down Conversion
- WLAN

Dual 8-bit 1 Gsps ADC

AT84AD001B Smart ADC™

Preliminary

Summary

For more information
please contact
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2153CS–BDC–12/03

Description

The AT84AD001B is a monolithic dual 8-bit analog-to-digital converter, offering low 1.4W power consumption and excellent digitizing accuracy. It integrates dual on-chip track/holds that provide enhanced dynamic performance up to 1 Gsps sampling rate and over 1.5 GHz input frequency bandwidth. The dual concept, the integrated demultiplexer and the easy interleaving make this device user-friendly for all dual channel applications, such as direct RF conversion or data acquisition. The 3-wire serial interface SMART function enables avoidance of all external components, which are usually needed for gain and offset tuning, etc... leading to space and power reduction as well as system flexibility.

Functional Description

The AT84AD001B is a dual 8-bit 1Gsps ADC based on an advanced high-speed BiCMOS technology.

Each ADC includes a front-end analog multiplexer followed by a Sample and Hold (S/H), and an 8-bit flash-like architecture core analog to digital converter. The output data is followed by a switchable 1:1 or 1:2 demultiplexer and LVDS output buffers (100Ω).

Two over-range bits are given for external gain control adjustment on each channel.

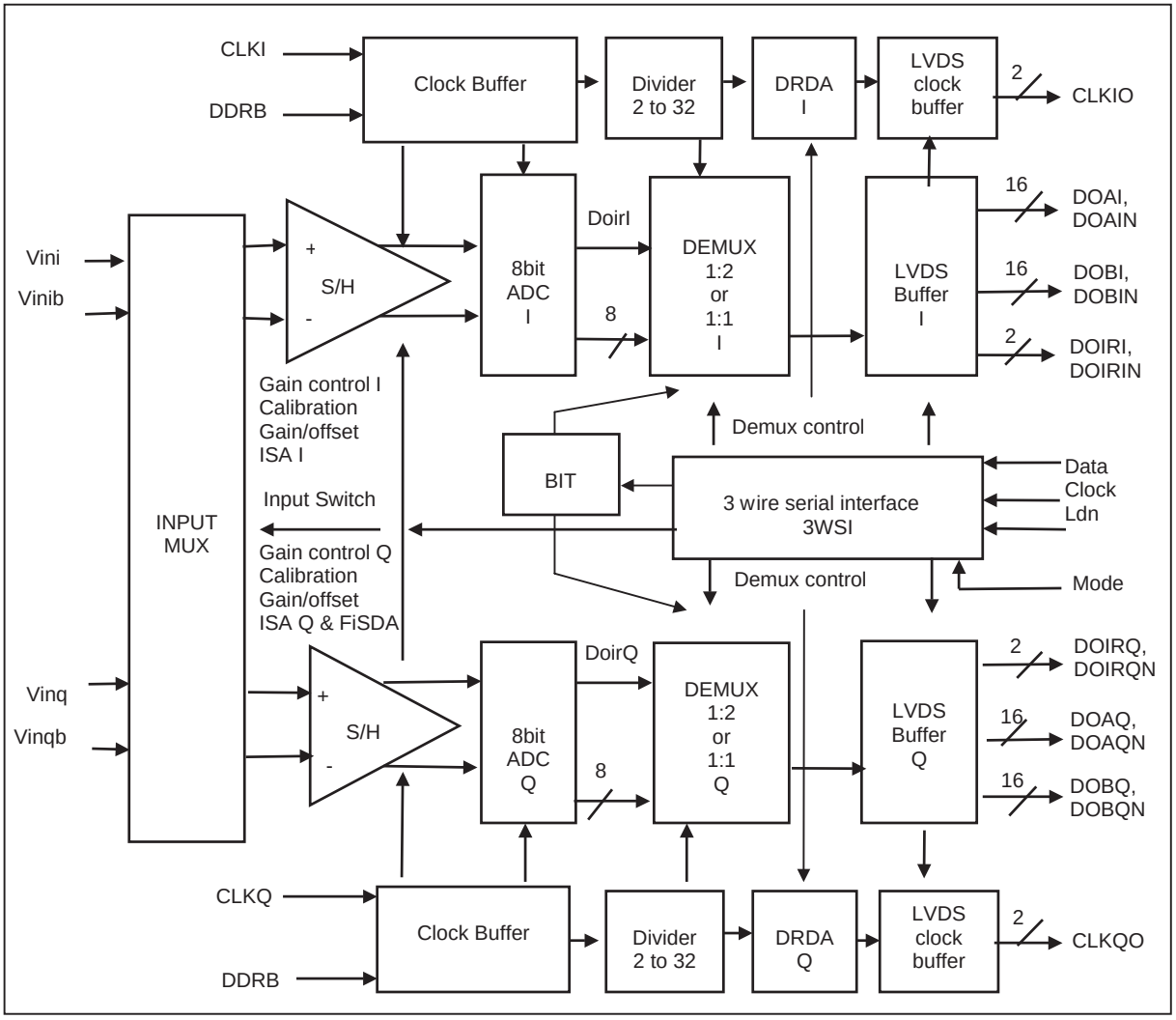
A 3-wire serial interface (3-bit address, 16-bit data) is included to provide several adjustments:

- Analog input range adjustment (±1.5 dB) with 8-bit data control using a 3-wire bus interface (step of 0.18 dB)
- Analog input switch: both ADCs can convert the same analog input signal I or Q
- Gray or binary encoder output. Output format: DEMUX 1:2 or 1:1 with control output frequency on data ready output signal
- Partial or full standby channel I or Q
- Clock selection:
  - Two independent clocks CLKI and CLKQ
  - One master clock (CLKI) with same phase for channel I and Q
  - One master clock but with two phases (CLKI for channel I, CLKIB for channel Q)
- ISA: Internal Settling Adjustment on channel I and Q
- FiSDA: Fine Sampling Delay Adjustment on channel Q
- Adjustable data ready output delay on both channels
- Test mode: decimation mode (by 16), Built-In Test.

A calibration phase is provided to set the two DC offsets of channel I and Q close to code 127.5 and calibrate the two gains to achieve a maximum difference of 0.5 LSB. The offset and gain error can also be set externally via the 3-wire serial interface.

The AD84AD001B works in fully differential mode from analog inputs up to digital outputs. The AD84AD001B features a full power input bandwidth of 1.5 GHz.

Figure 1. Simplified Block Diagram



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