TORISAN

ENGINEERING SPECIFICATIONS

TFT COLOR LCD MODULE

TM070WA-22L06

•18cm (7 inch) diagonal
•Resolution (480xR•G•Bx234 dots)
•With CFL backlight unit
•Nonglare surface type

(PRELIMINARY)

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■ ***REVISION HISTORY***

DATE	REVISION NO.	PAGE	DESCRIPTIONS
July.12,'01	Ver.1	-	Initial release

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■ *MECHANICAL CHARACTERISTICS*

Ta=25deg.

ITEM	SPECIFICATION	UNIT
Module size	167.0(W)×102.0(H)×11.0typ(t)	mm
Resolution	480×R•G•B(W)×234(H)	pixel
Dot pitch	0.107(W)×0.372(H)	mm
Pixel pitch	0.321(W)×0.372(H)	mm
Active viewing area	154.1(W)×87.05(H)	mm
Bezel opening area	158.1(W)×91.0(H)	mm
Weight	220 TYP.	g

■ *ABSOLUTE MAXIMUM RATINGS*

ITEM		SYMBOL		CONDITIONS	MIN	MAX	UNIT	NOTE
Logic/Source power supply voltage		VSH			-0.3	6.0	V	Common power supply voltage of Logic
Power supply voltage for gate driver	H	VGH			-0.3	28	V	
	H-L	VGH-VGL			0	33	V	
	L	VGL			-16.0	+0.3	V	
Common electrode driving signal		VCOM	DC		0	3.0	V	
			P-P		0	6.0	V	
TFT exclusive RGB		VR,VB,VG			-0.3	VSH+0.3	V	
Input signals		V_I			-0.3	VSH+0.3	V	
Output signals		V_O			-0.3	VSH+0.3	V	
Lamp current		L_I			3	4.5	mA	
Ambient temperature		T_{ST}		Storage	-30	85	deg.	Note 1),2)
		T_{OP}		Operation	-30	85		
Humidity		-		TaC=<60deg.		90	%RH	not beyond 240H Note 3)

Note 1) Care should be taken so that the LCD module may not be subjected to the temperature beyond this specification.

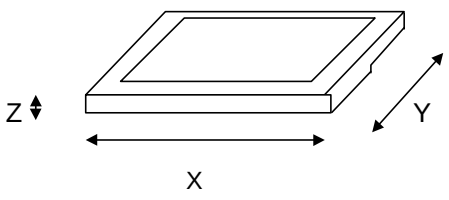
Note 2) Ambient temperature shows temperature on LCD surface. Module temperature is apt to increace while it's driving due to CFL heat etc. Please design carefully not to exceed +85 degree C on every surface of LCD that shoud come to contact with any other equipment. Temperature for operation is one which only assures LCD operation. Contrast, response time,or other LCD quality is regulated under condition of Ta=+25 degree C.

Note 3) Please be advised that dew condensation level should be less than maximum wet bulb temperature 58 degree C. Dew condensation may induce leak current, and also influence LCD performance.

■ *MECHANICAL ENVIRONMENT*

Vibration	-	Storage	-	2.9	G	Note 1)
Shock	-	Storage	-	100	G	XYZ 6ms/direction

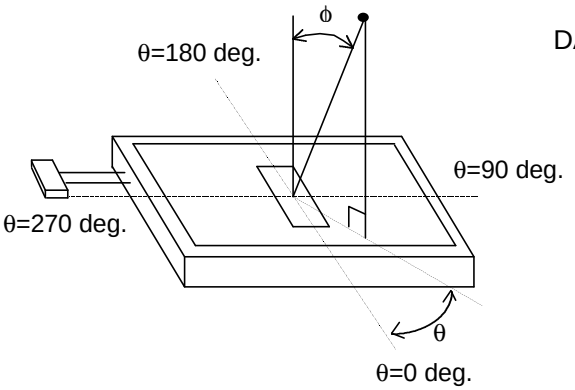
Note 1) Vibration frequency : 8 - 33.3 Hz displacement : 1.3mm
Vibration frequency : 33.3 - 400Hz
Sweep time : 15 min./1 sweep
total test time : X,Y-2Hr Z-4Hr



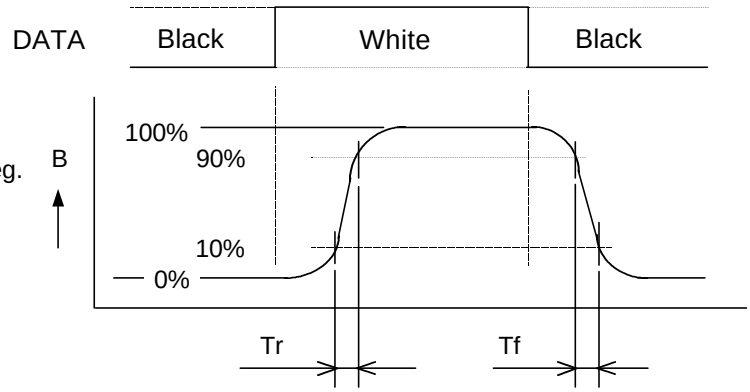
■ *OPTICAL CHARACTERISTICS (1)*

Ta=25deg., VSH=5.3V, fv=60Hz

ITEM		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	NOTE
Viewing angle range		ϕ	K=>5	θ = 0 deg.	-	-	40	deg.	Note 1),4)
				θ = 90 deg.	-	-	60		
				θ =180 deg.	-	-	30		
				θ =270 deg.	-	-	60		
Contrast ratio		K	θ =0 deg.,ϕ =0 deg.		100	-	-	-	Note 2),4)
Response time	Rise	tr	θ =0 deg.,ϕ =0 deg.		-	30	-	ms.	Note 3),4)
	Fall	tf			-	20	-		
Color of CIE Coordinate	White	x	θ =0 deg.,ϕ =0 deg.		-	0.300	-		Note 4)
		y			-	0.298	-		



Note 1) θandϕ are defined as above figure.



Note 3) Response time

Note 2) Contrast ratio "K" is defined below formula.

$$K = \frac{\text{Brightness at ON (White)}}{\text{Brightness at OFF (Black)}}$$

Note 4) Measurement codition

① VSH=5.3V,VGH=15V,VGL=-14.0V,VCOM DC=1.8V,VCOM P-P=5.0V
② VR/VG/VB DC=VSH/2, VR/VG/VB AC=4.0V
③ Follow brightness measurement condition in next item.

■ *OPTICAL CHARACTERISTICS (2)*

Ta=25 deg.

ITEM	SYM.	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Brightness	B		-	400	-	cd/m^2	Surface Brightness of LCD

Note) The brightness shall be the following point.

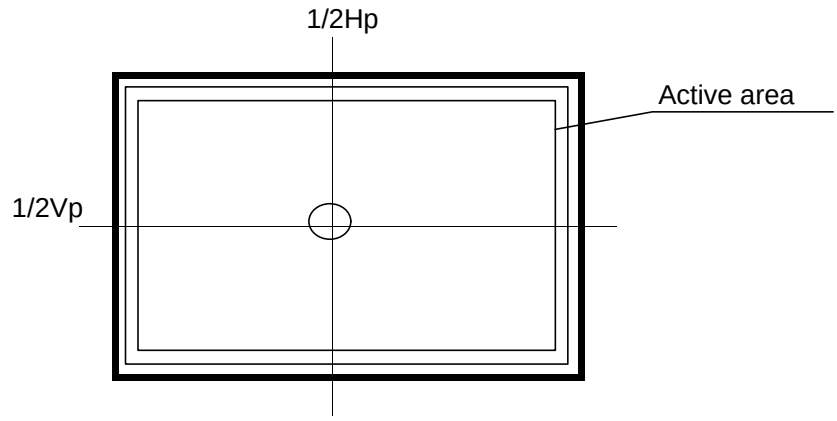


Fig.1 Measurement point

Vp :Total Number of Vertical pixel
Hp :Total Number of horizontal pixel

Measurement equipment : BM-7(TOPCON Corp.)
Measurement condition

① Ambient temperature : 25 ±2 deg.
② LCD : All pixels are WHITE
③ Measure after 30 minutes of CFL warm up.
④ IL=4.5mArms, CFL inverter:
Operating TDK CXA-L0612A-VJL or equivalent inverter with capability of frequency 50kHz, Lamp current max.4.5mA

■ *BACKLIGHT CHARACTERISTICS*

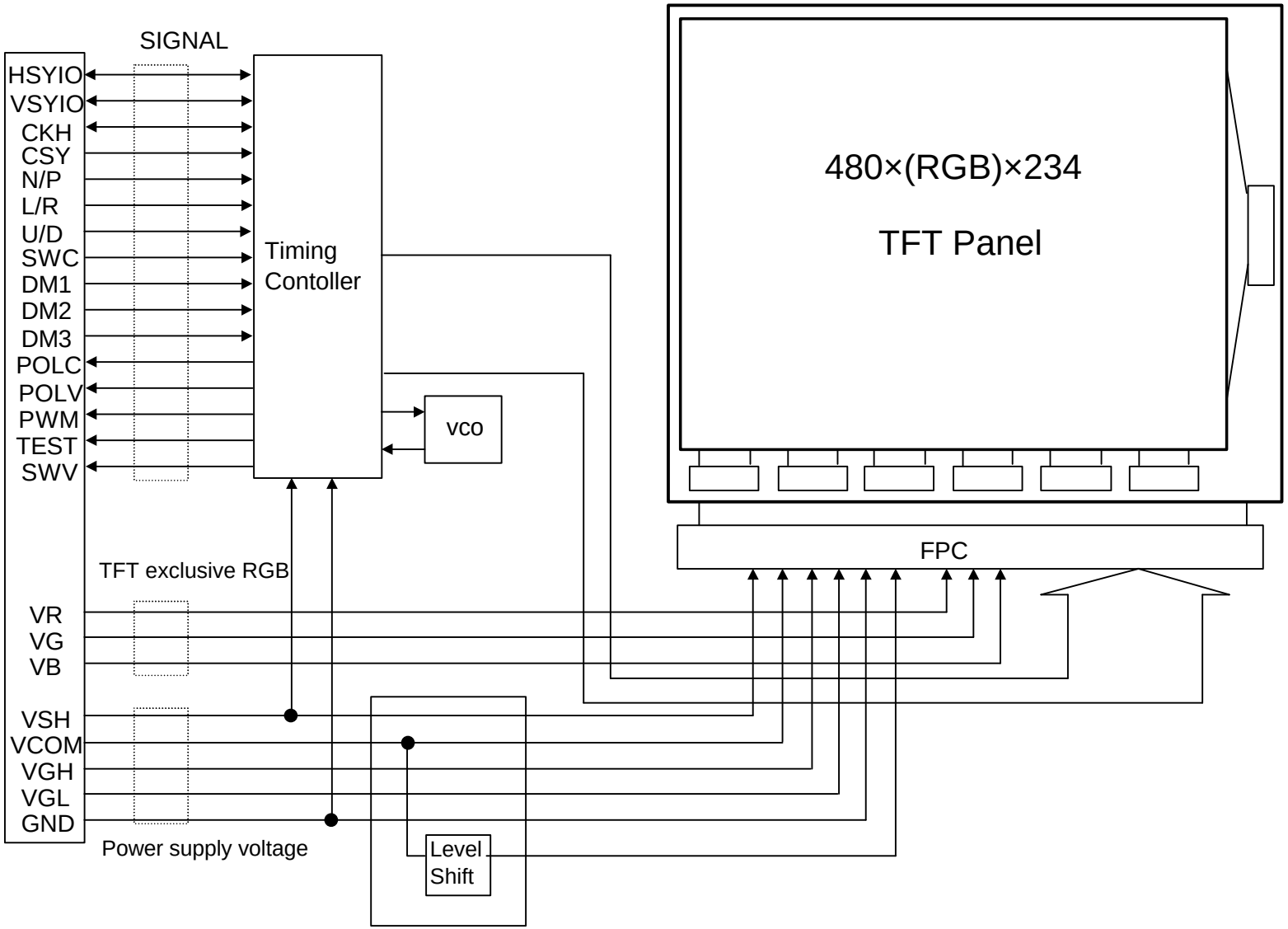
Ta=25 deg.

ITEM	SYM.	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Lamp voltage	V_L		-	740	-	Vrms	at IL=4.5mArms
Lamp current	I_L		3.0	-	4.5	mArms	(Recommended value)
Operating frequency	f_L		40	48	55	KHz	(Recommended value)
Start up voltage	V_{S1}		-	-	1750	Vrms	at Ta= 25 deg.
Start up voltage	V_{S2}		-	-	1800	Vrms	at Ta=-30 deg.
Lamp life	t_{OL}		10000	-	-	Hours	at IL=4.5mArms, Note 1)
Backlight power supply	WL		-	3.3	-	W	at IL=4.5mArms

Note 1) CFL Lamp life indicates time from initial Lamp brightness to half of original brightness.
Note 2) Inverter GND shall be connected to LCD frame.(Please refer to outer dimension drawing) LCD frame is connected to internal circuitry GND.

■ ***BLOCK DIAGRAM***

IF BLOCK 24PIN



■ *INTERFACE PIN CONNECTIONS*

LCM : CN

PIN NO.	SYMBOL	I/O	FUNCTION
1	HSYIO	I/O	Input/Output horizontal sync.signal(low active)
2	POLC	O	Polarity alternating signal for common signal
3	CSY	I	Composite sync.signal(high active)
4	VGH	I	Power supply for gate driver(high level)
5	POLV	O	Polarity alternating signal for video signal)
6	VB	I	Color video signal(Blue)
7	VR	I	Color video signal(Red)
8	VG	I	Color video signal(Green)
9	GND	I	GND
10	VSH	I	Positive power supply voltage
11	VGL	I	Power supply for gate driver(low level)
12	VCOM	I	Common electrode driving signal
13	N/P	I	Selection for NTSC or PAL(NTSC=VSH,PAL=GND)
14	VSYIO	I/O	Input/Output vertical sync.signal(low active)
15	L/R	I	Selection for horizontal scanning direction
16	U/D	I	Selection for vertical scanning direction
17	SWC	I	Selection for input/output direction of CKH,HSYNC,VSYNC
18	PWM	O	Timinng signal for PWM dimming of backlight
19	TEST	O	Open use only
20	CKH	I/O	Input/output clock signal
21	DM1	I	Selection for display mode
22	DM2	I	Selection for display mode
23	DM3	I	Selection for display mode
24	SWV	O	Video selection timming signal

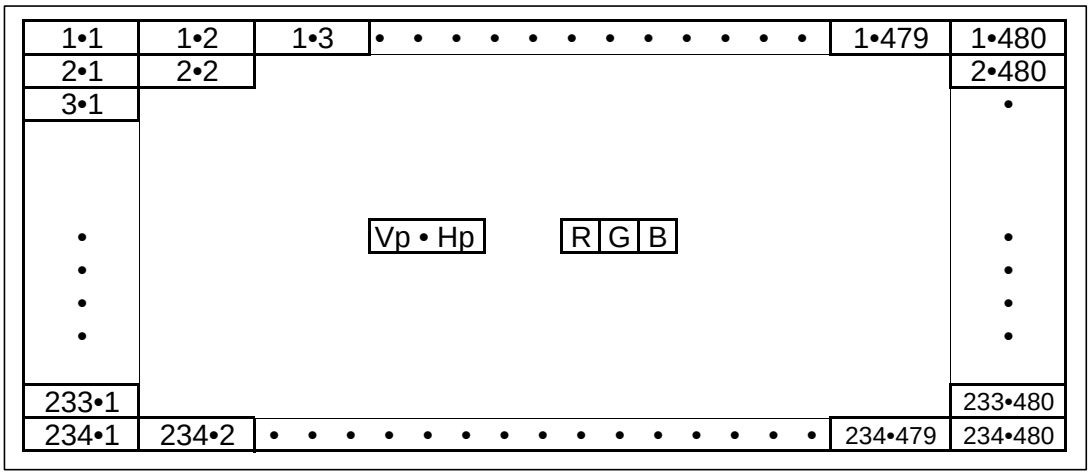
I/F CN : SFR24R-1ST(FCI)
Suitable FPC : Pitch 0.8mm,Width 20mm

Back Light : FLCN

PIN NO.	SYMBOL	FUNCTION
1	H.V	High voltage for CFL
2	N.C	No Connection
3	LGND	Low voltage for CFL

FLCN : BHR-03VS-1(JST)
Suitable mating connector : SM02(8.0)B-BHS-1(JST)

■ *RELATIONSHIP BETWEEN INPUT DATA AND DISPLAY POSITION*



■ *FUNCTION,MODE AND TERMINALS*

Mode terminals					Sync. signal I/O terminals					
SWC	N/P	DM1	DM2	DM3	HSYIO	VSYIO	CKH	SWV	CSY	Remarks
H	H or L	L L L	H L L	L H L	Hsync output	Vsync output	Lo output	Test signal output	Conposite sync input	Test mode
H	H or L	H	L	H	Hsync output	Vsync output	Lo output	masking signal output	Conposite sync input	NTSC or PAL mode (Normal mode)
H	H or L	other settings H or L			Hsync output	Vsync output	Lo output	Lo output	Conposite sync input	NTSC or PAL mode (Full,Wide,Cinema)
L	H	H	H	H	Hsync input	Vsync input	Pixel clock input	Lo output	Input Hi or Lo fixed value	External clock synchronous mode

Note 1) We recommend external clock synchronize method except for TV display usage.

Note 2) Please invert polarity of video signal VR,VG and VB in sync with invert timing of POLV signal.(Please refer Figure A.)

Note 3) Please invert polarity of VCOM in sync with invert timing of POLC signal. (Please refer Figure B.)

Note 4) Horizontal synchronized signal is output in sync with CSY signal when SWC is Hi. When SWC is Low, LCD module is operated in sync with Horizontal synchronized signal for HSYIO terminal.(Please refer Figure C,D,G and F.)

Note 5) In normal mode, non-display area at both edge of display can be better screened by masking video signal following SWV output signal. (Please refer timing chart E.)

Note 6) PWM signal for CFL brigtness control is output form PWM terminal. (Please refer Figure H.) But please use it when normal NTSC or PAL signals are inputted.

■ *DISPLAY METHOD AND CHARACTERISTICS*

H=VSH L=GND

DM1	DM2	DM3	Display Mode	Display method, Feature	SOURCE	Horizontal Disply area	Horizontal Sampling	Vertical Disply area NTSC	Vertical Disply area PAL	EXAMPLE
H	H	H	Full mode	Display 4:3 image long sideways.	4:3 signal Navigation Signal	Signal area	Senter Both side Same	S=1/1	S=6/7 Compress	Fig.2-1
H	H	L	Wide1 mode	Display perfect circle around center better than Full screen mode.	4:3 signal	Signal area	Senter :Slow Botn side:Fast	S=1/1	S=6/7 Compress	Fig.2-2
H	L	H	Normal mode	Display perfect circle all around the screen. Both edge screen can be masked with SWV.	4:3 signal	Signal area & Blank	Senter :Slow Botn side:Fast Modulation wide1,2<Nomal	S=1/1	S=6/7 Compress	Fig.2-3
H	L	L	Cinema mode	Display 16:9 image.	Wide signal(16:9)	Signal area	Senter Both side Same	S=4/3 Extend	S=20/21 Compress	Fig.2-4
L	H	H	Wide 2 mode	Display perfect circle around center better than Wide 1 mode. Top and bottom images are eliminated.	4:3 signal	Signal area	Senter :Slow Botn side:Fast	S=5/4 Extend	S=10/11 Compress	Fig.2-5
L	H	L	Test mode	This mode is unusable due to test mode.	-	-	-	-	-	-
L	L	H	Test mode	This mode is unusable due to test mode.	-	-	-	-	-	-
L	L	L	Test mode	This mode is unusable due to test mode.	-	-	-	-	-	-

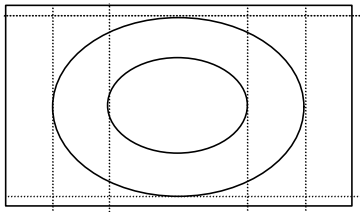


Fig2-1
Full mode

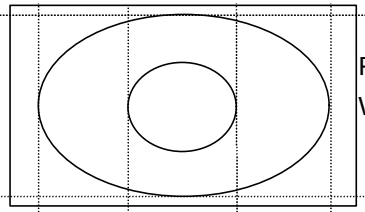


Fig2-2
Wide1 mode

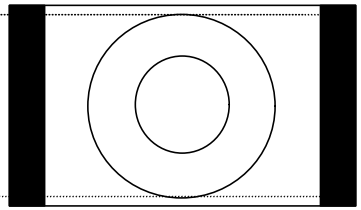


Fig2-3
Normal mode

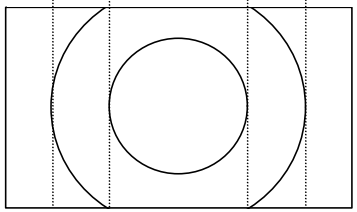


Fig2-4
Chinema mode

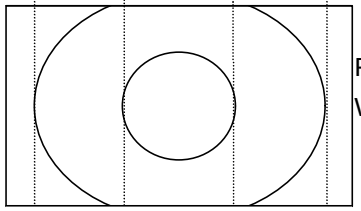


Fig2-5
Wide 2 mode

<DISPLAY AREA>

①NTSC MODE(N/P=H, SWC=H)

(a1)Horizontal…Full mode, Wide1 mode, Wide2 mode, Cinema mode

From falling edge of HSYIO output to 12.8-63.1μS.

(a2)Horizontal…Normal mode

From falling edge of HSYIO output to 7.5-68.5μS.

(b1)Vertical…Full mode, Wide2 mode, Normal mode

From falling edge of VSYIO output to 20H-253H.

(b2)Vertical…Cinema mode

From falling edge of VSYIO output to 49H-224H.

(b3)Vertical…Wide2 mode

From falling edge of VSYIO output to 42H-228H.

②PAL MODE(N/P=L, SWC=L)

(a1)Horizontal…Full mode, Wide1 mode, Wide2 mode, Cinema mode

From falling edge of HSYIO output to 12.8-63.1μS.

(a2)Horizontal…Normal mode

From falling edge of HSYIO output to 7.5-68.5μS.

(b1)Vertical…Full mode, Wide2 mode, Normal mode

From falling edge of VSYIO output to 26H-298H.

Except for Even Nunber Field (14n+12) and (14n+20),

Odd Number Field (14n+17) and (14n+23).

n=(1,2,3,…,20)

(b2)Vertical…Cinema mode

From falling edge of VSYIO output to 40H-284H.

Except for Even Nunber Field (42n+13) and (14n+35),

Odd Number Field (42n) and (42n+22).

n=(1,2,3,…,6)

(b3)Vertical…Wide2 mode

From falling edge of VSYIO output to 35H-289H.

Except for Even Nunber Field (22n+14) and (22n+24),

Odd Number Field (22n+21) and (22n+31).

n=(1,2,3,…,12)

③EXTERNAL CLOCK MODE(N/P=H, SWC=L,DM1,2,3=H)

(a1)Horizontal

From falling edge of HSYIO output to 99-578CLK.

CLK is indicated as external CLK number.

(b3)Vertical

From falling edge of VSYIO output to 20H-253H.

■ *ELECTRICAL CHARACTERISTICS*

VSH=5.3V, Ta=25 deg.

ITEM		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Logic/Source power supply voltage		VSH		5.0	5.3	5.5	V	Note 3)
Power supply voltage for gate driver	H	VGH		14.5	15.0	15.5	V	
	L	VGL		-14.5	-14.0	-13.5	V	
Common electrode driving signal		VCOM	DC center	1.0	1.8	2.5	V	Note 1)
			P-P	4.0	5.0	6.0	V	Note 2),4)
TFT exclusive RGB		VR,VG,VB	DC center	TYP-0.1	VSH/2	TYP+0.1	V	Note 3)
			AC White pattern	+1.5	2.0	VSH/2	V	POLV=H Note4),5)
			AC Black pattern	-1.5	-2.0	-VSH/2	V	POLV=H Note4),5)
			AC White pattern	-1.5	-2.0	-VSH/2	V	POLV=L Note4),5)
			AC Black pattern	+1.5	2.0	VSH/2	V	POLV=L Note4),5)
Input signals		V_{IH}	High level	0.7VSH	-	VSH	V	Note 6)
		V_{IL}	Low level	0	-	0.3VSH	V	
Input signals		V_{IH}	High level	0.8VSH	-	VSH	V	Note 7)
		V_{IL}	Low level	0	-	0.2VSH	V	
Output signals		V_{OH}	High level	VSH-2.1	-	-	V	Note 8)
		V_{OL}	Low level	-	-	0.4	V	
Power Supply current		I_{VSH}	VSH=5.3V	-	50	80	mA	Note 9,10)
		I_{VGH}	VGH=15V	-	1.2	3	mA	
		I_{VGL}	VGL=-14.0V	-	6	15	mA	
Power Supply		WS		-	367	679	mW	

Note 1) Please adjust DC voltage on opposite electrode (VCOM) to optimum BIAS voltage in order to minimize flicker.

Note 2) Please optimize voltage of each module to achieve optimum contrast.

Note 3) Please control voltage fluctuation less than 0.1V after VCOM is adjusted.

Note 4) =+/- amplitude shall be symmetry.

Note 5) In case of POLV=Low, the signal polarity inverts working with polarity of VCOM.

Note 6) Symmetric terminal name: HSYIO,VSYIO(CMOS INPUT)

Note 7) Symmetric terminal name: CSY,N/P,L/R,U/D,SWC,CKH,DM1,DM2,DM3(CMOS Schmitt INPUT)

Note 8) Symmetric terminal name: HSYIO,POLC,POLV,VSYIO<PWM,CKH,SWC(CMOS OUTPUT)
(COMS output level)

Note 9) Under the following conditions:

Display pattern: ALL BLACK FULL MODE fv:60Hz

VCOM DC=1.8V,VCOM P-P=5.0V
VR/VG/VB DC=VSH/2 VR/VG/VB AC=4.0V

Note10) Value for module circuitry portion (except for backlight)

■ *ELECTRICAL CHARACTERISTICS AC TIMING*

NTSC :fH=15.73kHz,fV=60Hz,t HI=4.7µs
PAL :fH=15.63kHz,fV=50Hz,t HI=4.7µs

<COMMON: EXTERNAL CLK MODE/BUILT-IN CLK MODE>(SWC=Hi or Low)

VSH=5.3V GND=0V, Ta=25 deg.

ITEM		SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Input voltage		VID	0	-	VSH	V	
Input composite sync	rising time	t rVI	-	-	0.2	µs	
[CSY]Vertical location	falling time	t fVI	-	-	0.2	µs	
Polarity alternating delay time [POLV-VRGB]		tDV	-	-	4	µs	
Polarity alternating delay time[POLC-VCOM]		tDC	-	-	4	µs	
Output polarty signal	rising time	t rPL	-	-	0.5	µs	
[POLC,POLV]	falling time	t fPL	-	-	0.5	µs	

<BUILT-IN CLK MODE>(SWC=Hi)

VSH=5.3V GND=0V, Ta=25 deg.

ITEM			SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Input composite sync	frequency	NTSC	fH(N)	15.13	15.73	16.33	kHz	Note 1
horizntal location		PAL	fH(P)	15.03	15.63	16.23	kHz	
	pulse wide	NTSC	tHI(N)	4.2	4.7	5.2	µs	
		PAL	tHI(P)	4.2	4.7	5.2	µs	
	rising time		trHI1	-	-	0.5	µs	
[CSY]	falling time		tfHI1	-	-	0.5	µs	
Input composite sync	frequency	NTSC	fV(N)	fH/284	fH/262.5	fH/258	Hz	Note 1
Vertical location		PAL	fV(P)	fH/344	fH/312.5	fH/304	Hz	
	pulse wide	NTSC	tVI(N)	-	3	-	H	
[CSY]		PAL	tVI(P)	-	2.5	-	H	
Output horizontal	frequency		fH0	-	fH	-	kHz	Note 2
sync signal	pulse wide		tH0	-	4.7	-	µs	
	rising time		trH0	-	-	0.5	µs	
[HSYIO]	falling time		tfH0	-	-	0.5	µs	
horizontal sync phase	rising HSY		tpd1	-	2.1	-	Hz	
[HSYIO-CSY]	falling HSY		tpd2	-	2.1	-	Hz	
Output vertical	frequency		fV0	-	fV	-	Hz	
sync signal	pulse wide		tV0	-	4	-	H	1H=1/fH
	Output phase		tVH0	-	11	-	µs	Sync HSYIO
[VSYIO]	rising time		trV0	-	-	0.5	µs	
	falling time		t fV0	-	-	0.5	µs	
Vertical sync phase	ODD FIELD		t DV1	-	1	-	H	
[CSY-VSYIO]	EVEN FIELD		t DV2	-	0.5	-	H	

Note 1) Standard complex synchronized signal [CSY] type of NTSC/PAL signal shall be inputted. It would be a factor of display quality degradation if nonstandard synchronized signal were inputted.

Note 2) Varied by tpd1 value.

<EXTERNAL CLK MODE>(SWC=Low)

VSH=5.3V GND=0V, Ta=25 deg.

ITEM		SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Input CLK sync signal [CKH]	frequency	fCL1	8.5	9.5	9.8	MHz	
	H pulse wide	tWH	20.0	-	-	ns	
	L pulse wide	tWL	20.0	-	-	ns	
	rising time	trCL1	-	-	10.0	ns	
	falling time	tfCL1	-	-	10.0	ns	
Input horizontal sync signal [HSYIO]	frequency	fHI	fCLI/650	fCLI/608	fCLI/590	kHz	
	pulse wide	tHI	1	5	9	µs	
	rising time	trHI2	-	-	0.05	µs	
	falling time	tfHI2	-	-	0.05	µs	
Input Vertical sync signal [VSYIO]	frequency	fVI	50	fHI/262	fHI/258	Hz	
	pulse wide	tVI	1	3	5	H	
Data setup time		t SU1	25	-	-	ns	Note 3)
Data hold time		t HO1	25	-	-	ns	
Data setup time		t SU2	1.0	-	-	µs	Note 4)
Data hold time		t HO2	1.0	-	-	µs	

Note 3) In external clock input mode, they show input phase contrast of CKH and HSYIO signal.
Data is loaded latching with CKH rising signal.

Note 4) In external clock input mode, they show input phase contrast of HSYIO andVSYIO signal.
Data is loaded latching with HSYIO falling signal.

■ *ELECTRICAL CHARACTERISTICS AC TIMING*

<COMMON: EXTERNAL CLK MODE/BUILT-IN CLK MODE>(SWC=Hi or Low)

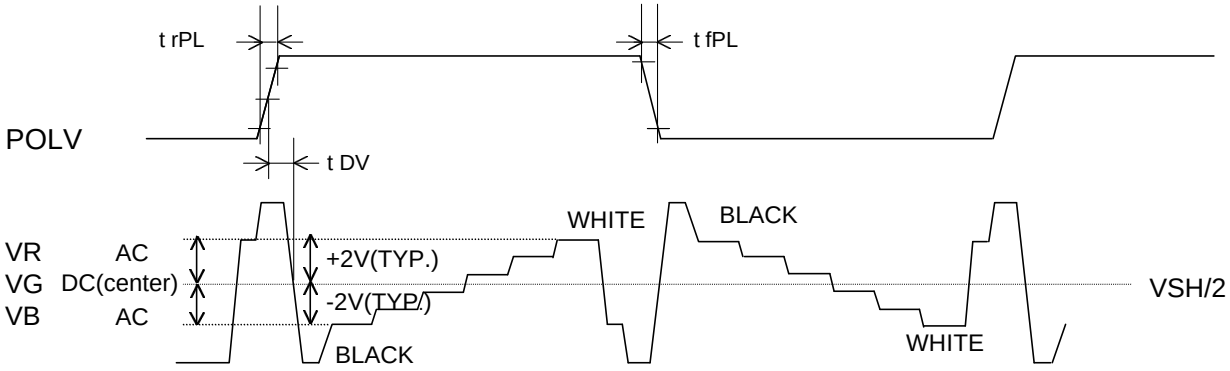


Fig-A

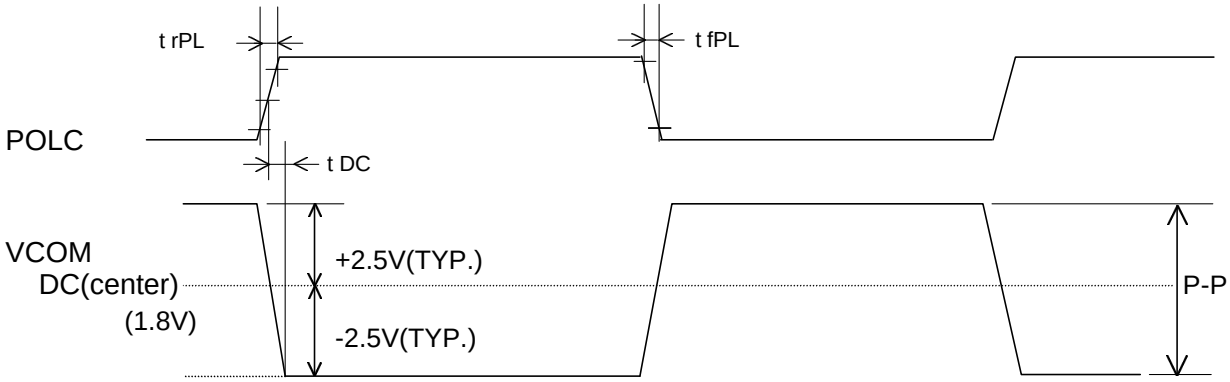


Fig-B

<BUILT-IN CLK MODE>(SWC=Hi NTSC/PAL)

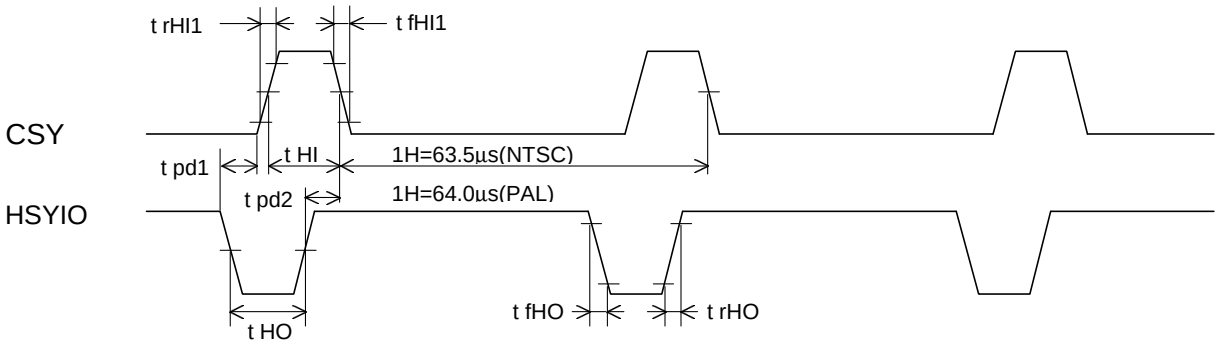


Fig-C

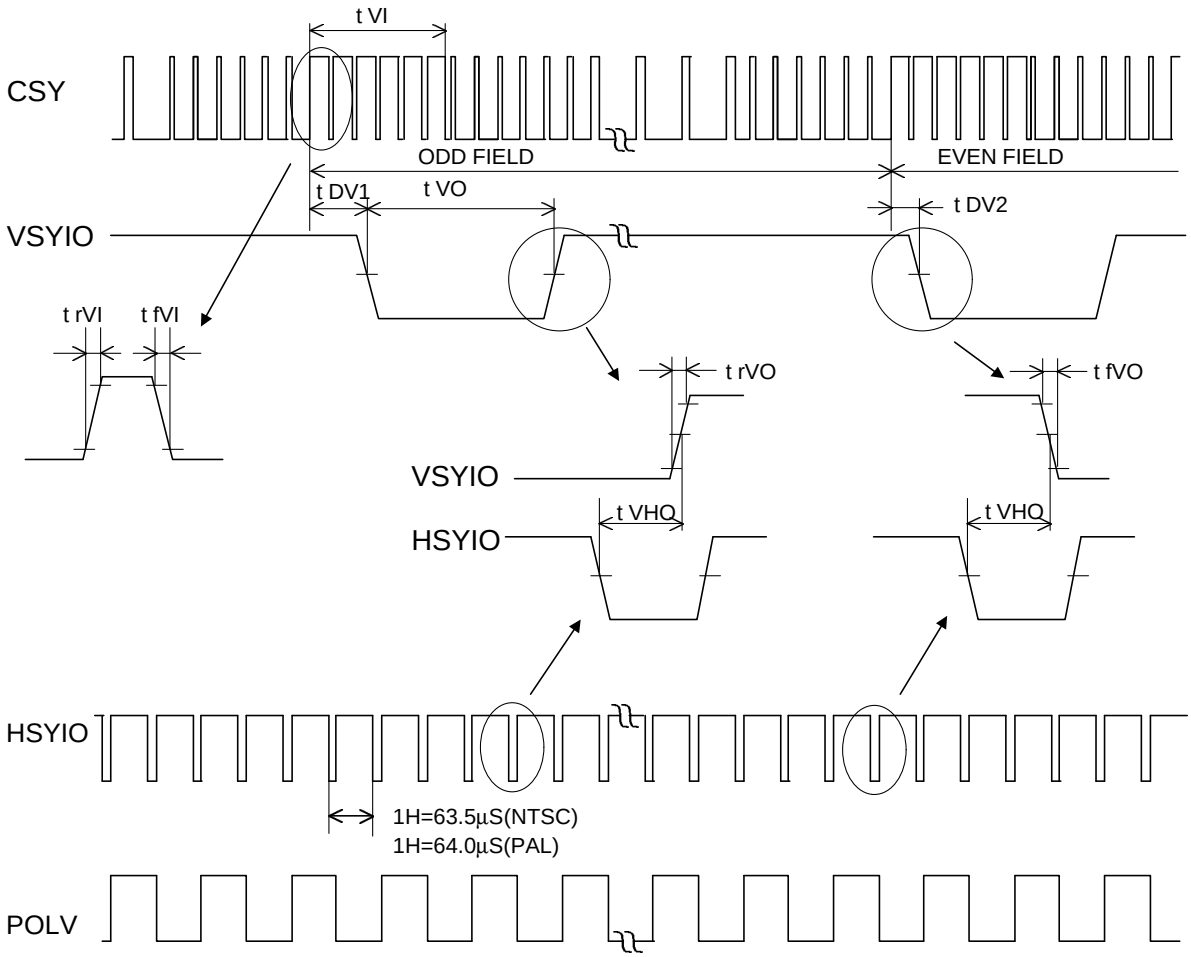


Fig-D

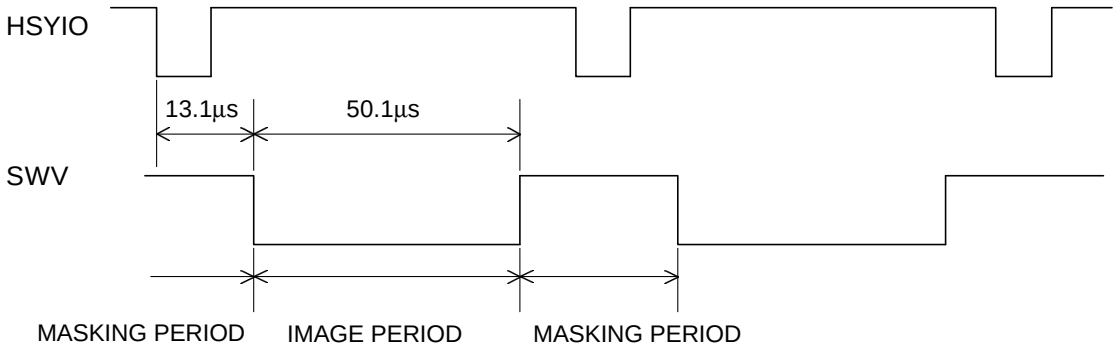


Fig-E (NORMAL MODE DM1=Hi, DM2=Low, DM3=Hi)

<EXTERNAL CLK MODE>(SWC=Low)

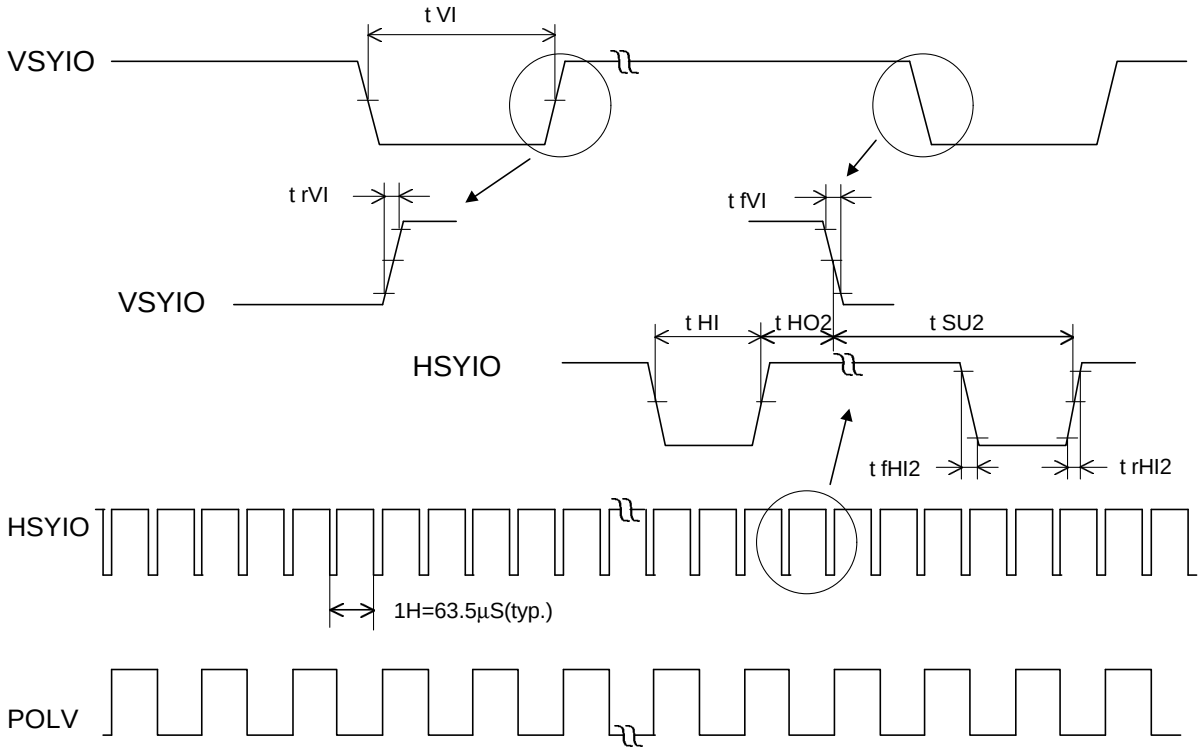


Fig-F (N/P=Hi)

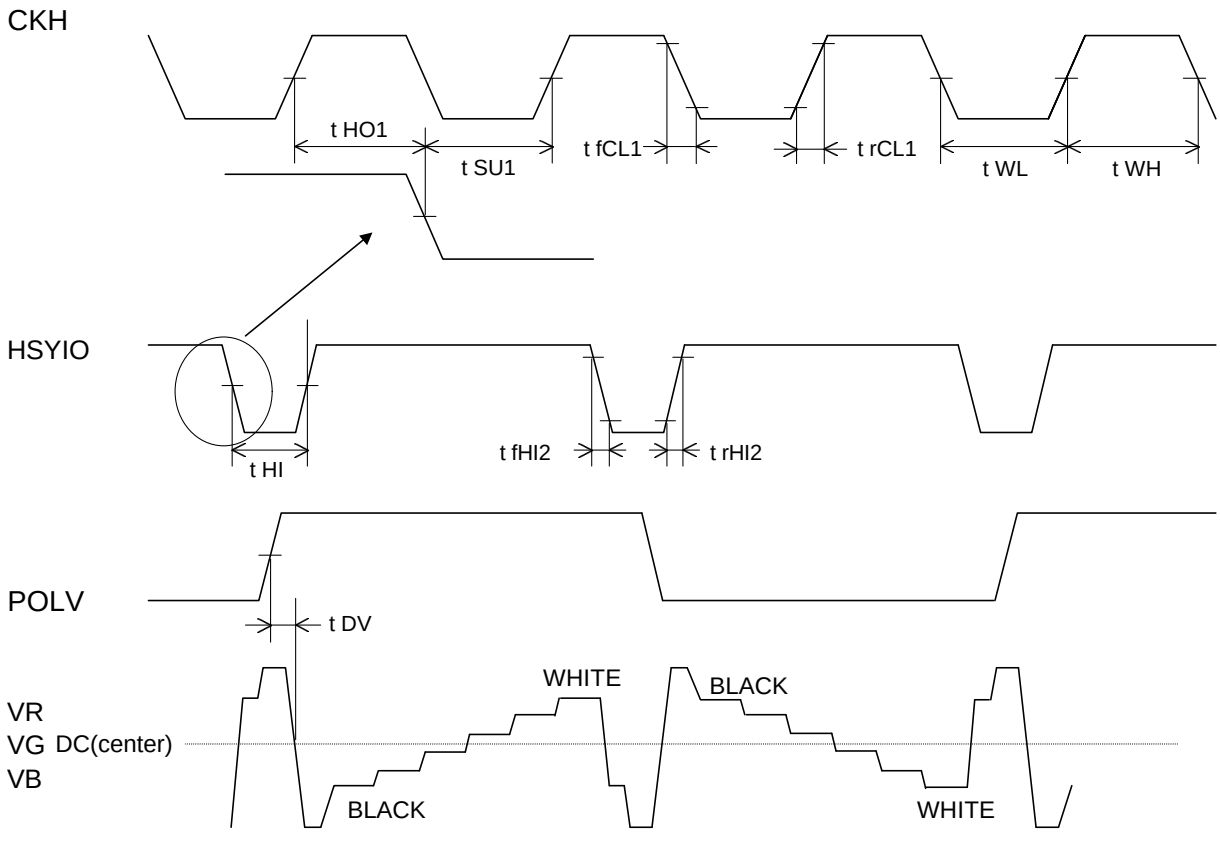


Fig-G(N/P=Hi, DM1=DM2=DM3=Hi)

■ ***PWM DIMMING TIMING***

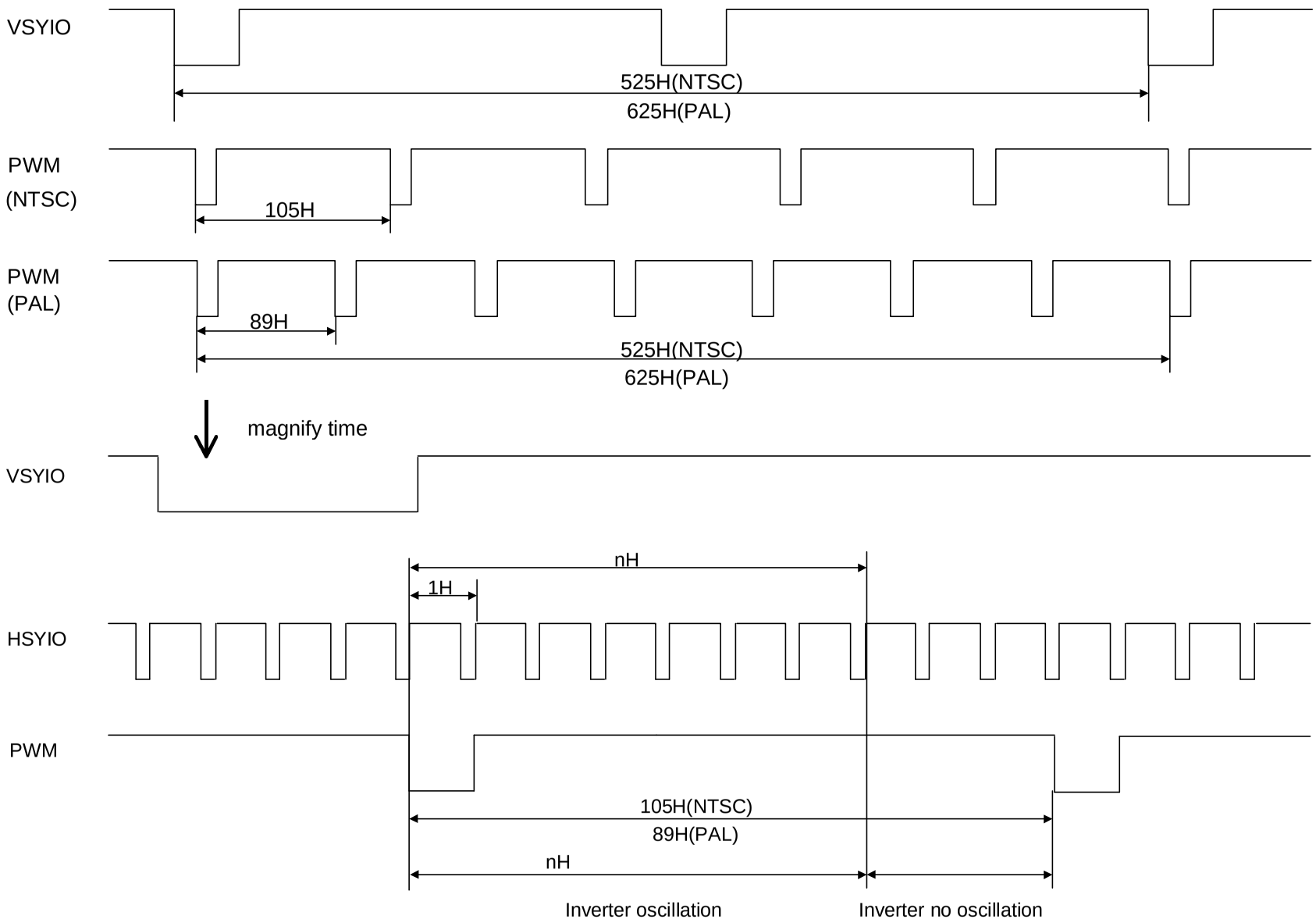
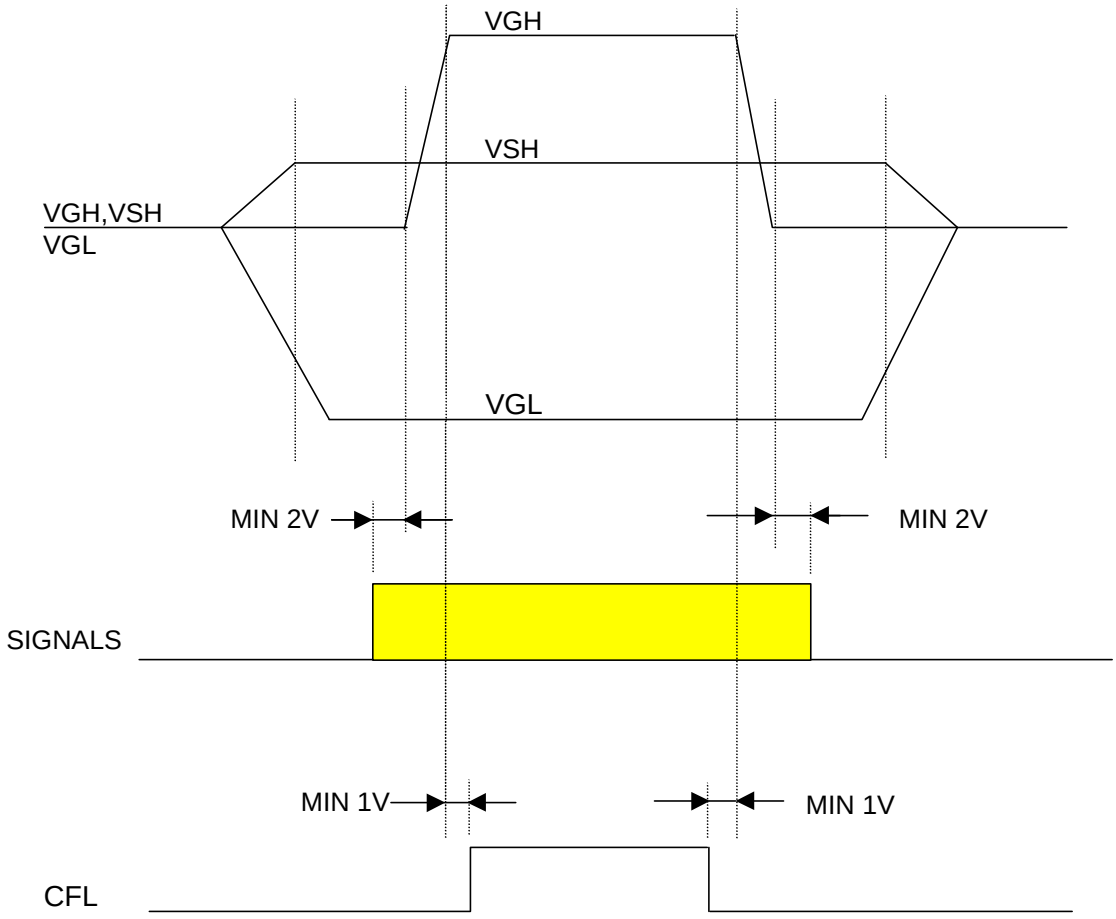


Fig-H

■ *POWER ON/OFF SEQUENCE REQUIREMENT*



* (V=1 FIELD time)

■ *PRECAUTIONS*

Caution for designing

1. This technical spec just explains general specification of the LCD module.
   Please request us customer specification before you start designing.

2. Please apply waterproof design to avoid any moisture or saline matter
   into LCD module.

3. Long CFL wiring may result in increase of leak current.
   Please carefully design the wiring in order to minimize leak current,
   which causes reduction of inverter start-up voltage.

4. Please implement enough shielding for LCD's excess nose radiation
   not to interfere other peripheral device by.

Caution for LCD handling

1. Disassembling or remodeling of LCD module is prohibited.

2. Please do not touch volume control no the backside of module.
   In the case you change it, LCD module may not achieve proper
   performance mentioned in the spec.

3. LCD shall be stored in same packing material during import,
   and under the condition of room temperature (10-30 degree C).
   Please do not leave LCD modules under the direct sunlight or
   strong infra-red radiation for a long period time to prevent liquid

4. LCD module integrates semi-conductor components.
Please handle it with static electricity protection.

5. Please turn off the power supply before plugging or unplugging LCD module.

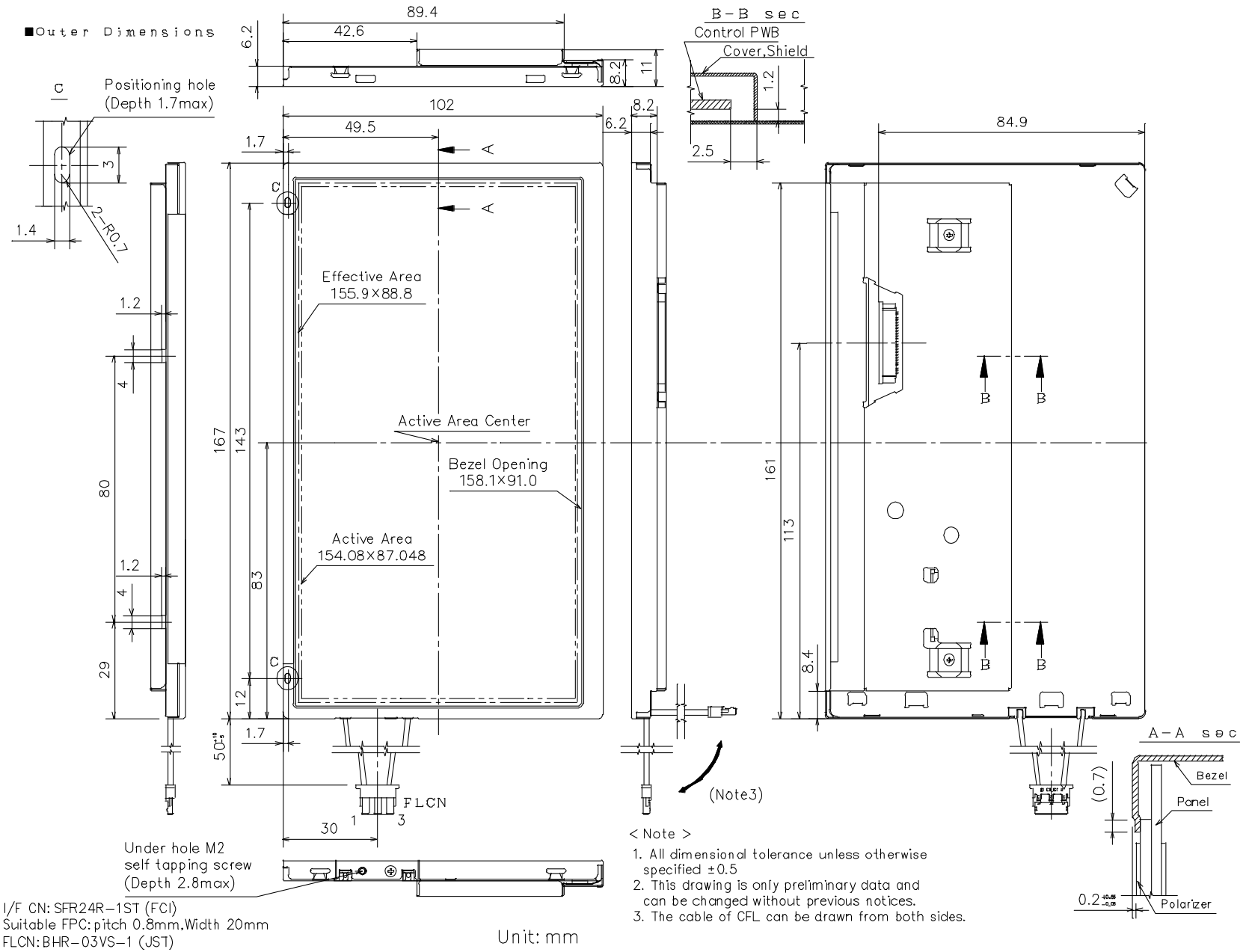
6. Since high voltage is supplied to CFL when it's driving,
please make careful treatment and design around CFL portion.
And please be sure that CFL connector does not have a loose connection
to prevent large risk of fire due to high voltage.

7. Please do not rub, push, or hit LCD surface with hard tool etc.
Film on surface is easily scratched.
When droplets of water or dirt are on the surface,
please gently remove them with soft fabric.

8. Glass in LCD module is easily damaged or broken when it is dropped,
strongly pinched or hit.
Please be careful not to cut your hand if you break the glass.

9. In case that liquid crystal fluid runs off from broken panel,
please do not swallow or handle the fluid for any reason.
If liquid crystal accretes hands or clothes, please remove it with
or alcohol and wash them. By any chance, liquid crystal ge.

10.Cold Cathode Lamp contains small amount of mercury.
Please follow local ordinances or regulation for disposal.



I/F CN: SFR24R-1ST (FCI)
Suitable FPC: pitch 0.8mm,Width 20mm
FLCN: BHR-03VS-1 (JST)

Unit: mm

< Note >

1. All dimensional tolerance unless otherwise specified ±0.5
2. This drawing is only preliminary data and can be changed without previous notices.
3. The cable of CFL can be drawn from both sides.