iT2009

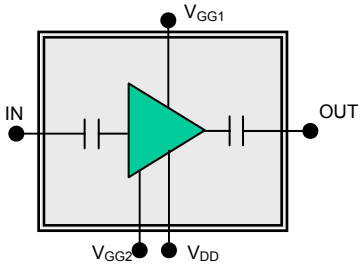
2 – 26.5 GHz High-Gain, High-Power Amplifier

Description

The iT2009 is a broadband GaAs MMIC traveling wave amplifier designed for high output power applications where high gain performance is also required. The iT2009 provides saturated output power of 1 W up to 7 GHz and greater than 29 dBm up to 15 GHz. High gain of 20 dB with flatness of +/-1 dB is provided up to 26.5 GHz. DC power consumption as low as 5.4 W is obtained by biasing for best output power and good linear performance. Input-output DC block capacitors are integrated on-chip.

Features

- Frequency range: 2 GHz – 26.5 GHz
- Psat (2 GHz – 7 GHz): 30 dBm
- Psat (7 GHz – 15 GHz): 29 dBm
- Psat (15 GHz – 26.5 GHz): 25 dBm
- Gain with +/-1dB flatness: 20 dB
- DC power consumption: 5.4 W
- DC bias conditions: 9 V at 600 mA
- Full chip passivation for high reliability



Absolute Ratings

Symbol	Parameters/conditions	Min.	Max.	Units
V_{DD}	Positive supply voltage		11	V
$V_{GG1,2}$	Negative supply voltage	-2	0	V
I_{DQ}	DC positive supply current		1300	mA
$I_{GG1,2}$	Negative supply current		1.6	mA
Pin	RF input power		17	dBm
Pdiss_DC	DC power dissipation (no RF)		10	W
Tch	Operating channel temperature		150	°C
Tm	Mounting temperature (30 s)		320	°C
Tst	Storage temperature	-65	150	°C

Recommended Operating Conditions

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
Tb	Operating temperature range (back side)	-40		85	°C
V_{DD}	Positive bias spply			9	V
V_{GG1}	Negative bias spply	-0.4	-0.6	-0.9	V
V_{GG2}	Negative bias supply	-0.4	-0.6	-0.9	V
I_{DQ}	DC supply drain current		600	750	mA

Electrical Characteristics

(at 25 °C)
50 ohm system
V_{DD} = +9 V
Quiescent current
I_{DQ} = 600 mA

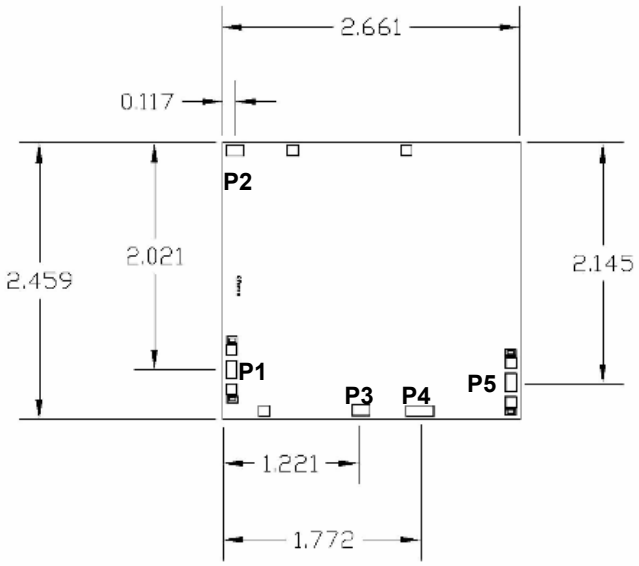
Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
BW	Frequency range	2		26.5	GHz
S21	Small signal ain	17	20		dB
	Gain flatness			+/-1	dB
S11	Input return loss	12	16		dB
S22	Output return loss	9	12		dB
S12	Isolation	50			dB
Psat	Saturated output power (3 dB gain comp.)				
	2 - 10 GHz	27.5	29.5		dBm
	2 - 20 GHz	26.5	28.5		dBm
	2 - 26.5 GHz	24	25		dBm
P_{1dB}	Output power at 1 dB gain compression point				
	2 - 10 GHz	27	29		dBm
	2 - 20 GHz	26	28		dBm
	2 - 26.5 GHz	22.5	24.5		dBm

Thermal Characteristics

Symbol	Parameters/conditions	Rth_jb (°C/W)	Tch (°C)	MTFF (h)
Rth_jb	Thermal resistance junction-backside of die NO RF: DC bias V_{DD}=9 V, I_{DD}=600 mA , P_{DC}=5.4 W Tbase=70 C	5	97.0	>> +1E7
Rth_jb	Thermal resistance junction-backside of die RF applied: Saturated power 1 W, V_{DD}=9 V, Pdiss=7 W Tbase=70 C	5	105.0	>> +1E7

Chip Layout and Bond Pad Locations

(Back of chip is RF and DC ground)



Pinout and Pad Dimensions:

P1: RF input (100 x 150 mm^2)

P2: VGG1, negative voltage (150 x 100 mm^2)

P3: VGG2, negative voltage (150 x100 mm^2)

P4: VDD positive voltage (250 x 100 mm^2)

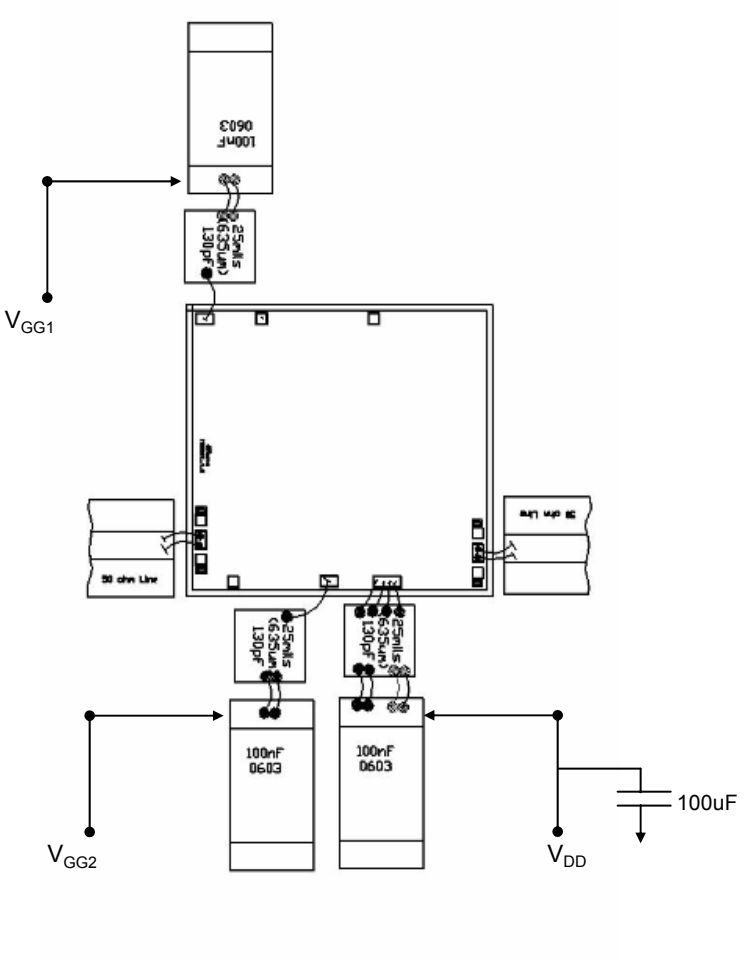
P5: RF output (100 x150 mm^2)

Note: All dimensions are in millimeters

Chip size tolerance: ± 20 µm
Chip thickness: 4 mil with a tolerance of ± 0.4 mil.

Recommended Assembly Diagram

Bypass capacitor must be large enough to isolate bias supply (=>10 μF)

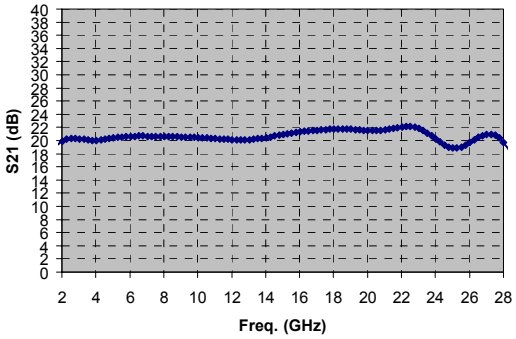


Performance Data

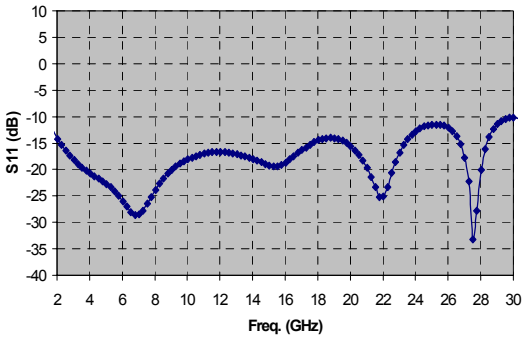
T = 25° C

Measured data includes effect of two parallel RF input/output bond wires

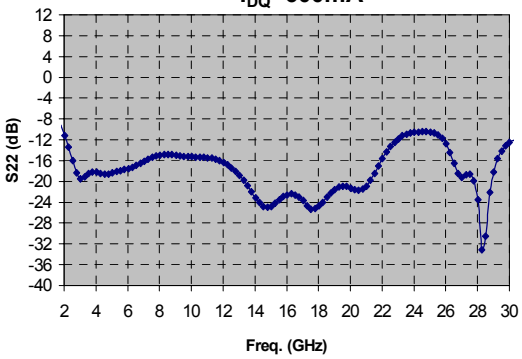
Small Signal Gain, V_{DD}=9V, I_{DQ}=600mA



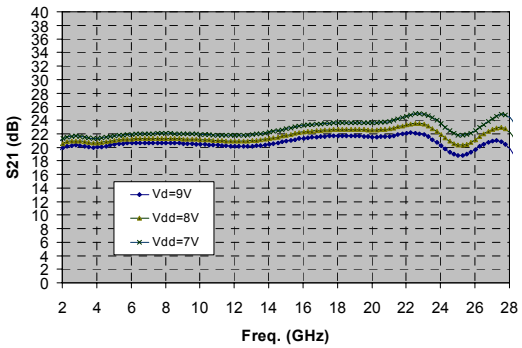
Input Return loss, V_{DD}=9V, I_{DQ}=600mA



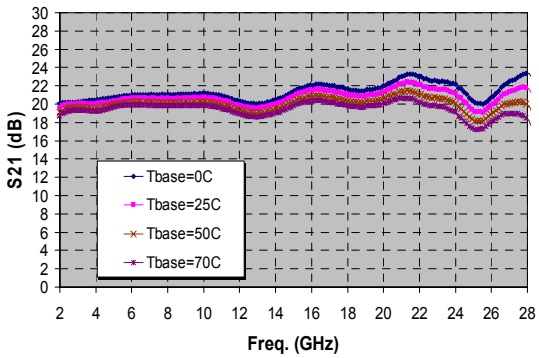
Output Return loss, V_{DD}=9V, I_{DQ}=600mA



Gain vs. Drain Bias V_{DD}, I_{DQ}=600mA



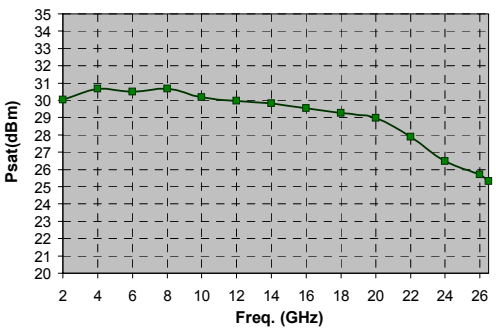
Gain vs. Temperature, V_{DD} =9V



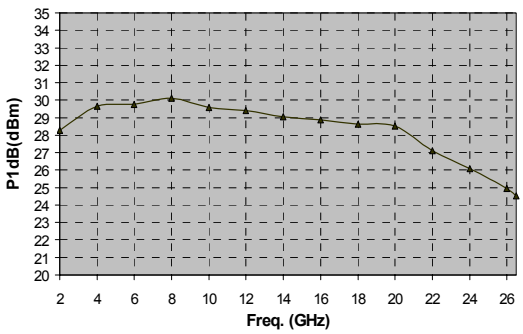
Performance Data

T = 25° C

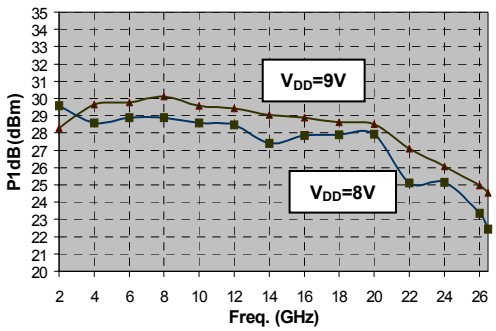
Saturated Power, V_{DD}=9V, I_{DQ}=600mA



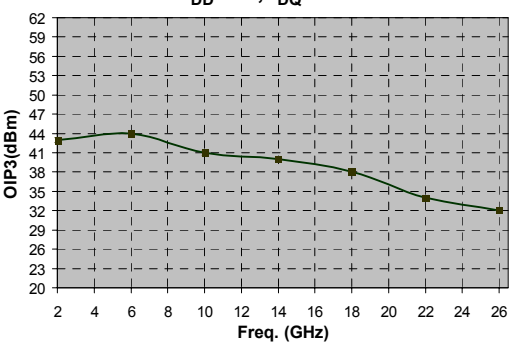
P_{1dB}, V_{DD}=9V, I_{DQ}=600mA



P1dB vs. V_{DD}, I_{DQ}=600mA



Output Third Order Intercept Point
V_{DD}=9V, I_{DQ}=600mA



* Measured data includes effect of two parallel RF input/output bond wires

Recommended Procedure for Biasing and Operation

CAUTION: LOSS OF GATE VOLTAGE ($V_{GG1,2}$) WHILE CORRESPONDING DRAIN VOLTAGE (Vdd) IS PRESENT CAN DAMAGE THE AMPLIFIER.

The following procedure must be considered to properly test the amplifier.

The iT2009 amplifier is biased with a positive drain supply (V_{DD}) and two negative gate supply (V_{GG1} and V_{GG2}). The recommended bias conditions for the iT2009 is V_{DD}= 9.0V, I_{DQ} = 600mA. To achieve this drain current level, V_{GG1} and V_{GG2} are typically biased between –0.6V and –0.9V. The gate voltages (V_{GG1} and V_{GG2}) MUST be applied prior to the drain voltage (V_{DD}) during power up and removed after the drain voltage is removed during the power down.

Bias Procedure

1. Apply –1.1 V to V_{GG1}
2. Apply –1.1V to V_{GG2}
3. Apply +9 V to V_{DD}
4. Adjust V_{GG1} and V_{GG2} to attain I_{DQ} = 600 mA total current (V_{GG1} = V_{GG2}, typically biased between –0.6 V and –0.9 V)

Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325° C for 15 min.

Die attachment for power devices should utilize gold/tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist-grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3 mil wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 12 mil long corresponding to a typical 2 mil gap between the chip and the substrate material.