


OptiMOS^(TM)3 Power-Transistor
Features

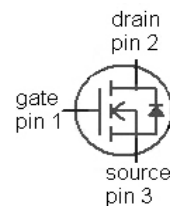
- Ideal for high frequency switching and sync. rec.
- Optimized technology for DC/DC converters
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC¹⁾ for target applications

Product Summary

V_{DS}	80	V
$R_{DS(on),max}$	10	m Ω
I_D	40	A



Type	IPA100N08N3 G
	
Package	PG-TO220-FP
Marking	100N08N


Maximum ratings, at $T_j=25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ }^\circ\text{C}^{2)}$	40	A
		$T_C=100\text{ }^\circ\text{C}$	30	
Pulsed drain current ³⁾	$I_{D,pulse}$	$T_C=25\text{ }^\circ\text{C}$	160	
Avalanche energy, single pulse ⁴⁾	E_{AS}	$I_D=40\text{ A}, R_{GS}=25\text{ }\Omega$	110	mJ
Gate source voltage	V_{GS}		± 20	V
Power dissipation	P_{tot}	$T_C=25\text{ }^\circ\text{C}$	35	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	$^\circ\text{C}$
IEC climatic category; DIN IEC 68-1			55/175/56	

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¹⁾J-STD20 and JESD22

²⁾ Current is limited by package; with an $R_{thJC}=1.5\text{ K/W}$ in a standard TO-220 package the chip is able to carry 72A.

³⁾ See figure 3 for more detailed information

⁴⁾ See figure 13 for more detailed information

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}		-	-	4.3	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ⁵⁾	-	-	40	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	80	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=46\text{ }\mu\text{A}$	2	2.8	3.5	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=80\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.1	1	μA
		$V_{DS}=80\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=40\text{ A}$	-	8.4	10	m Ω
		$V_{GS}=6\text{ V}, I_D=20\text{ A}$	-	10.9	18.2	
Gate resistance	R_G		-	1.6	-	Ω
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=40\text{ A}$	28	55	-	S

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=40\text{ V},$ $f=1\text{ MHz}$	-	1810	2410	pF
Output capacitance	C_{oss}		-	490	652	
Reverse transfer capacitance	C_{rss}		-	20	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=40\text{ V}, V_{GS}=10\text{ V},$ $I_D=40\text{ A}, R_G=1.6\ \Omega$	-	13	-	ns
Rise time	t_r		-	30	-	
Turn-off delay time	$t_{d(off)}$		-	23	-	
Fall time	t_f		-	5	-	

Gate Charge Characteristics⁶⁾

Gate to source charge	Q_{gs}	$V_{DD}=40\text{ V}, I_D=40\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	9	-	nC
Gate to drain charge	Q_{gd}		-	5	-	
Switching charge	Q_{sw}		-	10	-	
Gate charge total	Q_g		-	26	35	
Gate plateau voltage	$V_{plateau}$		-	5.1	-	V
Output charge	Q_{oss}	$V_{DD}=40\text{ V}, V_{GS}=0\text{ V}$	-	35	47	nC

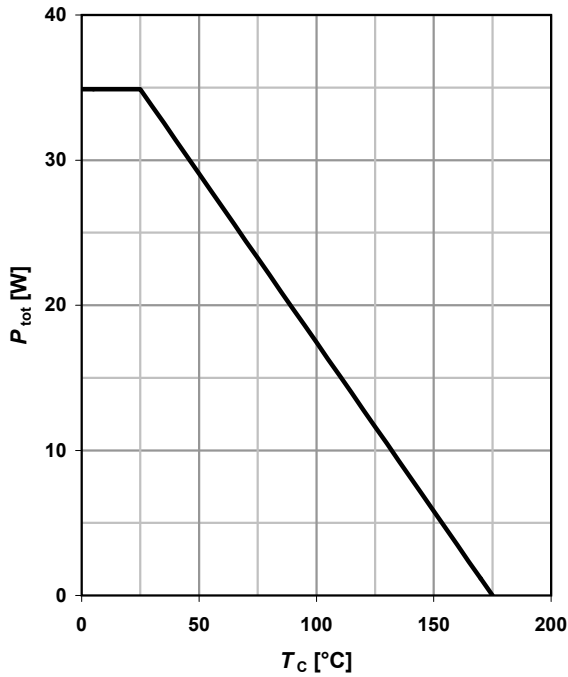
Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	40	A
Diode pulse current	$I_{S,pulse}$		-	-	160	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=40\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	1.0	1.2	V
Reverse recovery time	t_{rr}	$V_R=40\text{ V}, I_F=40\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	57	-	ns
Reverse recovery charge	Q_{rr}		-	91	-	nC

⁶⁾ See figure 16 for gate charge parameter definition

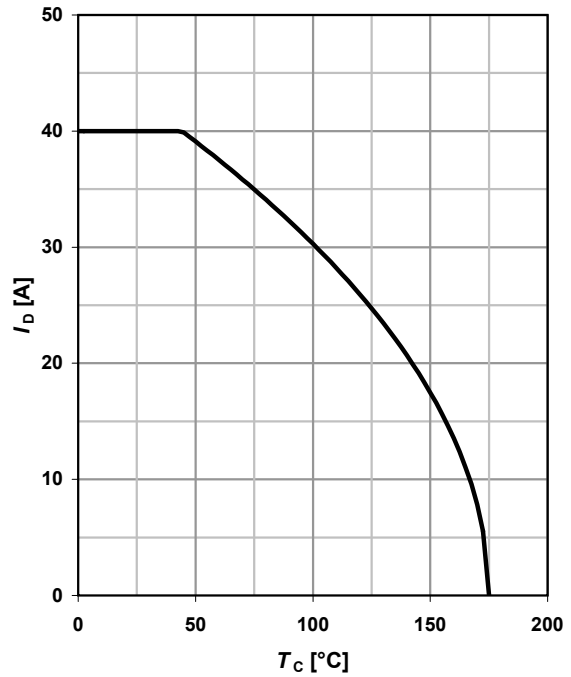
1 Power dissipation

$$P_{tot} = f(T_C)$$



2 Drain current

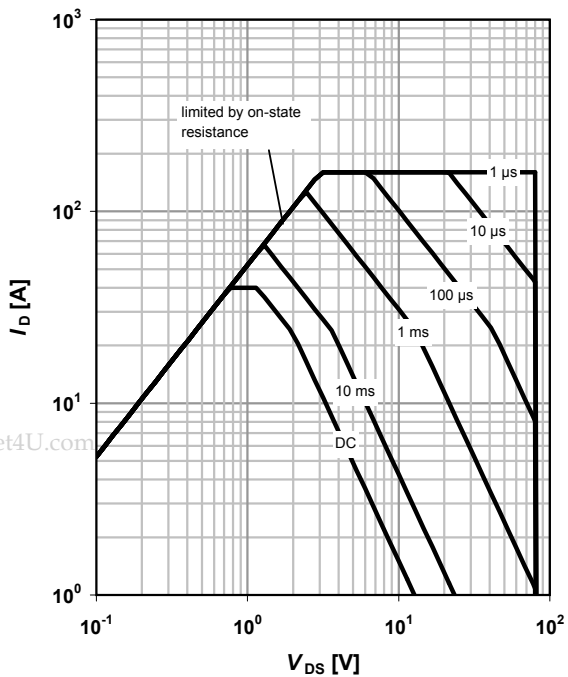
$$I_D = f(T_C); V_{GS} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{DS}); T_C = 25 \text{ °C}; D = 0$$

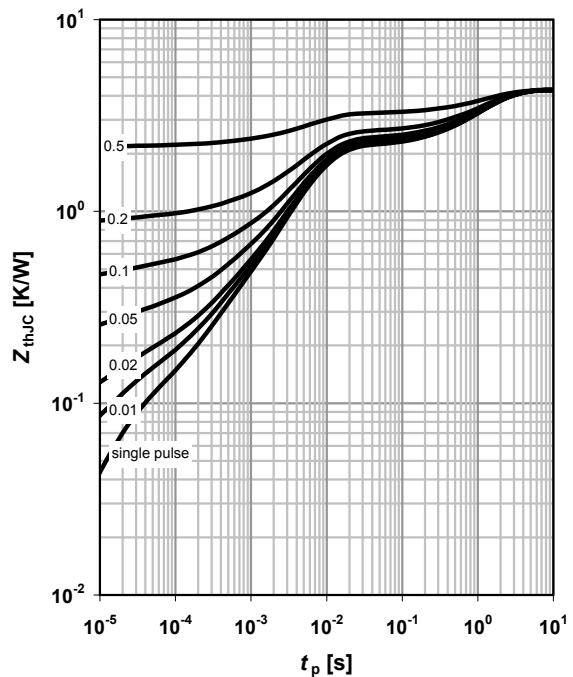
parameter: t_p



4 Max. transient thermal impedance

$$Z_{thJC} = f(t_p)$$

parameter: $D = t_p / T$

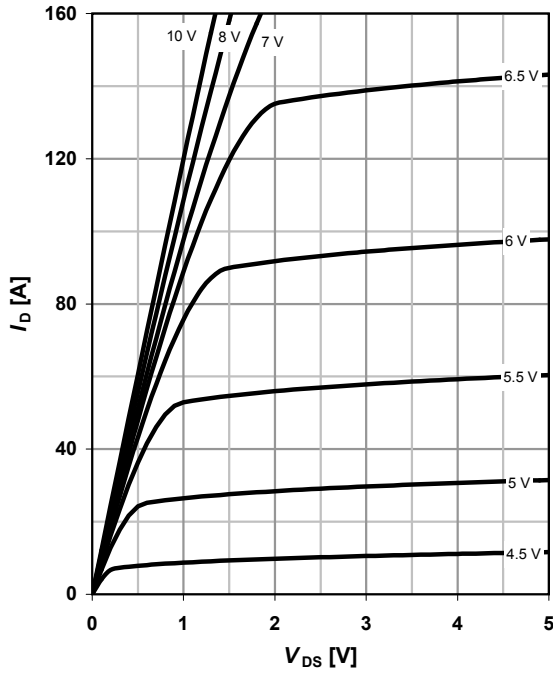


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5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

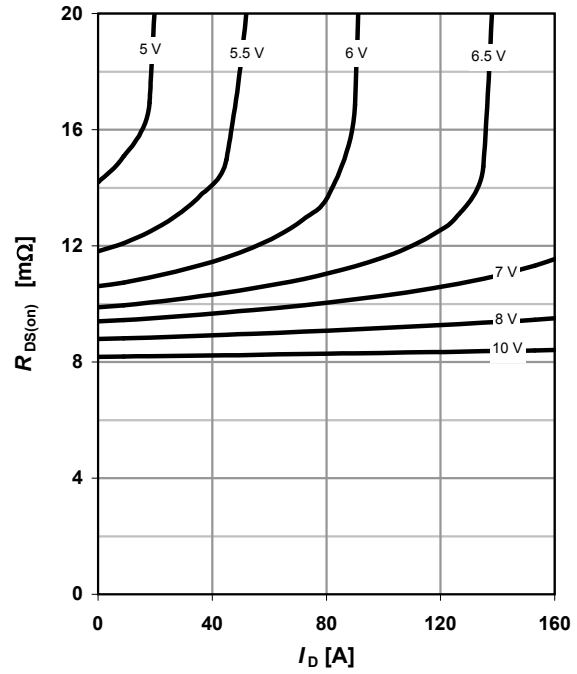
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

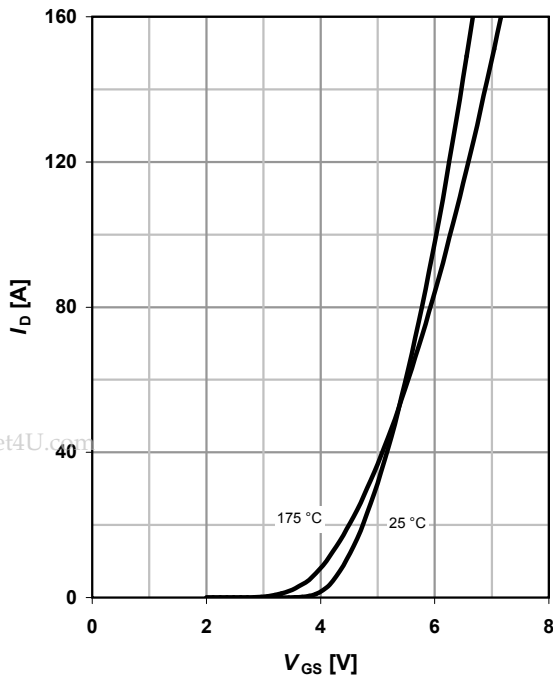
parameter: V_{GS}



7 Typ. transfer characteristics

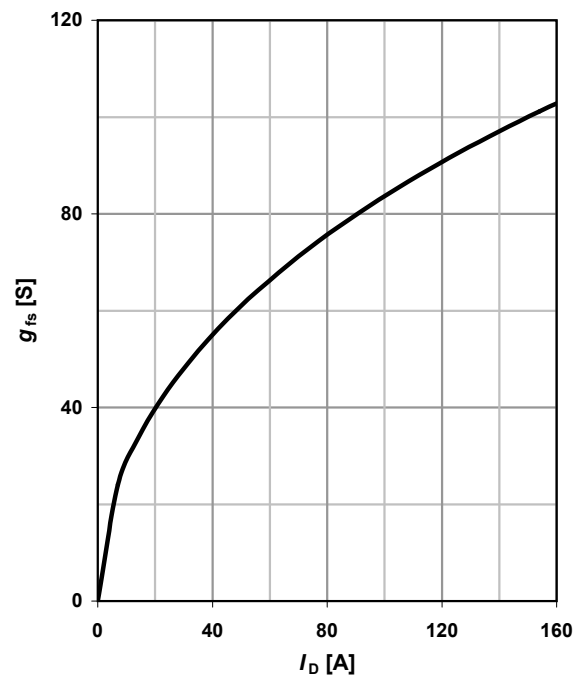
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter: T_j



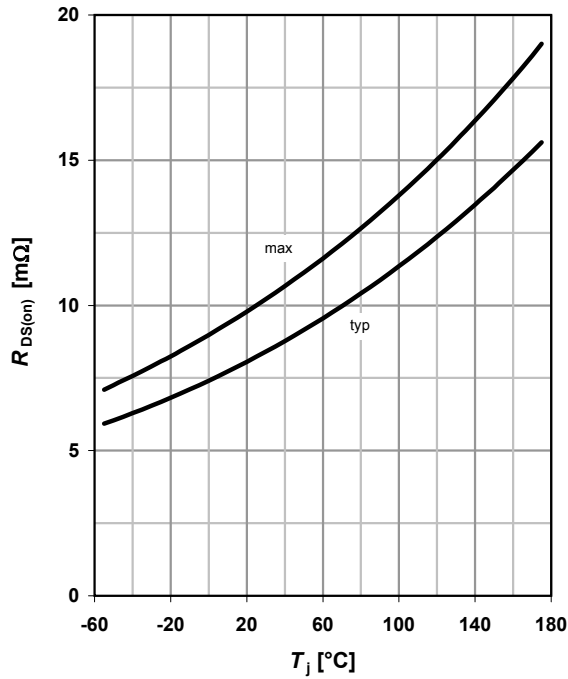
8 Typ. forward transconductance

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$



9 Drain-source on-state resistance

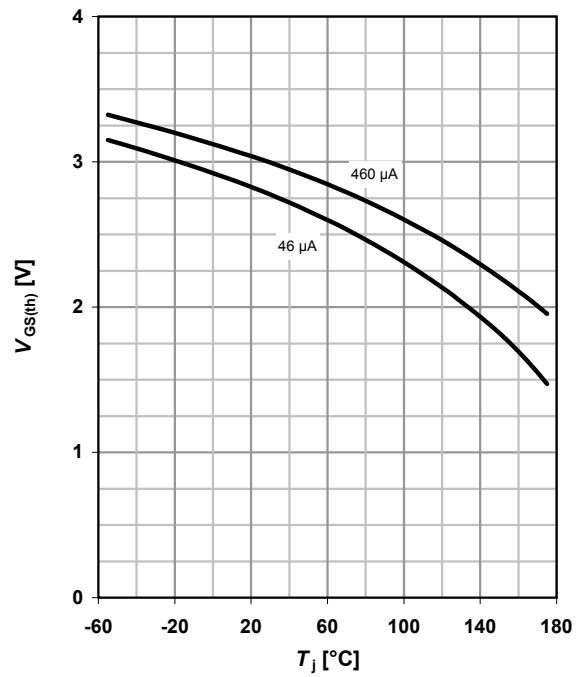
$R_{DS(on)} = f(T_j); I_D = 40 \text{ A}; V_{GS} = 10 \text{ V}$



10 Typ. gate threshold voltage

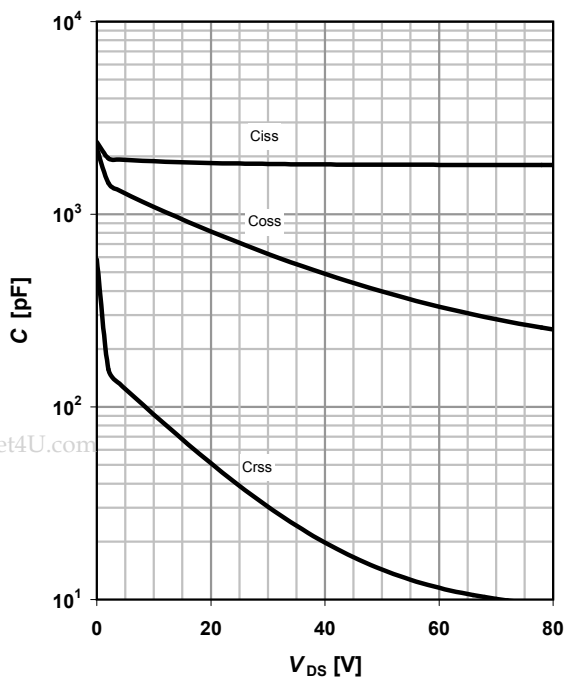
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



11 Typ. capacitances

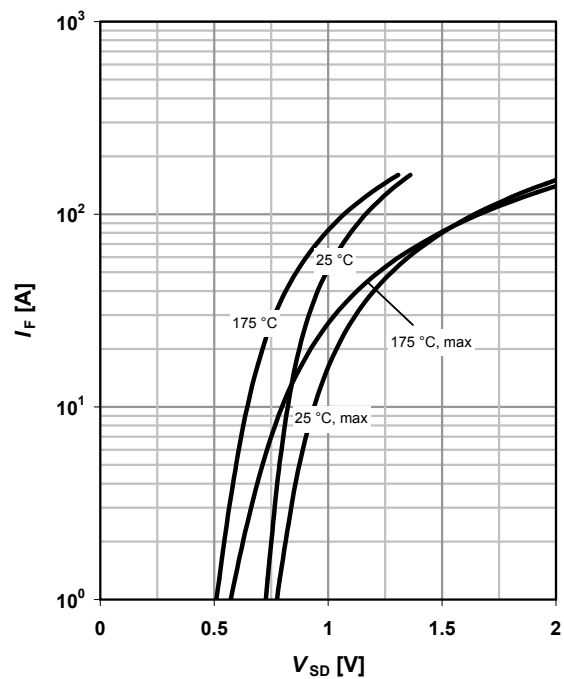
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



12 Forward characteristics of reverse diode

$I_F = f(V_{SD})$

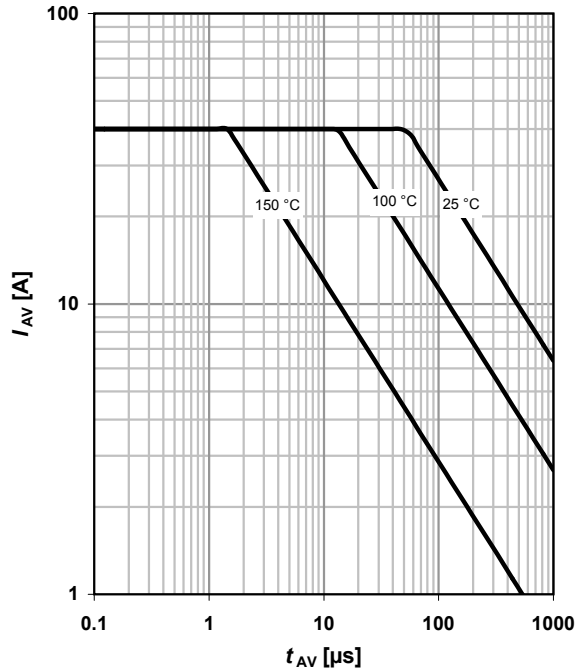
parameter: T_j



13 Avalanche characteristics

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

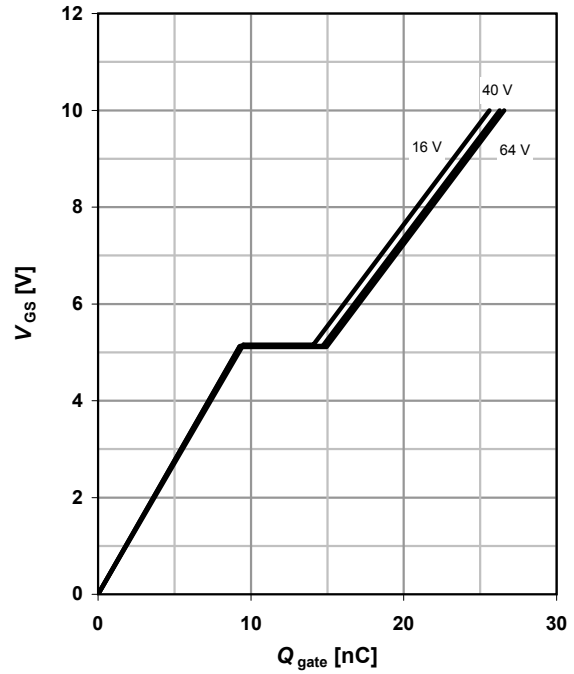
parameter: $T_{j(start)}$



14 Typ. gate charge

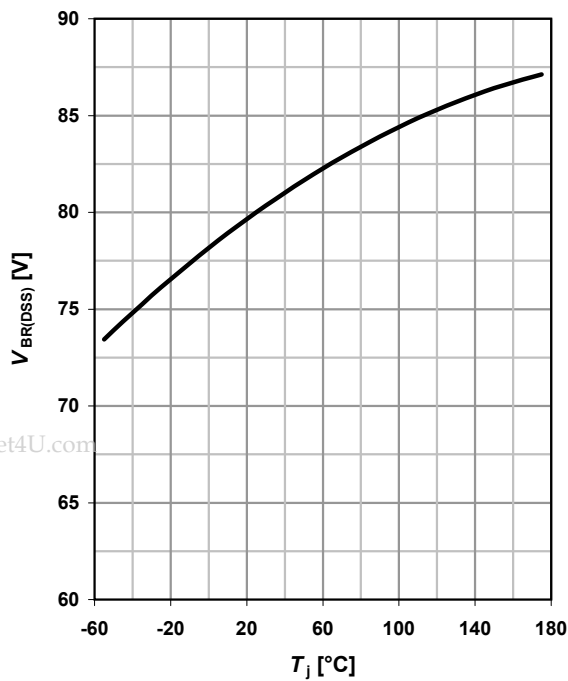
$V_{GS}=f(Q_{gate}); I_D=40 \text{ A pulsed}$

parameter: V_{DD}



15 Drain-source breakdown voltage

$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

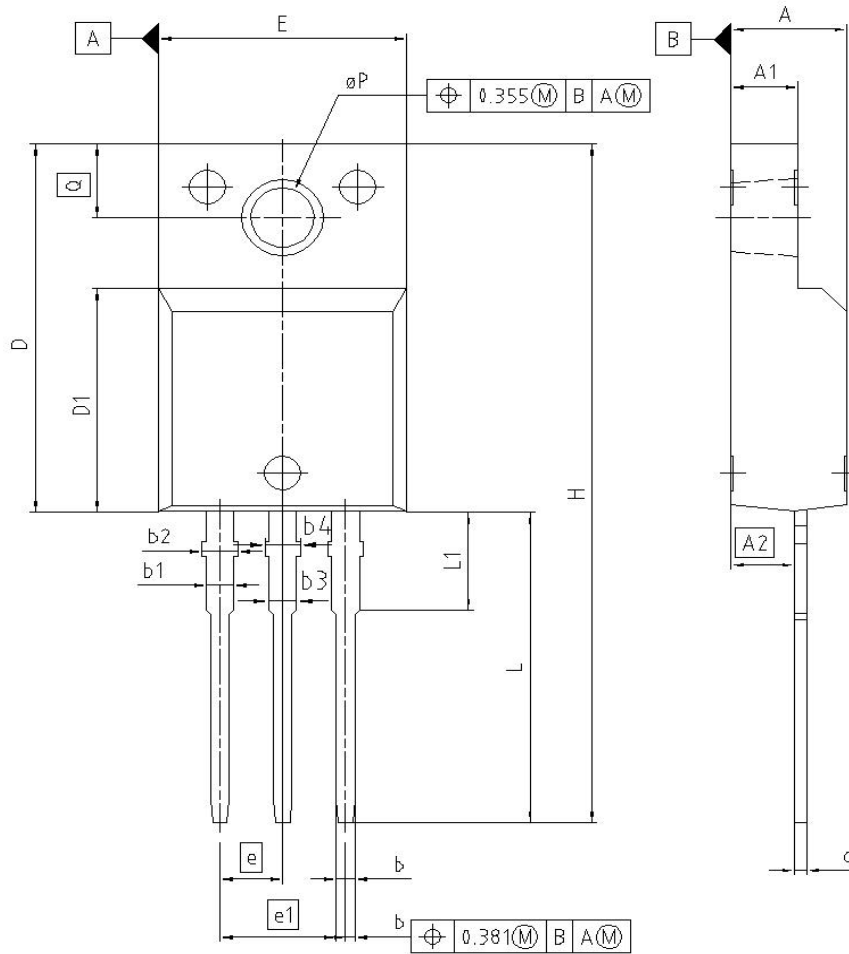


16 Gate charge waveforms

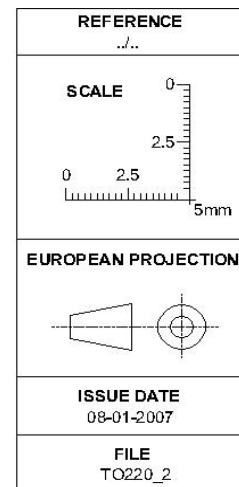


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PG-TO220-3-FP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.55	4.85	0.179	0.191
A1	2.55	2.85	0.100	0.112
A2	2.42	2.72	0.095	0.107
b	0.65	0.85	0.026	0.033
b1	0.95	1.33	0.037	0.052
b2	0.95	1.51	0.037	0.059
b3	0.65	1.33	0.026	0.052
b4	0.65	1.51	0.026	0.059
c	0.40	0.63	0.016	0.025
D	15.85	16.15	0.624	0.636
D1	9.53	9.83	0.375	0.387
E	10.35	10.65	0.407	0.419
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H	29.45	29.75	1.159	1.171
L	13.45	13.75	0.530	0.541
L1	3.15	3.45	0.124	0.136
pP	2.95	3.20	0.116	0.126
Q	3.15	3.50	0.124	0.138



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Infineon Technologies AG
81726 Munich, Germany
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