

HN27C4096H Series

Preliminary

4M (256K x 16-bit) UV EPROM

T-46-13-29

■ DESCRIPTION

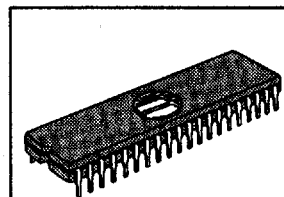
The Hitachi HN27C4096H is a 4-Megabit Ultraviolet Erasable and Electrically Programmable Read Only Memory organized as 262,144 x 16-bits.

The HN27C4096H features high speed access times of 70 and 85 ns and low power dissipation. This combination makes the HN27C4096H suitable for high speed 16 and 32-bit microcomputer systems. The HN27C4096H offers high speed programming using page programming mode.

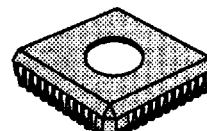
Hitachi's HN27C4096H is offered in JEDEC-Standard Word-Wide EPROM pinouts in 40-pin Ceramic DIP and 44-lead Ceramic LCC packages. This allows socket replacement with Mask ROMs.

■ FEATURES

- High Speed Access Times:
 - 70 ns/85 ns (max)
- Single Power Supply:
 - $V_{CC} = 5 V \pm 10\%$
- Low Power Dissipation:
 - Active Mode: 35 mW/MHz (typ)
 - Standby Mode: 30 mA (max)
- High Speed Page and Word Programming:
 - Page Programming Time: 3.5 sec (min)
- Programming Power Supply:
 - $V_{PP} = 12.5 V \pm 0.3 V$
- Pin Arrangement:
 - JEDEC Standard Word-Wide EPROM
 - Mask ROM Compatible
- Packages:
 - 40-pin Ceramic DIP
 - 44-lead Ceramic LCC



(DG-40A)



(CC-44)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN27C4096HG-70	70 ns	40-pin Ceramic DIP
HN27C4096HG-85	85 ns	(DG-40A)
HN27C4096HCC-70	70 ns	44-lead Ceramic LCC
HN27C4096HCC-85	85 ns	(CC-44)

HITACHI

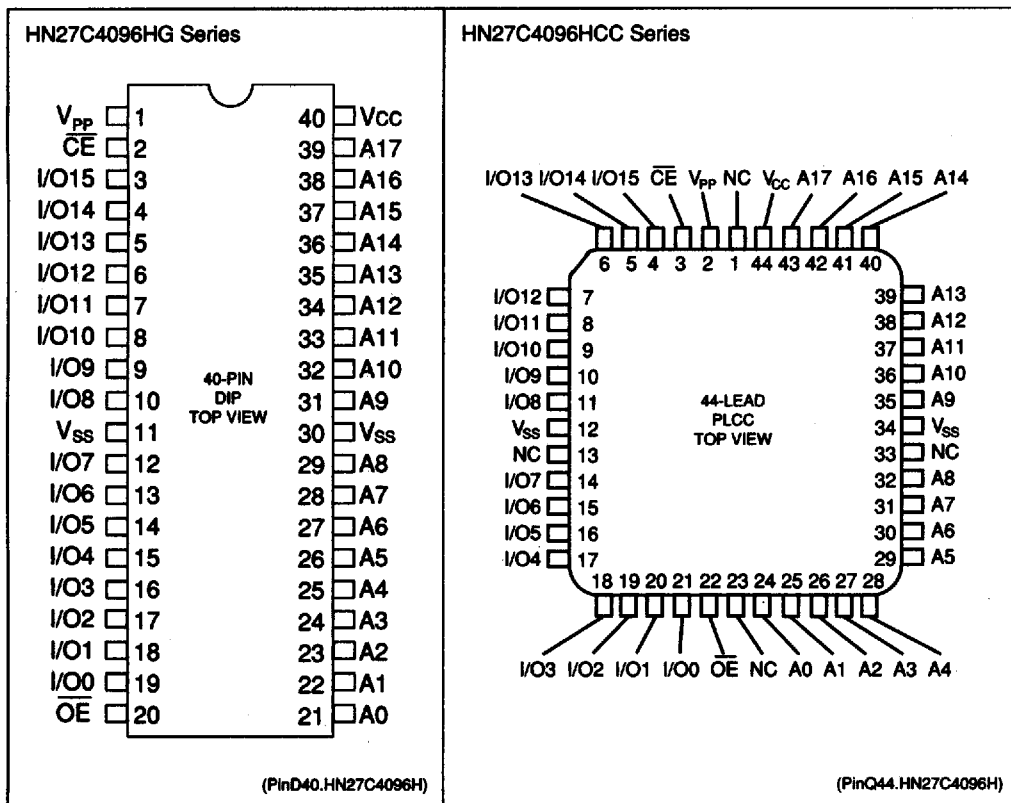
Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

4-77

HN27C4096H Series

T-46-13-29

■ PIN ARRANGEMENT



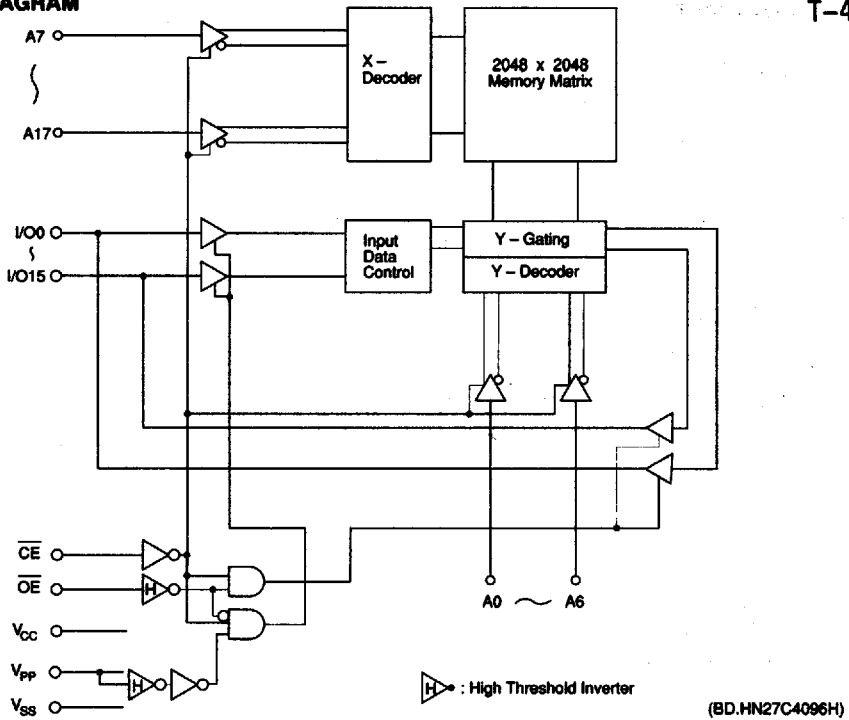
■ PIN DESCRIPTION

Pin Name	Function
A ₀ - A ₁₇	Address
I/O ₀ - I/O ₁₅	Input/Output
CE	Chip Enable
OE	Output Enable
V _{CC}	Power Supply
V _{PP}	Programming Supply
V _{SS}	Ground
NC	No Connection

HITACHI

T-46-13-29

■ **BLOCK DIAGRAM**



■ **MODE SELECTION**

Mode	V_{PP}	V_{CC}	\overline{CE}	\overline{OE}	A_9	I/O	
Read	$V_{SS}-V_{CC}$	V_{CC}	V_{IL}	V_{IL}	X ¹	D_{OUT}	
Output Disable	$V_{SS}-V_{CC}$	V_{CC}	V_{IL}	V_{IH}	X	High-Z	
Standby	$V_{SS}-V_{CC}$	V_{CC}	V_{IH}	X	X	High-Z	
Page Prog.	Page Prog. Set	V_{PP}	V_{CC}	V_{IH}	V_H^2	X	High-Z
	Page Data Latch	V_{PP}	V_{CC}	V_{IL}	V_H	X	D_{IN}
	Page Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	X	High-Z
	Page Prog. Verify	V_{PP}	V_{CC}	V_{IH}	V_{IL}	X	D_{OUT}
	Page Prog. Reset	V_{CC}	V_{CC}	V_{IH}	V_{IH}	X	High-Z
Word Prog.	Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	X	D_{IN}
	Program Verify	V_{PP}	V_{CC}	V_{IH}	V_{IL}	X	D_{OUT}
	Optional Verify	V_{PP}	V_{CC}	V_{IL}	V_{IL}	X	D_{OUT}
	Program Inhibit	V_{PP}	V_{CC}	V_{IH}	V_{IH}	X	High-Z
Identifier	$V_{SS}-V_{CC}$	V_{CC}	V_{IL}	V_{IL}	V_H	ID	

- Notes: 1. X = Don't Care. $V_{PP} = 0V$ to V_{CC} .
 2. $11.5V \leq V_H \leq 12.5V$

HITACHI

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

4-79

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage ¹	V_{CC}	-0.6 to +7.0	V
Programming Voltage ¹	V_{PP}	-0.6 to +13.5	V
All Input and Output Voltage ^{1,2}	V_{IN}, V_{OUT}	-0.6 to +7.0	V
A_0 and OE Voltage ²	V_{ID}	-0.6 to +13.0	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range ³	T_{STG}	-65 to +125	°C
Storage Temperature Under Bias	T_{BIAS}	0 to +80	°C

- Notes: 1. Relative to V_{SS} .
 2. V_{IN} , V_{OUT} , and V_{ID} min = -2.0V for pulse width \leq 20 ns.
 3. Device storage temperature range before programming.

■ CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	12	pF	$V_{IN} = 0\text{V}$
Output Capacitance	C_{OUT}	-	-	20	pF	$V_{OUT} = 0\text{V}$

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

($V_{CC} = 5\text{V} \pm 10\%$, $V_{PP} = V_{SS}$ to V_{CC} , $T_a = 0$ to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LU}	-	-	2	μA	$V_{IN} = 5.5\text{V}$
Output Leakage Current	I_{LO}	-	-	2	μA	$V_{OUT} = 5.5\text{V}/0.45\text{V}$
Operating V_{CC} Current	I_{CC1}	-	-	30	mA	$I_{OUT} = 0\text{mA}$, $f = 1\text{MHz}$
	I_{CC2}	-	-	140	mA	$I_{OUT} = 0\text{mA}$, $f = 14.3\text{MHz}$
Standby V_{CC} Current	I_{SB}	-	-	30	mA	$\overline{CE} = V_{IH}$
V_{PP} Current	I_{PP1}	-	1	20	μA	$V_{PP} = 5.5\text{V}$
Input Voltage	V_{IH}	2.2	-	$V_{CC} + 1^2$	V	
	V_{IL}	-0.3 ¹	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	$I_{OH} = -400\mu\text{A}$
	V_{OL}	-	-	0.45	V	$I_{OL} = 2.1\text{mA}$

- Notes: 1. V_{IL} min = -1.0 V for pulse width \leq 50 ns.
 V_{IL} min = -2.0 V for pulse width \leq 20 ns.
 2. V_{IH} max = $V_{CC} + 1.5\text{V}$ for pulse width \leq 20 ns.
 If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.

HITACHI

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

T-46-13-29

 $(V_{CC} = 5V \pm 10\%, V_{PP} = V_{SS} \text{ to } V_{CC}, T_a = 0 \text{ to } 70^\circ\text{C})$

HITACHI/ LOGIC/ARRAYS/MEM

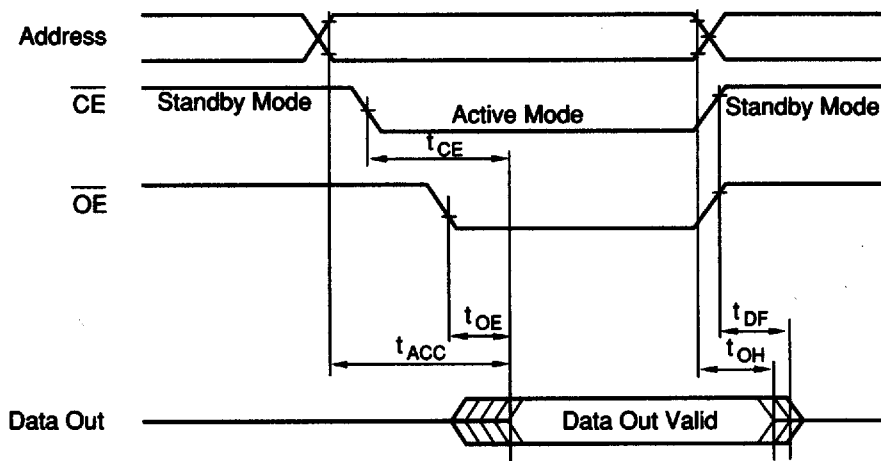
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 1.5 V

Item	Symbol	HN27C4096H-70		HN27C4096H-85		Unit	Test Condition
		Min.	Max.	Min.	Max.		
Address Access Time	t_{ACC}	-	70	-	85	ns	$\overline{CE} = \overline{OE} = V_{IL}$
Chip Enable Access Time	t_{CE}	-	70	-	85	ns	$\overline{OE} = V_{IL}$
Output Enable Access Time	t_{OE}	-	40	-	45	ns	$\overline{CE} = V_{IL}$
Output Disable to High-Z ¹	t_{DF}	0	30	0	30	ns	$\overline{CE} = V_{IL}$
Output Hold to Address Change	t_{OH}	5	-	5	-	ns	$\overline{CE} = \overline{OE} = V_{IL}$

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN27C4096H)

4

HITACHI

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

4-81

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

 $(V_{CC} = 6.25 V \pm 0.25 V, V_{PP} = 12.5 V \pm 0.3 V, T_a = 25^\circ C \pm 5^\circ C)$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_U	-	-	2	μA	$V_{IN} = 6.5 V / 0.45 V$
Operating V_{CC} Current	I_{CC}	-	-	50	mA	
Operating V_{PP} Current	I_{PP}	-	-	70 ⁷	mA	$\overline{CE} = V_{IL}$
Input Voltage ³	V_{IH}	2.2	-	$V_{CC} + 5.6^6$	V	
	V_{IL}	-0.1 ⁵	-	0.8	V	
	V_H	11.5	12.0	12.5	V	
Output Voltage	V_{OH}	2.4	-	-	V	$I_{OH} = -400 \mu A$
	V_{OL}	-	-	0.45	V	$I_{OH} = 2.1 mA$

- Notes:
- V_{CC} must be applied before V_{PP} and removed after V_{PP} .
 - V_{PP} must not exceed 13 V, including overshoot.
 - Device reliability may be adversely affected if the device is installed or removed while $V_{PP} = 12.5 V$.
 - Do not change V_{PP} from V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE} = \text{low}$.
 - V_{IL} min = -0.6 V for pulse width ≤ 20 ns.
 - If V_{IH} is over the specified maximum value, programming operation can not be guaranteed.
 - $I_{PP} = 40$ mA in Word Programming Mode.

HITACHI

■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

T-46-13-29

 $(V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V}, V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}, T_a = 25^\circ\text{C} \pm 5^\circ\text{C})$ **Test Conditions**

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: $\leq 20 \text{ ns}$
- Reference levels for measuring timing: 0.8 V / 2.0V

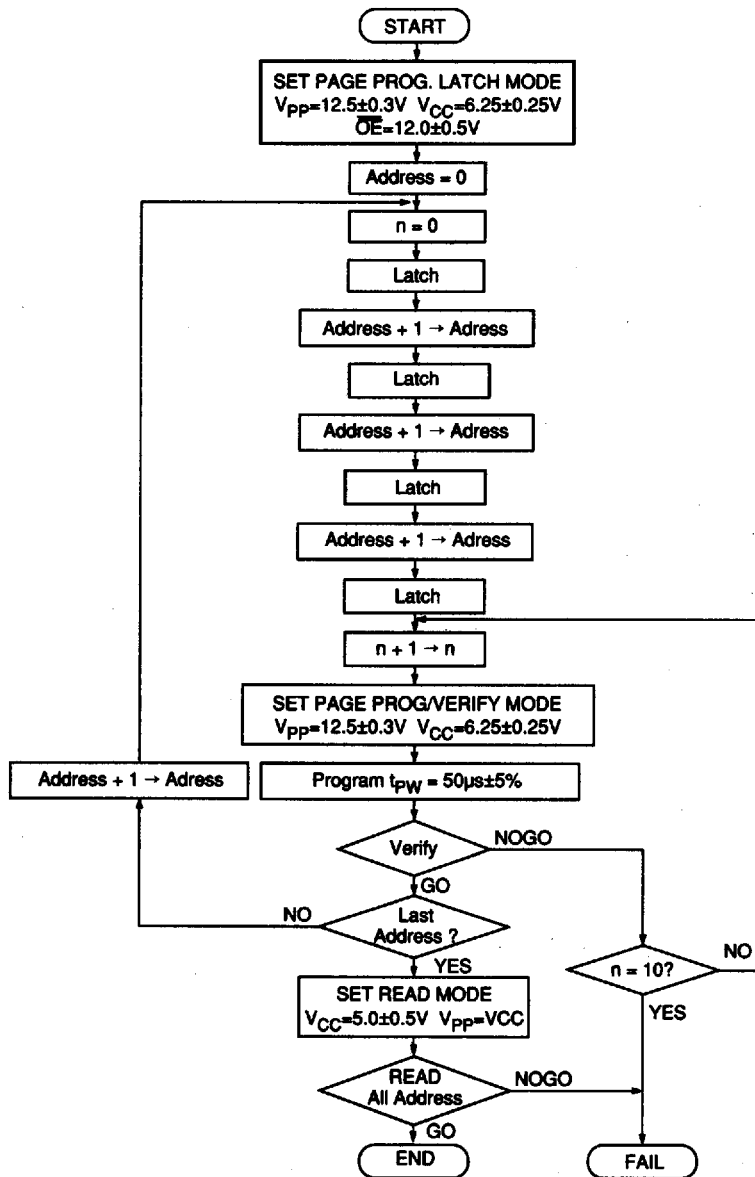
Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	2	-	-	μs	
Address Hold Time	t_{AH}	0	-	-	μs	
Data Setup Time	t_{DS}	2	-	-	μs	
Data Hold Time	t_{DH}	2	-	-	μs	
Chip Enable Setup Time	t_{CES}	2	-	-	μs	
V_{PP} Setup Time	t_{VPS}	2	-	-	μs	
V_{CC} Setup Time	t_{VCS}	2	-	-	μs	
Output Enable Setup Time	t_{OES}	2	-	-	μs	
Output Disable Time	t_{DF}	0	-	130	ns	
Programming Pulse Width	t_{PW}	47.5	50.0	52.5	μs	
Data Valid from Output Enable Time	t_{OE}	0	-	150	ns	
Chip Enable Pulse Width During Data Latch	t_{LW}	1	-	-	μs	
Output Enable = V_H Setup Time	t_{OHS}	2	-	-	μs	
Output Enable = V_H Hold Time	t_{OHH}	2	-	-	μs	
Output Enable Hold Time	t_{OEH}	2	-	-	μs	
V_{PP} Hold Time	t_{VRS}	1	-	-	μs	
Page Programming Reset Time	t_{VLW}	1	-	-	μs	

- Note:
1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.
 2. Page Program Mode will be reset when V_{PP} is set to V_{CC} or less.

■ PAGE PROGRAMMING FLOWCHART

The Hitachi HN27C4096H can be programmed with the high performance Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.

- Note:
1. To set the device into Page Programming, apply 12.5 V to V_{PP} then followed by applying 12 V to OE. The device operates in Page Program Mode until reset.
 2. To reset the Page Program Mode, set $V_{PP} = V_{CC}$ or less.

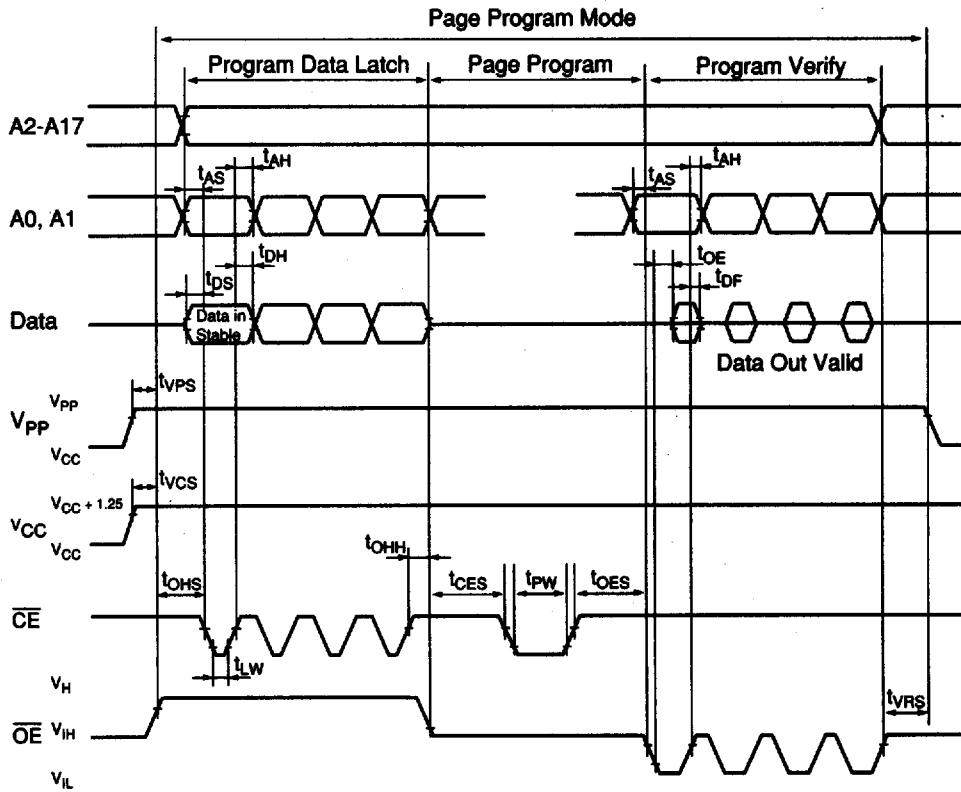


(FC.PP.HN27C4096H)

HITACHI

■ PAGE PROGRAMMING TIMING WAVEFORM

T-46-13-29



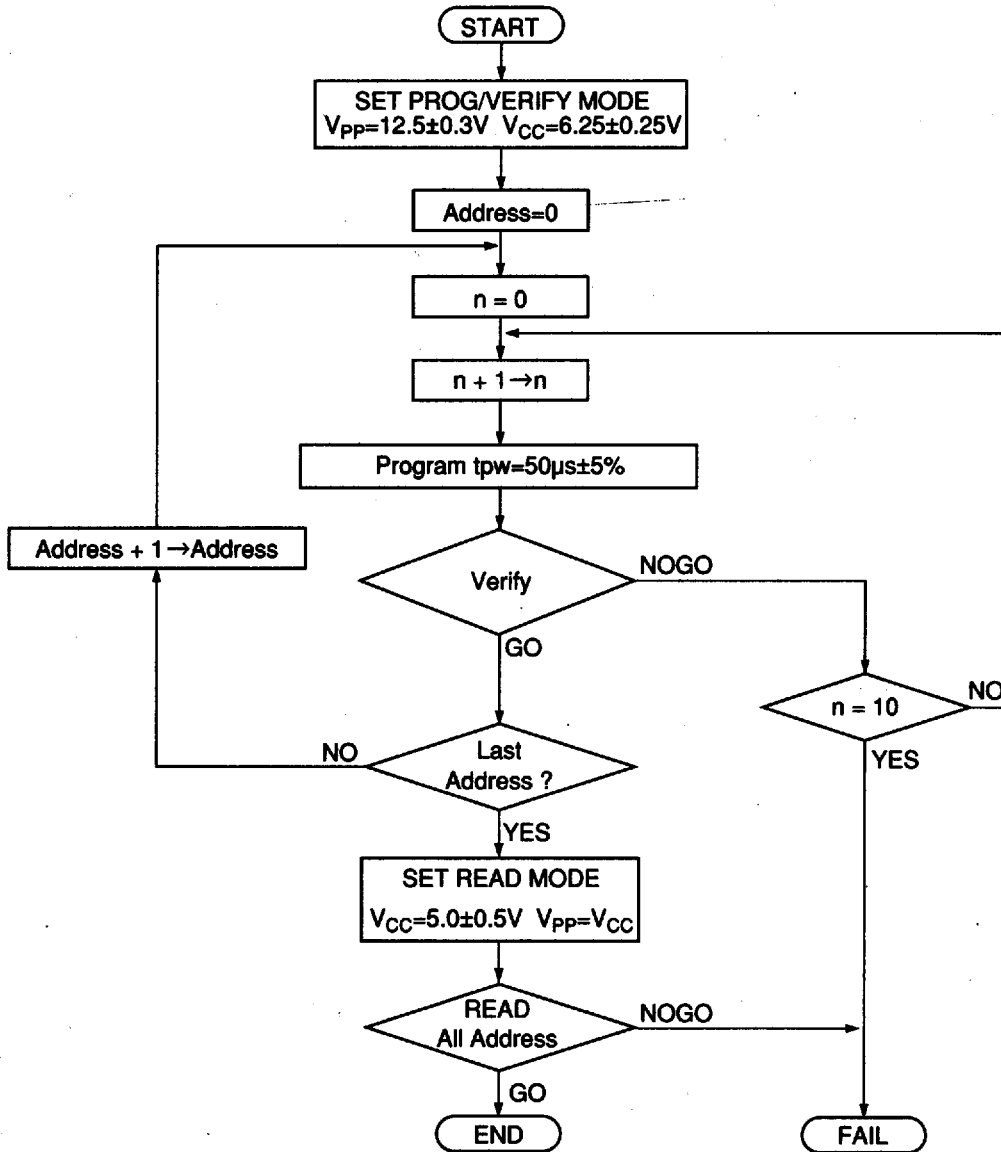
(TD.PP.HN27C4096H)

HN27C4096H Series

T-46-13-29

■ WORD PROGRAMMING FLOWCHART

The Hitachi HN27C4096H can be programmed with the high performance Word Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.

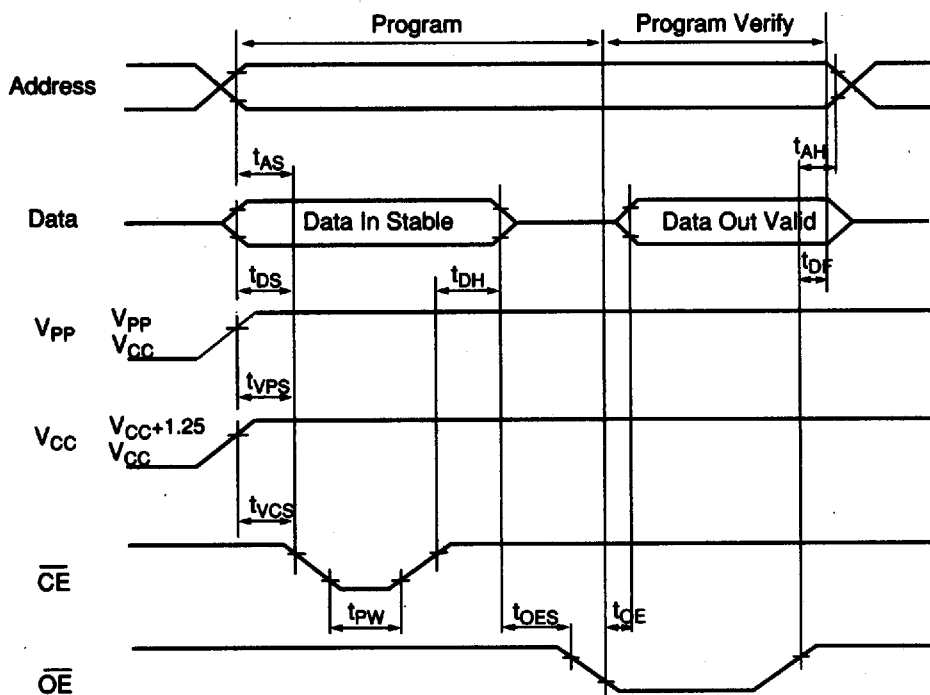


(FC.P.HN27C4096H)

HITACHI

WORD PROGRAMMING TIMING WAVEFORM

T-46-13-29



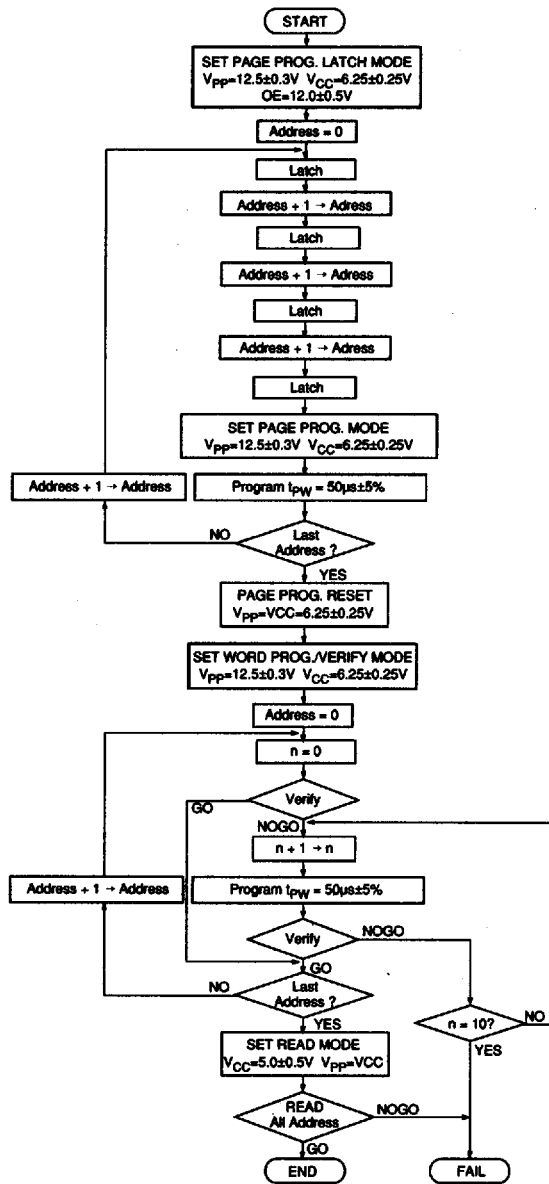
(TD.P.HN27C4096H)

■ OPTIONAL PAGE PROGRAMMING FLOWCHART

The Hitachi HN27C4096H can be programmed with the high performance Optional Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.

This programming algorithm is a combination of Page Programming and Word Verify. It can be used to avoid the increased programming verify time when a programmer with a slower machine cycle is used and shorten the total programming time.

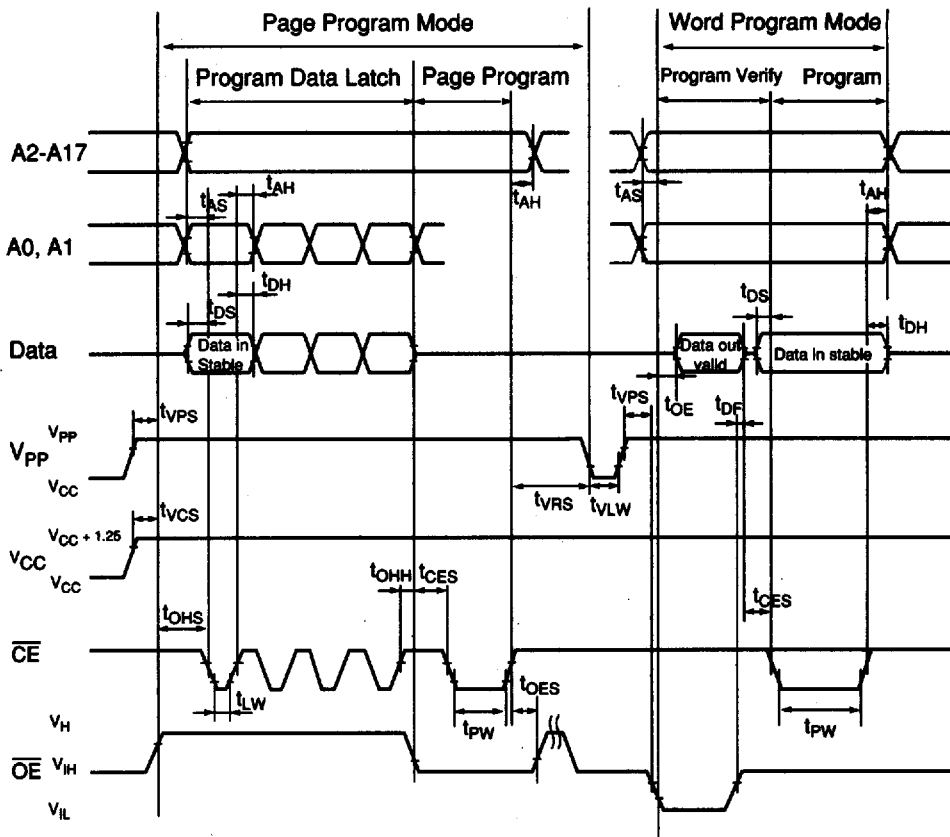
Please refer to the timing specifications for page programming and word programming.



(FC.OPP.HN27C4096H)

■ OPTIONAL PAGE PROGRAMMING TIMING WAVEFORM

T-46-13-29



(TD.OPP.HN27C4096H)

HN27C4096H Series

T-46-13-29

■ **ERASING THE HN27C4096H**

The Hitachi HN27C4096H is erased by exposure to ultraviolet light of 2537Å. All of the data is changed to "1" after this erasure procedure. The minimum integrated dose (UV intensity x exposure time) for erasure is 15 W-sec/cm².

■ **DEVICE IDENTIFIER MODE DESCRIPTION**

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

■ **HN27C4096H SERIES IDENTIFIER CODE**

Identifier	A ₀	I/O ₆ -I/O ₁₅	I/O ₇	I/O ₈	I/O ₉	I/O ₄	I/O ₃	I/O ₂	I/O ₁	I/O ₀	Hex Data
Manufacturer Code	V _{IL}	X	0	0	0	0	0	1	1	1	07
Device Code	V _{PI}	X	1	0	1	0	0	0	1	0	A2

- Notes:
1. $V_{CC} = 5.0 V \pm 10\%$
 2. $A_9 = 12.0 V \pm 0.5V$
 3. $A_1-A_8, A_{10}-A_{17}, \overline{CE}, \overline{OE} = V_{IL}$
 4. X = Don't Care

HITACHI