

ET1011

Evaluation Board

User Guide

Revision 2.0

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Introduction

The ET1011 Evaluation Board (EB) provides an evaluation platform for the Agere Systems single Gigabit Ethernet Transceiver (a.k.a. PHY) device, the *TruePHY™* ET1011. This card is designed to demonstrate many of the PHY's capabilities. The ET1011 EB is designed to accommodate two (2) different versions of the *TruePHY™* device:

1. ET1011 – 128TQFP
2. ET1011 – 68 MLCC

1. Board Design

1.1. Overview

The ET1011 Evaluation Board is a simple board to operate, yet allowing for the evaluation of the ET1011 PHY's capabilities. An overview of the board can be seen in Figure 1-1 - Block Diagram.

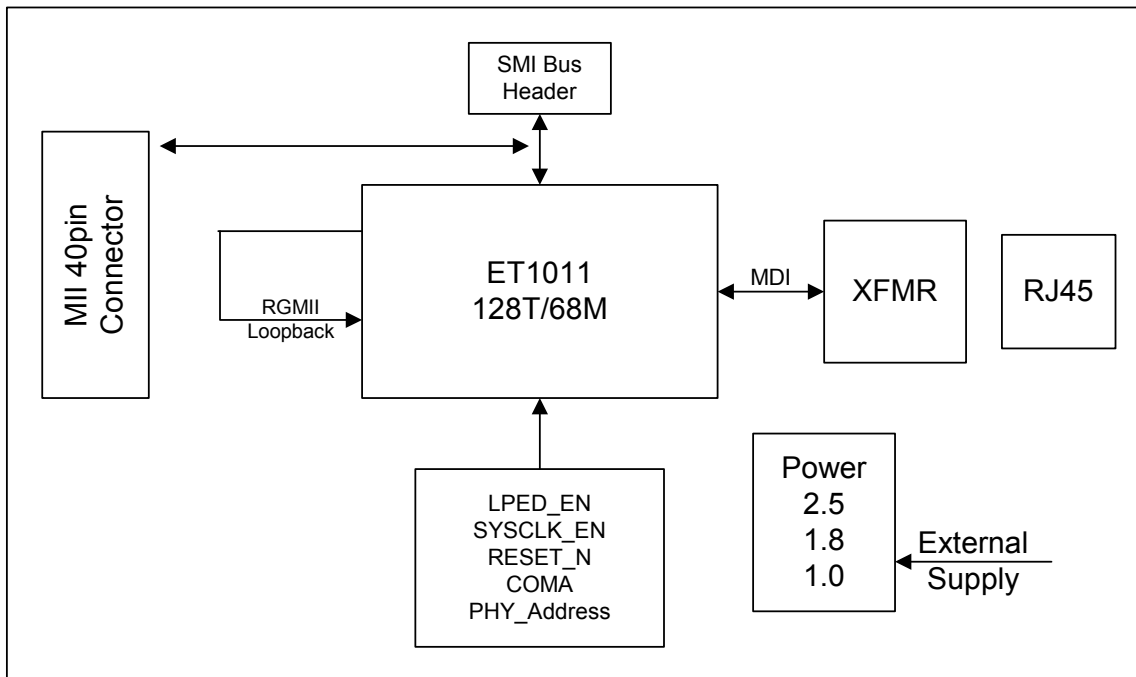


Figure 1-1 - Block Diagram

The board is intended to operate as part of a system. Through the use of an external serial management interface controller and Agere's *TruePHY™* Evaluation System software, the user is able to configure and monitor the PHY's operation. By connecting the board's RJ45 connector to the user's Ethernet test system, cable reach and data performance can be evaluated. The MAC interface is configured to loopback the data in RGMII format.

1.2. Features

The ET1011 Evaluation Board allows for the following features to be evaluated:

- Software configuration
- Hardware configuration
- Ethernet link evaluation
- RGMII Loopback Data
- Power Rail tolerance evaluation

2. Functional Area Descriptions

The functions of the ET1011 Evaluation Board are divided into 5 different areas of discussion. In each of these sections, the reference designators are listed and a brief description of the function follows.

Refer to

Figure 2-1 - ET1011 EB Top Assembly View for the location.

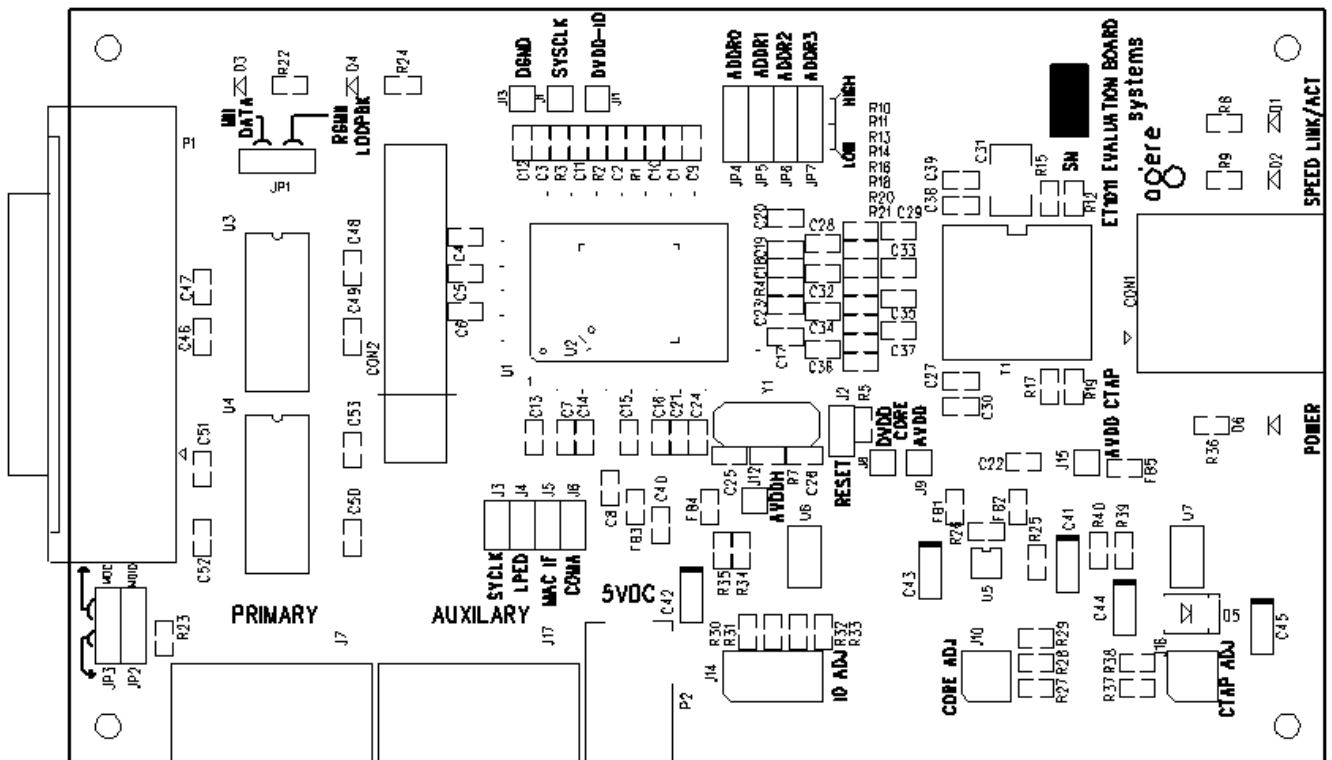


Figure 2-1 - ET1011 EB Top Assembly View

2.1. Serial Management Interface

The Serial Management Interface (SMI) allows for register configuration. The SMI bus consists of MDIO (Data) and MDC (Clock). For the ET1011 EB, this configuration path can be directed to either the MII Connector (P1) or to a header (J7). Two jumpers on board determine which communication path controls the SMI bus. When communicating with the PHY on the SMI, it is necessary to configure the PHY's SMI address. This is accomplished using jumpers (JP4-7). The address range is from 0-15. Refer to Table 2-1- PHY Address Selection for configuration. An auxiliary SMI header (J17) is provided for "Daisy Chaining" multiple evaluation boards together.

- J7 – Primary connection
- J17 – Auxiliary connection to allow for daisy-chaining of boards
- JP3 – MDC selection between MII connector and J7/J17 headers
- JP2 – MDIO selection between MII connector and J7/J17 headers
- JP4, JP5, JP6, JP7 – SMI Address Selection

3	2	1	0	PHY Address
JP7	JP6	JP5	JP4	Address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Table 2-1- PHY Address Selection

2.2. Hardware Configuration

The ET1011 PHY has many hardware configuration options. For simplicity, the ET1011 EB has pre-configured most options for easy use.

There are four configuration options that the user has access to:

- J2 – Reset: Strap to enable hardware reset.
- J3 – SysClk: Strap to disable SYS_CLK output
- J4 – LPED: Strap to disable Low Power Energy Detect mode
- J6 – Coma: Strap to enable COMA mode

2.3. Data Modes

The ET1011 EB allows for RGMII mode data to be looped back on the MAC interface. In this RGMII loopback mode, data can be evaluated on 10Base-T, 100Base-TS, or 1000Base-T links

- U4 – RGMII Loopback
- D4 – RGMII Loopback Data Path Enable LED
- D1 – Speed Indication LED
- D2 – Link/Activity Indication LED

2.4. Power Supplies

The ET1011EB allows for the three different voltage rails to be independently adjusted. The modification is accomplished by adding or removing straps on headers J10, J14, and J16.

Note: The adjustment is based upon the number of straps and not the location.

- P2 – Input connector, 5vDC 240mA
- J14 – I/O Voltage Adjust: 0= -10%, 1=-5%, 2=Nominal, 3=+5%, 4=+10%
- J10 – Core Voltage Adjust: 0= -5%, 1=Nominal, 2=+5%
- J16 – Center Tap Voltage Adjust: 0= -5%, 1=Nominal, 2=+5%
- D6 – Power LED

2.5. Monitor Test Points

Several test points have been provide to allow the user to easily monitor data, clocks, and power rails:

- CON2 – Logic Analyzer compression probe contacts
- J1 – SysClk Output
- J13 – DGND
- J11 – DVDD-IO
- J12 – AVDDH
- J8 – DVDD Core
- J9 – AVDD Core
- J15 – AVDD CTAP

3. Installation and Setup

3.1. Equipment

The *TruePHY™* Evaluation System consists of a combination of custom software, and hardware developed by Agere. A summary of the components and equipment included in the *TruePHY™* Evaluation System is listed below.

Components developed and provided by Agere:

- ET1011 Evaluation Board (ET1011EB)
- 5 Vdc external power supply
- Serial Management Interface (SMI) cable (2x4 header to 2x5 header)
- PC-I2C-DEV board
- Installation and documentation CD for *TruePHY™* Evaluation Software
- Parallel port cable (DB-25 to DB-25)

3.2. Installation

Step 1: Connect PC-I2C-DEV Board to Parallel Port.

- ❑ Connect the PC-I2C-DEV board to a parallel port on the local PC using supplied parallel port cable.

Step 2: Connect SMI Cable Between PC-I2C-DEV Board and ET1011EB.

- ❑ Connect 2x4 header connector of cable to 2x4 header on the PC-I2C-DEV board. Connect 2x5 header connector of cable to 2x5 header labeled 'PRIMARY' on the ET1011EB.

Step 3: Supply Power to ET1011EB.

- ❑ Plug the power supply barrel connector into ET1011EB (P2).
- ❑ Plug converter into any (110 V) ac power supply.

Step 4: Connect to ET1011EB.

- ❑ Launch the *TruePHY™* Evaluation System application.
- ❑ Select the "LPT1" connection type from the "Connect To Target" window, and click 'OK'.



Figure 3-1, Connect to Target Window