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EUREKA Microelectronics, Inc.

EK7308

Preliminary Rev. 0.1

DATA SHEET

240-Output TFT Gate Driver IC

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240- Output TFT Gate Driver IC

1. DESCRIPTION

The EK7308 is a 240-output TFT gate driver IC suitable for driving TFT LCD panels.

2. FEATURES

- Output channels：240 outputs+2 pins (fixed to VEE)
- Driver operating frequency：max. 200 KHz
- LCD supply voltage：VEE+40V
- Driver output levels：Two
- Logical interface：+2.7V ~ -5.5V
- Incorporates bi-directional shift register.
- COG type

3. BLOCK DIAGRAM

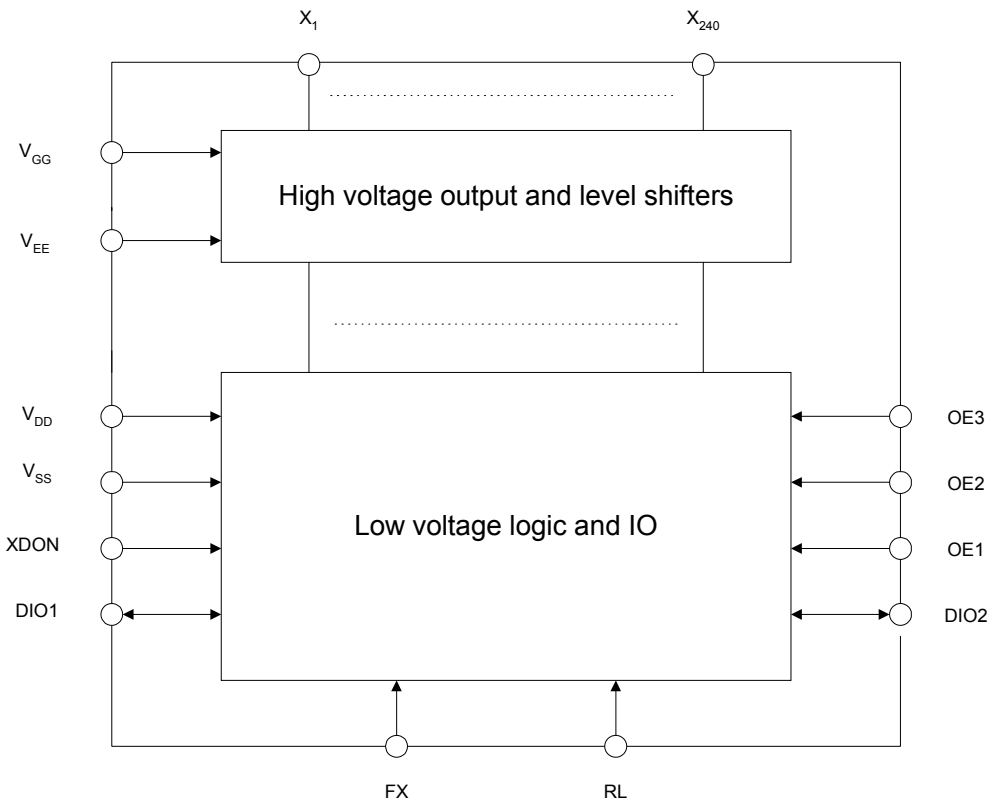

Fig. 1 Block diagram

4. PIN FUNCTION DESCRIPTIONS

Table 1. Pad description

Pad Name	I/O	Function	DESCRIPTION		
X_1-X_{240}	O	TFT gate driver output	Under the control of the shift register data, OE1 or OE2 or OE3, and DIO1 or DIO2, the driver outputs are V_{GG} or V_{EE} and change their value at the rising edge of FX		
PATH	-	-	Short internally		
X_0, X_{241}	-	-	LCD panel auxiliary pins. This pins output V_{EE} level.		
V_{EE}	-	Supply	Negative power supply for Level shifters. Chip ground		
V_{SS}	-	Supply	Logic ground, Reference of the voltages		
RL	I	Shift direction selection signal	RL = "H" : X_1 to X_{240} (Shift left) RL = "L" : X_{240} to X_1 (Shift right)		
DIO1 DIO2	I/O	Start pulse input and output		**DIO1**	**DIO2**
			RL = "H"	Input	Output
			RL = "L"	Output	Input
XDON	I	Negative active input pin	When XDON = "L" then the driver outputs are at the V_{GG} level independence of any other input or register value.		
FX	I	Shift register clock input	The start pulse is sampled at the rising edge of FX, The carry pulse changes at the falling edge of FX.		
OE1 OE2 OE3	I	Negative active input pin	When OE_N = "H" then the associated outputs are set to V_{EE} independent of the register data. This function is not synchronized with FX.		
V_{DD}	-	Supply	Logic positive power		
V_{GG}	-	Supply	High voltage power and TFT driver output high level		

5. FUNCTIONAL OPERATIONS

Power supplies

The TFT voltage is relative to the logic ground, it can be a negative voltage value.

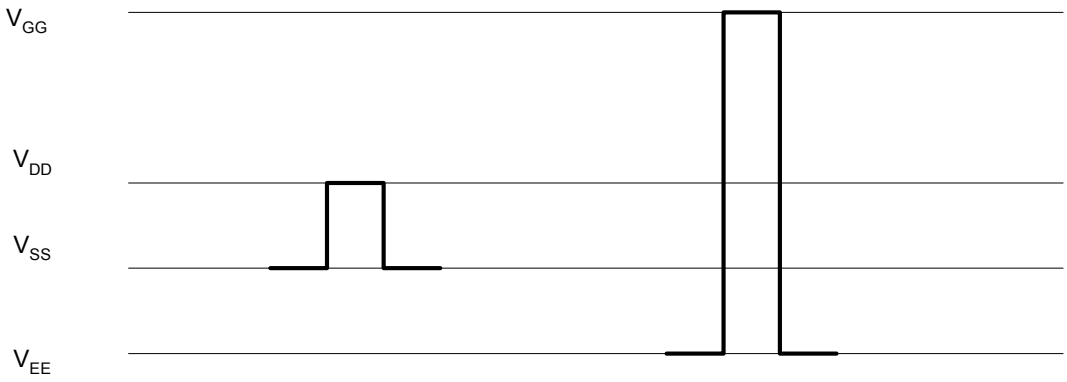

Fig. 2 Relative position of the different supply voltages

Shift direction

The input signals OE1, 2, 3 and the shift data control the value of the outputs (X_1 till X_{240}). Their value can be either V_{GG} or V_{EE}.

The signal LR controls the shift direction of the shift register. The shift register takes its value from one of the input/output pins DIO at the rising edge of the clock FX and shifts the value to the other input/output pin DIO where it is presented at the falling edge of FX.

Table 2. RL shift direction relation

RL	Start pulse taken from:	Data shift direction	Output pulse given at:
RL="H"	DIO1	$X_1 \rightarrow X_{240}$	DIO2
RL="L"	DIO2	$X_{240} \rightarrow X_1$	DIO1

OE function

When the OE1, OE2, OE3 inputs are “H” than the outputs are driven to V_{EE} regardless of the contents of the shift register. Each of the three inputs drives it own set of outputs. This function is not synchronized with FX. The signal XDON can override this function. In the Table below the relation between each OE1,2,3 and their related outputs is given.

Table 3. OE1,2,3 to Output relation

Signal input	Symbol	LCD driver outputs
OE1	X(3i+1) i =0~79	$X_1,X_4,X_7,X_{10},\cdots\cdots,X_{231},X_{232},X_{235},X_{238}$
OE2	X(3i+2) i =0~79	$X_2,X_5,X_8,X_{11},\ \cdots\cdots,\ X_{239}$
OE3	X(3i+3) i =0~79	$X_3,X_6,X_9,X_{12},\ \cdots\cdots,X_{234},X_{237},X_{240}$

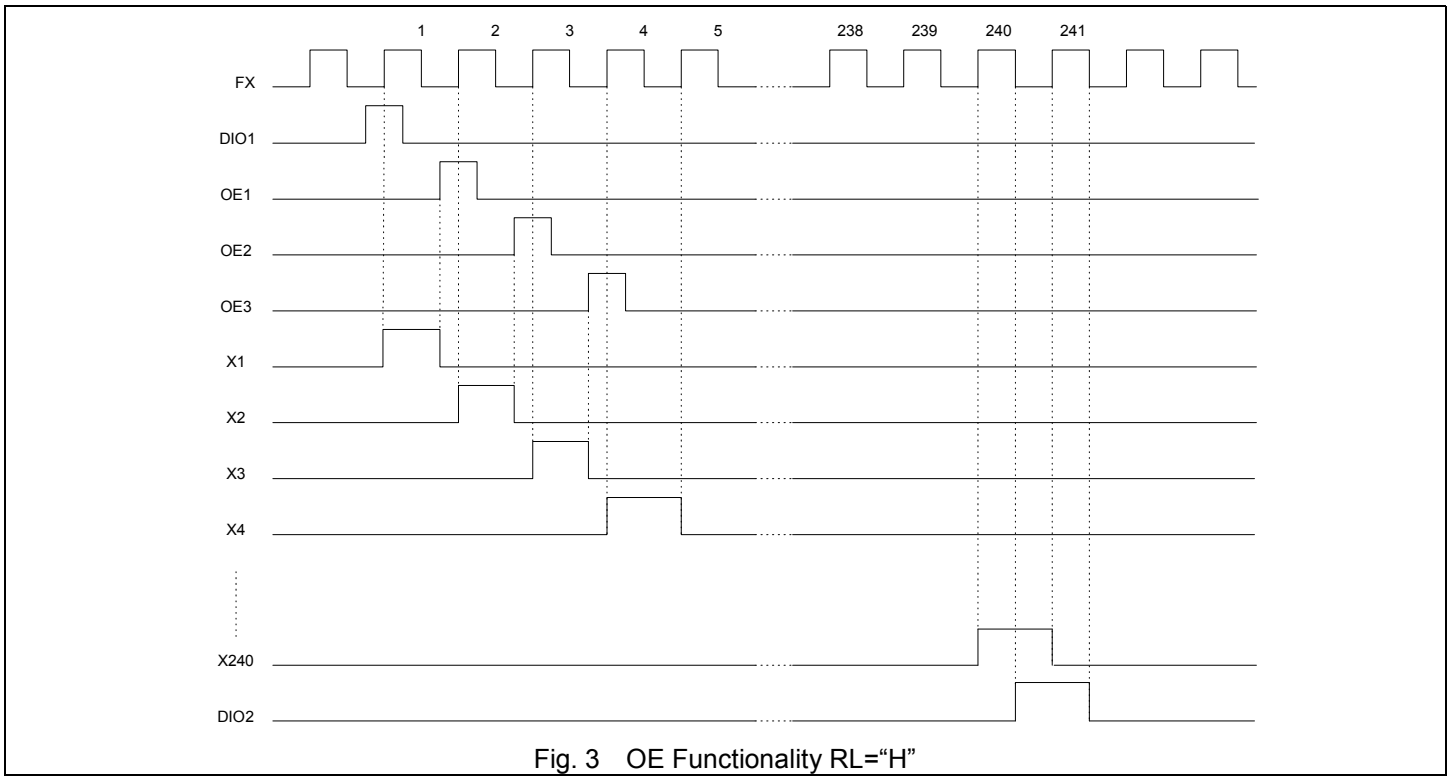

Fig. 3 OE Functionality RL=“H”

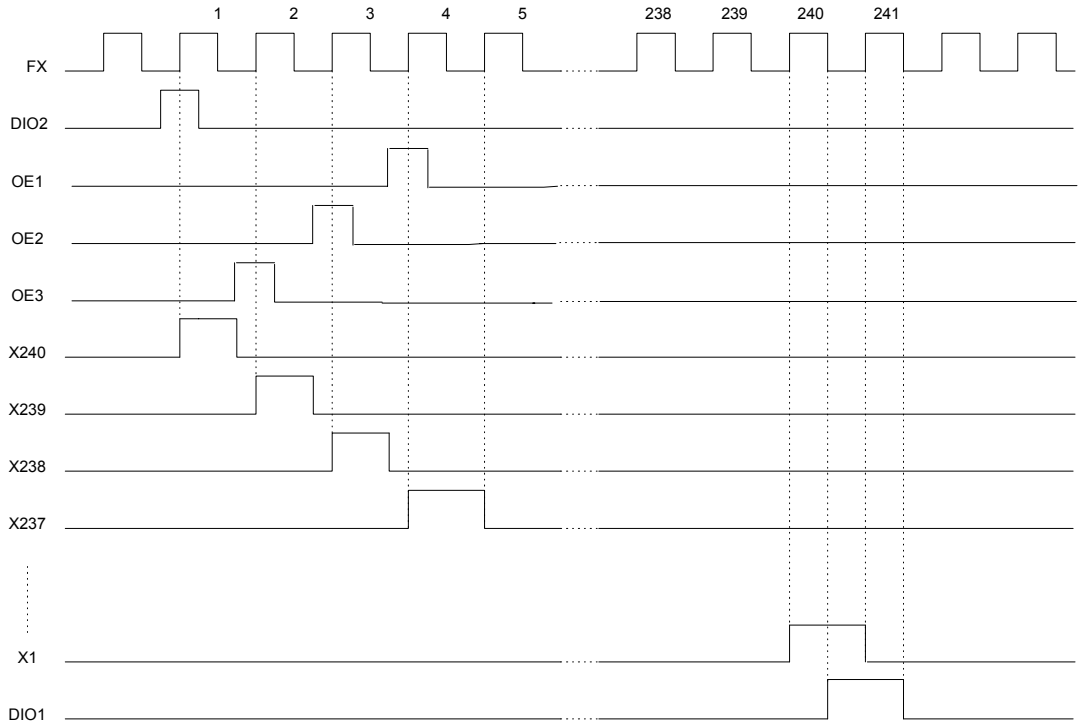

Fig. 4 OE Functionality RL= “L”

XDON function

When XDON input is “L” then all outputs are driven to the V_{GG} level. This function is overriding all other inputs. With this input all TFT gates are set to high to enable a display off function. This function is not synchronized with FX.

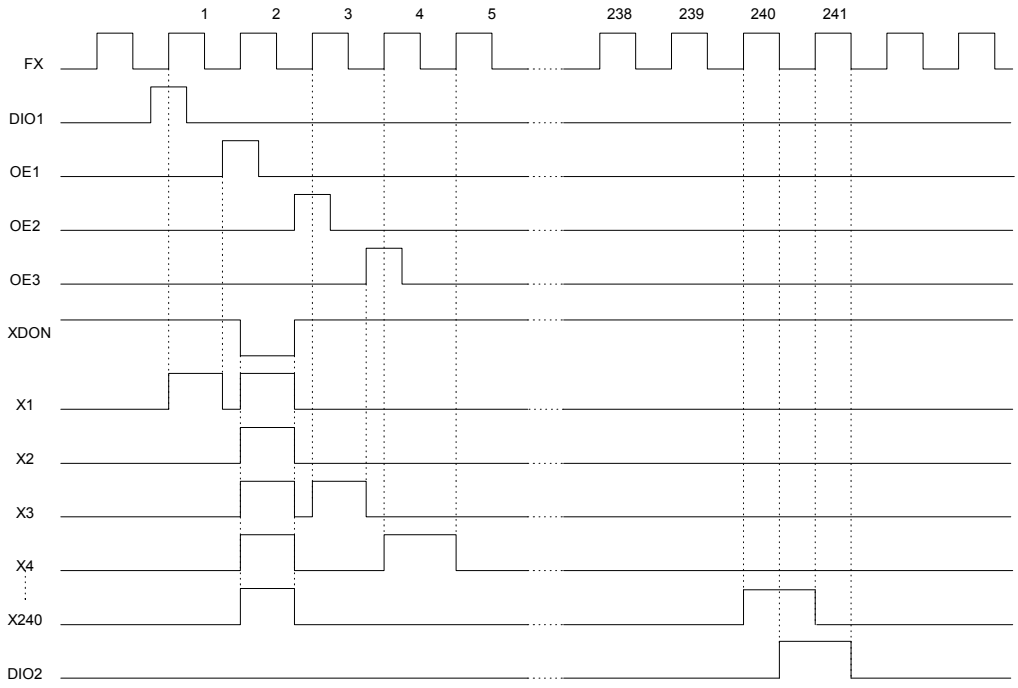

Fig. 5 XDON Functionality RL=“H”

PRECAUTIONS

Precaution when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow, if voltage is supplied to the LCD driver power supply while the logic system power supply is floating. The detail is as follows.

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power.

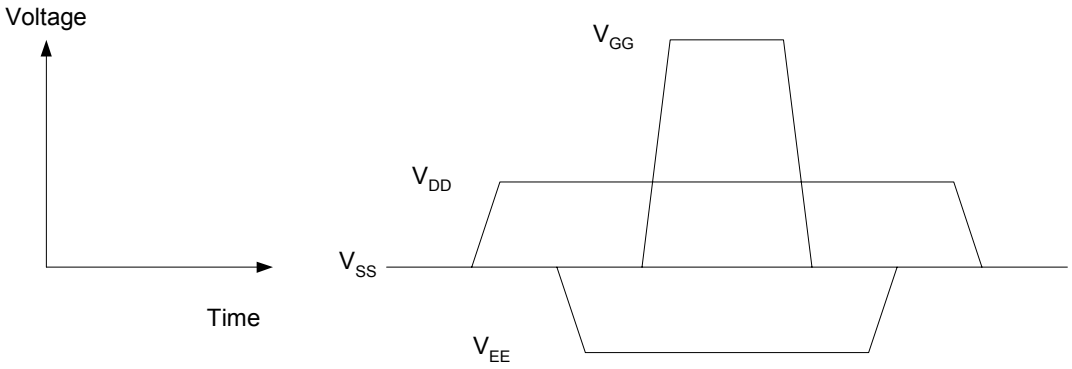

Fig. 9 Power ON/OFF sequence

6. ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

In accordance with the Absolute Maximum Ratings System (IEC 134); See notes 1 and 2

Parameter	Symbol	Applicable Pins	Ratings	Unit	NOTE
Supply voltage(1)	V_{DD}	V_{DD}	V_{SS} -0.3 to +7.0	V	1, 2
Supply voltage(2)	V_{GG}	V_{GG}	-0.3 to +45.0	V	
	V_{EE}	V_{EE}	V_{GG} -45 to +0.3	V	
Input voltage	V_I	EO1, EO2, EO3, DIO1 DIO2, RL, FX, XDON	V_{SS} -0.3 to V_{DD}+0.3	V	
Storage temperature	T_{stg}		-45 to +125	℃	

Notes:

1. Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device
2. Parameters are valid over operating temperature range unless otherwise specified.

RECOMMENDED OPERATING CONDITIONS

Table 5. Recommended operating conditions

Parameter	Symbol	Applicable pins	Min.	Typ.	Max.	Unit	Notes
Supply voltage(1)	V_{DD}	V_{DD}	+2.7		+5.5	V	1, 2
Supply voltage(2)	V_{GG}	V_{GG}	+7.0		+25	V	
Supply voltage(3)	V_{EE}	V_{EE}	-16		-5	V	
Operating temperature	T_{OPR}		-20		+75	℃	

Notes:

1. All voltages are with respect to V_{SS} unless otherwise noted (0 V).
2. Ensure that voltages are set such that $V_{EE} \leq V_{SS} < V_{DD} < V_{GG}$.

7. ELECTRICAL CHARACTERISTICS

Table 6. DC Characteristics

(V_{SS}=0 V, V_{DD}=+2.5V to +5.5V, V_{GG}=+15.0 to +40.0 V, T_{OPR}=-25℃)

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit	Note
Operating Supply Current	IDD	fFX=15.7kHz V_{DD}=3.3V V_{EE}=-15V V_{GG}=15V Output with no load	V_{DD}			800	μA	
	IGG		V_{GG}			300	μA	
Standby Quiescent Supply Current	IDS	Standby V_{DD}=3.3V V_{EE}=-15V V_{GG}=15V	V_{DD}			600	μA	
	IGS		V_{GG}			100	μA	
Input pin								
H input voltage	VIH1		RL,FX, OE1~3,	0.7x V_{DD}		V_{DD}	V	
L input voltage	VIL1			0		0.3x V_{DD}	V	
Input leakage current	VLI1			-1		1	μA	XDON except
Output pin								
H input voltage	VIH3		DIO1, DIO2	0.7x V_{DD}		V_{DD}	V	
L input voltage	VIL3					0.3x V_{DD}	V	
H output voltage	VOH	I_O = -100 μA		V_{DD} -0.4			V	
L output voltage	VOL	I_O = 100 μA				0.4	V	
Liquid crystal driving output pin								
Output leakage current	VLO1		X1~X240	-50		50	μA	
Output ON resistance	RON-V_{GG}	V_{GG}=15V V_{EE}=-15V V_{OM}=VGG-0.5V V_{OM} is X1~X240			600	1000	Ω	
	RON-V_{EE}	V_{GG}=15V V_{EE}=-15V V_{OM}=V_{EE}+0.5V V_{OM} is X1~X240			600	1000	Ω	

Table 7. AC Characteristics

(V_{SS}= 0 V, V_{DD}=+2.5V to +5.5V, V_{GG}-V_{EE}=+30.0 to +40.0 V, T_{OPR}=25℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock period	t_{FX}		-		200	KHz In cascade connection
Pulse width of clock H level	t_{WH}		500			ns
Pulse width of clock L level	t_{WL}		500			ns
DIO data set up time	t_{su}		200			ns
DIO data hold time	t_h		300			ns
DIO output delay time	t_{pd1}	CL=20pF			500	ns
Xn output delay time	t_{pd2}	CL=220pF			10	us
Input Rise Time	t_r				100	ns
Input Fall Time	t_f				100	ns
OEX output delay time	t_{pd3}	CL=220pF			900	ns

Timing Chart

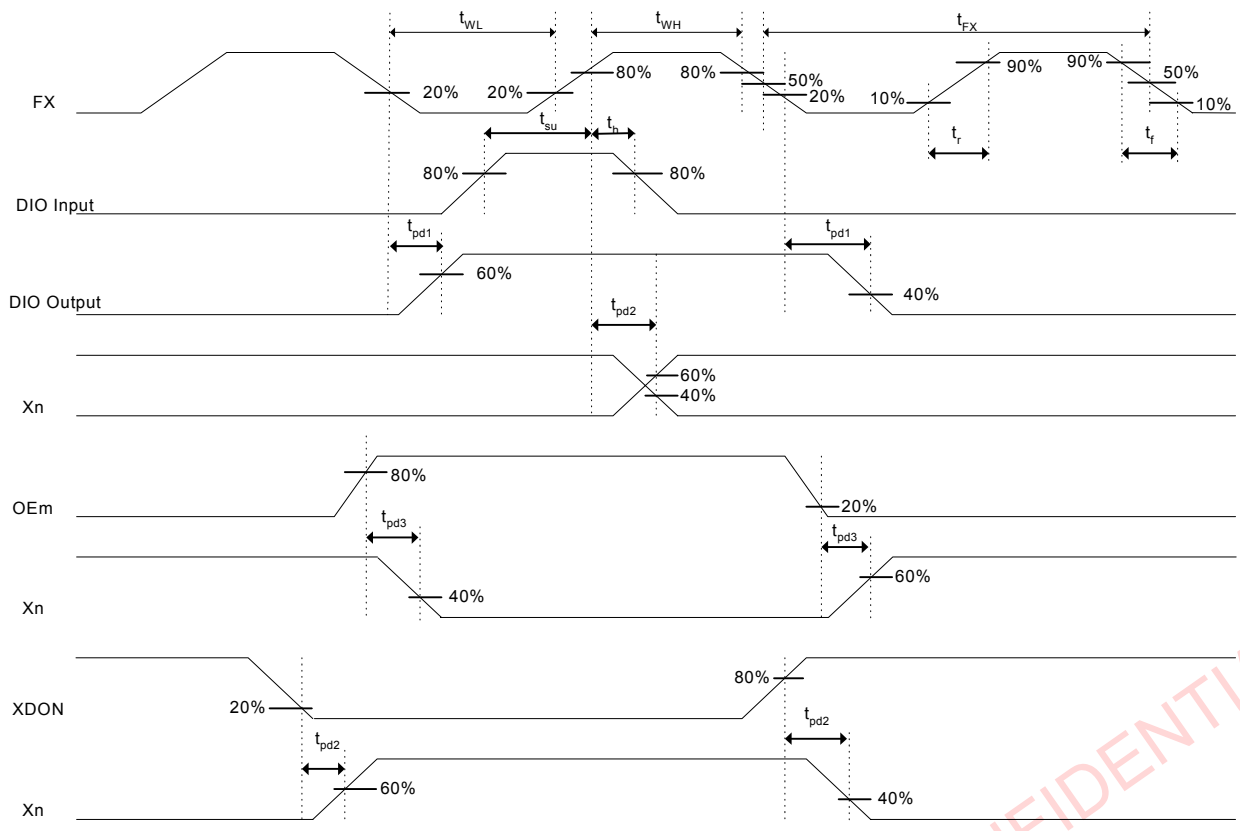

Fig. 10 Timing

8. DEFINITIONS

Data Sheet status	
Objective specification	This data sheet contains target or goal specification for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specification.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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