APPLICATION NOTE

AN1777

Low voltage front-end circuits: SA601, SA620

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CONTENTS

I. INTRODUCTION

The objectives of this application note are to highlight key features and distinguish key differences between the SA601 and SA620. The power, gain, noise figure, and third-order intercept point of the LNA and mixer will be characterized. A resonant circuit implementing a high loaded-Q μ-strip inductor and an extensive discussion of open-collector mixer outputs and how to match them will also be presented.

The SA601 and SA620 are products designed for high performance low power RF communication applications from 800 to 1200MHz. These chips offer the system designer an alternative to discrete front-end designs which characteristically introduce a great deal of end-product variation, require external biasing components, and require a substantial amount of LO drive. The SA601 and SA620 contain a low noise amplifier and mixer, offering an increase in manufacturability and a minimum of external biasing components due to integration. The LO drive requirements for active mixers are less stringent than passive mixers, thus minimizing LO isolation problems associated with high LO drive-levels. These chips also contain power down circuitry for turning off all or portions of the chip while not in use. This minimizes the average power consumed by the front-end circuitry. The SA620 features an internal VCO that eliminates additional cost and space needed for an external VCO. The SA601 and SA620 fit within a 20-pin surface mount plastic shrink small outline package (SSOP), thus saving a considerable amount of space.

II. KEY ATTRIBUTES OF THE SA601 AND SA620

The primary differences between the SA601 and SA620 are the LNA power down capability, the implementation of the mixer output circuitry, and the incorporation of an integrated VCO.

Table 1 below summarizes the attributes of both parts.

Table 1. Showing SA601 and SA602 Attributes

Product	Diff. Mixer Output	LNA Thru Mode	Mixer Power Down	Int. VCO and VCO Pwr Down
SA601	Yes	No	Yes	No
SA620	No	Yes	Yes	Yes

III. POWER CONSUMPTION

As mentioned above, the average power consumed by the front-end circuitry can be decreased by selectively turning off circuitry that is not in use. The supply current at a given voltage will decrease more than 3mA for each LNA, mixer, or VCO disabled. When the LNA is disabled on the SA620 it is replaced by a 9dB attenuator. This is useful for extending the dynamic range of the receiver when an overload condition exists. Tables 2 and 3 below contain averaged data taken on the SA601 and SA620 while in an application board environment.

Table 2. Showing SA601 Supply Current

V_{CC}	I_{CC} (mA)	I_{CC} (mA) Mixer Disabled
3.0	8.4	4.9
4.0	8.4	4.7
5.0	8.3	4.5

Table 3. Showing SA620 Supply Current

V_{CC}	I_{CC} (mA)	I_{CC} (mA) LNA Disabled	I_{CC} (mA) Mixer Disabled	I_{CC} (mA) VCO Disabled	I_{CC} (mA) Chip Fully Powered Down
3.0	11.4	8.0	8.1	8.2	1.4
4.0	11.6	8.5	8.0	8.2	1.6
5.0	11.7	8.9	8.0	8.2	1.7

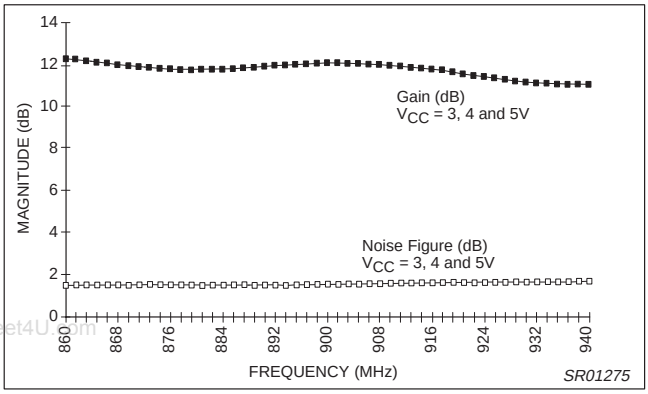


Figure 1. Noise Figure and Gain vs Frequency SA601 LNA

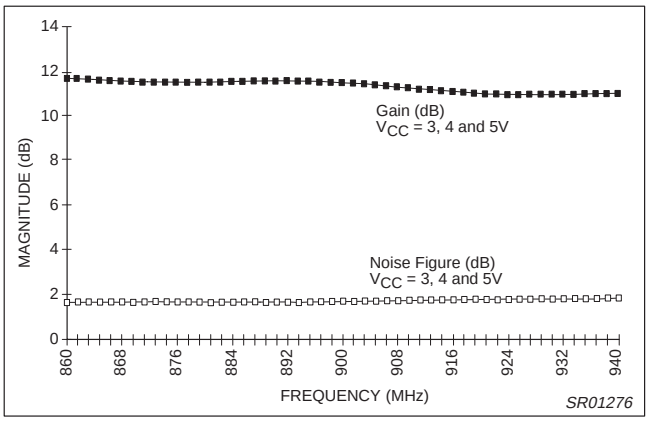


Figure 2. Noise Figure and Gain vs Frequency SA620 LNA

IV. LOW NOISE AMPLIFIERS

The performance of the SA601 and SA620 low noise amplifiers are virtually identical. You can expect an average gain of approximately 11.5 ±1.5dB and a noise figure of approximately 1.6 ±0.3dB. The LNA input and output networks are matched for optimum return loss, gain and best noise figure over the 869 - 894MHz band. They also perform well when utilized in the 902 - 928MHz band without any additional modification to the LNA matching networks. Figures 1 and 2 show gain and noise figure of a typical SA601 and SA620 LNA in the application board environment. Both the gain and the noise figure remain almost constant as V_{CC} is adjusted to 3, 4 and 5V. Therefore, only one curve is shown for clarity.

V. SA620 MIXER

The SA620 mixer is intended for operation with the integrated VCO and employs a single open-collector output structure. The open-collector output structure allows the designer to easily match any high impedance load for maximum power transfer with a minimum of external components. This eliminates the need for elaborate matching networks. The external mixer output circuitry also incorporates a network which distributes the power from the mixer output to two unequal loads. This enables the mixer output to be matched to a high impedance load such as a SAW bandpass filter (typically 1kΩ) while simultaneously providing a 50Ω test point that can be used for production diagnostics. The mixer output circuitry generates the majority of questions for those utilizing this part in their current applications, so some basic concepts regarding open-collector outputs are presented below, as well as a discussion of the network used to provide the 50Ω diagnostic point.

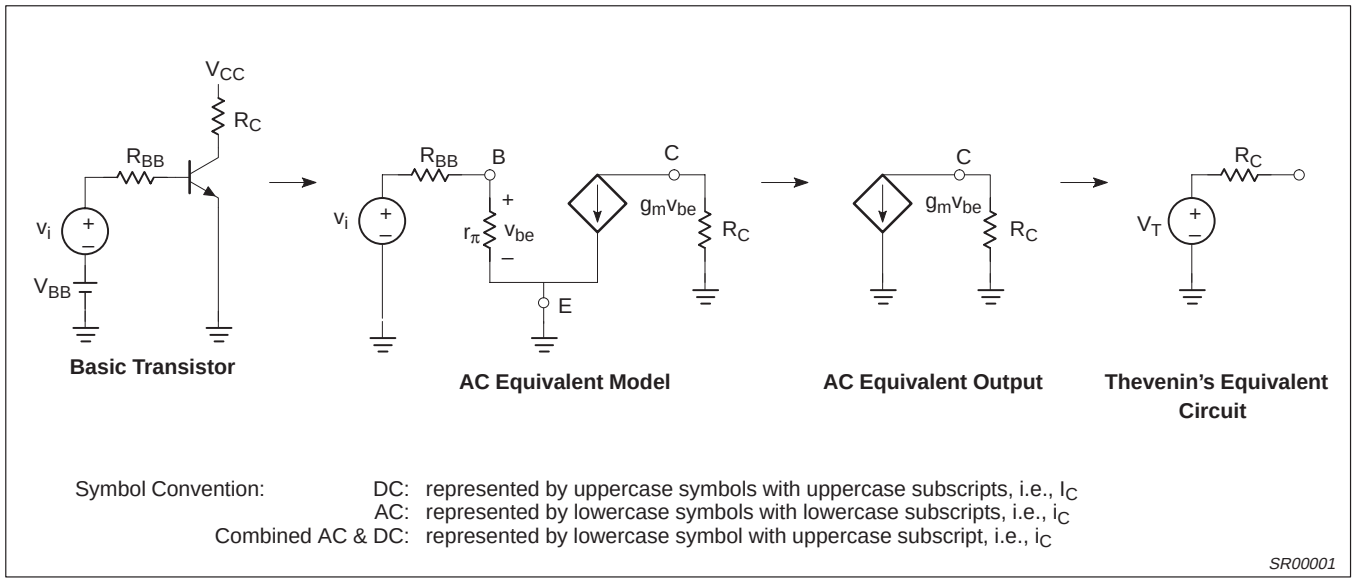


Figure 3. R_C as Source Resistor

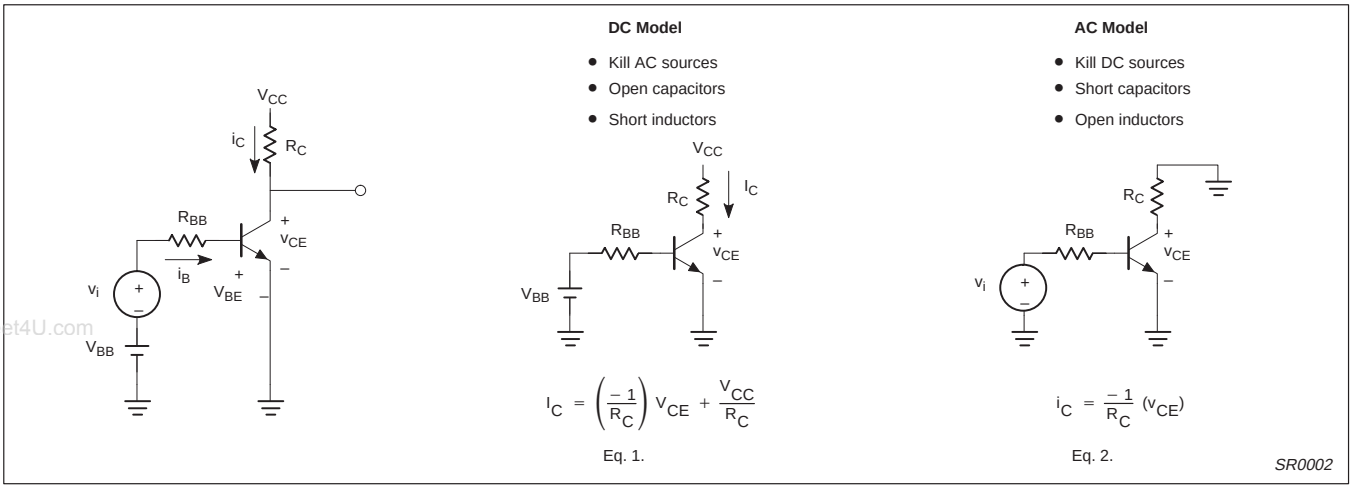


Figure 4. Basic Transistor Analysis

Open-Collector Output Basics [1, 2, 3, 6]

Why R_C Acts Like A Source Resistor

An open-collector output allows a designer the flexibility to choose the value of the R_C resistor. Choosing this resistor value not only sets the DC bias point of the device but also defines the source impedance value. Figure 3 shows the AC model of the transistor. Converting the output structure by applying a Norton and Thevenin transformation, one can conclude that R_C becomes the source resistance. Thus, by choosing R_C to be equal to the load, maximum power transfer will then occur.

Figure 4 shows an active transistor with a collector and base resistor. From basic transistor theory Equation 1 is generated and has the same form as the general equation for a straight line

$$y = mx + b$$

The slope of the DC load line is generated by the value of the collector resistor (m = -1/Rc) and is shown in Figure 5. For a given small signal base current, the collector current is shown by the dotted curve.

The intersection of the dotted curve and the DC load line is called the Quiescent point (Q-point) or DC bias determinant. The location of the Q-point is important because it determines where the transistor is operated; in the cutoff, active, or saturation regions. In most cases, the Q-point should be in the active region because this is where the transistor acts like an amplifier.

Figure 6 shows the ac collector-emitter voltage (V_{CE}) output swing with respect to an AC collector current (i_c). Collector current is determined by the AC voltage presented to the input transistor's base (v_i) because it effects the base current (i_b) which then effects i_c. This is how the v_i is amplified and seen at the output. Recall that this is with no external load (R_{LOAD}) present at the collector. Since no load is present, the AC load line has an identical slope as the DC load line as seen in equation 1 and 2 (m = -1/Rc).

Open-Collector With R_{LOAD}

A filter with some known input impedance is a typical load for the output of the transistor. For simplicity, we will assume a resistive load (R_{LOAD}) and neglect any reactance. Since a resistive load is used (see Figure 7), the AC output swing is measured at V_{OUT} or V_{CE}.

A DC blocking capacitor is used between the R_{LOAD} and the V_{CE} output to assure that the Q-point is not influenced by R_{LOAD}. It is also necessary to avoid passing DC to the load in applications where the load is a SAW filter. However, R_{LOAD} will affect the AC load line which is seen in Equation 4 in Figure 7. Notice that the V_{CE} voltage swing is reduced and thus, the V_{OUT} signal is reduced (see Figure 8).

Since the value of R_C and R_{LOAD} affects the AC load line slope, the value chosen is important. The higher the impedance of R_{LOAD} and Rc, the greater the AC output swing will be at the output, which means more conversion gain in a mixer. This is due to the slope getting flatter, thus allowing for more output swing.

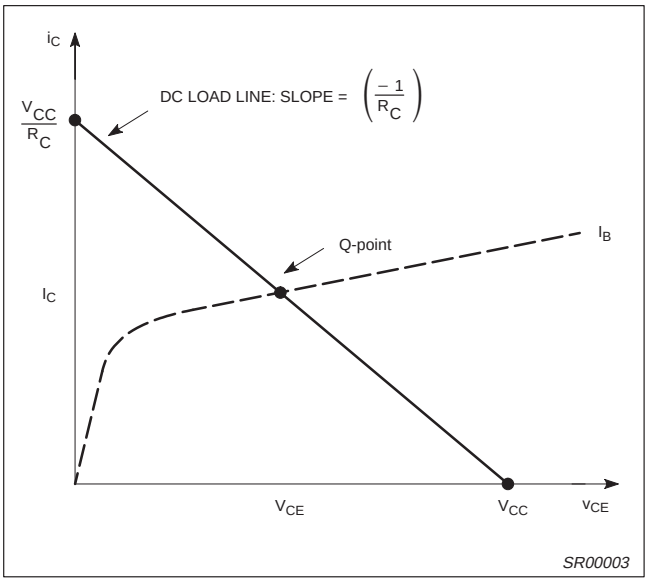


Figure 5. Load Line and Q-Point Graph

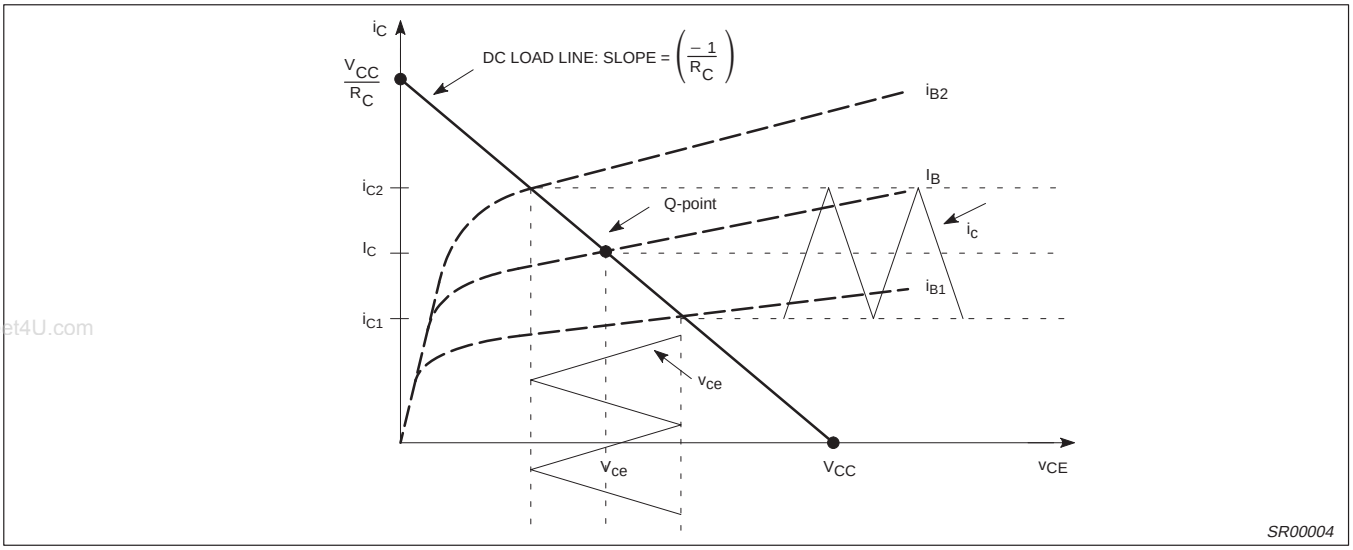


Figure 6. Graphical Analysis for the Circuitry in Figure 4

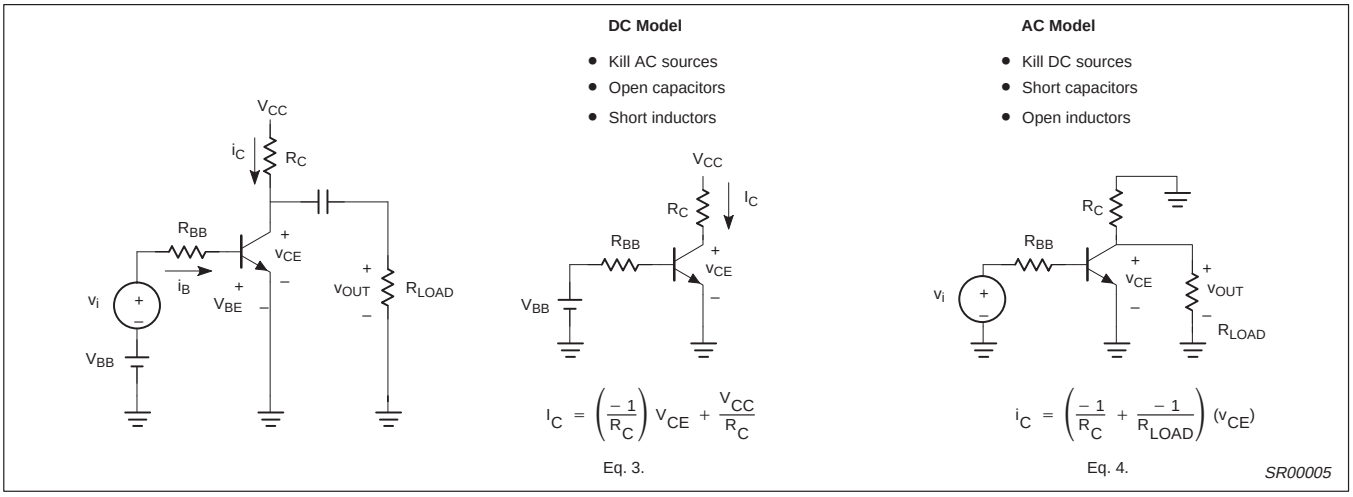


Figure 7. Basic Transistor Analysis with R_{LOAD}

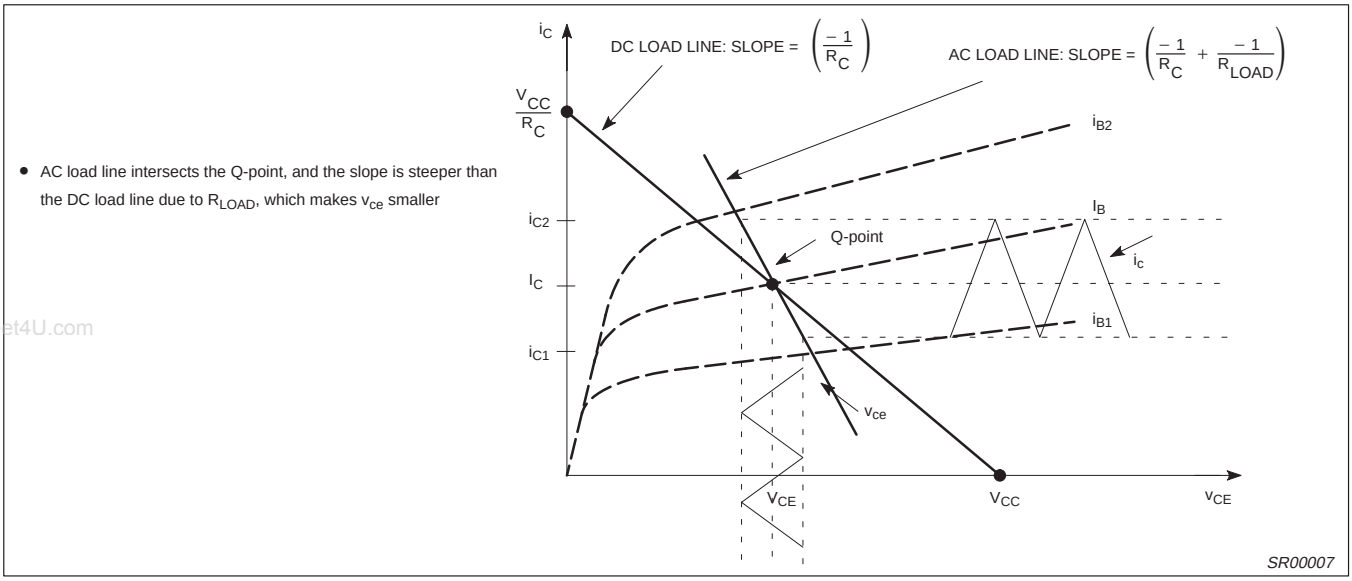


Figure 8. Graphical Analysis for the Circuitry in Figure 7

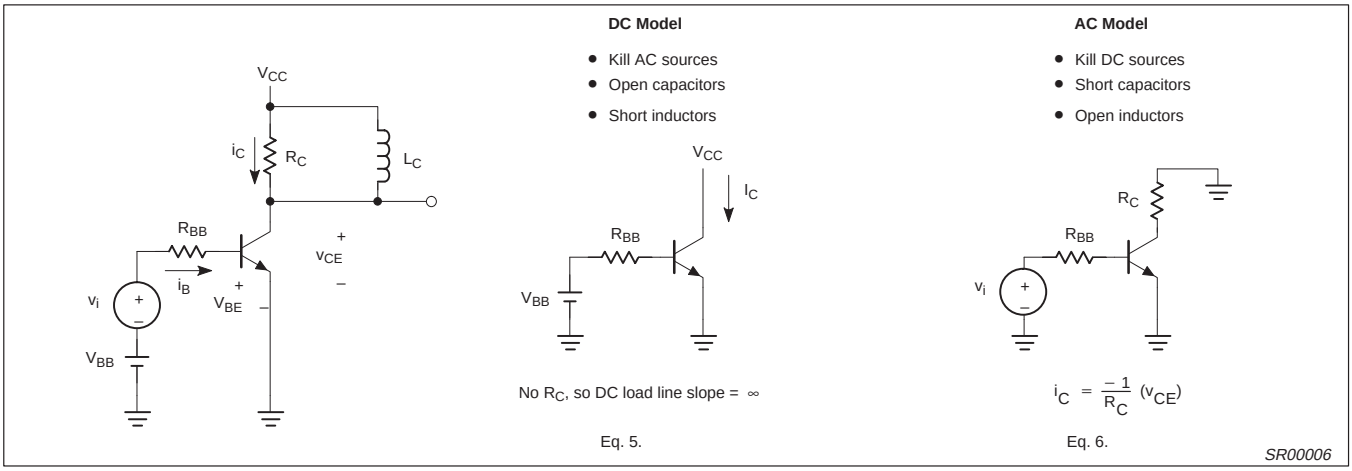


Figure 9. Basic Transistor Analysis with Inductor Added to Collector

Open-Collector With Inductor (L_C)

Adding an inductor in parallel with R_C can increase the AC output signal V_{CE}. Figure 9 shows the DC and AC analysis of this circuit configuration. In Equation 5, there is no R_C influence because the inductor acts like a short in the DC condition. This means the slope of the DC load line is infinite and causes the Q-point to be centered around V_{CC}, thus moving it to the right of the curve. The AC load line slope is set only by R_C because no load is present. Notice that it has the same AC load line slope as the first condition in Figure 4, Equation 2.

Referring to Figure 10, one might notice that the base current (AC and DC) curves spread open as V_{CE} increases. This is caused by a non-infinite early voltage (see Figure 11), which causes the collector current to be dependent on V_{CE}. Taking advantage of this non-ideal condition, the peak-to-peak AC output swing V_{CE}, can thereby be increased by moving the DC Q-point to the right due to the wider spreading between the curves corresponding to different base currents. Figure 12 combines Figures 6 and 10 to show the different AC output signals with different Q-points.

Looking at the AC output level, one might ask how the V_{CE} peak voltage can exceed the supply voltage V_{CC}. Recall that the inductor is an energy storing device (v=Ldi/dt). Therefore, total instantaneous voltage is V_{CC} plus the voltage contribution of the inductor.

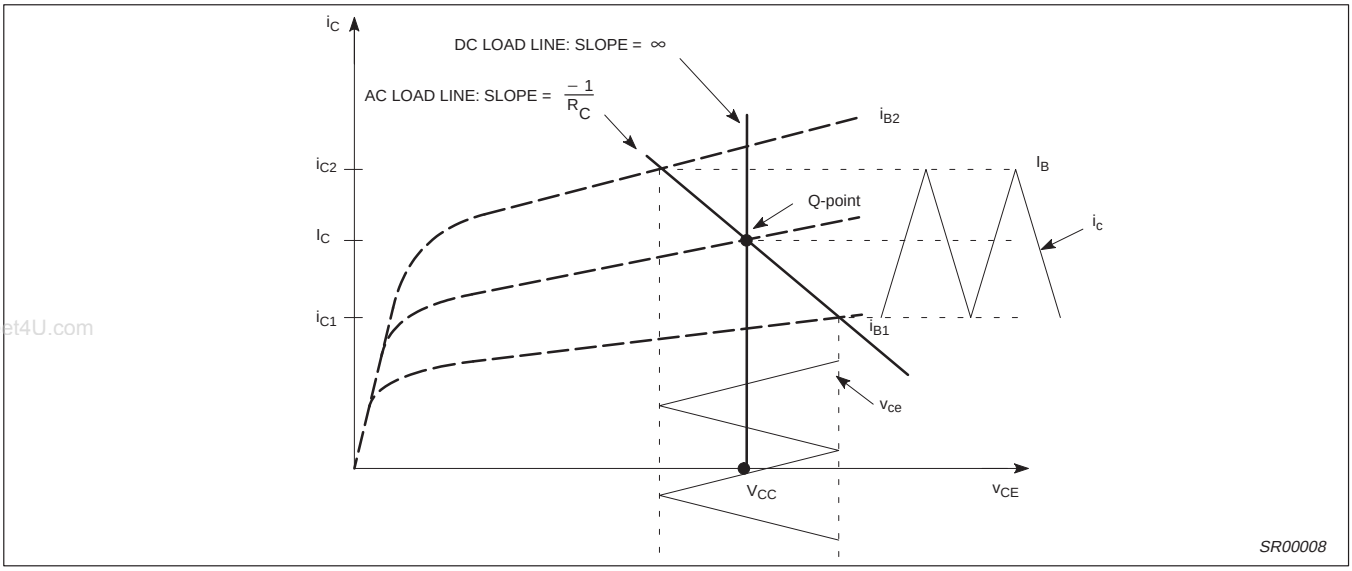


Figure 10. Graphical Analysis for the Circuitry in Figure 9

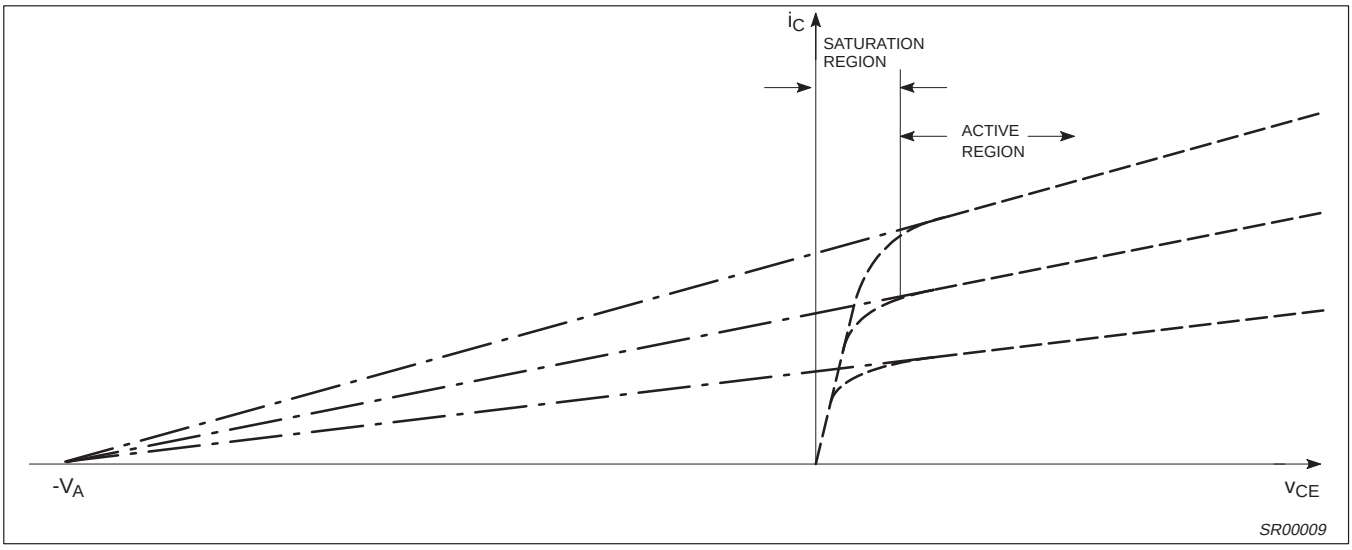


Figure 11. Graphical Representation of Early Voltage Effect

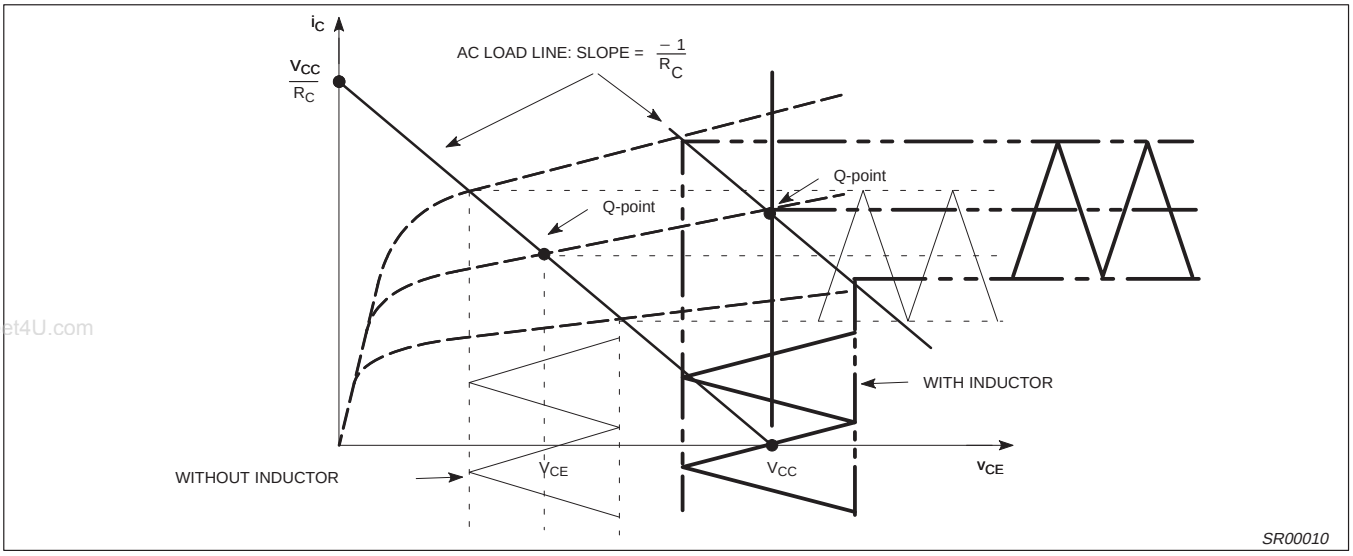


Figure 12. Comparison of Open-Collector Circuit With Inductor vs Without Inductor

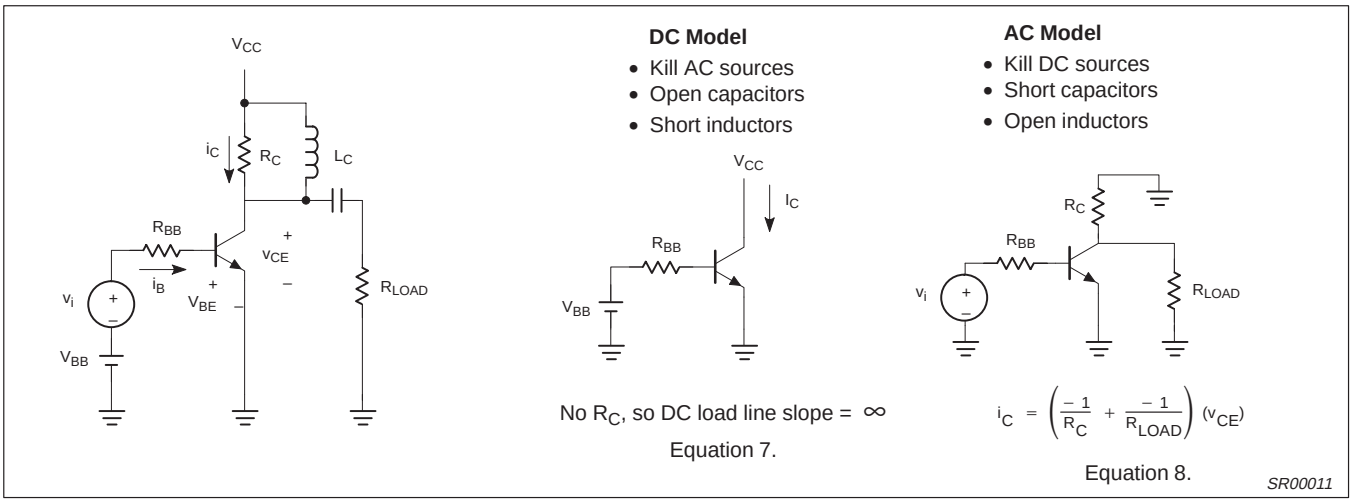


Figure 13. Basic Transistor Analysis with Inductor and R_{LOAD}

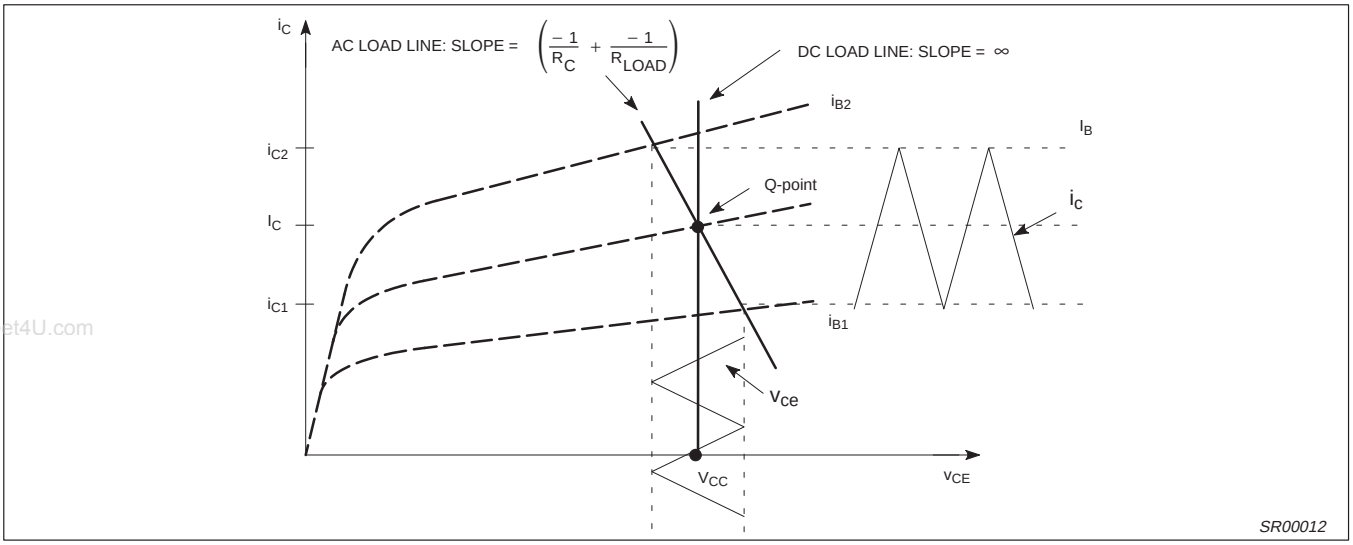


Figure 14. Graphical Analysis for the Circuitry in Figure 13

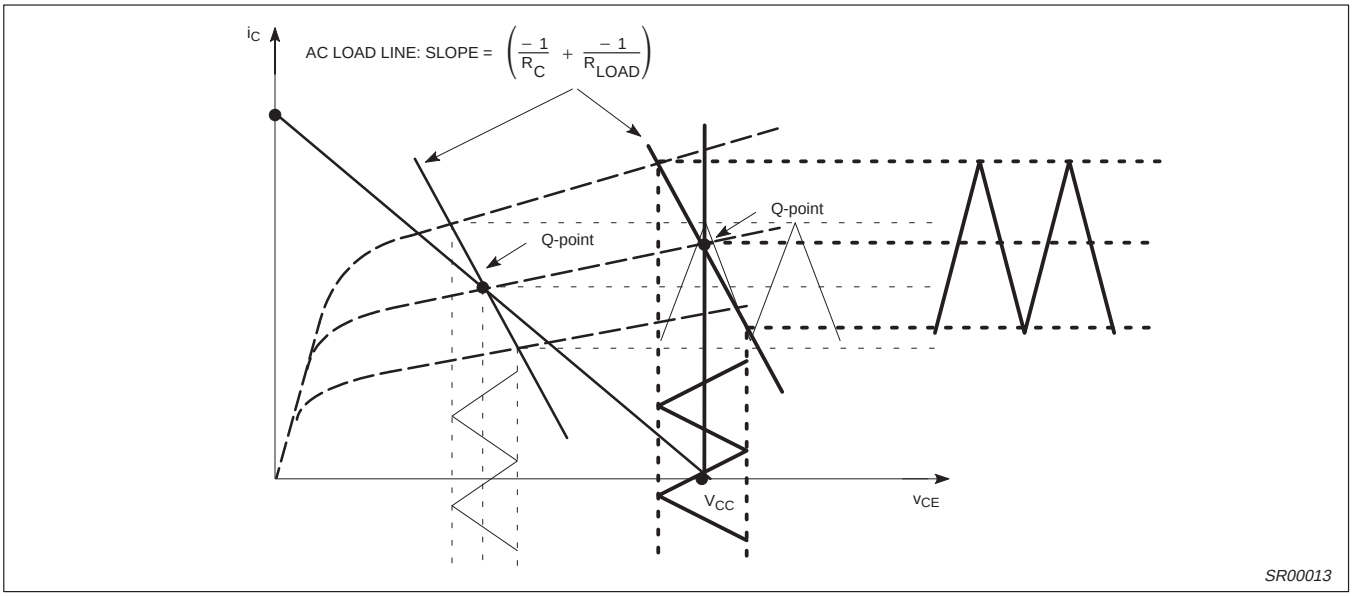


Figure 15. Comparison of Open-Collector R_{LOAD} Circuit With Inductor vs Without Inductor

Open-Collector With Inductor (L_C) and R_{LOAD}

Figure 13 shows the DC and AC analysis with the inductor and load resistor. Again, from the DC analysis, the inductor causes R_C to be non-existent so the DC load line is vertical. In the AC analysis, the AC load line slope is influenced by both R_C and R_{LOAD} resistors (see Equation 8). The AC load line slope is the same as the example of the open-collector without the inductor. Figure 14 shows the response for the open-collector with L_C and R_{LOAD}. Figure 15 combines Figures 8 and 14 showing the increase in AC output swing.

In conclusion, for the load line, R_C plays a role in setting up the bias determined Q-point as well as the AC source impedance. However, when an inductor is placed in parallel with R_C, a different Q-point is set and the AC source impedance is altered. Moving the Q-point takes advantage of the transistor's non-ideal i_c dependence on V_{CE} to get more signal output without having to change the base current. Since R_C is in parallel with R_{LOAD} in the AC condition, it influences the AC load line slope.

VI. FLEXIBLE MATCHING CIRCUIT [6]

A useful variation of the open collector matching concepts previously outlined provides the capability of delivering equal power to two unequal resistive loads. This allows the power delivered to the load to be measured indirectly at another test point in the circuit where the impedance can be arbitrarily defined. If this impedance is defined to be 50Ω, a spectrum analyzer can be easily placed directly into the circuit. This is an excellent troubleshooting technique and a valuable option to have available in high production environments.

Figure 16 shows the schematic for this flexible matching circuit. In this circuit, C_B functions only as a DC blocking capacitor and presents a negligible impedance at the frequency of interest. Recall from the previous open collector matching dicussions that, when R_C

is placed in parallel with an inductor, it has no effect on the Q-point, but does influence the slope of the AC load line as

$$\text{Slope} = \frac{-1}{R_C} + \frac{-1}{R_{LOAD}}.$$

The capacitor C_S functions not only as a DC blocking capacitor, but is also chosen such that the impedance presented by the combination of L, R_C and C_S is equal to R_{LOAD} for optimum power transfer. The analysis is done in the following manner. First, note that inductor L is connected to V_{CC} which is an effective AC ground. So, L can be redrawn to ground. Next, R_C and C_S are converted to their parallel equivalent values as shown in Figure 17.

The resulting parallel LCR circuit is shown in Figure 18. At resonance, the parallel L, C_P combination will be an effective open circuit leaving only R_P. R_P is then simply chosen to be equal to R_{LOAD}.

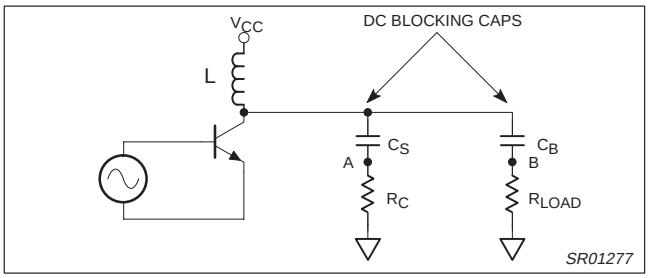


Figure 16. Flexible Matching Circuit

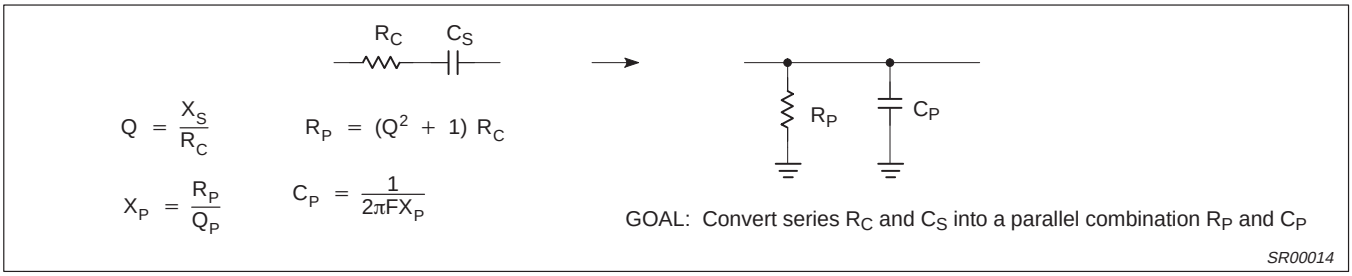


Figure 17. Converting from Series to Parallel Configuration

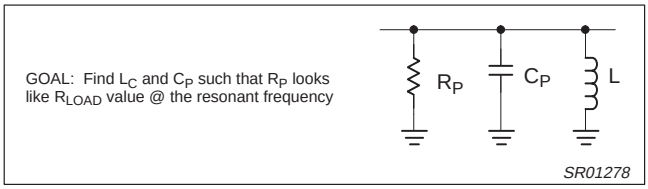


Figure 18. Converting from Series to Parallel Configuration

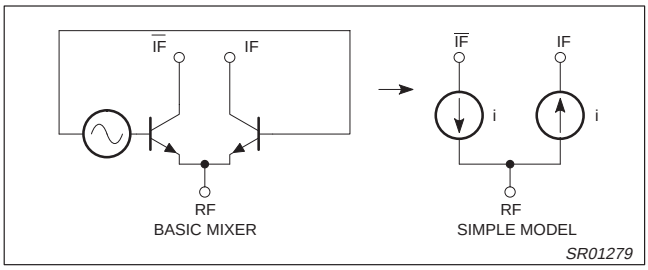


Figure 19. Circuit Model of Differential Open-Collector Output

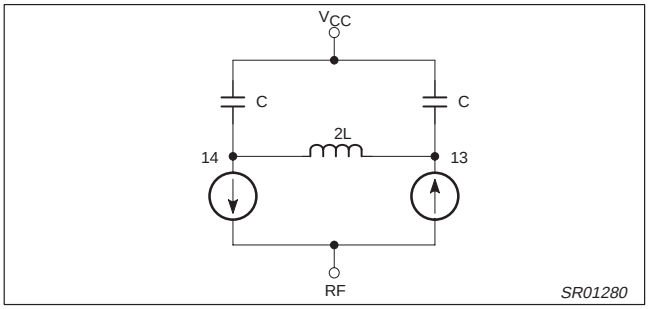


Figure 20. External current-combiner Circuit

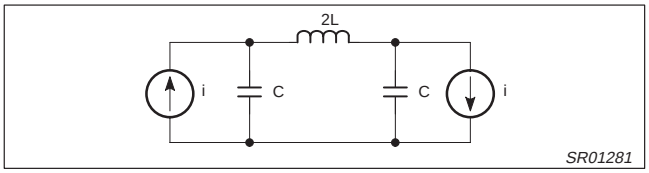


Figure 21. Ideal AC Equivalent Circuit

VII. SA601 MIXER [6]

The SA601 mixer is intended for operation with an external VCO and employs a differential output structure. The current wireless markets demand front-end solutions with low power, and high gain. The differential output offers higher gain than the conventional single-ended open-collector output without an increase in supply current. An equivalent model can be seen in Figure 19. A characteristic of the differential output is that the two output currents are 180° out of phase. This is why the mixer output is labeled IF and $\overline{IF}$.

The current-combiner circuit shown in Figure 20 consists of two capacitors and one inductor. The purpose of the current-combiner is to combine the currents such that they are in phase with one another. By aligning the currents in phase with one another, the output will have a larger AC output swing due to the increased signal current.

Figure 21 shows the ideal AC equivalent model. In the ideal case, it is assumed that all component Q's are high enough to be neglected and the output impedances of the current sources are also high enough to be neglected. By source transformation, the parallel capacitor and current source can be converted to a voltage source and a source capacitor. The inductor, 2L, can be split into two inductors where L becomes the new value (See Step 2 in Figure 22). Since two inductors of equal value in series will be twice that

value, we can split the one inductor into two series inductors each equal to L.

The series capacitor and inductor (L) at resonance will act like a short circuit. Therefore, for this analysis we can redraw the circuit, as seen in Figure 22, step 3.

In Step 4, the voltage source and series inductor (L) is converted back into a current source and parallel inductor. Source transformation, in this simple form, the values of L and C do not change. It is the value of the current and voltage source that changes.

Using Ohm's Law, i=v/z and v = i(1/jωc), while Z =jωL, the imaginary j causes the current to be negative at the resonant frequency specified in Equation 9 of Figure 22. Therefore, by switching the current's direction, the negative sign disappears and the current source is aligned in the same direction as the other one.

VIII. MATCHING THE OPEN-COLLECTOR DIFFERENTIAL OUTPUT

Figure 23 shows the current-combiner and the open-collector matching circuit. The collector current is increased and passes through the load resistor which allows for more AC output swing.

Since the SA601 has differential open-collector outputs, it is possible to implement both a current-combiner and a flexible matching circuit (see Figure 24).

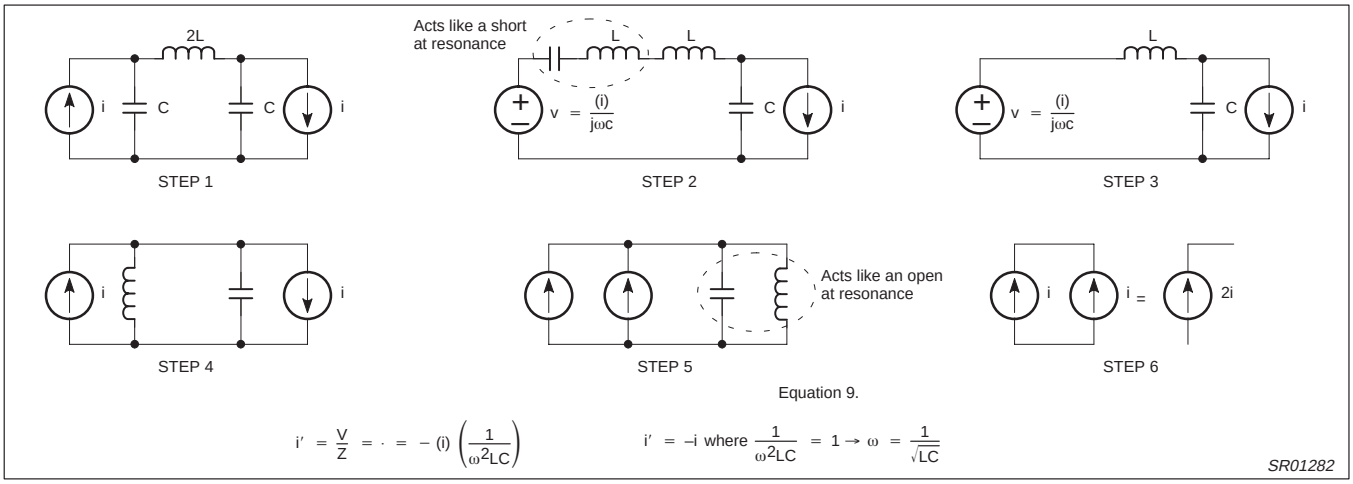


Figure 22. Equivalent Circuit Transformations at Resonance

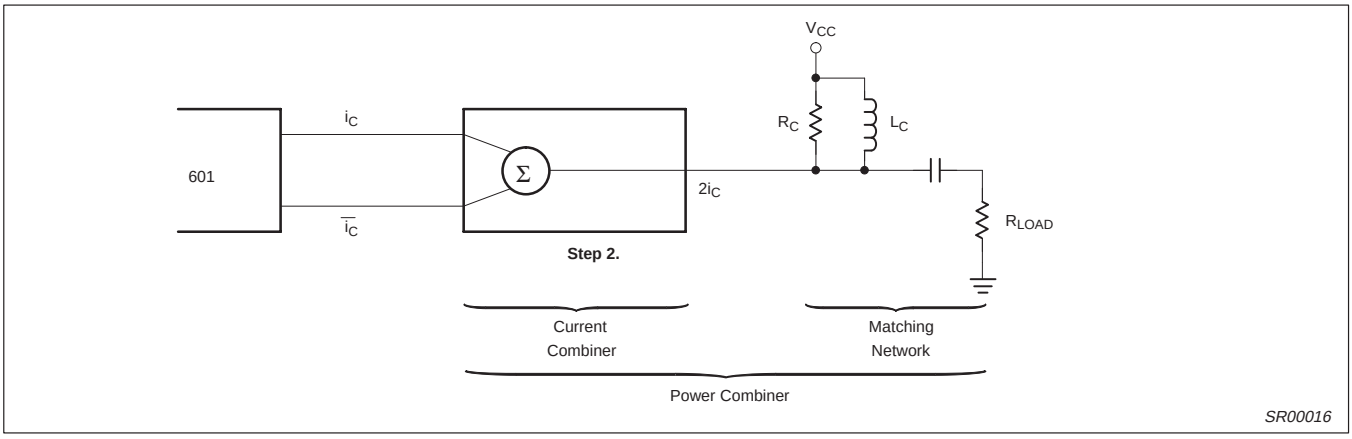


Figure 23. Power Combiner

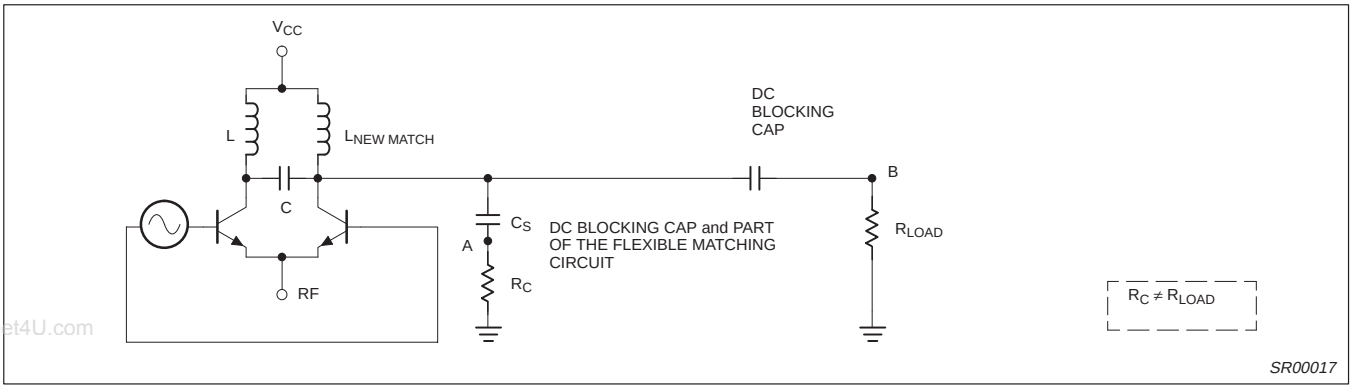


Figure 24. current-combiner with Flexible Matching Circuit

Understanding and implementing the mixer output match is most likely the biggest challenge for those using the SA601. As in most cases, there are many solutions to obtaining the required match for a given circuit. The method selected for the following examples was chosen in order to simply demonstrate some key principles involved in obtaining both high impedance and 50Ω matching while also maintaining some continuity to the previous discussions pertaining to the ideal current-combiner circuit. Each component in the current-combiner/matching circuit will be identified as well as the role each plays in obtaining the required matched condition. In addition, a general procedure for acquiring a good matching circuit along with Smith chart documentation will be provided.

The schematic of the mixer output circuitry utilized on the SA601 demo-board is reproduced here in Figure 25 for convenience.

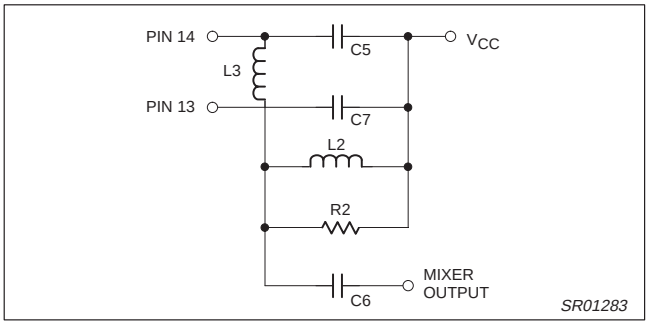


Figure 25. External Mixer Output Circuit

The following is a descriptive summary of the components comprising the external mixer output circuitry.

Inductor L_2
In order to minimize the deviation from the ideal current-combiner circuit, this inductor is chosen to be as large as possible. The inductor will then function only as a choke at the IF frequency and, therefore, should not interact with the current-combiner circuit or effect the matching conditions. This inductor is also necessary to provide the needed DC path from V_{CC} to Pins 13 and 14. In all the examples to follow, a 6.8µH inductor was used for L_2.

Capacitors C_5 and C_7
Also, in order to adhere to the analysis set forth in the ideal current-combiner discussions, these capacitors will be set equal to each other in the examples to follow. The main function of these capacitors is to define the resonant frequency of the current-combiner. They also play a secondary role in defining the output impedance.

Inductor L_3
This inductor also defines the resonant frequency of the current-combiner as well as the output impedance of the current-combiner at resonance.

Capacitor C_6
This capacitor is used to determine the output impedance for 50Ω matches only. For high impedance matches greater than or equal to 1kΩ this capacitor is not very effective. Thus, in this case it is usually replaced with a large capacitance value, adding almost no contribution to the match. A 1000pF is used in the high impedance examples that follow.

Resistor R_2
This resistor is used to simplify the high impedance matching process. In a 50Ω match, the series impedance presented by capacitor C_6 greatly simplifies the process of moving to the 50Ω point on the Smith chart. At high impedance, C_6 is no longer effective and it is often extremely difficult to obtain the proper match by varying just the components associated with the current-combiner circuit. A simple solution to this problem is to obtain the proper resonance condition at a higher impedance than the targeted impedance and then reduce it by placing a resistor of the correct value in parallel with it.

The best way to configure the mixer output circuitry for optimum gain is to optimize the return loss (S_{11}) for this port at the required IF. This, by itself, does not guarantee that optimum gain will occur at this frequency due to the phase relationships of the signals inside the current-combiner, but it is usually very close. The best tool available for this is a network analyzer.

Method of Achieving High Impedance Matching with a Network Analyzer

The network analyzer lends itself very nicely to obtaining 50Ω matches. However, for high impedance matches the Smith chart data will be far to the right of the chart and will be inaccurate, hard to read, and hard to interpret. If the network analyzer were normalized to the impedance value to which you want to match, the data would be in the center of the Smith chart and easy to interpret.

One method of doing this is to disconnect the 'A' port from an HP network analyzer and attach a high impedance probe to this port. Next take an SMA connector (or whatever connector type your analyzer uses) and solder two resistors each equal to the target impedance in the following manner: Solder one end of one of the resistors to the center lead of the connector and leave the other end open. This resistor will define the normalization on the network analyzer during calibration. Next, solder one end of the other resistor to the ground of the connector and leave the other end

open. This resistor will function as a dummy load during calibration. Connect this SMA connector to port '1' on the network analyzer. You are now ready to calibrate. Prior to initiating the open portion of the one-port calibration procedure, contact the open end of the resistor soldered to the center lead of the connector with the high impedance probe (see Figure 26). After this has been completed, contact ground on the connector with the high impedance probe prior to initiating the short portion of the one-port calibration procedure (see Figure 26). Then connect the two open ends of the resistors with solder. Prior to initiating the load portion of the one-port calibration procedure, contact the connection between the resistors with the high impedance probe (see Figure 27). The network analyzer should now be normalized to your target impedance. Thus, the optimum match will once again be in the center of the chart. When making connection to a circuit it is necessary to include a resistor of the same value used during the calibration between the center lead of the connector and its connection to the circuit. Impedance measurements are taken by contacting the high impedance probe at the end of this resistor nearest the circuit (see Figure 28).

Another tip concerning the calibration of the network analyzer should be mentioned. It is often useful to be able to look at a Smith chart over more than one frequency range. A wide frequency range is useful initially when your results are far off the target. Then the narrower range is useful for fine tuning your results. So, it is recommended that you calibrate in both frequency ranges and save the settings in the internal registers of the network analyzer if possible.

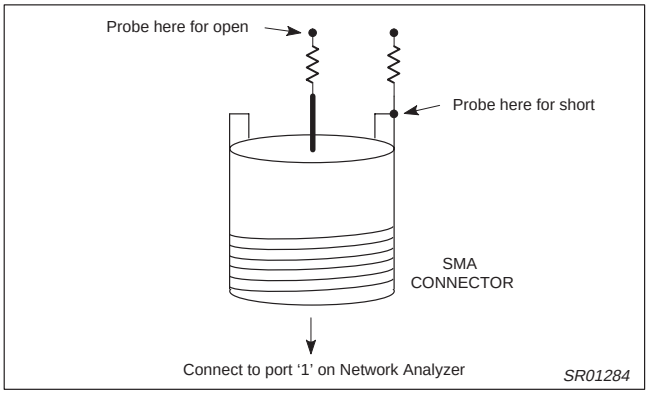


Figure 26. Open- and Short-circuit Calibration Locations

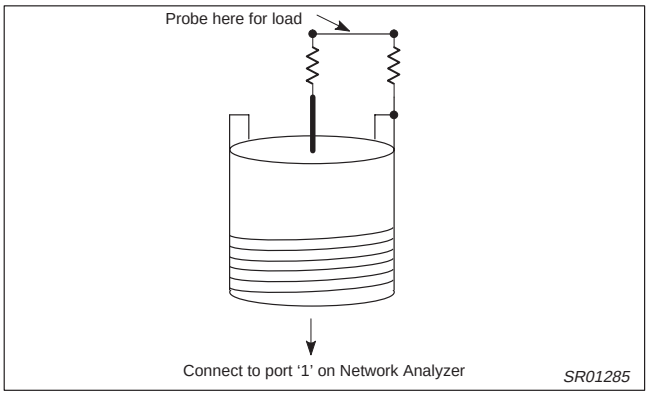


Figure 27. Load Impedance Calibration Location

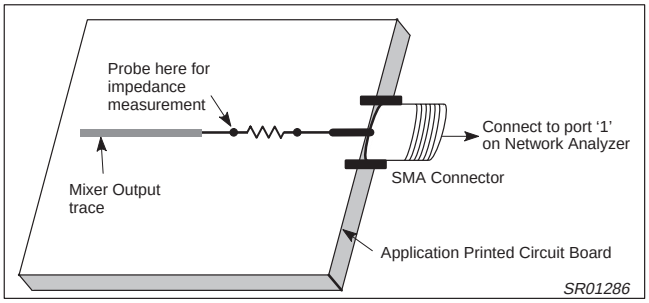


Figure 28. PCB Impedance Measurement Configuration

Non-Ideal Current-Combiner Ckt Considerations

Before we go through some actual impedance matching examples, some key differences between the ideal current-combiner circuit presented earlier and a non-ideal circuit which takes into account the finite Q of inductor L_3 as well as the output impedances of the current sources should be discussed. Through a series of Thevenin/Norton conversions and Series/Parallel equivalent impedance conversions similar to the analysis of the ideal circuit, the mixer output circuit can be modeled by the circuit shown in Figure 29.

The two main things to note in this circuit are the presence of the shunt resistors, R_O and R_Q, and that the current-combiner circuit looks like a simple parallel LRC circuit to capacitor C_6.

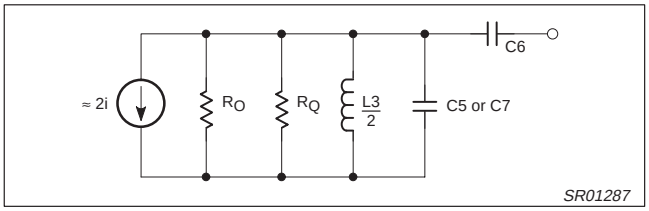


Figure 29. Non-ideal Mixer Output Equivalent Circuit

The significance of the resistors is their role in determining the output impedance of the overall circuit. R_Q is smaller in value than R_O which is the relatively high impedance of the open-collector outputs. Thus, because they are in parallel, R_Q defines the output impedance of the current-combiner circuit at resonance. The value of R_Q is a function of frequency, the component Q of inductor L_3, and the inductance value of inductor L_3. We do not have direct control over component Q or frequency, so the value of R_Q is adjusted by simply changing the value of inductor L_3. A more detailed explanation of this will be shown in the examples to follow.

It is not intuitively obvious why the matching portion of the mixer output circuitry used to obtain the 50Ω matches is composed of a single series capacitance. Many customers using the SA601 have asked why this works because it does not seem to adhere to basic two element matching concepts. To answer this, let's first take a quick look at the general parallel LC circuit shown in Figure 30. This circuit will resonate according to the simple resonance calculation

$$\omega = \frac{1}{\sqrt{LC}}$$

If the capacitor of this circuit is cut in half and the inductor is equivalently represented by two parallel inductors, the circuit in Figure 31 results. At the original resonant frequency $\omega = \frac{1}{\sqrt{LC}}$, the capacitor and one of the inductors will resonate $\omega = [(0.5C)\ (2L)]^{-\frac{1}{2}} = (LC)^{-\frac{1}{2}}$. What is left over is a shunt inductance of 2L presented to the output. Thus, the general

principle is that by decreasing the capacitance of a parallel LC circuit, you will present a shunt inductance to the output of that circuit at the same frequency. This concept when applied to the circuit in Figure 29 offers an explanation of where the missing shunt inductance element is coming from. If capacitors C_5 and C_7 are decreased, this will present a shunt inductance to capacitor C_6. Thus, two element matching concepts would still apply to this circuit. How much inductance is referred to C_6, and what value of C_6 it takes to obtain the matching conditions, is difficult to predict. So, we will rely on the network analyzer to point us in the right direction.

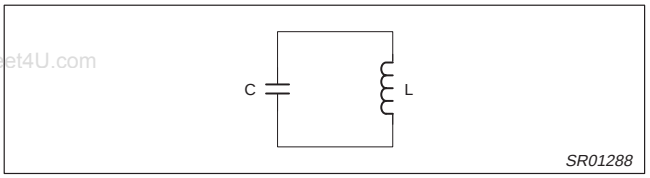


Figure 30. Parallel L_C Network

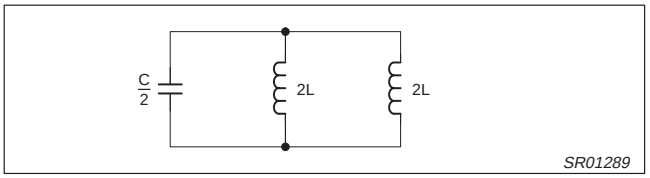


Figure 31. Parallel L_C Network with Decreased Capacitance

One of the most frustrating parts of matching on the network analyzer is it often does not give you very much information until you are at least “in the ball park” of the component values required. The first example will purposely begin with component values to create this condition to give an idea of what might initially be encountered. Additionally, Table 4 at the end of this section contains values for the components required to obtain optimum gain from the mixer at IF frequencies of 45, 83 and 110MHz at both a high impedance of 1kΩ and a low impedance of 50Ω. Using this table you should be able to obtain a good guess for the initial values for your particular application.

IX. MATCHING EXAMPLES

A procedure for acquiring a good high impedance matching circuit for providing optimum gain from the mixer output can be summarized as follows:

1. Normalize the network analyzer to the impedance of interest.
2. Set inductor L_2 to be a large inductance value.
3. Choose “ball park” values for the initial component values based on the simple resonance calculation and /or the tabulated data provided in Table 4.
4. Adjust $C_{5,7}$ to obtain the required match.
5. If the output impedance at resonance is above its target and resonance occurs at the targeted IF, the required match can be obtained with the appropriate value for R_2.
6. If the resonant frequency is above the target IF and the output impedance at resonance is below its target, change inductor L_3 to a higher value and return to step 4.
7. If the resonant frequency is below the target IF and the output impedance at resonance is above its target, change inductor L_3 to a lower value and return to step 4.
8. Design a matching circuit to bring the impedance back down to 50Ω.
9. Make final fine tuning adjustments to $C_{5,7}$ based on the frequency response as observed on a spectrum analyzer.

A procedure for acquiring a good 50Ω impedance matching circuit for providing optimum gain from the mixer output can be summarized as follows:

1. Set inductor L_2 to be a large inductance value.
2. Choose “ball park” values for the initial component values based on the simple resonance calculation and/or the tabulated data provided.
3. If the output impedance at resonance is greater than its target, increase capacitor C_6 until the curve on the Smith chart passes through the center of the chart.
4. If the output impedance at resonance is less than its target, decrease capacitor C_6 until the curve on the Smith chart passes through the center of the chart.
5. If the resonant frequency is greater than the target IF, increase the values of C_5 and C_6 until resonance occurs at the target IF.
6. If the resonant frequency is less than the target IF, decrease the values of C_5 and C_6 until resonance occurs at the target IF.
7. Make final fine tuning adjustments to $C_{5,7}$ based on the frequency response as observed on a spectrum analyzer.

83MHz, 1 kΩ Match

The objective of the first matching circuit we will look at is intended to provide a 1kΩ match at 83MHz. It has inductance values L_2 = 6.8μH and L_3 = 270nH. (These will be the values for these inductors in all the examples unless stated otherwise.) This match is a high impedance 1kΩ match so capacitance C_6 was set to 1000 pF. The simple resonant calculation

$$\omega = [(0.5CL)]^{-\frac{1}{2}} = [(0.5)\ (270nH)\ (C)]^{-\frac{1}{2}} = 2\pi\ (83MHz)$$

suggests that $C_{5,7}$ should be approximately 27pF. The actual value needed to optimize the gain is always less than the value predicted by this equation. Figure 32 shows what an unfavorable Smith Chart might look like when you go in the wrong direction. In this example $C_{5,7}$ was set to 33pF. The chart shows resonance does not occur anywhere between 75 and 95MHz. If you were to continue this curve, it would eventually hit the real axis at a much lower frequency. According to the simple resonance calculation this suggests that our capacitance value is too large. As $C_{5,7}$ is decreased, the plot on the Smith chart starts to resemble a constant admittance circle. Figure 33 shows that a $C_{5,7}$ value of 23pF yields a more favorable curve where resonance occurs at 83MHz as desired. The only problem is the impedance at resonance is not 1kΩ as desired. The Smith chart in Figure 33 has been normalized to 1kΩ. The real part coordinate of 61.984Ω. shown on the Smith chart must be converted in the following manner:

Z_O = (61.984/50) (1kΩ) = 1.24kΩ.

We could at this point choose another value for inductor L_3 and then again find the right value for $C_{5,7}$ to acquire resonance. However, we will take this opportunity to demonstrate how resistor R_2 might be used. The needed shunt resistance R_2 can be calculated from the simple formula for combining parallel resistances.

$$R_2 = \frac{(Z_O)\ (Z_{TARGET})}{(Z_O - Z_{TARGET})} = \frac{(1.24)\ (1)}{(1.24 - 1)} = 5.17k\Omega$$

Figures 34 and 35 show the resulting output match when a 5kΩ resistor is used for R_2.

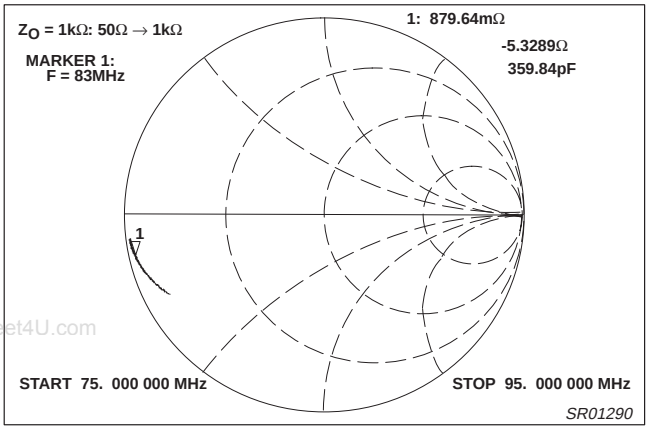


Figure 32. Smith Chart S_{11}: Showing Poor Initial Conditions

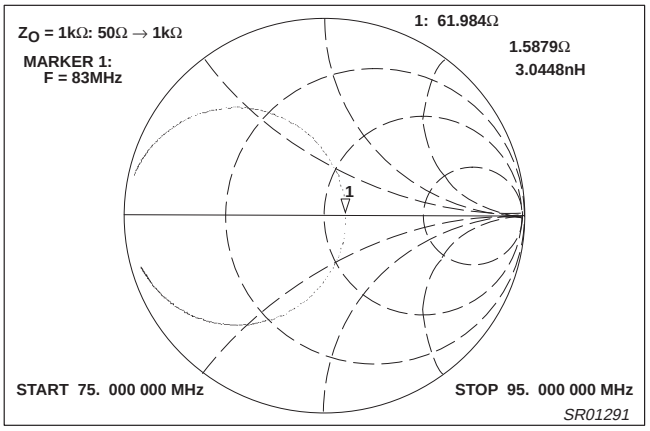


Figure 33. Smith Chart S_{11}: Showing Targeted Resonant Frequency, But Output Impedance Is Too High

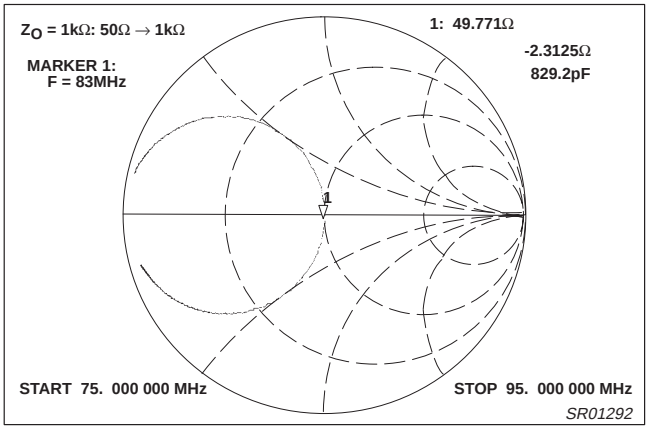


Figure 34. Smith Chart S_{11}: Showing Targeted Resonant Frequency And Output Impedance

In order to verify the high impedance match in the absence of a system in which to test it, a wideband matching circuit was designed to convert the high impedance 1kΩ match back down to 50Ω where it can then be terminated into a standard 50Ω test equipment port. Figures 36, 37 and 38 show the design of such a circuit. A detailed discussion of the design of this type of circuit can be found in [1]. Figure 39 shows the frequency response of the mixer output as the LO was varied to change the IF output. The envelope of this response has been added for clarity. The RF input signal to the mixer was -30dBm. So, the plot shows a very favorable gain of approximately 10.6dB at 81.75MHz. At 83MHz, which is the intended IF, the gain is only about 1dB lower.

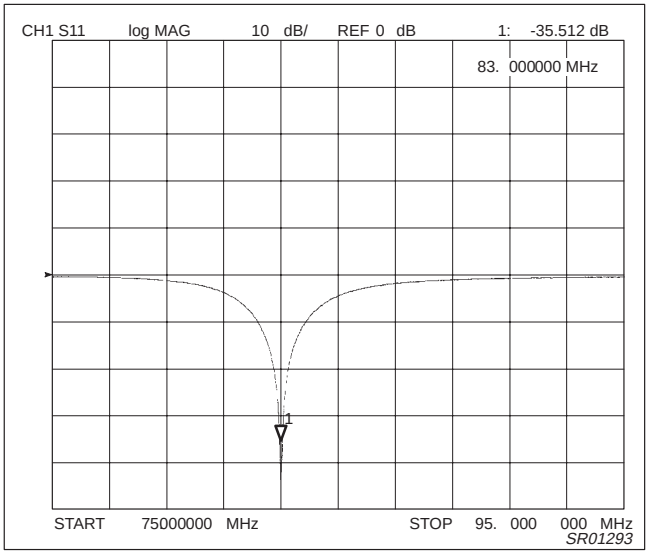


Figure 35. S_{11} Reflection at Mixer Output

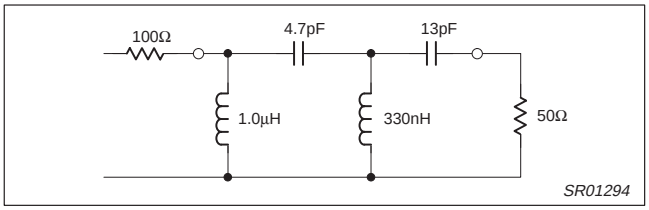


Figure 36. Wideband 1kΩ to 50Ω Matching Network

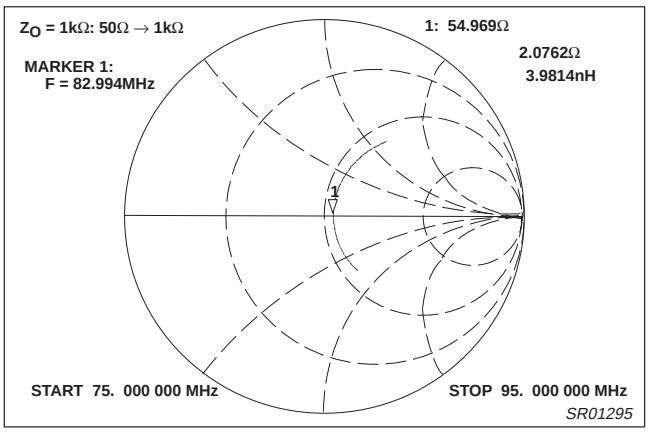


Figure 37. Smith Chart S_{11}: Showing Wideband Matching of Circuit in Figure 36

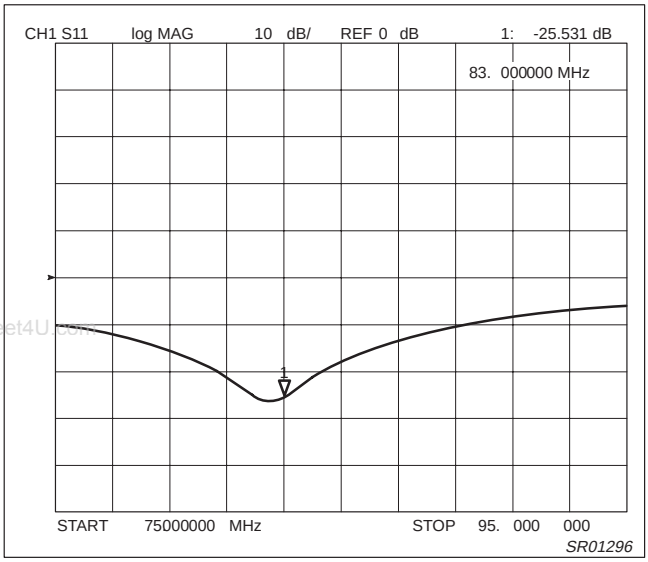


Figure 38. Smith Chart S_{11}: Showing Wideband Matching of Circuit in Figure 36

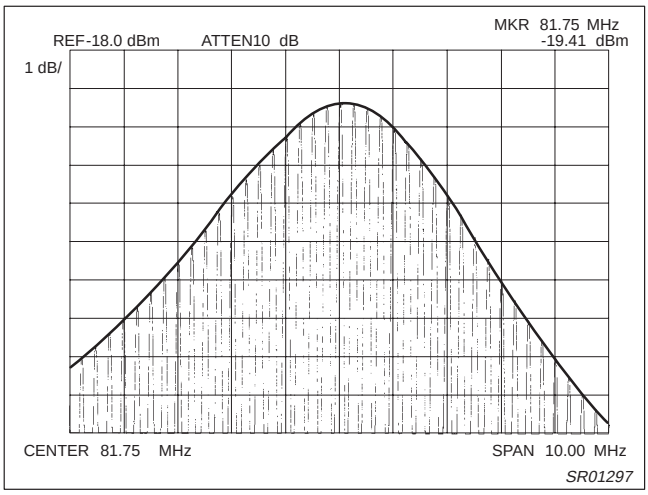


Figure 39. Showing the Frequency Response of the Mixer Output

45MHz, 1 kΩ Match

The next example is designed to show how to determine when inductor L3 is too low or too high to enable you to acquire the proper matching conditions. The objective is to provide a 1kΩ match at the much lower IF of 45MHz. Before we can determine if we have the wrong inductance value for L_3, we must first understand what effect adjusting C_5 and C_7 has on the circuit. The simple resonance calculation suggests that a decrease in $C_{5,7}$ should increase the frequency at which resonance occurs. This also causes a change in the output impedance at resonance. When $C_{5,7}$ is decreased the output impedance at the new higher resonant frequency will also be higher. As $C_{5,7}$ is adjusted the resonant frequency and the output impedance at resonance will change in the same direction. In other words, both will increase as $C_{5,7}$ is decreased or both will decrease as $C_{5,7}$ is increased. This means that if a condition exists where the resonant frequency is greater than the target IF and the impedance at resonance is below its target, the inductance value used for inductor L_3 is too small. Conversely, if the resonant frequency is less than the target IF and the impedance at resonance is greater than its target, the inductance value used for L_3 is too large.

To demonstrate these concepts, inductor L_3 was chosen to be larger than usual (L_3 = 750nH) and $C_{5,7}$ was also chosen to be much larger than usual ($C_{5,7}$ = 82pF). Capacitor C_6 was again set to 1000pF making it negligible during high impedance matching. Again, it should be noted that the following Smith charts have been normalized to 1kΩ. Figure 40 shows that the component values listed above yield a 1kΩ output impedance at a resonant frequency of just 28MHz instead of the 45MHz target IF. In an effort to increase the resonant frequency $C_{5,7}$ was decreased to 33pF. Figure 41 shows that the resonant frequency is close but below the target IF and the impedance is well above 1kΩ. According to the discussions above, this suggests that inductor L3 is too large. Figure 42 shows the results when inductor L3 is decreased to 620nH. This chart shows that both the resonant frequency and the impedance at resonance are greater than their targeted values. This indicates that there is still a chance that the match can be made with some further adjustment of $C_{5,7}$. $C_{5,7}$ was increased to 39pF to lower the resonant frequency. Figure 43 shows that when this was done the condition that suggests that inductor L_3 is too large still exists.

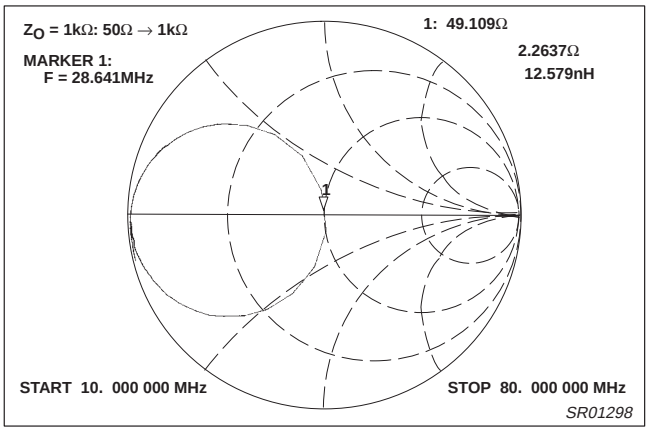


Figure 40. Smith Chart S_{11}: Showing Resonant Frequency Well Below 45MHz Target

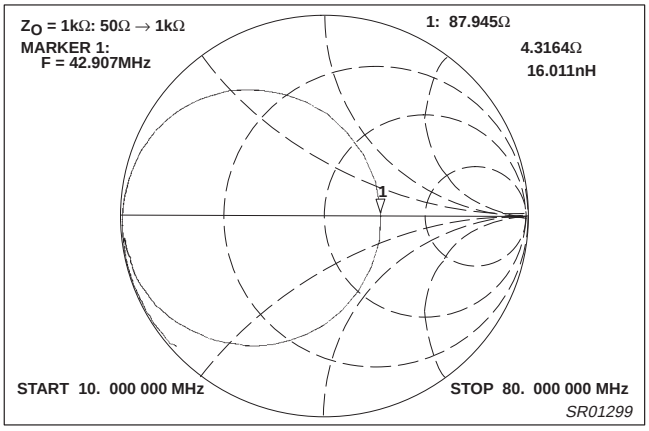


Figure 41. Smith Chart S_{11}: Showing Output Impedance Well Above the 1kΩ Target

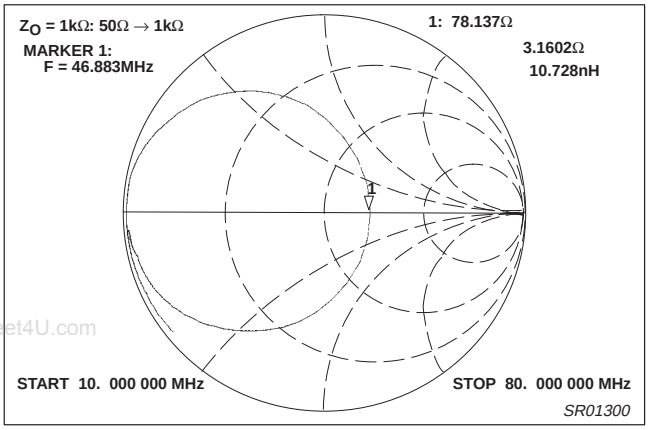


Figure 42. Smith Chart S_{11} , L_3 = 620nH: Showing the Resonant Frequency and the Output Impedance are Both Above the 45MHz, 1kΩ Target Values

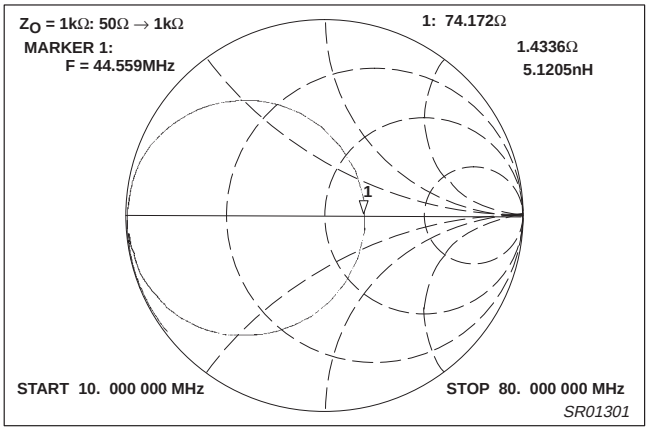


Figure 43. Smith Chart S_{11} , L_3 = 620nH: Showing the Resonant Frequency Below 45MHz Target and Output Impedance Above 1kΩ Target Values

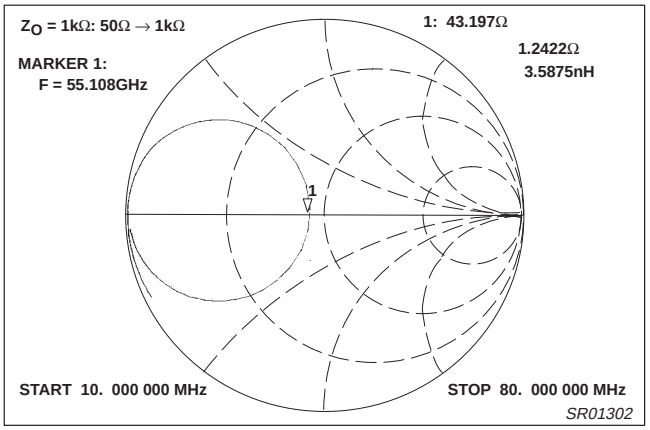


Figure 44. Smith Chart S_{11} , L_3 = 270nH: Showing the Resonant Frequency Above 45MHz Target and the Output Impedance Less than 1kΩ Target Values

Next, in order to demonstrate the other condition, inductance L_3 was changed to 270nH and $C_{5,7}$ was changed to 56pF. Figure 44 shows that the resonant frequency is greater than the target IF and the output impedance at resonance is less than 1kΩ. According to the discussions above, this is the condition which suggests that inductance L_3 is too small. So, inductance L_3 was then increased to 390nH. Figure 45 shows that the 390nH inductance yields a resonant frequency and an output impedance at resonance that are both slightly above their targets. At this point you are close enough to use another wideband matching circuit for dropping the 1kΩ impedance to 50Ω allowing you to check the frequency response directly. It was determined that changing $C_{5,7}$ from 56pF to 62pF yielded optimum gain at exactly the target IF. Figure 46 shows this gain to be approximately 10dB.

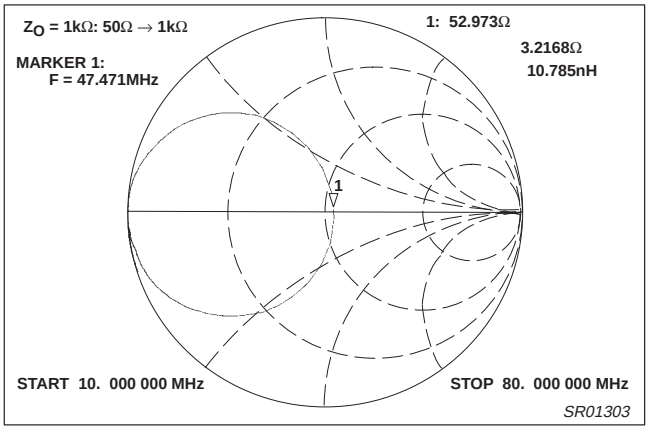


Figure 45. Smith Chart S_{11} , L_3 = 390nH

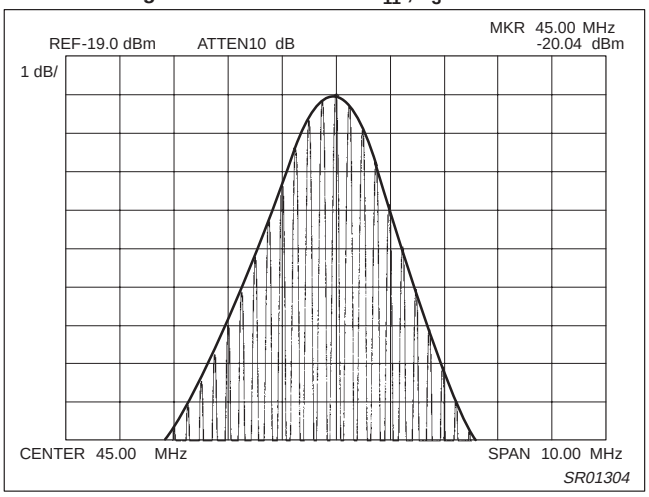


Figure 46. Frequency Response of the Mixer Output

110.592MHz, 50Ω Match

The next example will demonstrate how to obtain a 50Ω match. There are a couple of things to note concerning matching at a higher IF. The first is to expect an increase in the general sensitivity of the matching conditions with relatively small component variations. Secondly, the difference in frequency between the point of optimum gain and the point where the return loss (S_{11}) is minimized greatly increases when matching at a higher IF. To demonstrate these things the objective of the following example will be to provide a 50Ω match at 110.592MHz, which is a relatively high 1st IF.

The initial component values for this matching circuit (see Figure 25 are 6.8uH and 270nH for inductances L_2 and L_3, respectively. Capacitors C_5, C_6 and C_7 were all set to 10pF. It should be noted that C_6 is no longer set at 1000pF and plays a major role in determining the required match at 50Ω as we will see. Figure 47 shows the results of the initial component values. The Smith chart indicates that the resonance frequency is much too low and the impedance at resonance is too high. In our previous high

impedance matching discussions this meant that the inductor L_3 was too Large. In 50Ω matching this is no longer the case. Due to the lower impedance matching condition, the output impedance at resonance can now be significantly altered by varying the series capacitance element C_6. As mentioned previously, the matching circuit is much more sensitive to component variations at a higher IF. Figure 48 shows a small change in $C_{5,7}$ from 10pF to 4.7pF caused the resonant frequency to shift from well above the target IF to well below the target IF with very little change in the output impedance at resonance.

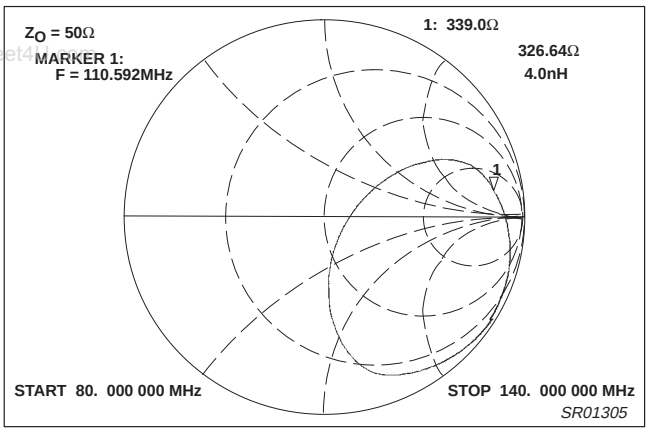


Figure 47. Smith Chart S_{11}: Showing Initial Component Results

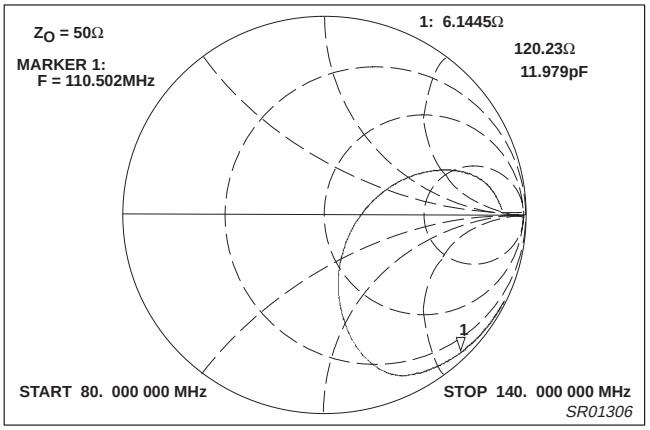


Figure 48. Smith Chart S_{11}: Showing Sensitivity to Small Changes in $C_{5,7}$

These observations suggest a general method of attack for obtaining the output impedance at 50Ω. When the series capacitance element C_6 is increased/decreased it will cause the somewhat circular curve on the Smith chart to increase/decrease in diameter. An effective method for obtaining the required match would be to adjust C_6 such that this curve passes through the center of the Smith chart and then make the necessary adjustments to $C_{5,7}$ to set the resonant frequency at the target IF. Looking at Figure 48 again, we see that the output impedance at resonance is too high. We should be able to decrease this by increasing the series capacitance element C6. In addition, from Figures 47 and 48 we know that the correct value for $C_{5,7}$ to obtain resonance at 110.592MHz is between 4.7pF and 10pF. So, we will increase C_6 to 12pF and set $C_{5,7}$ to 6pF and see what happens. Figure 49 shows the output impedance at resonance is very close to the target but the resonant frequency is still a bit too high. Figures 50 and 51 show that by adding 1pF to $C_{5,7}$ the required match is obtained. An additional matching network is not needed to evaluate the circuit because we are already at 50Ω.

In previous discussions, it was mentioned that the frequency at which the return loss is obtained does not guarantee optimum gain at this same frequency due to the phase relationships of the signals within the current-combiner circuitry. Figure 52 shows that approximately 12dB of gain is obtained but at a frequency of 115MHz, which is approximately 5MHz away from the targeted IF. To correct this we simply adjusted $C_{5,7}$ to 8.5pF to obtain a similar condition 5MHz lower than the previous result as shown in Figures 53, 54 and 55.

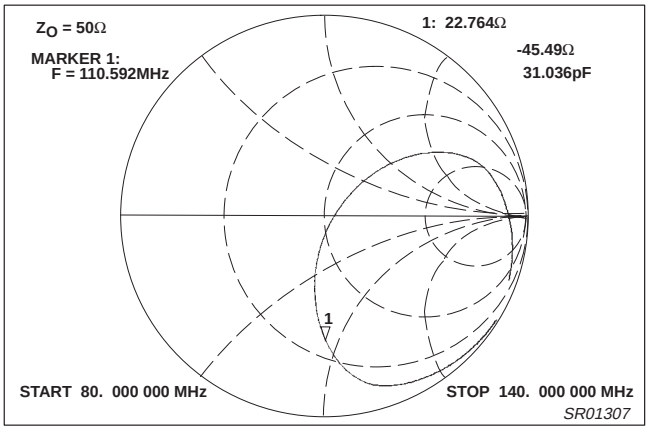


Figure 49. Smith Chart S_{11}: Showing Results of Adjustment to Capacitor $C_{5, 6, 7}$

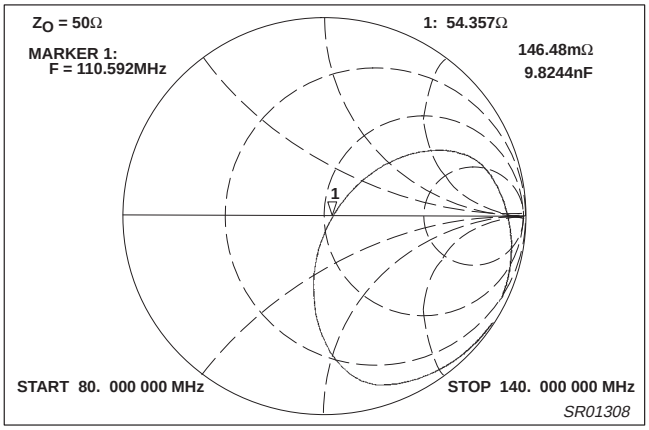


Figure 50. Smith Chart S_{11}: Showing Final 110.592MHz, 50Ω Results

Table 4. Mixer Output Component Values

	50Ω Match			1kΩ Match		
	MHz			MHz		
	45	83	110	45	83	110
L_1	6.8µH			6.8µH		
L_3	270nH			390nH	270nH	
$C_{3,7}$	80pF	18pF	8.5pF	62pF	22pF	10pF
C_6	22pF	15pF	12pF	1000pF		
R_2	— — — — —			—	5k	—

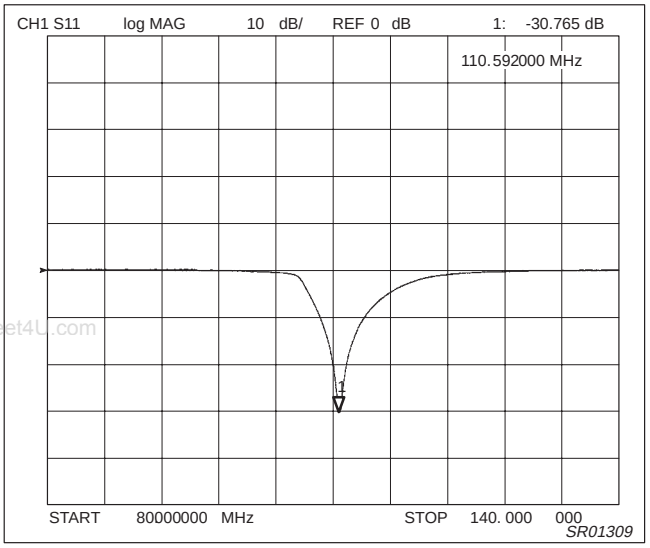


Figure 51. Final 110.592MHz, 50Ω Results

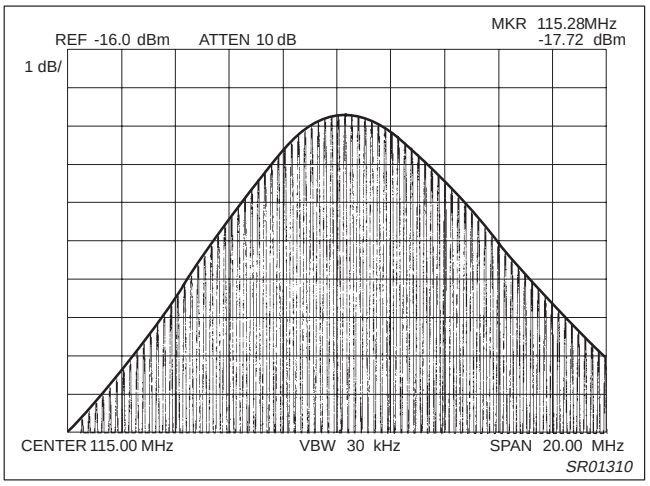


Figure 52. Mixer Output Freq. Resp. Peak is 5MHz Too High

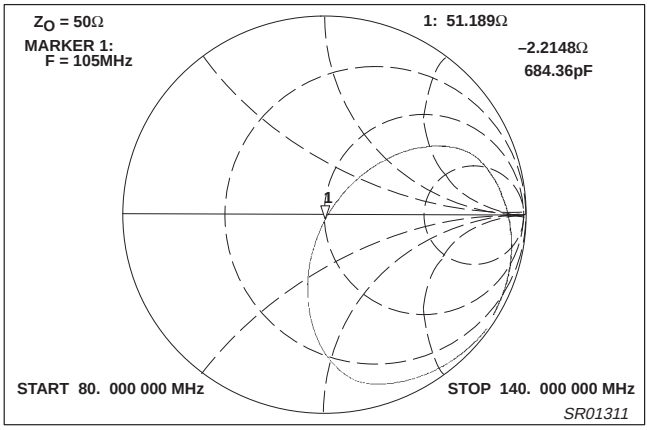


Figure 53. Smith Chart S_{11}: Showing Match With $C_{5,7}$ = 8.5pF

SA601 $IP3_{IN}$ Considerations

It should be noted that it is often necessary to give up some mixer gain of the device in order to obtain acceptable IP3in performance. The previous examples and procedures demonstrated how to optimize the gain. To meet the IP3in specifications of your particular application, it may be necessary to make some changes. The demoboard schematic for the SA601 in Figure 67 shows these changes. One difference between the previous discussions and this schematic is that C_5 and C_7 are not of equal value. It has been found that loading the differential output in an asymmetrical fashion by making C_5 less than C_7 is beneficial to $IP3_{IN}$ performance. So, your frequency adjustments would then be made by keeping C_7 constant and varying C_5. Also, inductor L_2 can no longer be chosen arbitrarily large. It must be chosen such that a high impedance parallel resonance condition occurs with C_7 at the frequency of interest. Resistance R_2 can then be used to obtain the required high impedance match. C_6 is used to acquire the 50Ω match exactly as before. The IP3in and gain performance for this configuration at 83MHz is shown in Figures 56 and 57. Notice the gain is approximately 8dB which is approximately 2dB less than that obtained in the previous examples. This was the trade-off for obtaining the better $IP3_{IN}$ performance (see Figure 57).

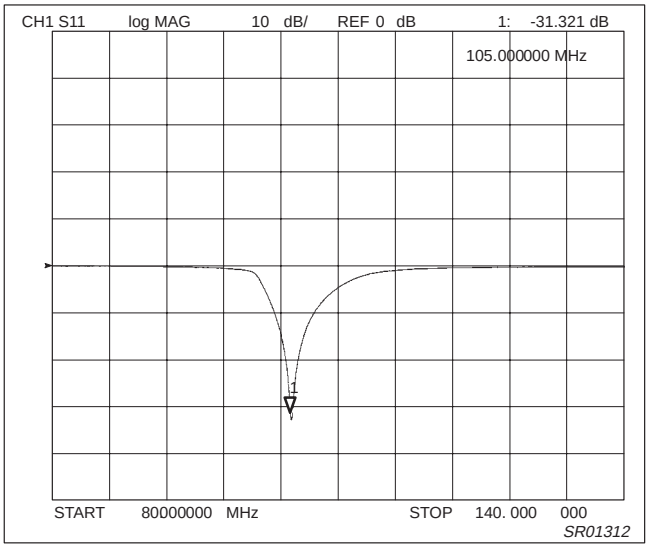


Figure 54. Mixer Output Set 5MHz Below Target to Get Final Result at 110.592MHz

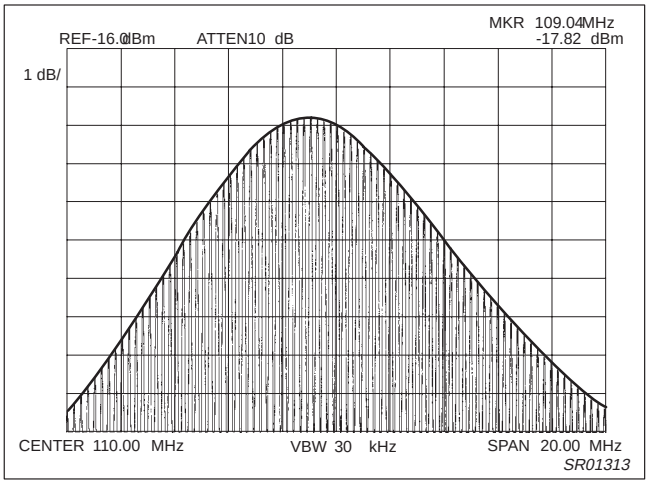


Figure 55. Mixer Output Set 5MHz Frequency Response Peak Very Near 110.592MHz Target

Summary of Mixer Open-Collector Output Concepts

The open-collector of a transistor offers a designer using the SA601 and SA620 the flexibility to provide impedance matching with minimal external components. Additionally, when an inductor is strategically located in the circuit, more AC output swing will occur due to the Early-Voltage effect of the device without adding any additional current.

When using the SA601 differential open-collector output, a designer can use the current-combiner circuit to combine the currents such that additional output signal swing is achieved. This preserves the RF signal and thus eliminates the need for interstage amplifiers. The current-combiner differential mixer output is not available on the SA620.

A flexible matching circuit can be used to deliver an equal amount of power to unequal resistive loads. The flexible matching circuit is ideal for trouble-shooting.

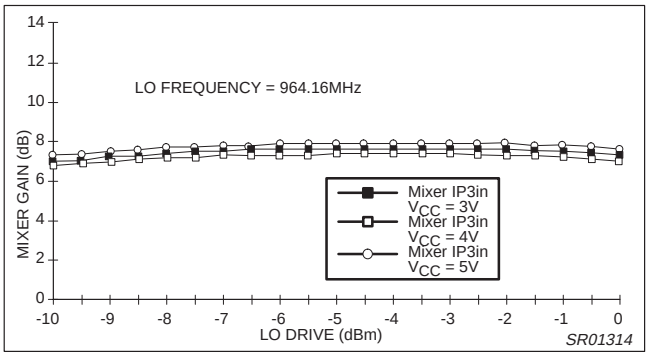


Figure 56. Mixer Gain vs LO Drive SA601

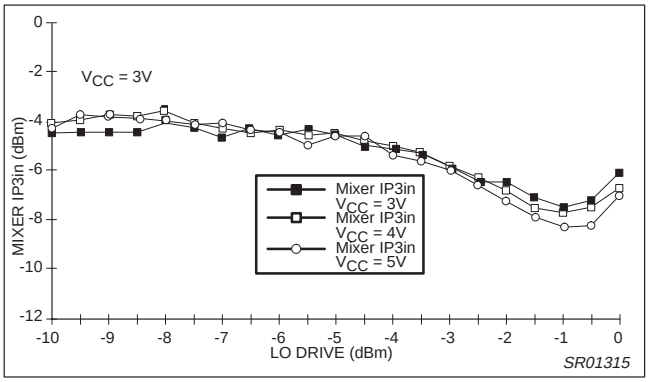


Figure 57. Mixer $IP3_{IN}$ vs LO Drive SA601

X. SA601 MIXER CHARACTERIZATION

Figure 56 shows a mixer gain vs. LO drive curve for a SA601 utilizing the current-combiner circuit in an application board environment. It shows that over an LO drive-level range of -10dBm to 0dBm the mixer gain deviates from an average value of 7.5dB by less than 0.5dB. It also shows that the gain will change by less than 0.5dB when V_{CC} is varied from 3V to 5V.

The noise figure of the SA601 generally increases with decreasing LO drive. Over the LO drive-level range of -10dBm to 0dBm the noise figure varied from approximately -12dB to approximately -8dB, respectively. The noise figure at - 5dBm LO drive is approximately 10dB.

Figure 57 shows the mixer's 60kHz $IP3_{IN}$ vs. LO drive curve for the SA601 in an application board environment. It should be noted that the $IP3_{IN}$ was measured with a -35dBm RF input at 881MHz and an offset of just 60kHz. 881MHz is the center of the 869 to 894 IS-54 Rx band, -35dBm was selected to ensure P_{IN} vs P_{OUT} linearity, and 60kHz was chosen as a suitable representation of current application alternate-channel constraints. The figure shows $IP3_{IN}$ to be constant at approximately -4.3dB over an LO drive-level range from -10dBm to approximately -5dBm. For LO drive-levels greater than -5dBm, $IP3_{IN}$ will decrease by approximately 1dB for every 1dB increase in LO drive. It is for this reason, that even though the mixer noise figure continues to decrease with larger LO drives, *the LO drive-level which optimizes gain, noise figure and $IP3_{IN}$ for current IS-54 applications is approximately -5dBm.*

SA601 System 12dB SINAD Performance

Figure 59 shows the 12dB SINAD vs RF input frequency of a receiver system composed of the SA601 utilizing the differential mixer output and the SA606 low-voltage FM-IF as shown in Figure 58. Data was taken over an input frequency range covering the 869 - 894MHz IS-54/AMPS Rx band as well as the 902 - 928 ISM band. *The 12dB SINAD performance in both bands was approximately -121 to -122dBm without a duplexer.* The system 12dB SINAD with a duplexer present will typically increase by approximately 3dB.

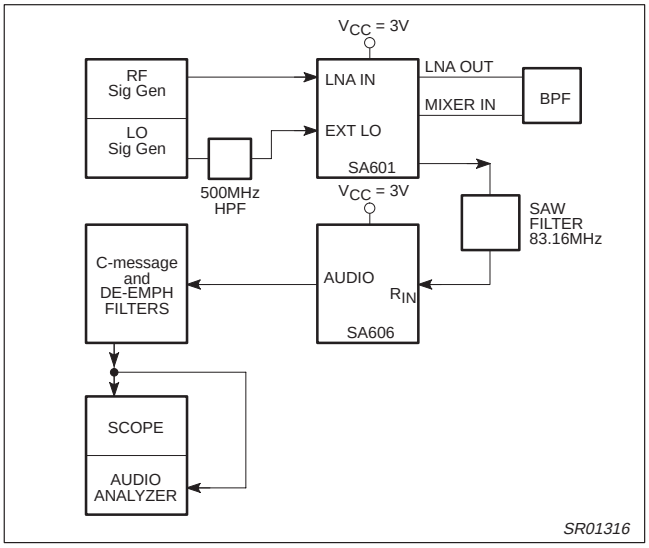


Figure 58. SA601 12dB SINAD System Test Configuration

XI. SA620 VCO

The SA620 features a low-power integrated VCO for providing an LO to the mixer. Thus, the additional cost and space associated with the use of an external VCO are eliminated. In the Philips SA620 application board environment shown in Figure 71, the VCO can be operated from 900MHz to approximately 1200MHz with the frequency range (using a 5V control voltage) increasing from 20MHz to 70MHz, respectively. Figure 60 shows the LO frequency vs. control voltage for two LO ranges centered at 960 and 995 MHz.

Figure 61 shows the VCO output power for the same LO ranges shown in Figure 60. The average VCO output power is approximately -20dBm and varies less than 0.5dB over the 5V control voltage range.

Figure 62 shows the VCO phase noise at a 60kHz offset for the same LO ranges shown in Figures 60 and 61. *The average phase noise (60kHz offset) is approximately -103dBc/Hz on*

non-silver-plated application boards and varies approximately 1dB across the 5V control voltage range. Phase noise performance may be improved another 1 – 2 dBc/Hz in with silver plating (see discussion below). It should be noted that a significant degradation of the phase noise performance was observed in the application board environment when the VCO was operated at frequencies above 1100MHz.

XII. μ-STRIP INDUCTOR OSCILLATOR RESONANT CIRCUIT [4, 5, 8]

The SA620 application board utilizes a high Q, μ-strip inductor in its oscillator resonant circuit to improve phase noise performance. Information concerning phase noise, μ-strips, and their implementation on the SA620 applications board is presented below

General Theoretical Background

Phase noise $S_\theta(fm)$ is a performance parameter of an oscillator circuit's spectral purity describing the energy it produces at frequencies fm on either side of the wanted carrier frequency f_c. To express how this works, an oscillator can be modeled as a feedback loop employing a phase modulator and noise-free amplifier to show how the resonator effects the phase characteristics of the resulting output. (A complete analysis of this model can be found in [4].)

In Figure 63, the phase spectral-density noise factor $S_{\theta IN}$ models internal phase noise produced by the oscillator's active components (e.g. BJT, FET etc.). Essentially, this factor is filtered by an external resonator that accepts energy from the noiseless amplifier which has sufficient gain G_O to sustain closed loop oscillations. Active circuitry with low internal phase noise will produce cleaner outputs for a given degree of filtering. Similarly, increasing the filtering will produce a cleaner output for a given internal spectral phase noise. Note that because of the feedback arrangement, the output spectral phase noise can never be less than that produced internally. These relations are summarized in the following equations, assuming the external resonator to be a simple parallel resonant LC tank circuit.

$$S\theta_{OUT}(fm) = |H(j\theta)|^2 \, S\theta_{IN}(fm) \quad (10)$$

$$S\theta_{OUT}(fm) = \left[1 + \left(\frac{f_o}{2Q_L \, fm}\right)^2\right] S\theta_{IN}(fm) \; ; (fm) > 0 \quad (11)$$

In practice, a spectrum analyzer is commonly used to obtain an indirect measure of phase noise by measuring power vs. frequency, or the power spectrum on some specified bandwidth at various carrier offset frequencies m and then normalizing each reading to the equivalent power in a bandwidth of 1Hz. This technique of measuring SSB phase noise L(m) usually takes the peak carrier power as the 0dB reference. Thus, Equation 11 can be expressed as

$$L_{OUT}(fm) = \frac{1}{2}\left[1 + \left(\frac{f_o}{2Q_L \, fm}\right)^2\right] S\theta_{IN}(fm) \; ; (fm) > 0 \quad (12)$$

SSB Phase Noise

and

$$L(fm) \equiv \frac{\text{noise power (in 1 Hz) with instrument corrections at } fm \text{ offset from the carrier } f_c}{\text{carrier power}} = \frac{N}{C} \quad (13)$$

Equation 12 shows two possible ways to decrease an oscillators output phase noise $L_{OUT}(fm)$. Basically, we can decrease $S_{\theta IN}(fm)$ or increase the loaded-Q, Q_L of the tank circuit. In the case of the SA620, only the latter is feasibly controllable since $S_{\theta IN}(fm)$ is a property of the internal circuitry and, as already noted, places a lower attainable bound on $L_{OUT}(fm)$ as $Q_L \Rightarrow \infty$.

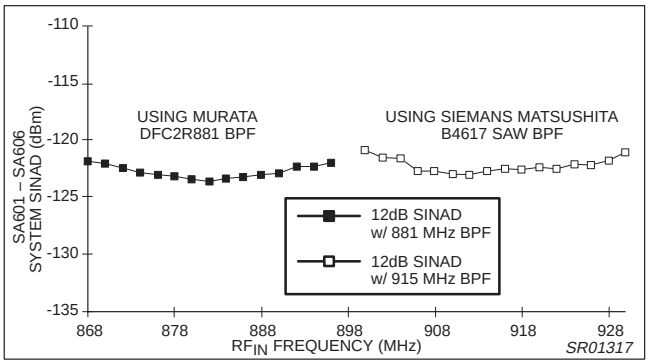


Figure 59. SA601 - SA606 System 12dB SINAD vs RF_{IN} Frequency

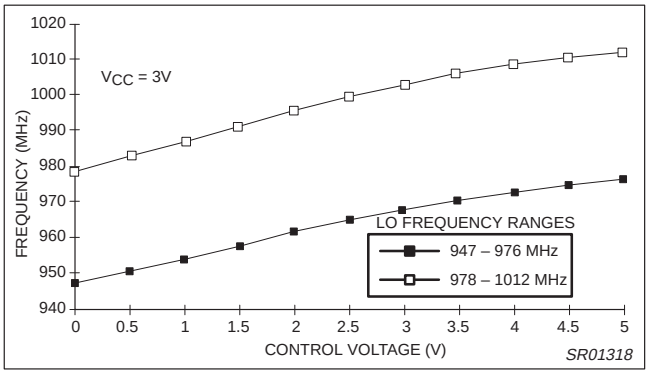


Figure 60. LO Frequency vs Control Voltage SA620 VCO

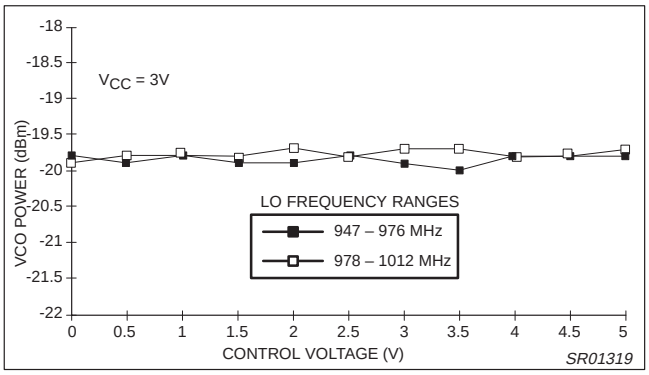


Figure 61. VCO Power vs Control Voltage SA620 VCO

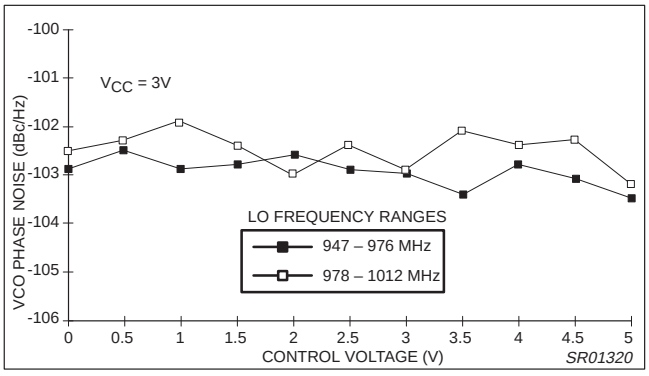


Figure 62. VCO Phase Noise vs Control Voltage SA620 VCO

Increasing Loaded-Q

Figure 64 shows the oscillator section of the SA620 with a conventional 2nd order parallel tuned tank circuit configured as the external resonator.

From the basic equations for parallel resonance, the resonator's loaded-Q is given by

$$Q_L = R_P \left[\frac{C_T}{L_T}\right]^{(1/2)} \quad (14)$$

where

$$R_P = R_T \;||\; R_C = \left[\left(\frac{1}{R_T}\right) + \left(\frac{1}{R_C}\right)\right]^{-1} \quad (15)$$

represents the net shunt tank resistance appearing across the network at resonance. R_T represents losses in the inductance L_T and capacitance C_T (almost always dominated by inductor losses), and R_C is the active circuits load impedance at resonance. Improving the quality (i.e., their Q) of the tank components, L_T and C_T will increase R_T, but since R_C is low in the case of the SA620, the resulting increase in R_P is relatively small. We can increase R_P by decoupling Z_C from the tank circuit (note that R_C is the real part of Z_C at resonance). Decoupling this impedance by using either tapped-L or tapped-C tank configurations is possible. Inspection of the circuit shows that DC biasing is necessary for Pins 9 and 10 (osc1 and osc2, respectively), so a tapped-C approach would require shunt-feeding these pins to V_{CC}. Thus, the most practical way is to employ a tapped-L network.

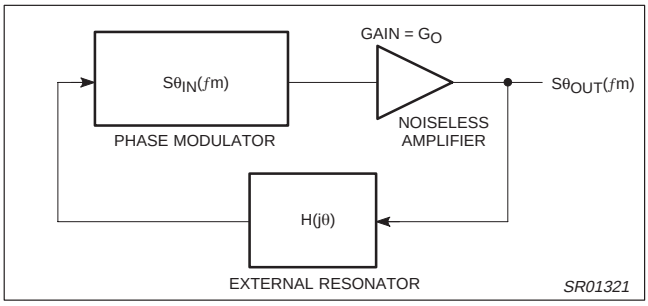


Figure 63. Oscillator Phase Noise Model

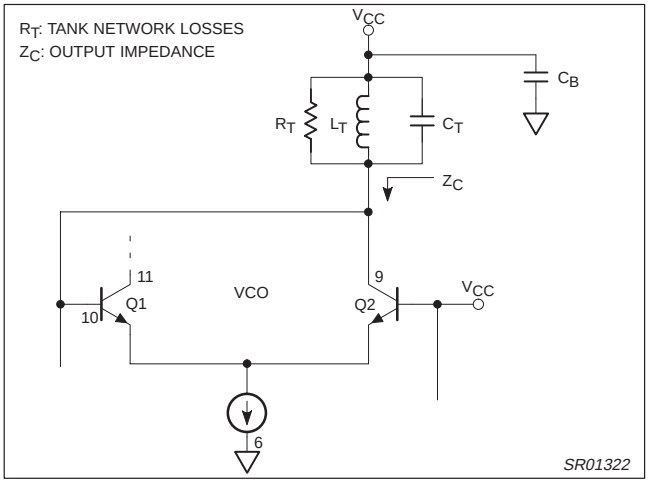


Figure 64. SA620 With External Resonator

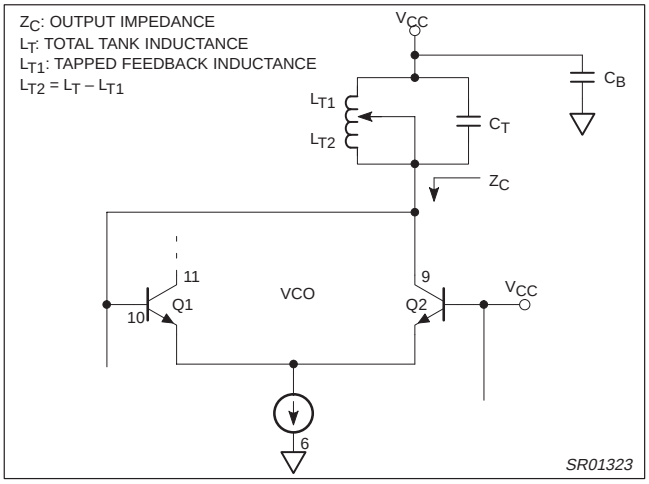


Figure 65. SA620 With Tapped-L Resonator

Figure 65 shows the basic tapped-L circuit. The effective multiplied shunt impedance at resonance across C_T is given by

$$\hat{R}_P = R_P \left[\left(\frac{L_{T2}}{L_{T1}}\right) + 1\right]^{1/2} \quad (16)$$

with a corresponding increase in loaded Q

$$\hat{Q}_L = Q_L \left[\left(\frac{L_{T2}}{L_{T1}}\right) + 1\right]^{1/2} \quad (17)$$

Feedback is caused by an RF voltage appearing across L_T, coupled through bypass capacitor C_B and its ground return to the cold end of the current source at Pin 6. The significance of this path increases with frequency. At 900MHz it becomes very critical to obtaining stable oscillations and must be kept as short as possible. Attention to layout detail cannot be overlooked here!

High-Q Short μ-Strip Inductor

Realizing a stable tapped-L network using lumped surface-mount inductors is impractical due to their low unloaded-Q and finite physical size. Another approach utilizes a high-Q short microstrip inductor. The conventional approach to microstrip resonators treats them as a length of transmission line terminated with a short which reflects back an inductive impedance which simulates a lumped inductor. The approach presented here deviates from this technique by specifically exploiting the very high unloaded-Q attainable with short microstrip inductors where we design for a large C/L ratio by making the microstrip a specific but short length. Resonance is achieved by replacing the short with whatever capacitance is needed for proper resonance. One equation for the inductance of a strip of metal having length l (mil) and width w (mil) is

$$L = [5.08E - 3]\,\ell\,[\ln(\ell/w) + 1.193 + 0.224(w/\ell)] \quad [nH/mil] \quad [4] \quad (18)$$

This technique results in a much shorter strip of metal for a given inductance. One intriguing property of microstrip inductors is that they are capable of very high unloaded-Q's. An equation describing the quality factor for a "wide" microstrip line is

$$Q_C = 0.63h\,[\sigma f_{GHz}]^{1/2} \quad [5] \quad (19)$$

where h is the dielectric thickness in centimeters, σ is the conductivity in [S/m] and f is frequency in GHz. This equation predicts an unloaded-Q exceeding 700 when silver-coated copper is used. Also, wide microstrip lines are defined as those whose strip width w to height h ratio is approximately or greater than 1, i.e. w/h > 1. The parallel capacitor formed by the metal strip over the

ground plane should also be included and may be calculated by the classic formula and included in the total needed to resonate with the inductance result found from equation (18). This “strip” capacitance is given by

$$C_S = K\varepsilon_o\varepsilon_r\ [wl/h]\ [Farad] \quad (20)$$

where ε_O= 8.86E-12 [F/cm] is the permitivity of free space, r is the relative dielectric constant of the substrate. A “fringe factor” K is included to account for necessary fringing (est 2% to 15%). These equations are meant to provide insight into circuit behavior and should, therefore, be applied cautiously to specific applications.

UHF VCO Using the SA620 at 900MHz

The basic electrical circuit involving the SA620 is shown in Figure 66. Feedback occurs when sufficient RF voltage develops across the tap inductances L_{T1} and L_{T2} (due to tap-1 and tap-2 respectively); note that inductance is reckoned from the cold end of the tank at node A. Taps 1 and 2 should be as close as possible to Pins 10 and 9, respectively. Also, nodes A (cold end of tank) and B (Pin 6) must be as physically close together and exhibit as low an impedance as possible to discourage parasitic oscillations. This “inner-loop” composed of L_{T2}, inductance of taps 1 and 2 connecting to Pins 10 and 9, and stray low Q inductance between nodes A and B create a parasitic loop that will favor oscillations that no longer depend on the full tapped-L tank circuit. This low-Q loop will exhibit very poor phase noise and typically oscillate well above 1200MHz; it has been observed as high as 1600MHz.

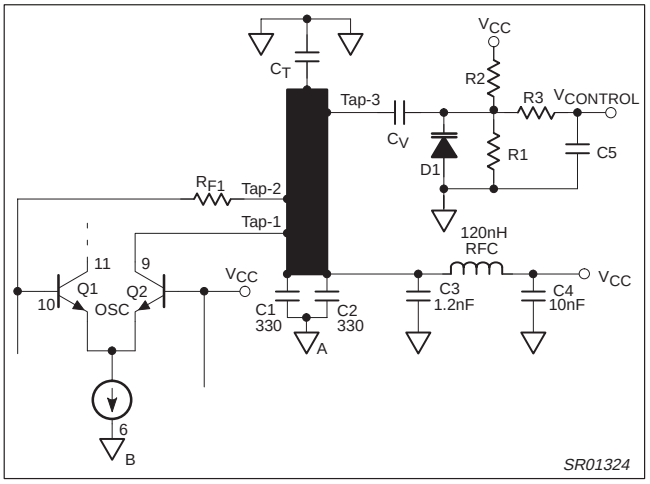


Figure 66. SA620 with Tapped-L μ-Strip Resonator

Another factor also affects this unwanted parasitic oscillation. As the loaded-Q of the tapped tank circuit decreases, the circuit becomes conditionally stable and will eventually favor the parasitic loop exclusively. This occurs because tapped-L loaded-Q affects the magnitude of the RF voltage appearing across the entire microstrip tank. Thus, feedback at taps 1 and 2 is reduced as the Q decreases. This increases the likelihood of the inner-loop parasitic controlling the oscillator, since its feedback voltage is largely independent of the μ-strip tank Q.

Equation 19 shows that microstrip inductors are capable of very high unloaded-Q’s. This depends on a number of physical factors: frequency, dielectric thickness and its quality, and the skin depth conductance of the metal strip itself. For example, at 900MHz, when coated with silver, unloaded-Q is somewhere about 750; when coated with lead (or sloppy soldering!) it drops to less than 230. If the unloaded-Q is too low, the loaded-Q also drops and the circuit becomes conditionally stable, and now will either oscillate at the higher parasitic inner-loop or the wanted tapped-L lower complete tank circuit frequency. Components should be connected by narrow traces closely connected to component pads to avoid soldering on the microstrip layer.

The addition of R_{F1} introduces necessary losses to control the inner-loop parasitic oscillation. Its size should be made as small as possible consistent with stability, startup and good phase noise performance. Since it also decreases feedback, LO injection falls off as it increases. Typically, experimental values from 4Ω to 30Ω have proved sufficient. Stability as a function of V_{CC} is a good way to assess conditional stability. Provided the microstrip tank has a high loaded-Q, stability should be independent of V_{CC} down to less than 2.5V, or so. When loaded-Q decreases, so as to favor the inner-loop parasitic, conditional stability will occur. This can readily be observed by increasing V_{CC} beginning at about 1.0V and noting whether the VCO jumps back and forth unpredictably. Mixer and LO port loading also affect this condition and should be considered.

Dimensions for the microstrip resonator are based on several criteria. The strip must be “wide”: its width to height must be on the order of 1 or greater. Minimum strip length seems to be about 200 mils for a 62 mil thick board. L/C ratios somewhere about 500 have yielded quite good results. Note that we usually specify the “L/C” ratio because it is always greater than 1, even though in a parallel resonant circuit it appears in the Q equation as C/L. Thus, decreasing the “L/C ratio” by making the microstrip shorter helps the loaded inductor Q, and the circuit loaded-Q_L, increase (see Equation 14). However, the effect of the lower Q of C_T, even when using a “hi-Q” SM type, decreased the expected larger increase in the net loaded circuit Q. Thus, the expected increase in Q_L may not be fully realizable. Assuming a 62 mil thick board with FR5 dielectric, a strip 50 by 300 mils gave very good experimental results where C_T was about 4.3pF with oscillations occurring from about 950 to 1000MHz for various test boards. A shorter inductor designed to increase the C/L ratio requiring 7.5pF experimentally resulted in only about 1–2dB improvement at 950MHz.

Tap-1 may be anywhere between the cold end of the tank (where C_1 and C_2 are located) and tap-2. Tap-2 yields good results at about 1/3 the strip length. Making it too close to the cold end in an effort to increase Q_L will result in loss of control over the inner-loop parasitic. To keep Q_L as large as possible, C_T should be a Hi-Q SM type. Differences greater than 5dB in SSB phase noise have been observed between a generic NPO SM and Hi-Q NPO SM capacitor.

Tap-3 can be at the end of the microstrip where C_T is connected. However, the varactor inevitably will cause a decrease in overall loaded-Q, typically by as much as 5dB. Moving it back some distance from the high end of the tank will decrease this effect and yield better results. A good starting point is about 1/4 back or 3/4 of the length from the cold end. C_1 and C_2 are paralleled lower value capacitors to yield a better low-impedance ground return to Pin 6 (node B) since relatively large RF currents flow through them. Note that as Q_L increases the peak circulating RF current will also increase, as will the RF voltage at the high end of the microstrip. At 900MHz good results have been obtained when both are about 330pF. RFC was chosen to be approximately series-resonant around 900MHz and constitutes the series feed path for DC biasing. It may be possible to neglect this component entirely, provided the PCB connection to the cold end of the tank is very close to RF ground. Finally, note that shielding of the entire microstrip may be necessary to meet part 15 emission limitations (where applicable).

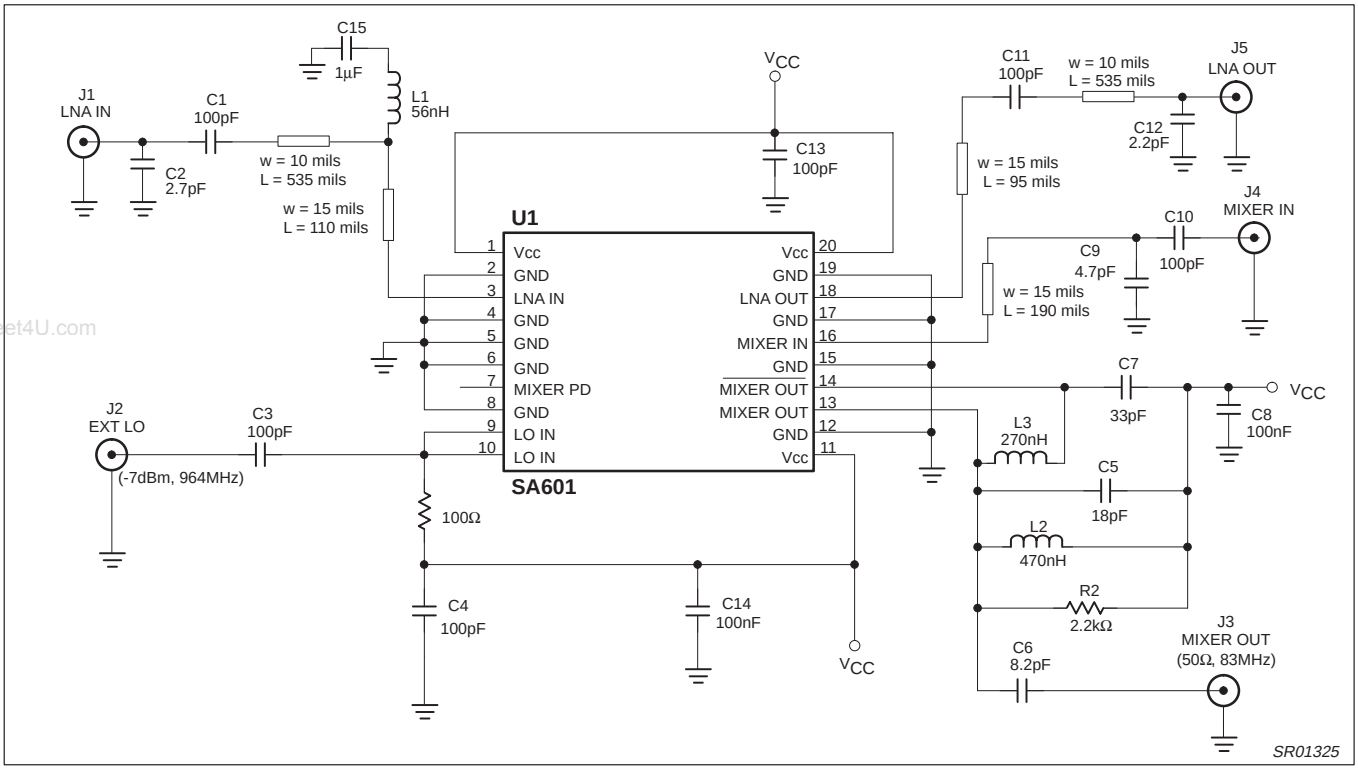
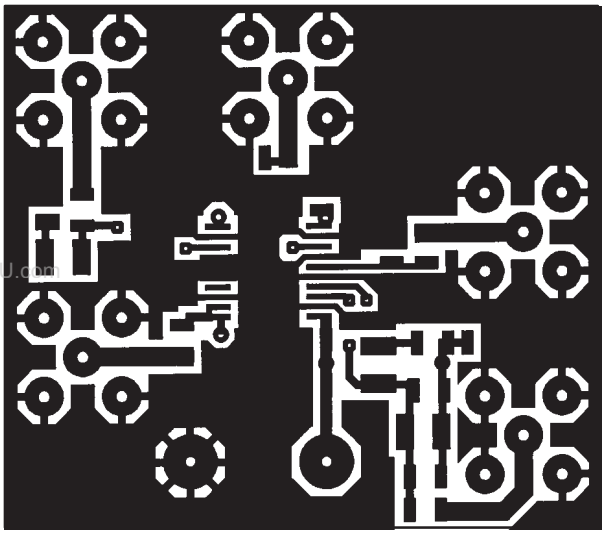
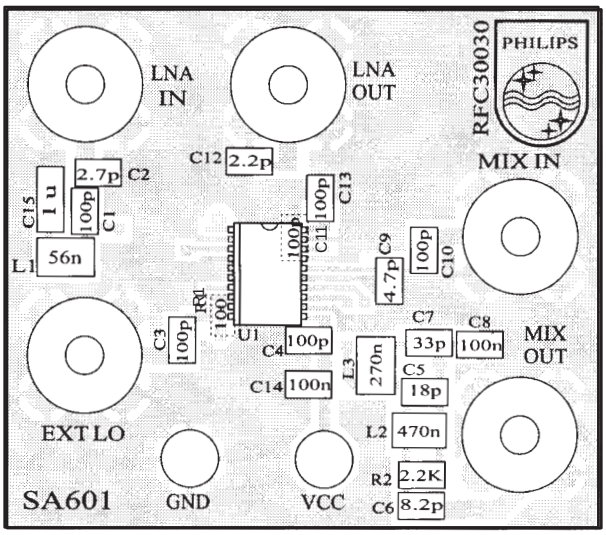


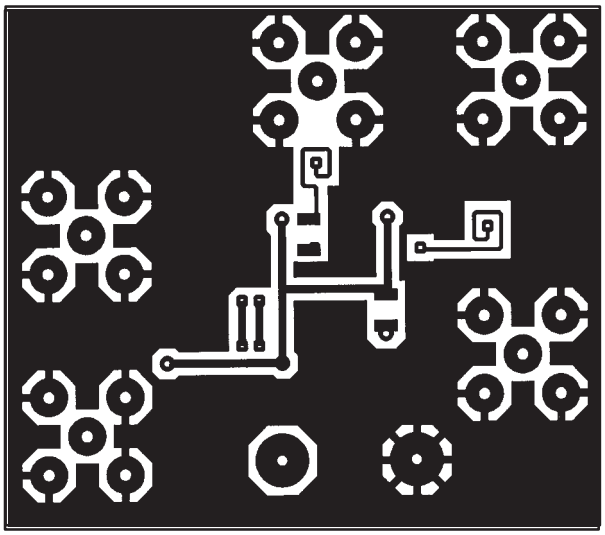
Figure 67. SA601 Application Board Schematic



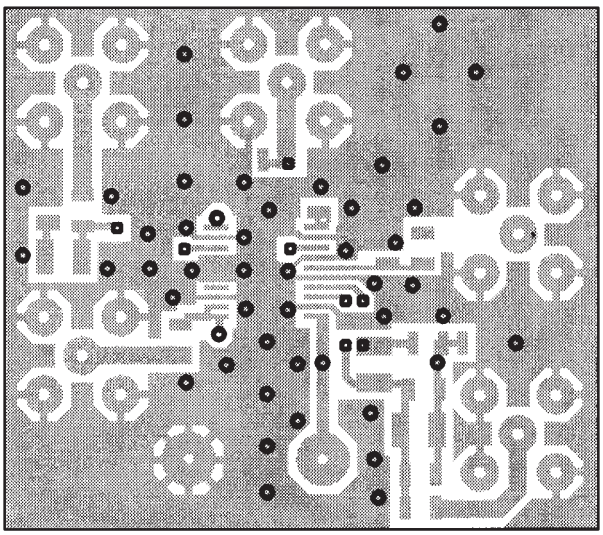
Top View



Silk Screen



Bottom View



Via Layer

SR01326

Figure 68. SA601 Demoboard Layout (Not Actual Size)

Table 5. Customer Application Component List for SA601

Qty.	Part Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	2.2pF	50V	C12	Cer Cap 0805 NPO ± .25pF	Garrett	Philips	0805CG229C9BB0
1	2.7pF	50V	C2	Cer Cap 0805 NPO ± .25pF	Garrett	Philips	0805CG279C9BB0
1	4.7pF	50V	C9	Cer Cap 0805 NPO ± .25pF	Garrett	Philips	0805CG479C9BB0
1	8.2pF	50V	C6	Cer Cap 0805 NPO ± 0.5pF	Garrett	Philips	0805CG829C9BB0
1	18pF	50V	C5	Cer Cap 0805 NPO ± 5%	Garrett	Philips	0805CG180J9BB0
1	33pF	50V	C7	Cer Cap 0805 NPO ± 5%	Garrett	Philips	0805CG330J9BB0
6	100pF	50V	C1, C3, C4, C10, C11, C13	Cer Cap 0805 NPO ± 5%	Garrett	Philips	0805CG101J9BB0
2	0.1µF	50V	C8, C14	Cer Cap 0805 Z5U ± 20%	Garrett	Philips	0805E104M9BB0
1	1µF	25V	C15	Cer Cap 1206 Y5V ± 20%	Garrett	Rohm	MCH312F105ZP
Surface Mount Resistors							
1	100Ω	50V	R1	Chip Res. 1/16W 0603 ± 5%	Garrett	Rohm	MCR10JW101
1	2.2kΩ	50V	R2	Chip Res. 1/16W 0603 ± 5%	Garrett	Rohm	MCR10JW222
Surface Mount Inductors							
1	56nH		L1	1008 size chip inductor ± 10%	Coilcraft	Coilcraft	1008HS-560XKBB
1	270nH		L3	1008 size chip inductor ± 10%	Coilcraft	Coilcraft	1008HS-271XKBB
1	470nH		L2	1008 size chip inductor ± 10%	Coilcraft	Coilcraft	1008HS-471XKBB
Surface Mount Integrated Circuit							
1		3V	U1	RF low noise amplifier / mixer	Philips	Philips	SA601DK
Miscellaneous							
5				SMA gold connector	Newark	EF–Johnson	142-0701-801
2				Terminal	Newark	Cambion	160-1558-02-01
1				Printed Circuit Board	Excel	Philips	SA601 - RFC30030
29 Total Parts							

XIII. APPLICATION BOARDS

SA601 Applications Board

Figure 67 shows the schematic of the current application board for the SA601.

The functional description of each pin and its associated external circuitry is summarized below.

Pins 1, 11 and 20 are all V_{CC} supply pins. Capacitor C_{13} is for decoupling purposes.

Pins 2, 4, 5, 6, 8, 12, 15, 17 and 19 are all ground connections and should be tied to a common ground plane and as close to the chip as possible.

Pin 3 is the LNA mixer input pin. The LNA input has an associated network for the purpose of optimizing the return loss while minimizing the degradation of the noise figure. This network is composed of Capacitor C_2, L_1 and the 535 mil spiral inductor. Capacitor C_1 is a DC blocking cap.

Capacitor C_{15} and inductor L_1 also provide the LNA with voltage compensation.

Pin 7 is the mixer power-down pin. It will disable the mixer if set low. The application board simply leaves this pin open.

Pin 9 and Pin 10 are both connected to the local oscillator input. It is important to have good return loss at this pin to allow small LO drive-levels to be used. Capacitors C_4 and C_{14} are decoupling caps. C_3 is a DC blocking cap.

Pin 13 and Pin 14 are the differential mixer outputs. Inductor L_3 and capacitors C_5 and C_7 comprise the differential-to-single-ended translation circuit which combines the output currents and forces them to be in phase with each other. This circuit is extensively described in the previous discussions. R_2 sets the output impedance of the mixer output and L_2 is the DC bypass inductor which increases the gain of the open-collector output. Capacitor C_6, in conjunction with L_2, is used to match the mixer output port to 50Ω.

Pin 16 is the mixer input pin. Capacitor C_9 is used to optimize return loss and noise figure. Capacitor C_{10} is a DC blocking cap.

Pin 18 is the LNA output pin. Capacitor C_{12} in conjunction with the 535 mil spiral inductor comprise a network for optimizing return loss and obtaining best noise figure. C_{11} is a DC blocking cap.

SA601 Application Board Modification For Increasing Mixer Gain

The SA601 application board can be modified by disconnecting the 2.2kΩ resistor R2 in Figure 67 and reconnecting it in parallel with C7. Figure 69 shows a comparison of the mixer gain with and without this modification. This modification yields a 2dB improvement in mixer conversion gain for LO drive-levels from -10dBm to 0dBm. Figure 70 shows a comparison of the mixer $IP3_{IN}$ with and without this modification over the same LO drive-level range as in Figure 69. This data shows that the $IP3_{IN}$ performance of the mixer is not degraded for LO drive-levels less than or equal to -5dBm. Some degradation does occur for LO drive-levels above -5dBm. Laboratory comparison data of noise figure performance also showed that over the LO drive-level range of -10dBm to 0dBm the modification of R_2 yielded a decrease in noise figure of approximately 0.3dB. The R_2 modification does draw about 0.3mA more supply current, however.

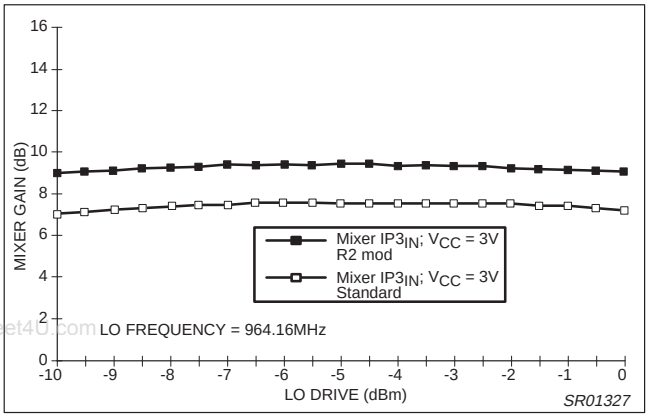


Figure 69. SA601 Mixer Gain vs LO Drive Standard/R2 Modification Comparison

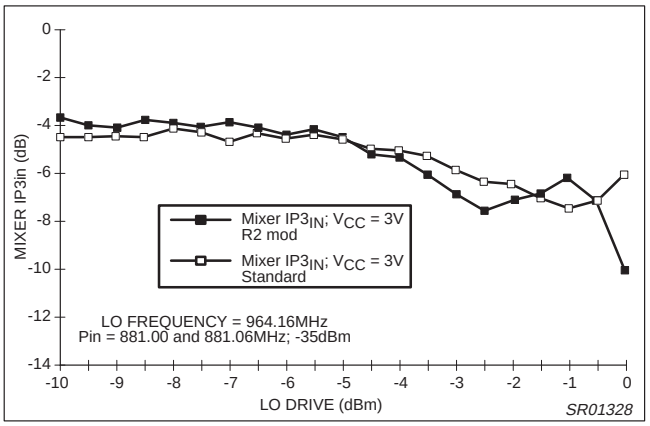


Figure 70. SA601 Mixer $IP3_{IN}$ vs LO Drive Standard/R2 Modification Comparison

SA620 Applications Board [7]

Figure 71 shows the schematic of the current application board for the SA620. The functional description of each pin and it's associated circuitry is summarized below.

Pin 1 is the LNA enable pin. This pin is used for selecting the gain in the LNA path.

The logic levels for the SA620 LNA enable are specified as:

Logic "1" level (LNA on):	+2.0V to V_{CC}
Logic "0" level (LNA off):	-0.3 to +0.8V

Referring to the application board schematic, resistor R_8 and capacitor C_{25} are used to improve LNA enable switching time. If fast switching is not a requirement, or if the LNA does not need to be disabled, these two components can be eliminated.

Pins 2, 4, 5 and 19 are ground connections. These pins provide the RF ground path for the LNA and should be tied to a common ground plane as close to the IC, and each other, as possible.

Pin 3 is the LNA input. The LNA input exhibits a return loss of 7dB at 900MHz. However, the designer can implement an external matching circuit to further improve the match. For this reason, S_{11} plots of the LNA input impedance measured right at Pin 3 are provided in the SA620 data sheet.

Referring again to the application board schematic, the 260 mil long transmission line, inductors L_1, the 4.7nH spiral inductor, and capacitor C_2 are the matching elements. Capacitor C_1 is a DC blocking capacitor. Conjugately matching the LNA input for optimum gain performance will degrade the noise figure slightly. Typically, 1.6dB noise figure can be achieved when the return loss is improved to 10dB.

Pin 6 and Pin 12 are the oscillator ground connections. These pins provide the RF ground path for the oscillator section of the SA620 and should be tied to a common ground plane as close to the IC, and each other, as possible.

Pin 7 and Pin 8 are the mixer and oscillator power down pins, respectively. These pins can be used to individually power down the mixer and the oscillator sections of the SA620.

The DC levels at Pins 7 and 8 are approximately 2.3V and 1.5V, respectively, and these levels must be established by the IC and not the power down circuitry. Placing a Schottky diode (V_f = 0.3V) between each power down pin and the LNA ENABLE pin will allow the designer to power-down the IC via a single control voltage, the LNA enable, while allowing the voltages at Pins 7 and 8 to float at the IC levels when in the power-up mode.

Pin 9 and Pin 10 drive the base of one and the collector of another of the broadband VCO differential pair input stage transistors as shown in Figure 64. Components C_5, C_6, C_7, C_8, C_9, C_{10}, C_{11}, L_2, R_1, R_2, R_3, R_4, D_1 and the 300 mil µ-strip comprise the resonant tank circuit described in detail above and shown in Figure 66.

Pin 11 is the open-collector VCO output and is provided to couple out VCO energy for frequency synthesis for example. Resistor R_5 is chosen to be small so as not to excessively load down the VCO. Hence, only about -20dBm of VCO fundamental output power will be measured at the VCO_{OUT} connector on the application board. Note that the second harmonic power level will actually be slightly higher than that of the fundamental. This is not a problem because this isn't the same signal that is driving the mixer, and the mixer develops its own second harmonic as a result of the mixing process anyway. The 4.7nH spiral inductor and capacitor C_{12} on the application board are the 50Ω matching elements. Capacitor C_{13} is a decoupling capacitor.

Pin 13 is the open-collector mixer output. Referring to the application board schematic, R_6 establishes the output impedance to be 1kΩ. Inductor L_3 and capacitors C_{15} and C_{16} are 50Ω matching elements.

Pin 14 is the mixer bypass pin. This is not a signal output. It is provided for designers to optimize the IP3 performance of the mixer circuit. If you look closely at the application board schematic, you will notice that the two circuit elements at Pin 14, the 2.5 - 6.0pF capacitor and the 4.7nH spiral inductor, are very small impedances at the 83MHz IF frequency. The intent is to reflect RF leakage energy back into Pin 14 to achieve phase cancellation of this energy inside the IC, thus reducing the level of third-order intermodulation products. While looking at the third-order intermodulation products on a spectrum analyzer, the designer can tune with C_{17} to minimize the level of these products at the IF output. To obtain the best $IP3_{IN}$ performance over the entire frequency range of the VCO the following procedure is recommended:

1. Set the VCO control voltage to its mid-range value of 2.5V.
2. Adjust capacitor C_9 to obtain the desired mid-range frequency,
3. Tune C_{17} for best $IP3_{IN}$.

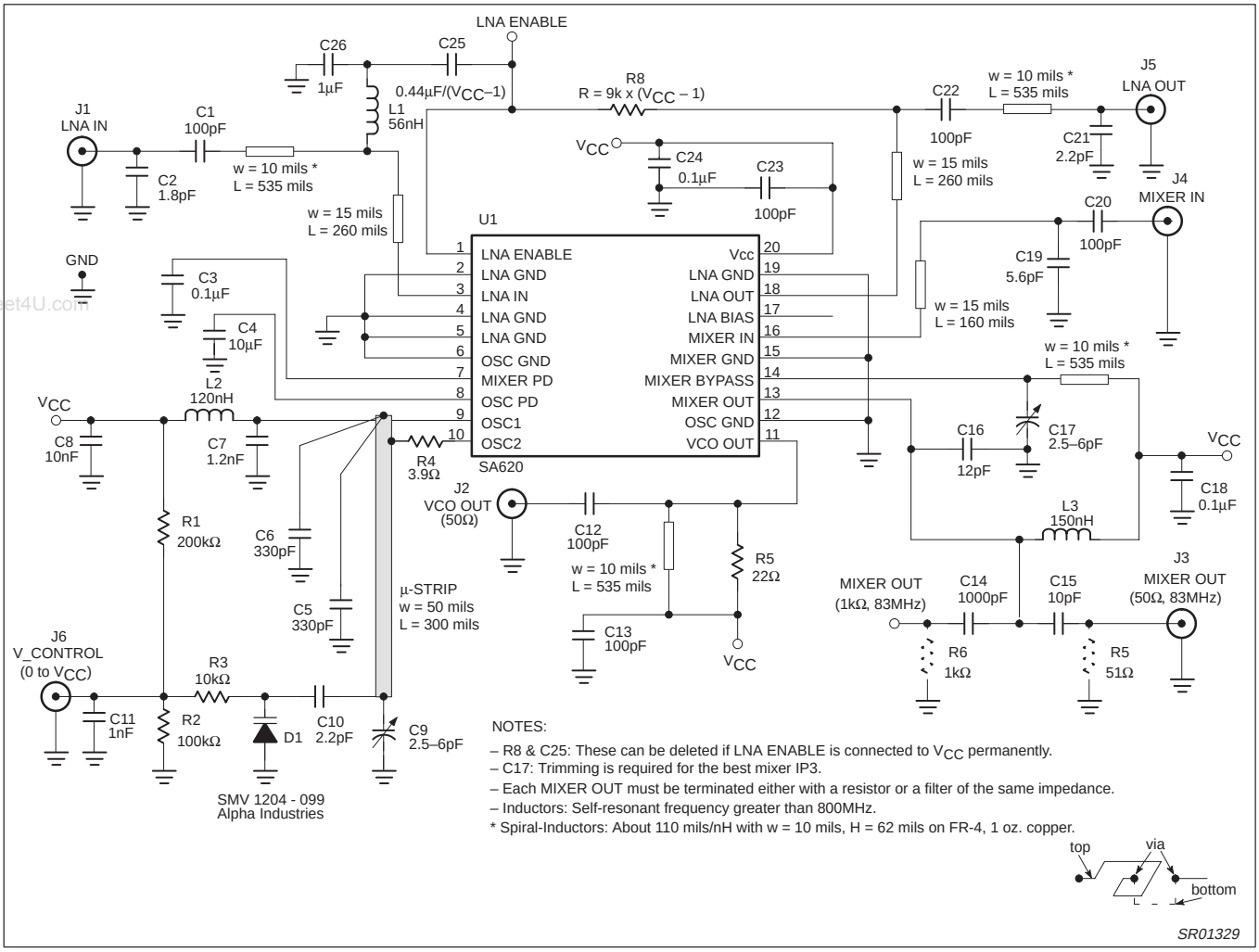


Figure 71. SA620 Application Board

Pin 15 is the mixer ground connection. This pin provides the RF ground path for the mixer section of the SA620 and should be tied to a common ground plane as close to the IC as possible.

Pin 16 is the mixer input pin. The mixer input is not matched to 50Ω, therefore, external matching elements are required to achieve optimum performance. The 160 mil long transmission line and capacitor C_{19} are the matching elements on the application board. C_{20} is a DC blocking capacitor. If no matching elements are used, the IP3 performance is typically maximized at +3dBm at the expense of gain, which will be reduced by 3dB.

Pin 17 is the LNA bias pin. This is a DC check pin for use during the manufacture of the SA620 only. Customers should float this pin in their designs.

Pin 18 is the LNA output pin. The LNA output has an intrinsic return loss of approximately 9dB at 900MHz. However, to achieve optimum performance from the SA620, the designer can implement an external matching circuit to further improve the match. For this reason, S_{22} plots of the LNA output impedance measured right at Pin 18 are provided in the SA620 data sheet. Referring again to the application board schematic, the 260 mil long transmission line, the 4.7nH spiral inductor, and capacitor C_{21} are the matching elements. Capacitor C_{22} is a DC blocking capacitor.

Pin 20 is the DC power input to the SA620 where capacitors C_{23} and C_{24} are strictly for decoupling purposes.

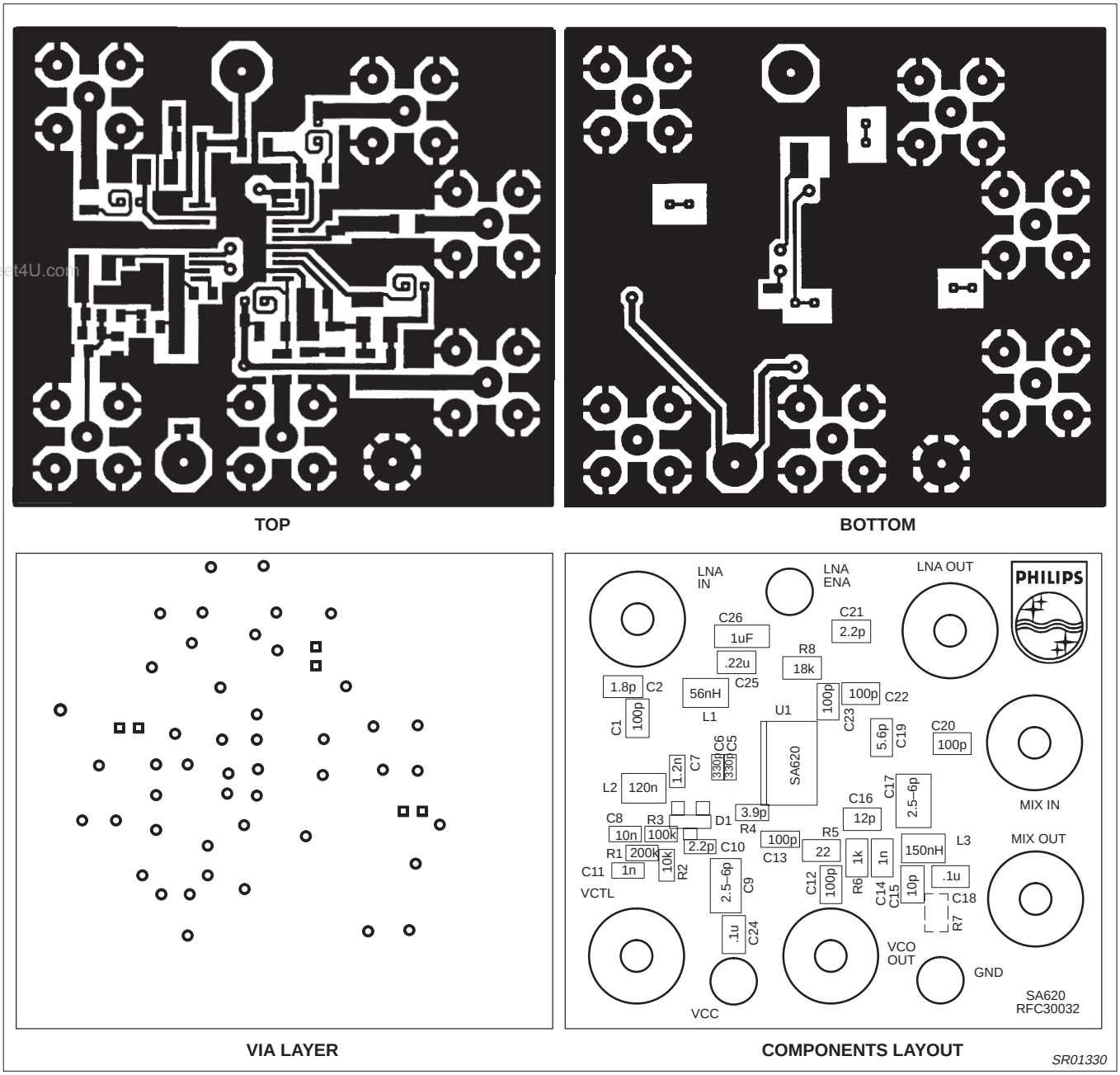


Figure 72. SA620 Demoboard Layout (Not Actual Size)

XIV. TEST AND MEASUREMENT TIPS

Noise Figure and Gain

The LNA of both the SA601 and SA620 can be tested identically. The gain and noise figure can be measured on a noise figure meter such as the HP8970. The correct measurement mode on this particular piece of equipment is obtained by selecting special function 1.0. It is important to do all noise figure measurements within a screen room to ensure the receiver of the noise figure meter is not picking up any stray signals. The LNA gain can also be measured on a spectrum analyzer. For accurate measurements, be sure to properly compensate for losses in the cables and connectors used. Also, make sure that the input power used is well below the 1dB compression point for the device. P_{IN} = -25dBm is a good value.

The SA601 and SA620 mixers require more precaution while testing. The correct measurement mode for mixer noise figure and gain measurements is obtained on the HP8970 by selecting special function 1.4. It should be stated again that all noise figure measurements should be done within a screen room. The noise source used in conjunction with the noise figure meter is generally a wideband noise source. So, for a given LO frequency there are two regions of the wideband noise power spectrum which will mix to the specified IF frequency. Thus, an image-reject bandpass filter should be placed between the noise source and the mixer input. In this way

the unwanted input noise power will be rejected yielding proper single sideband noise figure measurements. The loss through this image-reject filter should also be accounted for. Losses prior to the mixer input can be compensated for on the HP8970 by selecting special function 34.2. The noise figure of the mixers is highly dependent on the strength and quality of the LO signal. The LO signal should be passed through a high-pass filter. A 500MHz HPF is typically used. The noise figure is dependent on the LO drive-level. Generally, the noise figure will decrease as the LO drive-level is increased. The noise figure has also been observed to show some dependence on the range setting of the signal generator. The high-frequency components present at the IF output of the mixer should also be filtered out prior to entering the input port of the noise figure meter. This is typically done with a 300MHz low-pass filter. If the conversion gain of the mixer is to be measured directly on a spectrum analyzer, be sure that the input power is well below the 1dB compression point. Again, -25dBm is a good value.

Table 6. Customer Application Component List for SA620

Qty.	Part Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	2.2pF	50V	C10	Cer Cap 0603 NPO ± .25pF	Garrett	Rohm	MCH185A2R2CK
2	330pF	50V	C5, C6	Cer Cap 0603 NPO ± 5%	Garrett	Rohm	MCH185A331JK
1	1000pF	50V	C11	Cer Cap 0603 X7R ± 10%	Garrett	Rohm	MCH185C102KK
1	1200pF	50V	C7	Cer Cap 0603 X7R ± 10%	Garrett	Rohm	MCH185C122KK
1	0.01µF	25V	C8	Cer Cap 0603 X7R ± 10%	Garrett	Rohm	MCH185C103KK
1	1.8pF	50V	C2	Cer Cap 0805 NPO ± .25pF	Garrett	Philips	0805CG189C9BB0
1	2.2pF	50V	C21	Cer Cap 0805 NPO ± .25pF	Garrett	Philips	0805CG229C9BB0
1	5.6pF	50V	C19	Cer Cap 0805 NPO ± 0.5pF	Garrett	Philips	0805CG569C9BB0
1	10pF	50V	C15	Cer Cap 0805 NPO ± 5%	Garrett	Philips	0805CG100J9BB0
1	12pF	50V	C16	Cer Cap 0805 NPO ± 5%	Garrett	Philips	0805CG120J9BB0
6	100pF	50V	C1, C12, C13, C20, C22, C23	Cer Cap 0805 NPO ± 5%	Garrett	Philips	0805CG101J9BB0
1	1000pF	50V	C14	Cer Cap 0805 NPO ± 5%	Garrett	Philips	0805CG102J9BB0
3	0.1µF	50V	C3, C18, C24	Cer Cap 0805 Z5U ± 20%	Garrett	Philips	0805E104M9BB0
1	0.22µF	50V	C25	Cer Cap 0805 Y5V ± 20%	Garrett	Rohm	MCH212F224ZK
1	10µF	10V	C4	Tant Chip Cap B 3528 ± 10%	Garrett	Philips	49MC106C010KOAS
1	1µF		C26	Cer Cap 1206 Y5V ± 20%	Garrett	Rohm	MCH312F105ZP
Surface Mount Variable Capacitors							
2	2–6pF		C9, C17	Trimmer capacitor	Murata	Murata	TZV02Z060A110
Surface Mount Resistors							
1	3.9Ω		R4	Chip res. 1/16W 0603 ± 5%	Garrett	Rohm	MCR03JW3.9
1	10kΩ		R3	Chip res. 1/16W 0603 ± 5%	Garrett	Rohm	MCR03JW103
1	100kΩ		R2	Chip res. 1/16W 0603 ± 5%	Garrett	Rohm	MCR03JW104
1	200kΩ		R1	Chip res. 1/16W 0603 ± 5%	Garrett	Rohm	MCR03JW204
1	22Ω		R5	Chip res. 1/10W 0805 ± 5%	Garrett	Rohm	MCR10JW220
1	51Ω		R7	Chip res. 1/10W 0805 ± 5%	Garrett	Rohm	MCR10JW510
1	1kΩ		R6	Chip res. 1/10W 0805 ± 5%	Garrett	Rohm	MCR10JW102
1	18kΩ		R8	Chip res. 1/10W 0805 ± 5%	Garrett	Rohm	MCR10JW183
Surface Mount Inductors							
1	56nH		L1	Chip inductor 1008CS ± 10%	Coilcraft	Coilcraft	1008CS-560XKBB
1	120nH		L2	Chip inductor 1008CS ± 10%	Coilcraft	Coilcraft	1008CS-121XKBB
1	150nH		L3	Chip inductor 1008CS ± 10%	Coilcraft	Coilcraft	1008CS-151XKBB
Surface Mount Integrated Circuit							
1		3V	U1	Low voltage LNA & Mixer	Philips	Philips	SA620DK
Miscellaneous							
1			D1	Varactor	Wireless Components	Alpha Industries	SMV 1204-099
6				SMA gold connector	Newark	EF-Johnson	142-0701-801
3				Terminal	Newark	Cambion	160-1558-02-01
1				Printed Circuit Board	Excel	Philips	SA620 - RFC30032
49 Total Parts							

1dB Compression Point

This is determined by taking P_{OUT} vs. P_{IN} data at very low input power where the relationship between these quantities is linear. An input power range between -35dBm and -30dBm is sufficient for both the LNA and mixer. The input power is then increased to the

point where the difference between an extrapolation of the low input vs output power line and the output power is 1dB. The input power at which this occurs is the 1dB compression point. A shorter and more practical method of obtaining this parameter is to adjust the input power at a low level such that the output power is some integer number. Then increase the input power in 1dB increments. The output should also increase in 1dB increments. When the output power becomes exactly 1dB less than the expected value, the input power at which this occurs is the 1dB compression point.

Input Third-Order Intercept Point

$IP3_{IN}$ is typically measured on a spectrum analyzer by combining two input signals of equal power that are detuned by approximately 60kHz. This is then connected to the input of the device. Be sure to measure the output power of the two peaks after the power combiner because the two ports of the power combiner rarely attenuate equally. $IP3_{IN}$ is read off the spectrum analyzer by measuring the difference between the two carrier peaks and the intermodulation peaks, then adding half this difference to the input power.

It is extremely important to take this data at very low input power because this calculation assumes linearity. Input power of -35dBm is sufficient.

Phase Noise

The most economical way to measure phase noise is using the spectrum analyzer. As previously stated, this is done very simply by measuring the difference between the carrier frequency peak power and the power at some specified offset from the carrier. Unfortunately, the spectrum analyzer does not have the capability of measuring this with a 1Hz resolution bandwidth. Thus, a calculation must be made as follows:

$$\text{Phase Noise (dBc/Hz)} = -(|\Delta| + 10\log(\text{RBW}))$$

where Δ is the difference between the peak power at the carrier frequency and the power at the specified offset frequency, and RBW is the resolution bandwidth of the spectrum analyzer while taking the measurement.

XV. COMMON QUESTIONS AND ANSWERS

Q. I'm not getting the Mixer Noise Figure that is stated in the databook. What could be wrong?
A. There are quite a few things that can affect your noise figure. The most important thing to do initially is to check your measurement setup by following the suggestions in the test and measurement section of this application note. Aside from that, maintaining a good match at the LO input is very important and using the same LO drive-level specified in the databook is also necessary.

Q. Does the SA620 VCO meet AMPS stringent phase noise requirements?
A. The SA620 VCO phase noise is typically about -102dBc/Hz @ 60kHz. This does not meet AMPS specifications of -110dBc/Hz @ 60kHz.

Q. Can the SA620 be used with an external VCO to get better phase noise performance?
A. Although possible, this is not recommended due to the higher output power of the external VCO causing LO leakage problems at the mixer output.

Q. Why was the current-combiner implemented with a C - L - C arrangement instead of its dual circuit approach?
A. The C - L - C arrangement has the advantage of being low-pass in nature. Thus, it supplies additional rejection of the higher frequency RF_{IN} and LO signals at the mixer output.

Q. Why am I not getting the $IP3_{IN}$ values that are stated in the databook?
A. In addition to checking your test setup, you might want to check what the offset is between your two RF input signals. Some of the databook values are taken with an offset of 1MHz. Chances are that your offset is much smaller. For instance, AMPS alternate channel spec is only 60kHz. $IP3_{IN}$ will decrease when this offset is decreased.

Q. What are the necessary components needed to ensure unconditional stability of the LNAs.
A. Capacitor C_{15} and inductor L_1 on the SA601 schematic of Figure 67 are the necessary components needed to ensure stability. Without these components, the amplifier will generate spurs approximately 1.5MHz off the carrier at V_{CC} = 3V. The similar components on the SA620 schematic in Figure 71 are capacitor C_{26} and inductor L_1.

XVI. REFERENCES

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