TCC731

Single Chip Digital Audio Encoder/Decoder with MCU

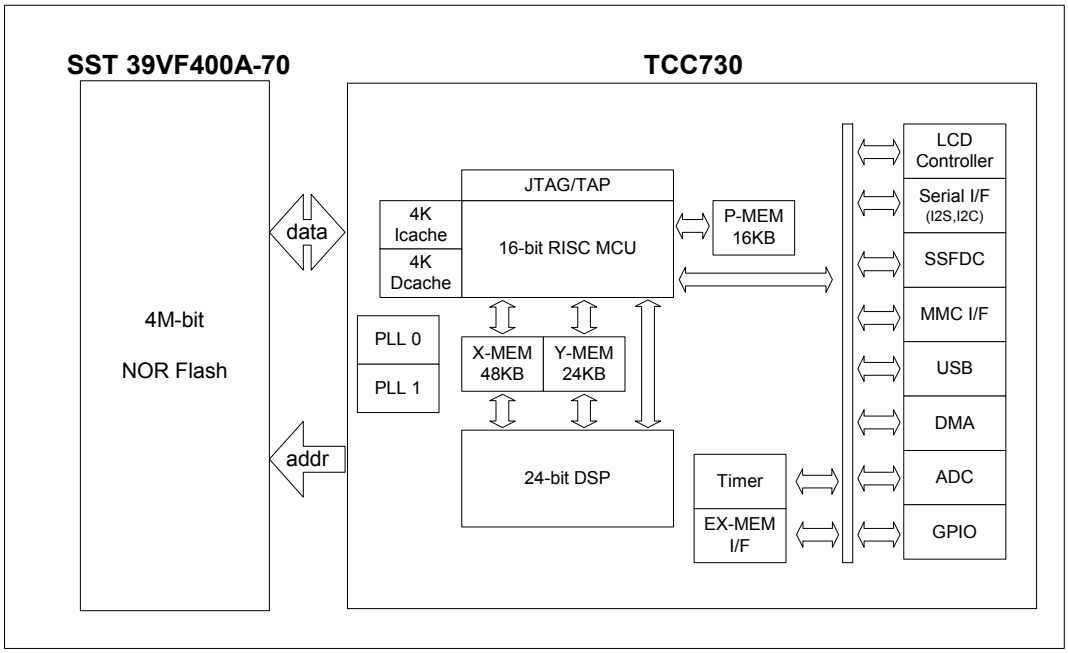
Apr. 21 2003 **Specification V1.00**

FEATURES

- 16-bit RISC type MCU core
- 24-bit fixed point DSP core
- 72KB internal data memory
- 16KB internal program memory
- Icache : 4KB direct-mapped cache
- Dcache : 4KB 2-way set asso. Cache
- 4-Mbit NOR Flash (SST39VF400A-70)
- On-chip peripherals
  - Basic timer & watchdog timer
  - Three 16 bit timers
  - One I^2C & two I^2S I/F
  - Full-duplex UART controller
  - USB ver1.1 compliance
  - SSFDC(SMC) I/F
  - Intelligent interrupt controller
  - Six 10-bit resolution A/D channels
  - LCD controller for STN/TFT LCD
  - PLL based on 32.768KHz OSC
- 80MHz(max) operation frequency
- 3V operation voltage
- 208-pin CABGA package
- Low power consumption
- MP3 encoder/decoder
- WMA™ decoder
- Flash file-system
  - SSFDC for SMC
  - FAT12/FAT16 for MMC and SD
- USB driver for Windows™ 98/Me/2K/XP
- Mass Storage Class

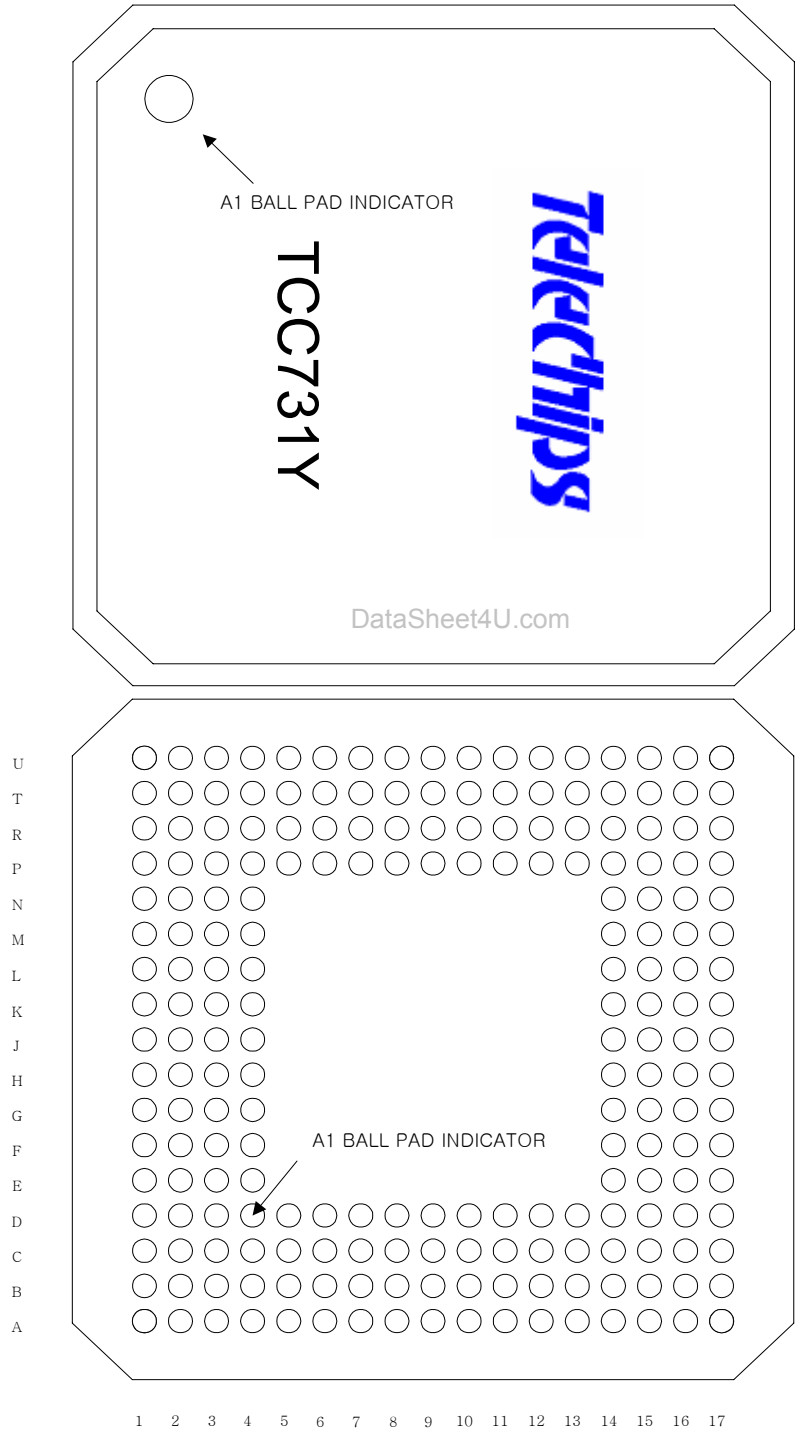
APPLICATIONS

- Portable MP3/WMA recorder/player
- MP3 juke box
- Digital audio encoder/decoder
- Digital internet radio server
- Digital satellite radio server/receiver
- CD type MP3/WMA player



TCC731 Functional Block Diagram

1. PIN DESCRIPTIONS (208 CABGA)



Number	Pin name	Type	Pin description
A1	PA.0	I/O	GPIO PORT A
C2	PA.1	I/O	GPIO PORT A
D4	PA.2	I/O	GPIO PORT A
B1	PA.3	I/O	GPIO PORT A
C1	PA.4	I/O	GPIO PORT A
D2	PA.5	I/O	GPIO PORT A
D3	VDD	-	Power supply
E4	PA.6	I/O	GPIO PORT A
D1	PA.7	I/O	GPIO PORT A
E2	FCSN	I	Internal Flash Chip Select Low: The internal flash is enabled for read/write access High: The internal flash is disabled.
E3	NC	-	No connection
F4	TEST1	I	Pull-down required for normal operation
E1	TEST2	I	Pull-down required for normal operation
F2	VSS	-	Ground
F3	XI	I	Oscillator (32.768KHz) for PLL
G4	XO	O	Oscillator (32.768KHz) for PLL
F1	TEST3	I	Pull-down required for normal operation
G2	PJ.0	I/O	GPIO PORT J
G3	PJ.1	I/O	GPIO PORT J
H4	PJ.2	I/O	GPIO PORT J
G1	PJ.3	I/O	GPIO PORT J
H2	VDD	-	Power supply
H3	PJ.4	I/O	GPIO PORT J
J4	PB.0	I/O	GPIO PORT B
H1	PB.1	I/O	GPIO PORT B
J2	PB.2	I/O	GPIO PORT B
J3	PB.3	I/O	GPIO PORT B
K4	VSS	-	Ground
J1	PB.4	I/O	GPIO PORT B
K2	PB.5	I/O	GPIO PORT B
K3	USB_DM	I/O	USB minus port
L4	USB_DP	I/O	USB plus port
K1	VDD_ADC	-	Power supply for ADC
L2	VSS_ADC	-	Ground for ADC
L3	AD_VREF	I	ADC reference voltage
M4	VDD_USB	-	Power supply for USB
L1	VSS_USB	-	Ground for USB
M2	VDD_PLL0	-	Power supply for PLL0
M3	CP0	-	Loop filter VCO input for PLL0
N4	CZ0	-	Loop filter pump output for PLL0
M1	VSS_PLL0	-	Ground for PLL0
N2	VDD_PLL1	-	Power supply for PLL1
N3	CP1	-	Loop filter VCO input for PLL1

N1	CZ1	-	Loop filter pump output for PLL1
P1	VSS_PLL1	-	Ground for PLL1
P2	MMC_DI/PC.0	I/O	MMC serial data input / GPIO PORT C
P3	MMC_DO/PC.1	I/O	MMC serial data output / GPIO PORT C
R1	MMC_SCLK/PC.2	I/O	MMC serial clock / GPIO PORT C
T1	IIC_SCL/PC.3	I/O	Serial clock for I^2C / GPIO PORT C
R2	IIC_SDA/PC.4	I/O	Serial data for I^2C / GPIO PORT C
R3	PC.5	I/O	GPIO PORT C
T2	UART_RX/PC.6	I/O	UART Rx input / GPIO PORT C
U1	VDD	-	Power supply
T3	UART_TX/PC.7	I/O	UART Tx output / GPIO PORT C
P4	INT8/PG.0	I	External interrupt 8 / GPIO PORT G
U2	INT9/PG.1	I	External interrupt 9 / GPIO PORT G
U3	SMC_CE2/PG.2	O	SmartMedia chip select 2 / GPIO PORT G
T4	ADC0//INT0/PD.0	I	ADC 0 input / External interrupt 0 / GPIO PORT D
R4	ADC1/INT1/PD.1	I	ADC 1 input / External interrupt 1 / GPIO PORT D
P5	VSS	-	Ground
U4	ADC2//INT2/PD.2	I	ADC 2 input / External interrupt 2 / GPIO PORT D
T5	ADC3//INT3/PD.3	I	ADC 3 input / External interrupt 3 / GPIO PORT D
R5	ADC4//INT4/PD.4	I	ADC 4 input / External interrupt 4 / GPIO PORT D
P6	ADC5//INT5/PD.5	I	ADC 5 input / External interrupt 5 / GPIO PORT D
U5	ADC6//INT6/PD.6	I	ADC 6 input / External interrupt 6 / GPIO PORT D
T6	ADC7//INT7/PD.7	I	ADC 7 input / External interrupt 7 / GPIO PORT D
R6	SMC_CE0/PH.0	O	SmartMedia chip select 0 / GPIO PORT H
P7	VDD	-	Power supply
U6	SMC_CE1/PH.1	O	SmartMedia chip select 1 / GPIO PORT H
T7	SMC_CLE/PH.2	O	SmartMedia command latch enable / GPIO PORT H
R7	SMC_ALE/PH.3	O	SmartMedia Address latch enable / GPIO PORT H
P8	SMC_BUSY/PH.4	I	SmartMedia busy status / GPIO PORT H
U7	SMC_WP/PH.5	I	SmartMedia write protect / GPIO PORT H
T8	SMC_RE/PH.6	O	SmartMedia read enable strobe signal/GPIO PORT H
R8	SMC_WE/PH.7	O	SmartMedia write enable strobe signal/GPIO PORT H
P9	VSS	-	Ground
U8	SMC_IO0/PI.0	I/O	SmartMedia I/O port / GPIO PORT I
T9	SMC_IO1/PI.1	I/O	SmartMedia I/O port / GPIO PORT I
R9	SMC_IO2/PI.2	I/O	SmartMedia I/O port / GPIO PORT I
P10	SMC_IO3/PI.3	I/O	SmartMedia I/O port / GPIO PORT I
U9	SMC_IO4/PI.4	I/O	SmartMedia I/O port / GPIO PORT I
T10	SMC_IO5/PI.5	I/O	SmartMedia I/O port / GPIO PORT I
R10	VDD	-	Power supply
P11	SMC_IO6/PI.6	I/O	SmartMedia I/O port / GPIO PORT I
U10	SMC_IO7/PI.7	I/O	SmartMedia I/O port / GPIO PORT I
T11	PE.0	I/O	GPIO PORT E
R11	PE.1	I/O	GPIO PORT E
P12	PE.2	I/O	GPIO PORT E
U11	PE.3	I/O	GPIO PORT E
T12	VSS	-	Ground

R12	IIS_WCK0/PK.0	O	Word select clock for I^{2}S0 / GPIO PORT K
P13	IIS_BCK0/PK.1	O	Bit serial clock for I^{2}S0 / GPIO PORT K
U12	IIS_DATA0/PK.2	I/O	Serial data for I^{2}S0 / GPIO PORT K
T13	IIS_WCK1/PK.3	O	Word select clock for I^{2}S1 / GPIO PORT K
R13	IIS_BCK1/PK.4	O	Bit serial clock for I^{2}S1 / GPIO PORT K
U13	IIS_DATA1/PK.5	I/O	Serial data for I^{2}S1 / GPIO PORT K
U14	IIS MCK/PK.6	O	Master clock for I^{2}S / GPIO PORT K
T14	VDD	-	Power supply
R14	TEST4	I	Pull-down required
U15	TEST5	I	Pull-up required
U16	/TRST	I	Reset input for TAP controller
T15	TCK	I	TAP controller clock input
R15	TDI	I	TAP controller data input
T16	JTAG	I	JTAG interface mode selection
U17	TMS	I	TAP controller test mode selection
R16	UCLK	I	Serial clock input
P14	TEST6	O	No connection
T17	TEST7	O	No connection
R17	TDO	O	TAP controller data output
P16	VSS	-	Ground
P15	TEST8	I	Pull-down required
N14	TEST9	I	Pull-down required
P17	TEST10	I	Pull-down required
N16	TEST11	I	Pull-down required
N15	TEST12	O	No connection
M14	TEST13	O	No connection
N17	TEST14	O	No connection
M16	TEST15	O	No connection
M15	PF.0/LCD_DATA.8	I/O	GPIO PORT F / LCD higher byte data output
L14	PF.1/LCD_DATA.9	I/O	GPIO PORT F / LCD higher byte data output
M17	VDD	-	Power supply
L16	PF.2/LCD_DATA.10	I/O	GPIO PORT F / LCD higher byte data output
L15	PF.3/LCD_DATA.11	I/O	GPIO PORT F / LCD higher byte data output
K14	PF.4/LCD_DATA.12	I/O	GPIO PORT F / LCD higher byte data output
L17	PF.5/LCD_DATA.13	I/O	GPIO PORT F / LCD higher byte data output
K16	PF.6/LCD_DATA.14	I/O	GPIO PORT F / LCD higher byte data output
K15	VSS	-	Ground
J14	PF.7/LCD_DATA.15	I/O	GPIO PORT F / LCD higher byte data output
K17	LCD_DATA.0	O	LCD lower byte data output
J16	LCD_DATA.1	O	LCD lower byte data output
J15	LCD_DATA.2	O	LCD lower byte data output
H14	LCD_DATA.3	O	LCD lower byte data output
J17	LCD_DATA.4	O	LCD lower byte data output
H16	LCD_DATA.5	O	LCD lower byte data output
H15	VDD	-	Power supply
G14	LCD_DATA.6	O	LCD lower byte data output
H17	LCD_DATA.7	O	LCD lower byte data output

G16	LCD_BIAS	O	LCD AC bias
G15	LCD_FCLK	O	LCD frame synchronization clock
F14	LCD_LCLK	O	LCD line synchronization clock
G17	VSS	-	Ground
F16	LCD_PCLK	O	LCD pixel synchronization clock
F15	/RESET	I	Reset input
E14	/RESETO	O	Reset output
F17	TEST16	O	No connection
E16	TEST17	I	Pull-down required
E15	BA0	O	External SDRAM bank select 0
E17	BA1	O	External SDRAM bank select 1
D17	/CAS	O	External SDRAM column address strobe
D16	VDD	-	Power supply
D15	/DCS	O	External SDRAM chip select
C17	/DWE	O	External SDRAM write enable
B17	/RAS	O	External SDRAM row address strobe
C16	/SCS0	O	External SRAM chip select 0
C15	/SCS1	O	External SRAM chip select 1
B16	/SCS2	O	External SRAM chip select 2
A17	VSS	-	Ground
B15	/SCS3	O	External SRAM chip select 3
D14	/SOE	O	External SRAM output enable
A16	/SWE	O	External SRAM write enable
A15	CKE	O	External SDRAM clock enable
B14	DQM	O	External SDRAM data input/output mask
C14	VDD		Power supply
D13	CLKOUT	O	Internal system clock output
A14	EA.0	O	External address bus for off-chip memory
B13	EA.1	O	External address bus for off-chip memory
C13	EA.2	O	External address bus for off-chip memory
D12	EA.3	O	External address bus for off-chip memory
A13	EA.4	O	External address bus for off-chip memory
B12	VSS	-	Ground
C12	EA.5	O	External address bus for off-chip memory
D11	EA.6	O	External address bus for off-chip memory
A12	EA.7	O	External address bus for off-chip memory
B11	EA.8	O	External address bus for off-chip memory
C11	EA.9	O	External address bus for off-chip memory
D10	VDD	-	Power supply
A11	EA.10	O	External address bus for off-chip memory
B10	EA.11	O	External address bus for off-chip memory
C10	EA.12	O	External address bus for off-chip memory
D9	EA.13	O	External address bus for off-chip memory
A10	EA.14	O	External address bus for off-chip memory
B9	VSS	-	Ground
C9	EA.15	O	External address bus for off-chip memory
D8	EA.16	O	External address bus for off-chip memory

A9	EA.17	O	External address bus for off-chip memory
B8	EA.18	O	External address bus for off-chip memory
C8	EA.19	O	External address bus for off-chip memory
D7	VDD	-	Power supply
A8	EA.20	O	External address bus for off-chip memory
B7	ED.0	I/O	External data bus for off-chip memory
C7	ED.1	I/O	External data bus for off-chip memory
D6	ED.2	I/O	External data bus for off-chip memory
A7	ED.3	I/O	External data bus for off-chip memory
B6	ED.4	I/O	External data bus for off-chip memory
C6	VSS	-	Ground
D5	ED.5	I/O	External data bus for off-chip memory
A6	ED.6	I/O	External data bus for off-chip memory
B5	ED.7	I/O	External data bus for off-chip memory
C5	ED.8	I/O	External data bus for off-chip memory
A5	ED.9	I/O	External data bus for off-chip memory
A4	VDD	-	Power supply
B4	ED.10	I/O	External data bus for off-chip memory
C4	ED.11	I/O	External data bus for off-chip memory
A3	ED.12	I/O	External data bus for off-chip memory
A2	ED.13	I/O	External data bus for off-chip memory
B3	ED.14	I/O	External data bus for off-chip memory
C3	ED.15	I/O	External data bus for off-chip memory
B2	VSS	-	Ground

2. APPLICATION

All pins in TCC731 are same as those in TCC730 except the followings. Please refer to TCC730 data sheet for more details.

Number	Pin name	Type	Pin description
E2	FCSN	I	Internal Flash Chip Select Low: The internal flash is enabled for read/write access High: The internal flash is disabled.

User must connect the FCSN with /SCS0 to use internal flash as program ROM.
In case of development board, there must be switches or jumpers so that the /SCS0 can be connected with either external SRAM or internal flash exclusively.

The configurations of these are illustrated in the following figures.

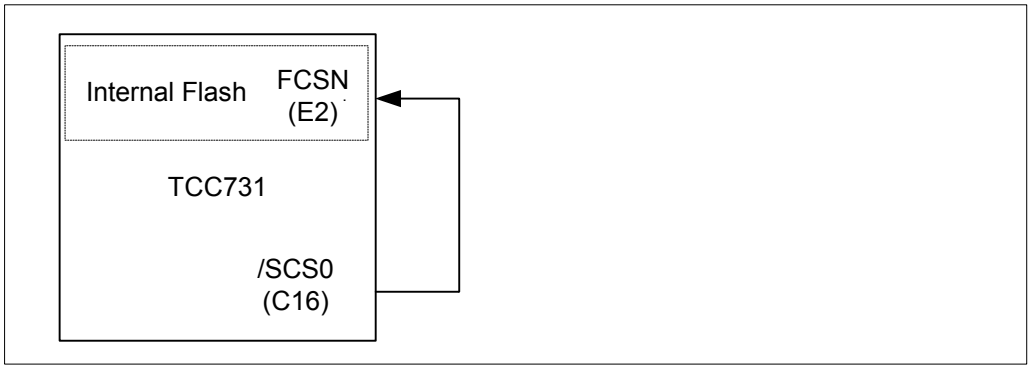


Figure 2.1 The configuration for application set board

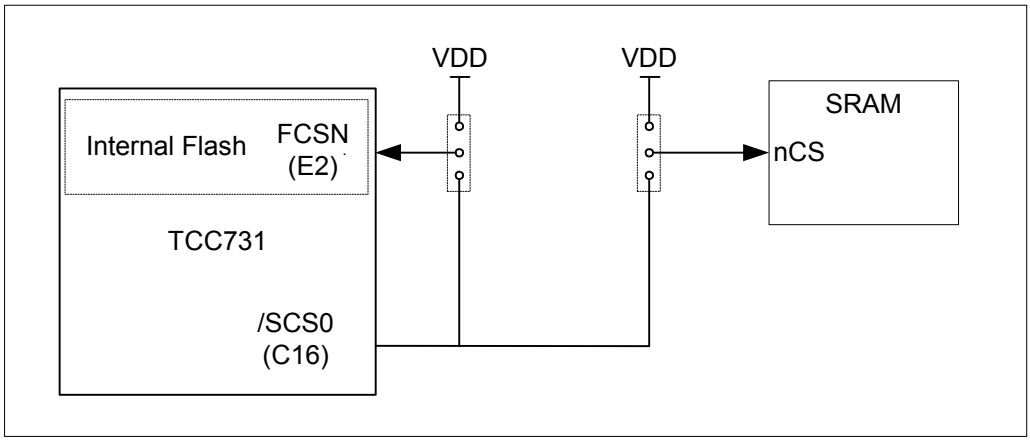


Figure 2.2 The configuration for development board

3. ELECTRICAL DATA

Table 3.1 Absolute Maximum Ratings

(T_A = 25ºC)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}	-	-0.3 to +4.5	V
Input voltage	V_I	-	-0.3 to V_{DD} + 0.3	V
Output voltage	V_O	-	-0.3 to V_{DD} + 0.3	V
Output current hugh	I_{OH}	One I/O pin active	-15	mA
		All I/O pins active	-100	
Output current low	I_{OL}	One I/O pin active	+20	mA
		Total pin current	+150	
Operating temperature	T_A	-	-40 to +85	ºC
Storage temparature	T_{STG}	-	-65 to +150	ºC

Table 3.2 DC Electrical Characteristics

(T_A = -40ºC to +85ºC, V_{DD} = 2.7V to 3.6V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	f_{OSC} = 40MHz	2.7	-	3.6	V
Input high voltage	V_{IH1}	RESET	0.85 V_{DD}	-	V_{DD}	V
	V_{IH2}	All input pins except V_{IH0}, V_{IH1}, and V_{IH3}.	0.8 V_{DD}			
	V_{IH3}	XI, TEST3	V_{DD} – 0.5			
Input low voltage	V_{IL1}	RESET	0	-	0.2 V_{DD}	V
	V_{IL2}	All input pins except V_{IL1}, V_{IL3}.			0.3 V_{DD}	V
	V_{IL3}	XI, TEST3			0.4	V
Output high voltage	V_{OH1}	V_{DD} = 2.7V to 3.6V I_{OH} = -1mA	V_{DD} – 1.0	-	-	V

Output low voltage	V_{OL1}	V_{DD} = 2.7V to 3.6V I_{OH} = 5mA All output pins	-	-	1.0	V
Input high leakage current	I_{LIH1}	V_{IN} = V_{DD} All input pins except I_{LIH2}.	-	-	3	uA
	I_{LIH2}	V_{IN} = V_{DD} XI, TEST3			20	
Input low leakage current	I_{LIL1}	V_{IN} = 0V All input pins except I_{LIL2}.	-	-	-3	
	I_{LIL2}	V_{IN} = 0V XI, TEST3, RESET			-20	
Output high leakage current	I_{LOH}	V_{OUT} = V_{DD} All I/O pins and output pins	-	-	5	
Output low leakage current	I_{LOL}	V_{OUT} = 0V All I/O pins and output pins	-	-	-5	
Pull-up resister	R_{L1}	V_{IN} = 0V, V_{DD} = 3V, T_A = 25ºC All input pins except R_{L2}.	50	100	200	KΩ
	R_{L2}	V_{IN} = 0V, V_{DD} = 3V, T_A = 25ºC RESET only	100	250	400	
Supply current	I_{DD1}	V_{DD} = 3V ± 10% 40MHz crystal oscillator	-	45	80	mA
		V_{DD} = 3V ± 10% 32.768KHz crystal oscillator		150	300	uA
	I_{DD2}	Idle mode: V_{DD} = 3V ± 10% 40MHz crystal oscillator	-	8	16	mA
		Idle mode: V_{DD} = 3V ± 10% 32.768KHz crystal oscillator		15	30	uA
	I_{DD3}	Stop mode V_{DD} = 3V ± 10%	-	1	10	uA

Table 3.3 AC Electrical Characteristics

(T_A = -40ºC to +85ºC, V_{DD} = 2.7V to 3.6V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt input high, low width	t_{INTH}, t_{INTL}	PG.0-PG.1, PD.0-PD.7 at V_{DD} = 3V	200	-	-	ns
RESET input low width	t_{RSL}	V_{DD} = 3V	10	-	-	us

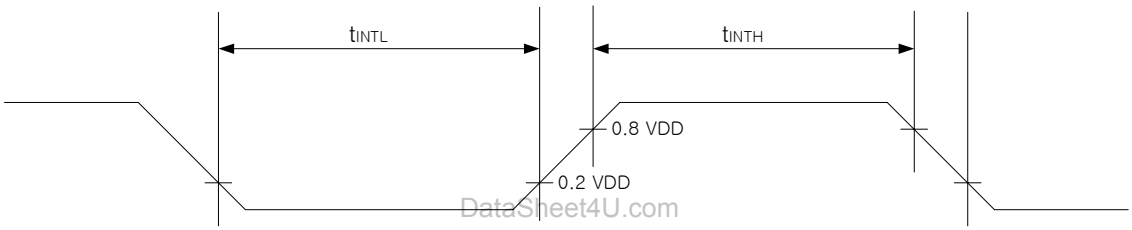


Fig 3.1 Input Timing for External Interrupts (PD, PG)

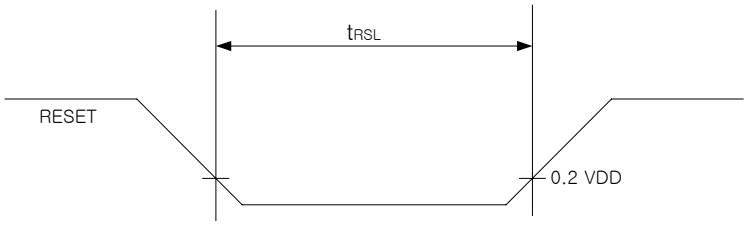


Fig 3.2 Input Timing for RESET

Table 3.4 Input/Output Capacitance

(T_A = -40ºC to +85ºC, V_{DD} = 0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	f = 1MHz, unmeasured pins are returned to V_{SS}.	-	-	10	pF
Output capacitance	C_{OUT}					
I/O capacitance	C_{IO}					

Table 3.5 AC Electrical Characteristics

(T_A = -40ºC to +85ºC, V_{DD} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Resolution			-	10		
Integral Linearity Error	ILE	AV_{REF} = 3.3V	-	-	±1	
Differential Linearity Error	DLE	AV_{SS} = 0V	-	-	±1	LSB
Offset Error of Top	EOT	-	-	±1	±2	
Offset Error of Bottom	EOB	-	-	±0.5	±2	
Conversion Time	t_{CON}	-	20	-	-	us
Analog input voltage	V_{IAN}	-	AV_{SS}	-	AV_{REF}	V
Analog input impedance	R_{AN}	-	2	1000		MΩ
Analog reference voltage	AV_{REF}	-	V_{DD}	-	V_{DD}	V
Analog ground	AV_{SS}	-	V_{SSv}	-	V_{SS}	V
Analog input current	I_{ADIN}	AV_{REF} = V_{DD} = 3.3V	-	-	10	uA
Analog block current	I_{ADC}	AV_{REF} = V_{DD} = 3.3V		1	3	mA
		AV_{REF} = V_{DD} = 3V		0.5	1.5	mA

Table 3.6 Data Retention Supply Voltage in Stop Mode

(T_A = -40ºC to +85ºC, V_{DD} = 2.7V to 3.6V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}		2	-	3.6	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2V	-	-	1	uA

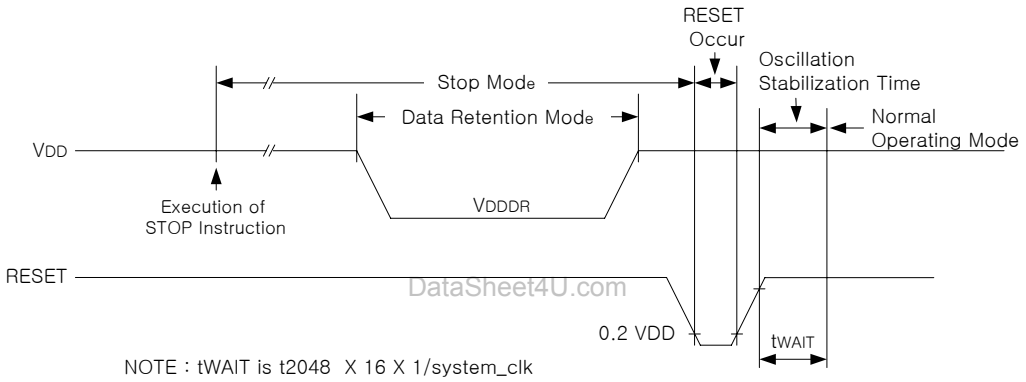
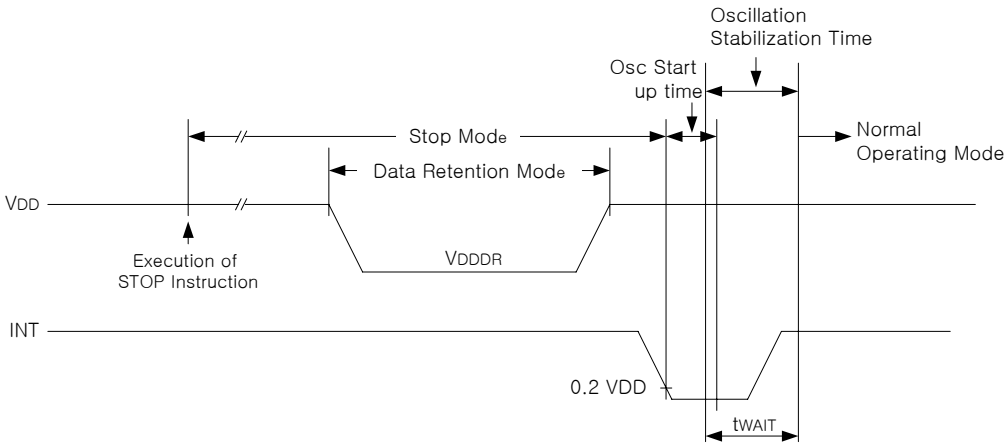


Fig 3.3 Stop Mode Release Timing When Initiated by a RESET



NOTE : tWAIT is 2048 X 16 X 1/system_clk. The value of 2048 which is selected for the clock source of the basic timer counter can be changed. then the value of tWAIT wil be changed.

Fig 3.4 Stop Mode Release Timing When Initiated by Interrupts

Table 3.7 Synchronous SIO Electrical Characteristics

(T_A = -40ºC to +85ºC, V_{DD} = 2.7V to 3.6V, V_{SS} = 0V, System Clock = 30MHz)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
MMC_SCLK cycle time	t_{CYC}	-	200	-	-	ns
Serial clock high width	t_{SCKH}	-	60	-	-	
Serial clock low width	t_{SCKL}	-	60	-	-	
Serial output data setup time	t_{OD}	-	-	-	50	
Serial input data setup time	t_{ID}	-	40	-	-	
serial input data hold time	t_{IH}	-	100	-	-	

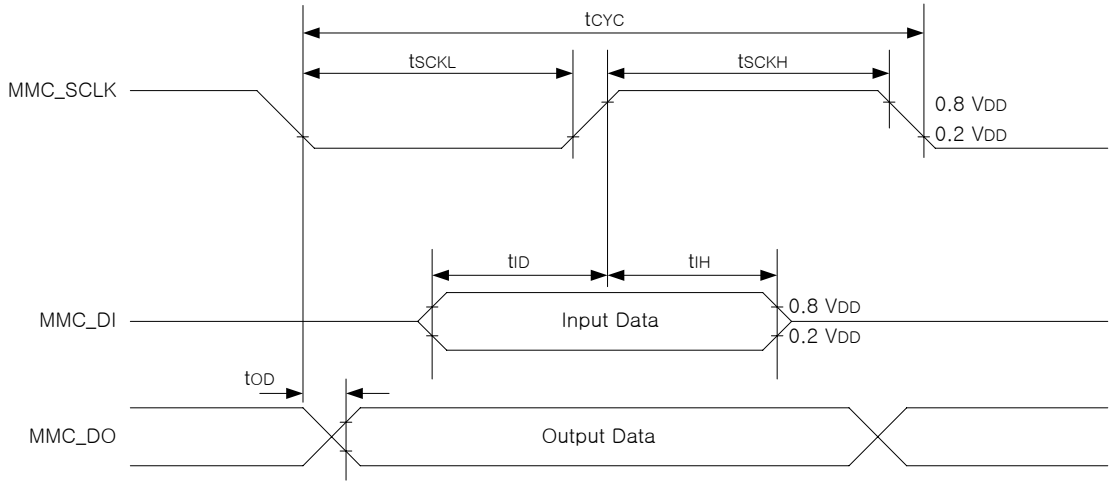
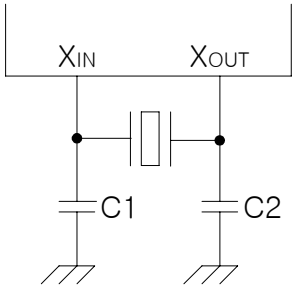
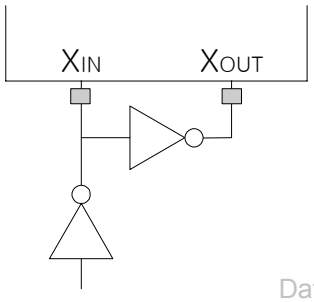


Fig 3.5 Serial Data Transfer Timing

Table 3.8 Oscillator Frequency

(T_A = -40ºC to +85ºC, V_{DD} = 2.7V to 3.6V)

Oscillator	Clock Circuit	Test Conditions	Min	Typ	Max	Unit
Crystal		Oscillation frequency	32	32.768	35	KHz
		Stabilization time	-	1	3	s
External Clock		X_{IN} input frequency	32	-	35	KHz
		X_{IN} input high and low level width(t_{XH}, t_{XL})	14	-	1	us

NOTE : Oscillation stabilization time is the time that the amplitude of a oscillator input reaches to 0.8 V_{DD}.

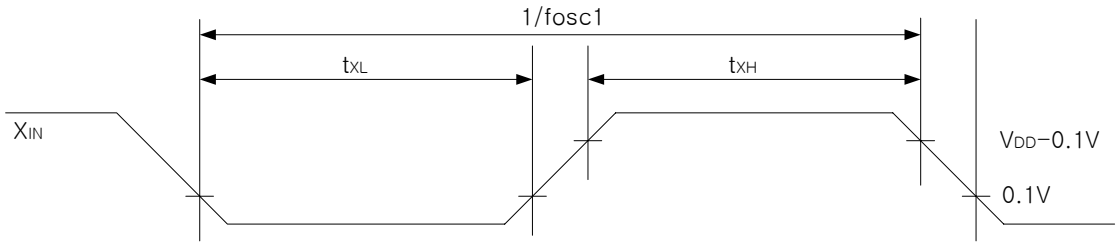


Fig 3.6 Clock Timing Measurement at X_{IN}

Table 3.9 External SDRAM Access Electrical Characteristics

(T_A = -40ºC to +85ºC, V_{DD} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ICLK cycle time	t_{CYC}	-	12.5	-	-	ns
NDCS ready time	t_{Dndcs}	-	3	-	-	
NRAS ready time	t_{Dnras}	-	3	-	-	
NCAS ready time	t_{Dncas}		3.3	-	-	
NDWE ready time	t_{Dndwe}		3	-	-	
BA ready time	t_{Dba}	-	3	-	-	
EXTDA ready time	t_{Dextda}	-	3.8	-	-	
DATA ready time	t_{Ddbo}		3.4	-	-	
DATA setup time	t_{Ddbi}	-	4.8	-	-	

SDRAM Read Timing Diagram

(tRAS= 4cyc, tRP=2cyc, tRCD=2cyc : burst-4 access)
(Output load = 30pF)

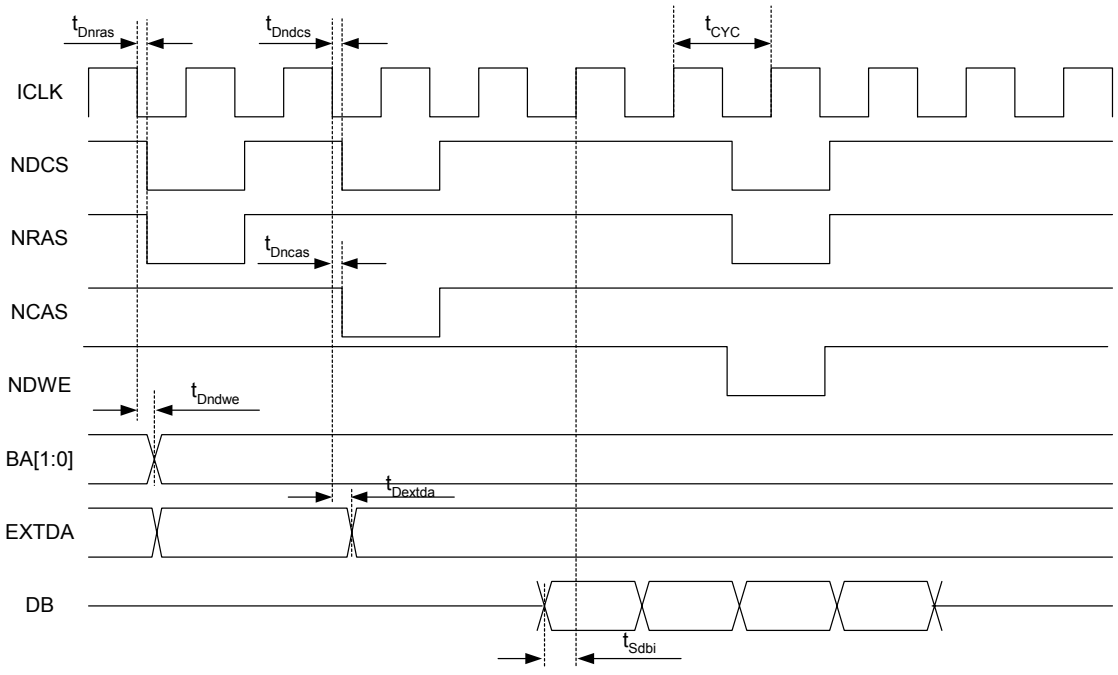


Fig 3.7 SDRAM Read Timing

SDRAM Write Timing Diagram

(tRAS= 4cyc, tRP=2cyc, tRCD=2cyc : burst-4 access)
(Output load = 30pF)

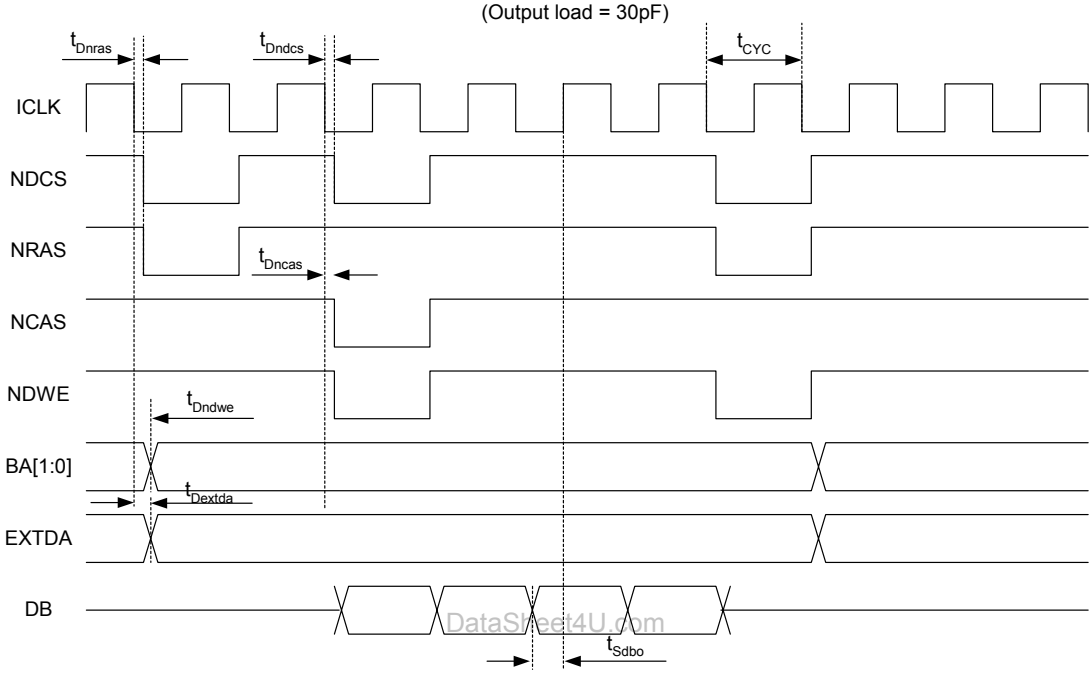


Fig 3.8 SDRAM Write Timing

Table 3.10 External SRAM Access Electrical Characteristics

(T_A = -40ºC to +85ºC, V_{DD} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CS ready time	T_{DCS}		3			ns
CS low duration	t_{CSlow}	0 wait, System Clock = 80MHz	50(+T_W)	-	-	
Address ready time	t_{ADS}	-	0	-	-	
OE falling delay	t_{DOE1}	-	0	-	-	
OE rising delay	t_{DOE2}	-	-2	-	2	
NDWE ready time	t_{Dndwe}	-	3	-	-	
DATA ready time	t_{DAS}	0 wait, System Clock = 80MHz	-	-	8(+T_W)	
DATA hold time	t_{DAH}	-	4	-	-	

SRAM/NOR FLASH Read Timing Diagram

(Read Cache 1 Line : 4 word access)
(Output load = 30pF)

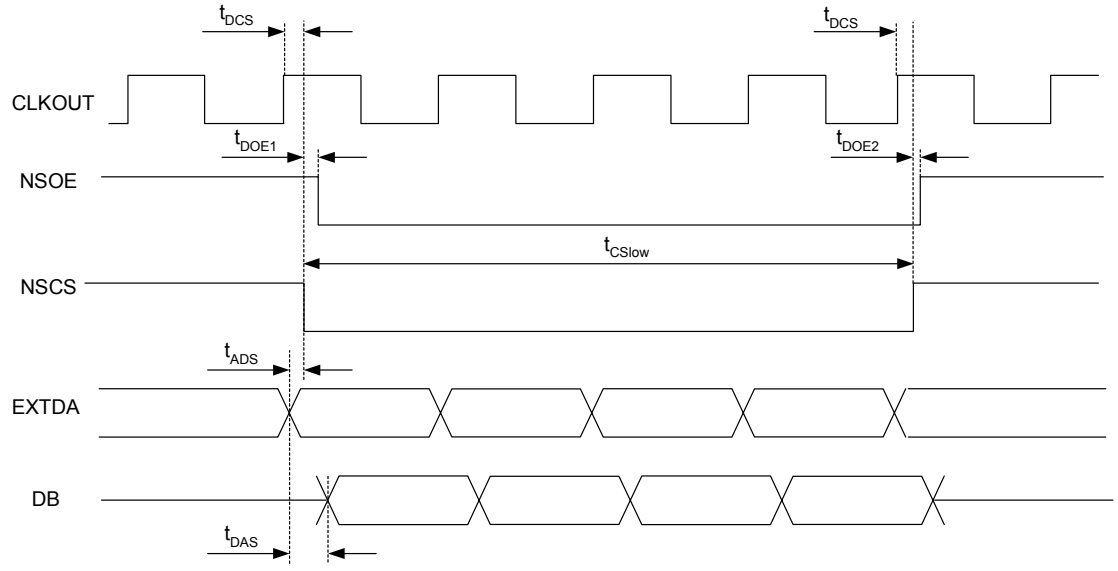


Fig 3.9 SRAM Read Timing

SRAM/NOR FLASH Write Timing Diagram

(Read Cache 1 Line : 4 word access)
(Output load = 30pF)

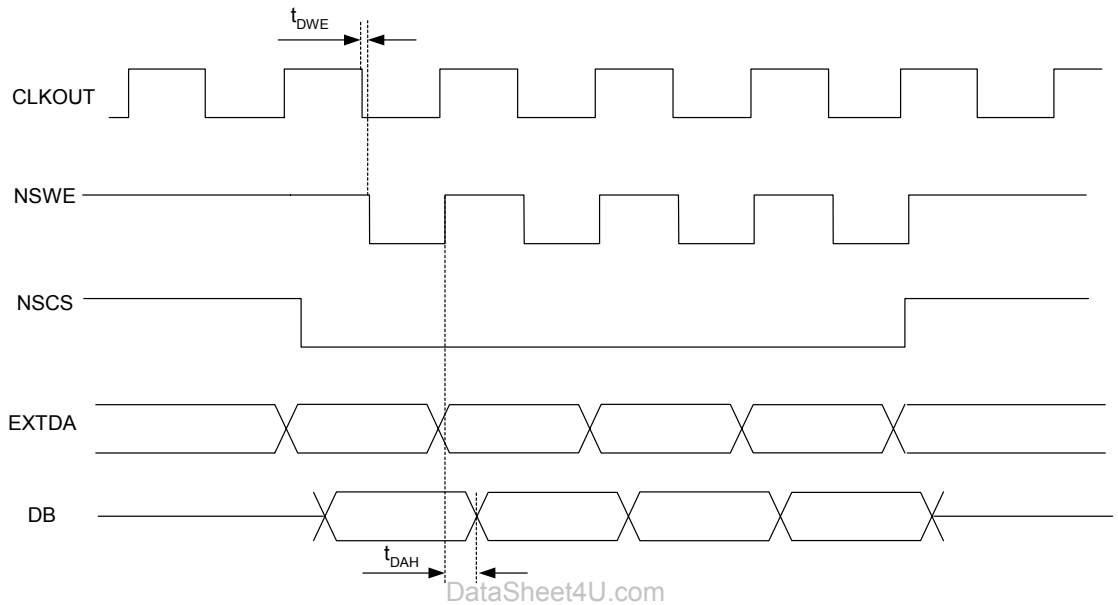


Fig 3.10 SRAM Write Timing

SRAM/NOR FLASH Write Timing Diagram

(Wait Cycle = 1, 2, 3)
(Output load = 30pF)

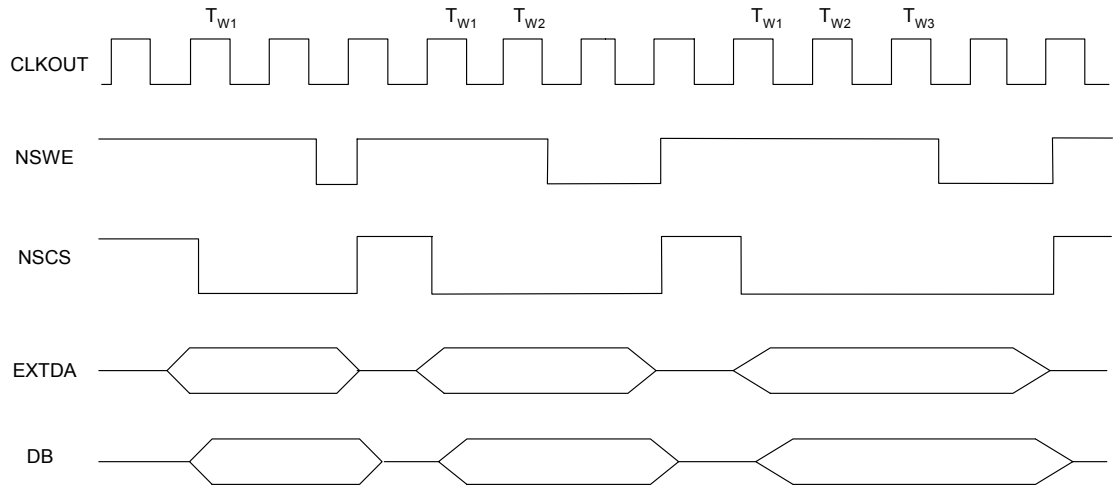


Fig 3.11 SRAM Write Timing (Wait Cycle = 1, 2, 3)

DMA Transfer from External SRAM to Internal SRAM Timing Diagram

(Output load = 30pF)

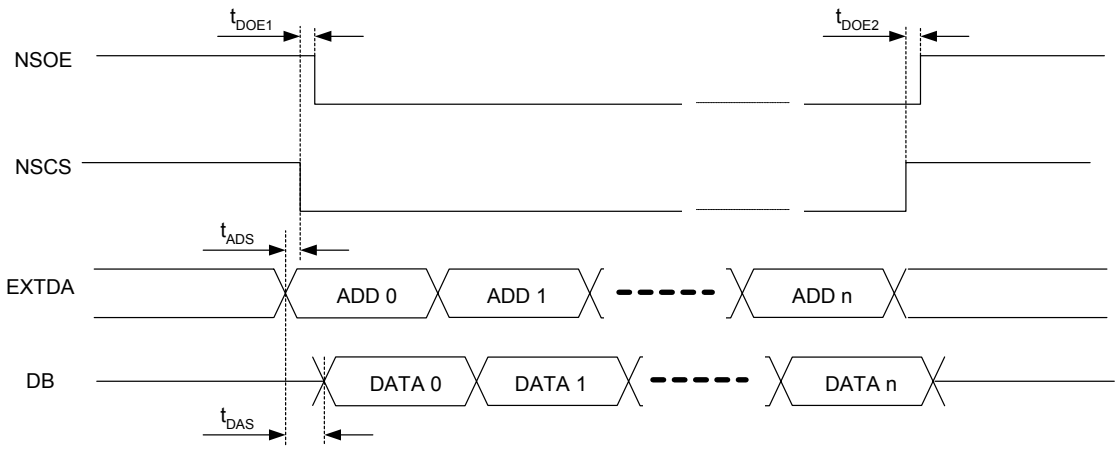
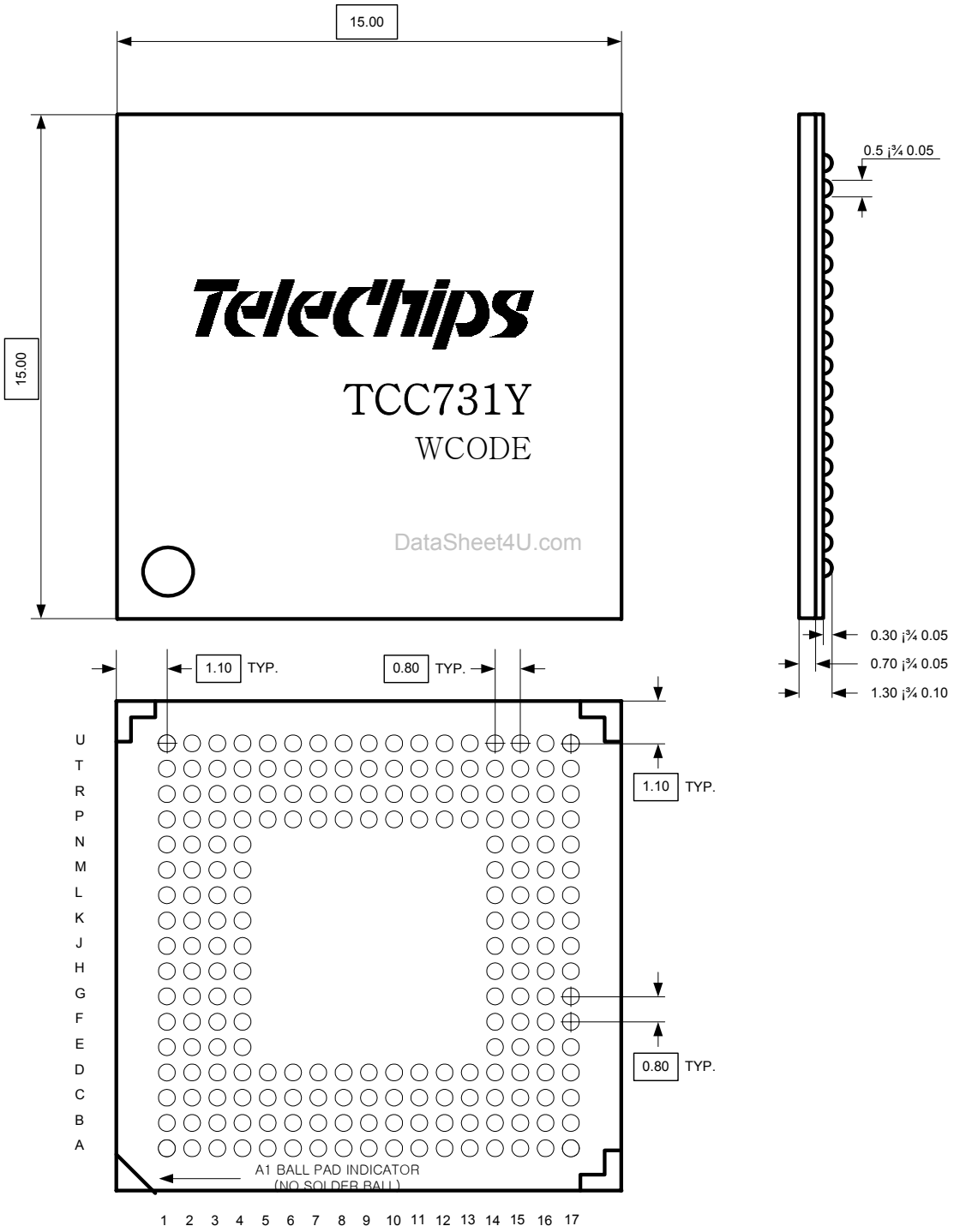


Fig 3.12 DMA Transfer Timing

4. PACKAGE DIMENSION

4.1 208 Pin FBGA



Dimension : mm

Revision History

V1.00	Apr, 21, 2003	First released.