M54959P

PLL FREQUENCY SYNTHESIZER FOR PERSONAL RADIOS

DESCRIPTION

The M54959P is a semiconductor integrated circuit consisting of a PLL frequency synthesizer for use in personal radio equipment. It contains an 1/128 and 1/129 2-modulus prescaler allowing the direct synthesis of local oscillator frequency up to 500MHz.
The reference frequency is provided by a 12.8MHz crystal oscillator.

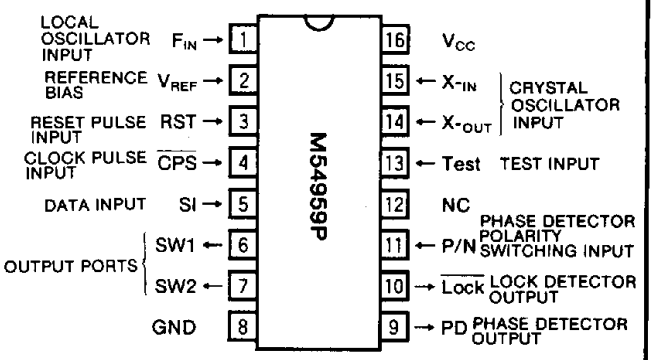
FEATURES

- Built-in 1/128 and 1/129 2-modulus prescaler (fmax=500MHz)
- Low power consumption (I_{CC}=20mA, at V_{CC}= 5 V)
- Reference frequency selectable from four values (25k, 12.5k, 6.25k, 5 k)
- Wide range of division ratio (16384~131071, binary coded)
- Serial data input (3 data-transfer lines)
- PLL Lock/unlock status display output
- Output-ports state can be set by date from a controller

APPLICATION

Personal radio

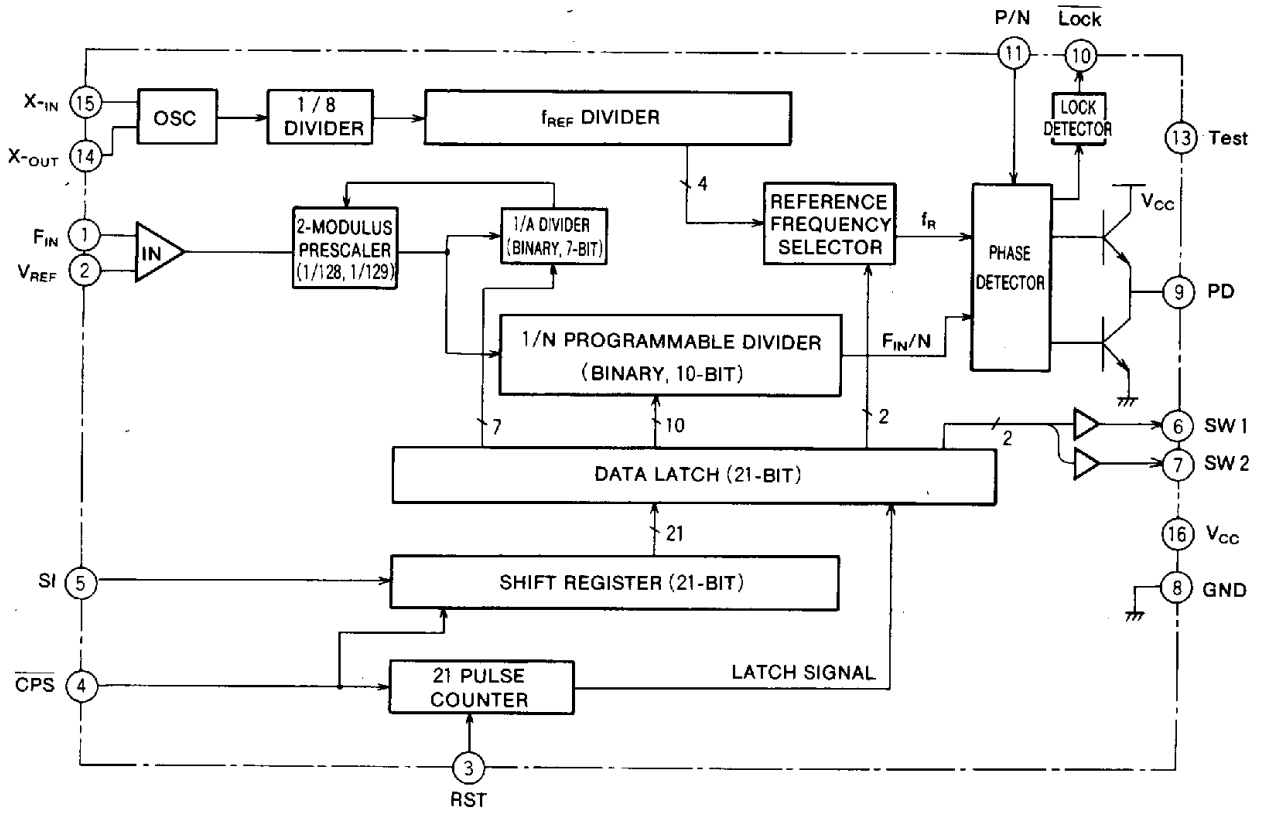
PIN CONFIGURATION (TOP VIEW)



Outline 16P4

NC : No connection

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

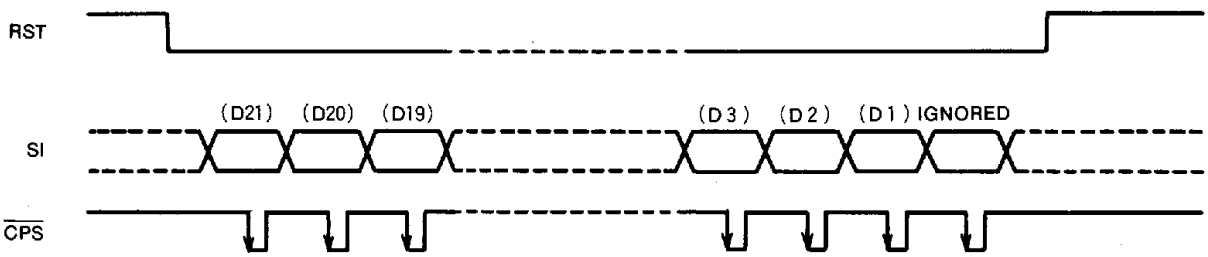
PIN DESCRIPTION

No.	Symbol	Pin name	Description
1	F_{IN}	Local oscillator input	Local oscillator frequency (V.C.O) input. f_{max}=500MHz
2	V_{REF}	Reference bias	Ground through a 1000pF capacitor
3	RST	Reset pulse input	Reset pulse input for 21-pulse counter
4	$\overline{CPS}$	Clock pulse input	Clock pulse input for shift register
5	SI	Data input	Data input for shift register
6	SW1	Output port	Open collector output port. State can be set by data from a controller.
7	SW2		
8	GND	GND	0 V
9	PD	Phase detector output	Three-state
10	$\overline{Lock}$	Lock detector output	Low when PLL locked, and high when unlocked. Open collector.
11	P/N	Phase detector polarity switching	When high, PD goes high as the phase advances and low as the phase delays. When low, PD goes low as the phase advances, and high as the phase delays.
12	NC	No connection	Open or GND
13	Test	Test input	Normally set low. When set high, f_R (reference frequency) is output from SW1 (pin 6), and f_{IN}/N (programmable divider output) is output from SW2 (pin 7).
14	$X\text{-}_{OUT}$	Crystal oscillator input	Apply the output from the 12.8MHz reference oscillator to $X\text{-}_{IN}$. A crystal resonator can also be connected.
15	$X\text{-}_{IN}$		
16	V_{CC}	Power supply pin	4.5~5.5V

FUNCTION

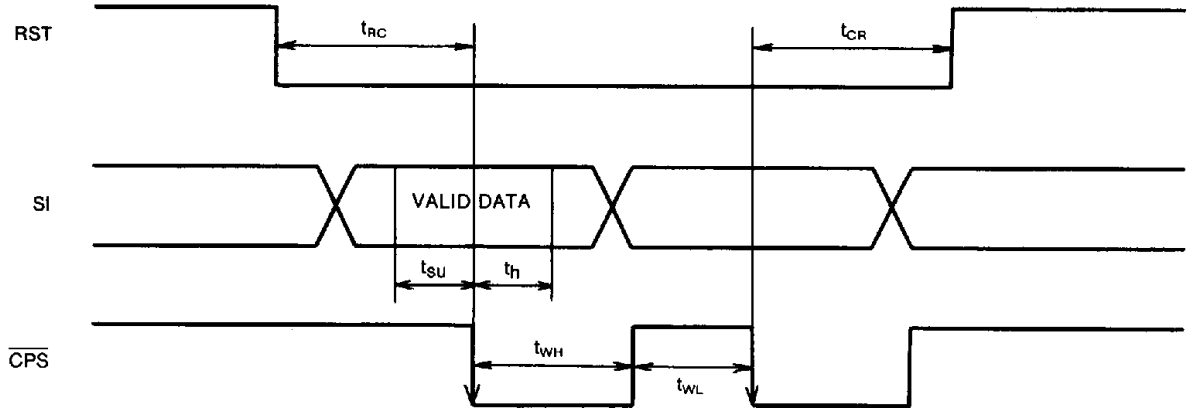
1. DATA INPUT

Configuration of input signal



Note 1 : Data at input SI is read into shift register sequentially by the falling edge of the clock signal at input $\overline{CPS}$.
2 : All data (N value, port, reference frequency) are set by the falling edge of the 21st clock pulse at $\overline{CPS}$.
Additional pulses at CPS are ignored.
3 : When RST is high, inputs are accepted at neither $\overline{CPS}$ nor SI.

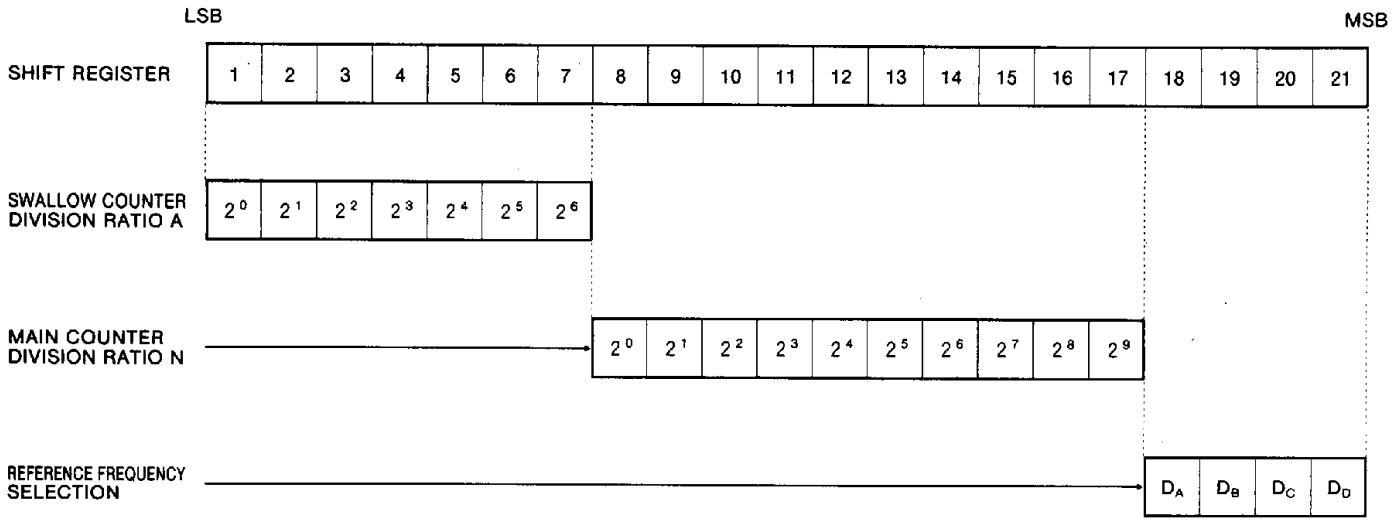
Timing of input signal



$t_{su}=t_h=t_{WH}=t_{WL}=10\mu S$ min.

$t_{RC}=t_{CR}=20\mu S$ min.

2. BIT CONFIGURATION OF SHIFT REGISTER



Note 4 : Total division ratio M is given by M=A+128N.

Note 5 : The reference frequency is selected by D_A and D_B.

Data		Reference
D_A	D_B	frequency
L	L	50k
H	L	25k
L	H	12.5k
H	H	6.25k

Note 6 : The output port is selected by DC and DD.

Data		Output port	
D_C	D_D	SW1	SW2
L	L	L	L
H	L	H	L
L	H	L	H
H	H	H	H

3. DATA CODING EXAMPLE

Reference freqency 6.25kHz, M=76892, SW 1 ="H", SW 2 ="L"

LSB

SHIFT REGISTER	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
DATA	L	L	H	H	H	L	H	L	L	L	H	H	L	H	L	L	H	H	H	H	L

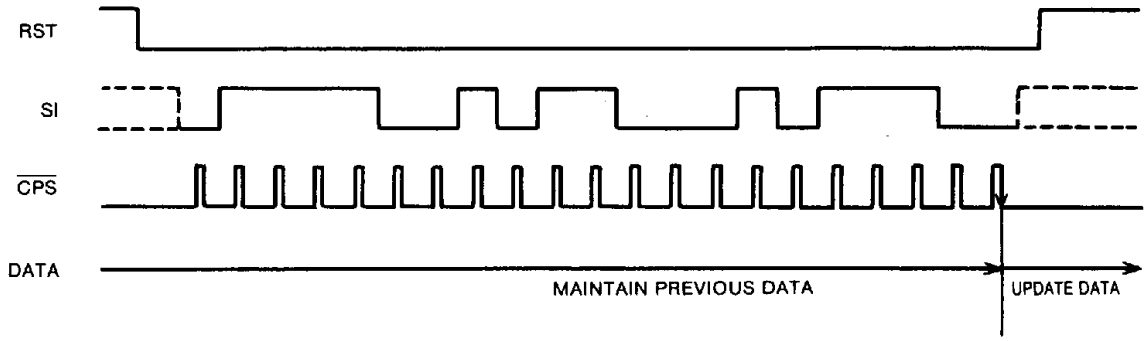
DIVISION RATIO OF SWALLOW COUNTER
$A=2^2+2^3+2^4+2^6=92$

DIVISION RATIO OF MAIN COUNTER
$N=2^3+2^4+2^6+2^9=600$

REFERENCE FREQUENCY SELECT 6.25kHz

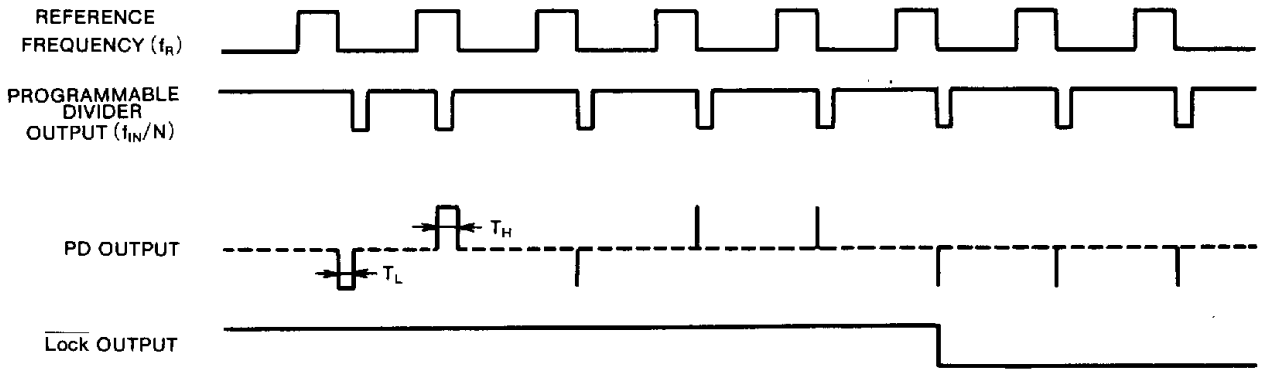
SW1 IS SET HIGH

SW2 IS SET LOW



Note 7 : Total division ratio is set by M=A+128N=92+128×600=76892.
8 : When PLL is locked, f_{VCO}=6.25×76892=480575kHz
=480.575MHz

4. PD AND $\overline{Lock}$ WAVEFORMS

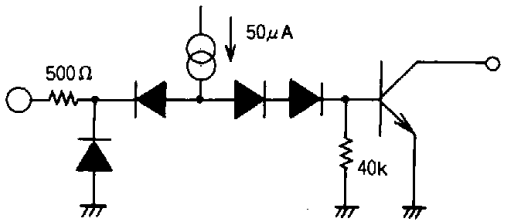


Note 9 : When the phase of programmable divider output f_{IN}/N is behind the phase of reference freqency f_R, PD is low; when $f_{IN/N}$ is ahead of f_R, PD is high.
10 : Broken lines indicate the high impedance state.
11 : If phase differnces T_L and T_H continue at less than 625ns for more than three cycles of reference frequency f_R, $\overline{LOCK}$ becomes low.

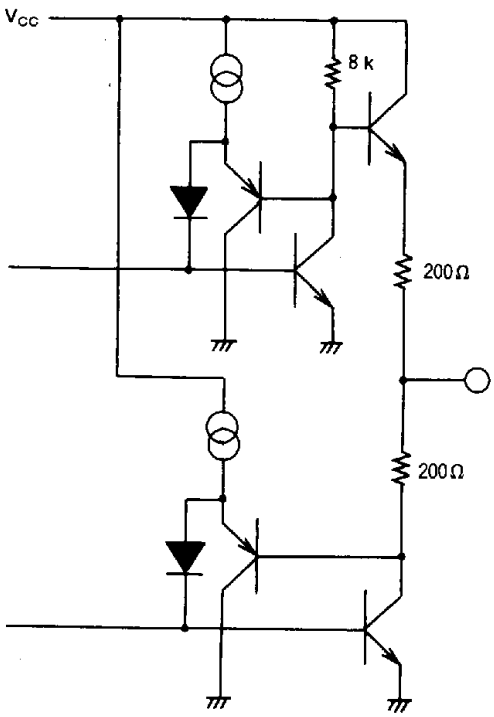
※The above description applies when input P/N (pin 11) is high.
When P/N is low, the output at PD is inverted.

I/O CIRCUITS

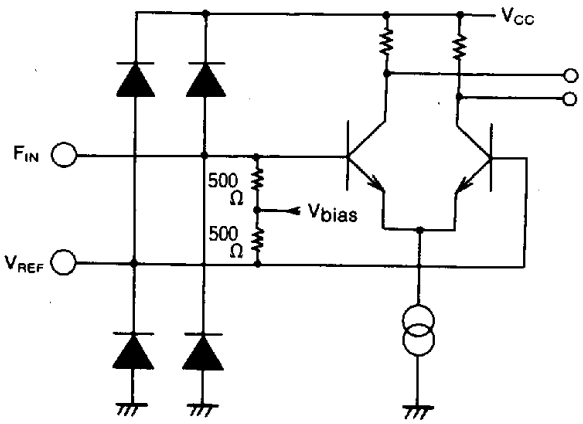
1 RST, $\overline{CPS}$, SI, P/N, and Test Inputs



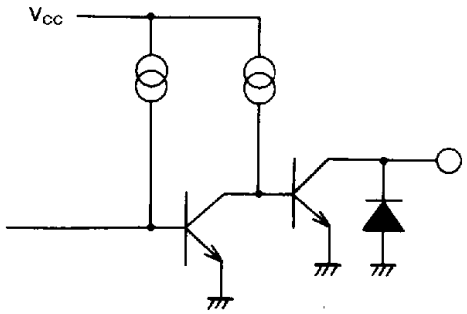
2 PD Output



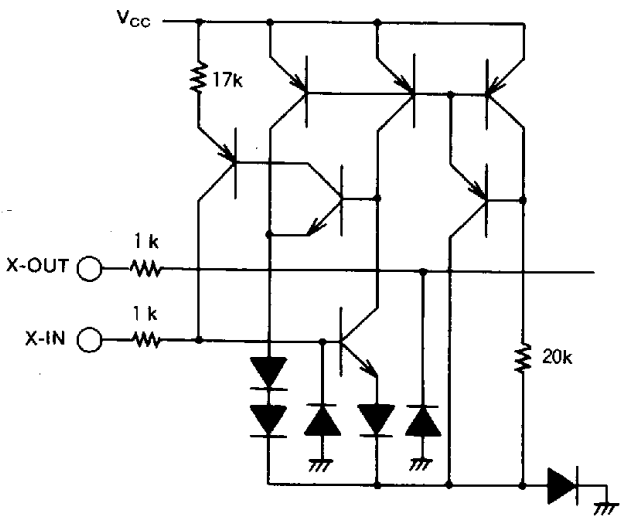
3 F_{IN}, and V_{REF} Inputs



4 SW1, SW2, and $\overline{Lock}$ Outputs



5 OSC Circuit



Note 12 : Resistance and current values are typical at V_{CC}= 5 V, T_a=25℃.

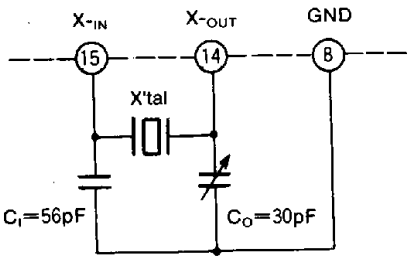
ABSOLUTE MAXIMUM RATINGS (T_a = −20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings		Unit	Remarks
			Min	Max		
V_{CC}	Supply voltage		−0.5	6.0	V	
V_I	Input voltage	All inputs	−0.5	6.0	V	
V_O	Output voltage	All outputs	−0.5	6.0	V	
P_d	Power dissipation	T_a =75℃		500	mW	Package permissible power dissipation
Topr	Operating temperature		−20	+75	℃	
Tstg	Storage temperature		−40	+125	℃	

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4.5~5.5V, T_a = −20~+75℃ unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit	Remarks
			Min	Typ	Max		
V_{CC}	Supply voltage		4.5	5	5.5	V	
V_{IN}	Input amplitude	F_{IN} =100~1000MHz	200		800	mV_{P-P}	
F_{IN1}	Input frequency	V_{IN} =200~800mV_{P-P}	100		500	MHz	
I_{OL}	Low-level output current	SW1, SW2, and Lock ontputs			5	mA	
V_{X-IN}	X_{-IN} input amplitude	Note 14	1		2	V_{P-P}	Sine wave
f_{OSC}	Reference oscillator frequency			12.8		MHz	

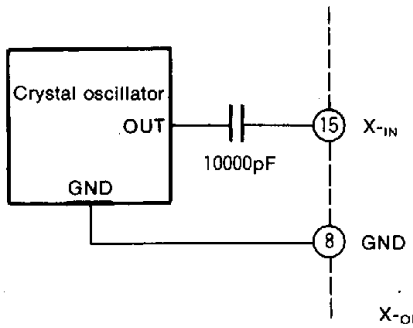
Note 13 : Cristal oscillator circuit



Lpad capacitance of crystal 20pF

Effective resistance less than 100Ω

Note 14 : Cristal oscillator circuit



X_{-OUT} (pin 14) is left open.

ELECTRICAL CHARACTERISTICS (T_a =−20~+75℃, unless otherwise noted)

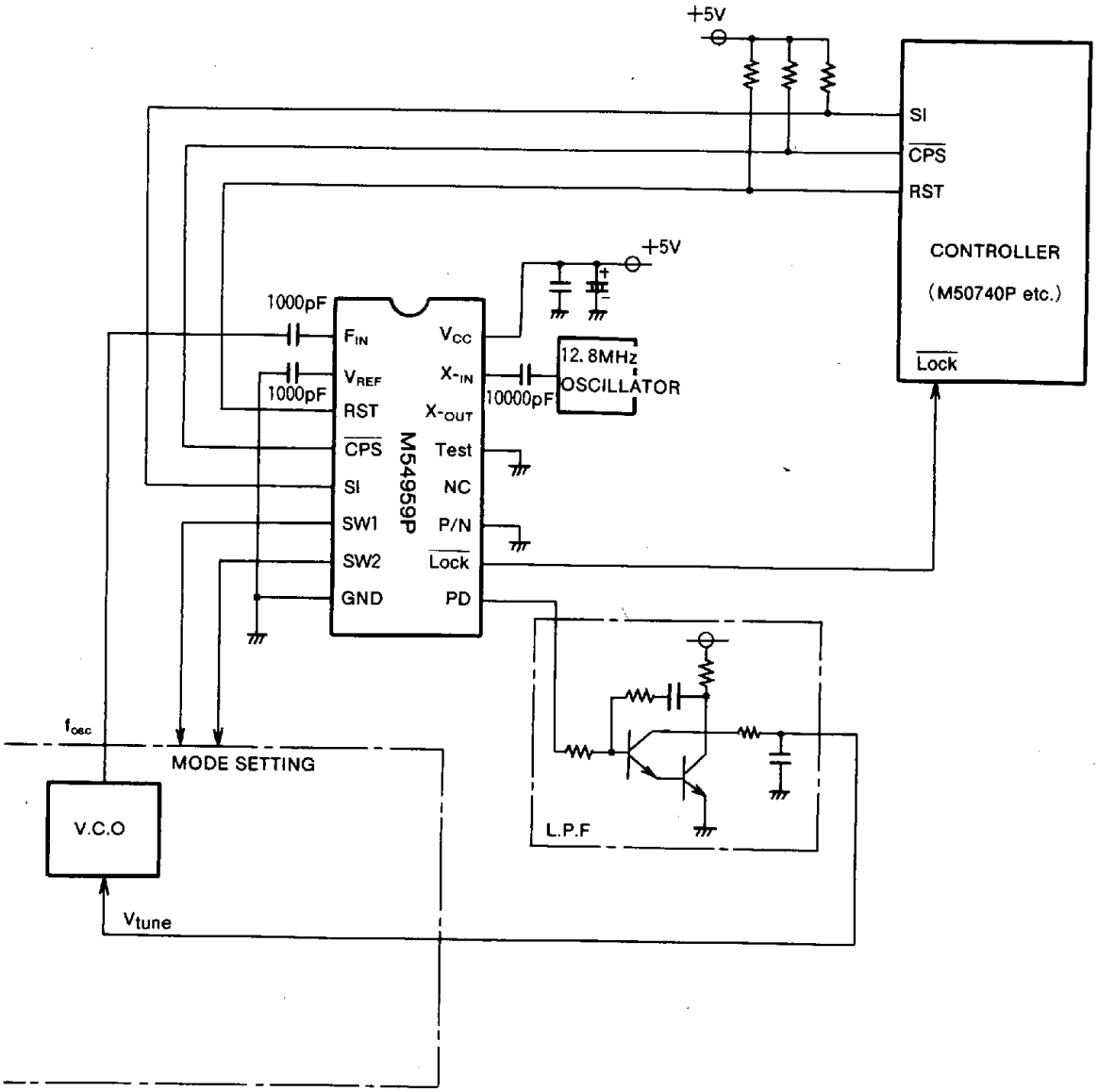
Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage	3, 4, 5, 11, 13	V_{CC}=5.5V	2.0			V
V_{IL}	Low-level input voltage	3, 4, 5, 11, 13	V_{CC}=5.5V			0.6	V
I_{IH}	High-level input current	3, 4, 5, 11, 13	V_{CC}=5.5V, V_{IH}=5.5V			30	μA
I_{IL}	Low-level input current	3, 4, 5, 11, 13	V_{CC}=4.5V, V_{IL}=0V		−50	−100	μA
V_{OL}	Low-level output voltage	6, 7, 10, 12	V_{CC}=4.5V, I_{OL}=5mA			0.5	V
V_{OHP1}	PD high-level output voltage	9	V_{CC}=4.5V, I_{OH}=−1mA	3.0			V
V_{OHP2}	PD high-level output voltage	9	V_{CC}=5V, I_{OH}=−0.1mA	4.0			V
V_{OLP1}	PD low-level output voltage	9	V_{CC}=4.5V, I_{OL}=1mA			1.5	V
V_{OLP2}	PD low-level output voltage	9	V_{CC}=5V, I_{OL}=0.1mA			1.0	V
I_{PD1}	PD leakage current	9	V_{CC}=5.5V, V_O=0.8~4.7V			±1.0	μA
I_{PD2}	PD leakage current	9	V_{CC}=5V, V_O=2.5V			±100	μA
I_{CC}	Supply current		V_{CC}=5.5V		20	30	mA
I_{OLK}	Output leakage current	6, 7, 10	V_{CC}=5.5V, V_{OH}=5.5V			30	μA

Note 15 : All voltages are measured with respect to circuit ground (pin 8)

16 : Currents are taken to be positive (negative sign) when flowing out of the circuit. The minimum and maximum values are taken to be absolute values.

17 : Typical values are at V_{CC}= 5V, T_a=25℃

APPLICATION EXAMPLE



TYPICAL CHARACTERISTICS

INPUT AMPLITUDE VS INPUT FREQUENCY