Audio Codec For Recordable DVD

Preliminary Technical Data

ADAV804

FEATURES

Stereo Analog to Digital Converter (ADC)
- **Supports 48/96 kHz Sample Rates**
- **102 dB Dynamic Range**
- **Single-Ended Input**
- **Automatic Level Control**

Stereo Digital to Analog Converter (DAC)
- **Supports 32/44.1/48/96/192 kHz Sample Rates**
- **103 dB Dynamic Range**
- **Differential Output**

Asynchronous operation of ADC and DAC

Stereo Sample Rate Converter (SRC)
- **Input/Output Range - 8 - 96 kHz**
- **140 dB Dynamic Range**

Digital Interfaces
- **Record**
- **Playback**
- **Aux Record**
- **Aux Playback**

S/PDIF (IEC60958) Input & Output
- **Digital Interface Receiver (DIR)**
- **Digital Interface Transmitter (DIT)**

PLL based Audio MCLK Generators

Generates Required DVDR System MCLKs

Device Control via I²C compatible serial port

64-Lead LQFP Package

APPLICATIONS

DVD-Recordable

All Formats

CD-R/W

PRODUCT OVERVIEW

The ADAV804 is a stereo audio codec intended for applications, such as DVD or CD recorders, requiring high performance, flexible and cost effective playback and record functionality. The ADAV804 features Analog Devices proprietary, high performance converter cores to provide record (ADC), playback (DAC) and format conversion (SRC) in a single chip. The ADAV804's record channel features variable input gain to allow for adjustment of recorded input levels, followed by a high performance stereo ADC whose digital output is sent to the record interface. The record channel also features Level Detectors which can be used in feedback loops to adjust input levels for optimum recording. The playback channel features a high performance stereo DAC with independent digital volume control.

The Sample Rate Converter (SRC) provides high performance sample-rate conversion to allow inputs and outputs requiring different sample rates to be matched. The SRC input can be selected from Playback, Auxiliary, DIR or ADC (record). The SRC output can be applied to the Playback DAC, both main and Auxiliary record channels and a DIT. (*continued on Page 12*)

FUNCTIONAL BLOCK DIAGRAM

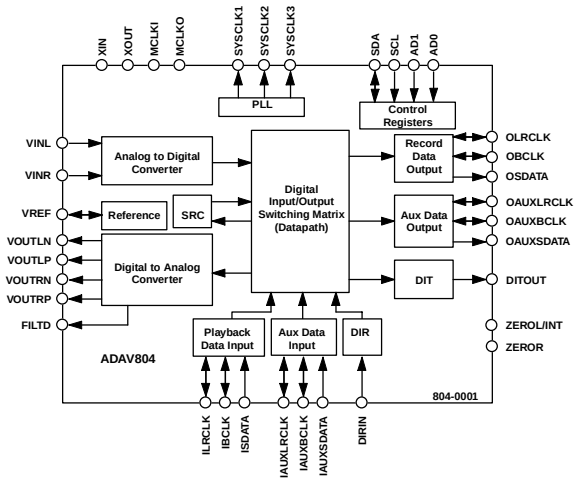

Figure 1.

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REVISION HISTORY

SPECIFICATIONS

Table 1. Test Conditions Unless Otherwise Noted

Supply Voltage	
Analog	+3.3 V
Digital	+3.3 V
Ambient Temperature	25°C
Master Clock (XIN)	12.288 MHz
Measurement Bandwidth	20 Hz to 20 kHz
Word Width (All Converters)	24-bits
Load Capacitance on Digital Outputs	100 pF
ADC Input Frequency	997Hz at –1 dBFS
DAC Output Frequency	997Hz at –1 dBFS
Digital Input: Slave Mode, I²S Justified Format	
Digital Output: Master Mode, I²S Justified Forma	

Table 2. PGA Section

	Min	Typ	Max	Unit	Conditions
Input Impedance		4		kΩ	
Minimum Gain		0		dB	
Maximum Gain		24		dB	
Gain Step		0.5		dB	
Gain Step Error		TBD		dB	

Table 3. Reference Section

	Min	Typ	Max	Unit	Conditions
Absolute Voltage, V_{REF}		1.5		V	
V_{REF}Temperature Coefficient		TBD		ppm/°C	

Table 4. ADC Section[1]

	Min	Typ	Max	Unit	Conditions
Number of Channels		2			
Resolution		24		Bits	
Dynamic Range					–60 dB Input
Unweighted	98	100		dB	
A-Weighted	99	102		dB	
Total Harmonic Distorton + Noise		–85		dB	Input = –1.0 dBFS
Analog Input					
Input Range (± Full Scale)		1.0		V_{RMS}	
V_{REF}		1.5		V	
DC Accuracy					
Gain Error		–1		dB	
Interchannel Gain Mismatch		0.01		dB	
Gain Drift		100		ppm/°C	
Offset		TBD		mV	
Crosstalk (EIAJ Method)		100		dB	
Volume Control Step Size (256 Steps)		0.39		% per step	
Maximum Volume Attenuation		-48		dB	
Group Delay		TBD		µS	

[1] The figures quoted are target specifications and subject to change before release

Table 5. ADC Low-Pass Digital Decmation Filter Characteristics[1]

Sample Rate (kHz)	Pass Band Frequency (kHz)	Stop Band Frequency (kHz)	Stop Band Attenuation (dB)	Pass Band Ripple (dB)
48	$0.45314 \times f_S$	$0.54648 \times f_S$	120	±0.01
96	TBD × f_S	TBD × f_S	TBD	±TBD

[1] Guaranteed by Design

Table 6. ADC High-Pass Digital Filter Characteristics (f_S = 48 kHz)

	Min	Typ	Max	Units
Cutoff Frequency		0.9		Hz

Table 7. SRC Section

	Min	Typ	Max	Unit	Conditions
Resolution		24		Bits	
Sample Rate	8		96	kHz	XIN = 27MHz
Maximum Sample Rate Ratios					
Minimum SRC MCLK	$138 \times f_{S\text{-}MAX}$				$f_{S\text{-}MAX}$ is the greater of the input or output sample rate
Upsampling			1:8		
Downsampling			7.75:1		
Dynamic Range					20 Hz to f_S/2, 1 kHz, –60 dBFS Input
Unweighted		120		dB	Worst Case - 96 kHz:8 kHz
A-Weighted		125		dB	Worst Case - 96 kHz:8 kHz
Total Harmonic Distortion + Noise		–110		dB	20 Hz to f_S/2, 1 kHz, 0 dBFS Input

Table 8. DAC Section[1]

	Min	Typ	Max	Unit	Conditions
Number of Channels		2			
Resolution		24		Bits	
Dynamic Range					(20 Hz to 20 kHz, –60 dB Input)
Unweighted		100		dB	
A-Weighted	TBD	103		dB	
A-Weighted		TBD		dB	f_S = 96 KHz
Total Harmonic Distorton + Noise		–96		dB	Digital Input = –1.0 dBFS
Total Harmonic Distorton + Noise		TBD		dB	Digital Input = –1.0 dBFS, f_S = 96 KHz
Analog Outputs					
Output Range (± Full Scale)		1.0		Vrms	
Output Resistance		TBD		Ω	
Common Mode Output Voltage		1.5		V	
DC Accuracy					
Gain Error		–1		dB	
Interchannel Gain Mismatch		0.01		dB	
Gain Drift		25		ppm/°C	
Crosstalk (EIAJ Method)		125		dB	
Phase Deviation		TBD		Degrees	
Mute Attenuation		–63		dB	
Volume Control Step Size (128 Steps)		0.5		dB	
Group Delay		TBD		µs	

[1] The figures quoted are target specifications and subject to change before release

Table 9. DAC Low-Pass Digital Interpolation Filter Characteristics

Sample Rate (kHz)	Pass Band Frequency (kHz)	Stop Band Frequency (kHz)	Stop Band Attenuation (dB)	Pass Band Ripple (dB)
44.1	$0.4535 \times f_S$	$0.5464 \times f_S$	70	±0.002
48	$0.4541 \times f_S$	$0.5464 \times f_S$	70	±0.002
96	$0.4161 \times f_S$	$0.5927 \times f_S$	70	±0.005

Table 10. PLL Section

	Min	Typ	Max	Unit	Conditions
Master Clock Input Frequency		27/54		MHz	
Generated System Clocks					
MCLKO		27/54		MHz	
SYSCLK1	256		768	$\times f_S$	256/384/512/768 × 32/44.1/48 kHz[1]
SYSCLK2	256		768	$\times f_S$	256/384/512/768 × 32/44.1/48 kHz[1]
SYSCLK3	256	512		$\times f_S$	256/512 × 32/44.1/48 kHz[1]
Jitter					
SYSCLK1			TBD	ps rms	
SYSCLK2			TBD	ps rms	
SYSCLK3			TBD	ps rms	

[1] Sample Frequency can be doubled

Table 11. DIR Section

	Min	Typ	Max	Unit	Condition
Input Sample Frequency	27.2		220	kHz	
DIR-MCLK Frequency			TBD	MHz	
DIR-MCLK Jitter			TBD	ps	
Differential Input Voltage	TBD			mV	

Table 12. DIT Section

	Min	Typ	Max	Unit	Condition
Output Sample Frequency	27.2		220	kHz	

Table 13. Digital I/O

	Min	Typ	Max	Unit	Condition
Input Voltage HI (V_{IH})	2.0		DVDD	V	
Input Voltage LO (V_{IL})			0.8	V	
Input Leakage (I_{IH}@ V_{IH} = 3.3 V)			10	µA	
Input Leakage (I_{IL}@ V_{IL} = 0 V)			10	µA	
Output Voltage HI (V_{OH} @ I_{OH} = 1 mA)	2.4			V	
Output Voltage LO (V_{OL} @ I_{OL} = -1 mA)			0.4	V	
Input Capacitance			15	pF	

Table 14. Power

	Min	Typ	Max	Unit	Condition
Supplies					
Voltage, AVDD	3.0	3.3	3.6	V	
Voltage, DVDD	3.0	3.3	3.6	V	
Voltage, ODVDD	3.0	3.3	3.6	V	
Analog Current			45	mA	All Supplies at 3.6V
Digital Current, DVDD			56	mA	All Supplies at 3.6V
Digital Interface Current, ODVDD			12	mA	All Supplies at 3.6V
Analog Current—Power Down		TBD		µA	$\overline{\text{RESET}}$ Low, No MCLK
Digital Current - Power Down		TBD		µA	$\overline{\text{RESET}}$ Low, No MCLK
Digital Interface Current - Power Down		TBD		µA	$\overline{\text{RESET}}$ Low, No MCLK
Power Supply Rejection					
1 kHz 300 mV_{P-P} Signal at Analog Supply Pins			TBD	dB	
20 kHz 300 mV_{P-P} Signal at Analog Supply Pins			TBD	dB	
Stopband (>0.55 × F_S)—any 300 mV_{P-P} Signal			TBD	dB	

TIMING SPECIFICATIONS

Table 15.

Parameter		Min	Max	Unit	Comments
MASTER CLOCK AND RESET					
f_{MCLK}	MCLKI Frequency		24.576	MHz	
f_{XIN}	XIN Frequency		54	MHz	
t_{RESET}	$\overline{\text{RESET}}$ Low	20		ns	
I^2C PORT					
f_{SCL}	SCL Clock Frequency		400	kHz	
t_{SCLH}	SCL High	0.6		µS	
t_{SCLL}	SCL Low	1.3		µS	
Start Condition -					
t_{SCS}	Setup Time	0.6		µS	Relevant for Repeated Start Condition
t_{SCH}	Hold Time	0.6		µS	After this period the 1st clock is generated
t_{DS}	Data Setup Time	100		ns	
t_{SCR}	SCL Rise Time		300	ns	
t_{SCF}	SCL Fall Time		300	ns	
t_{SDR}	SDA Rise Time		300	ns	
t_{SDF}	SDA Fall Time		300	ns	
Stop Condition					
t_{SCS}	Setup Time	0.6		µS	
SERIAL PORTS[1]					
Slave Mode					
t_{SBH}	xBCLK High	40		ns	
t_{SBL}	xBCLK Low	40		ns	
f_{SBF}	xBCLK Frequency	$64 \times f_S$			
t_{SLS}	xLRCLK Setup	10		ns	To xBCLK Rising Edge
t_{SLH}	xLRCLK Hold	10		ns	From xBCLK Rising Edge
t_{SDS}	xSDATA Setup	10		ns	To xBCLK Rising Edge
t_{SDH}	xSDATA Hold	10		ns	From xBCLK Rising Edge
t_{SDD}	xSDATA Delay	10		ns	From xBCLK Falling Edge
Master Mode					
t_{MLD}	xLRCLK Delay		5	ns	From xBCLK Falling Edge
t_{MDD}	xSDATA Delay		10	ns	From xBCLK Falling Edge
t_{MDS}	xSDATA Setup	10		ns	From xBCLK Rising Edge
t_{MDH}	xSDATA Hold	10		ns	From xBCLK Rising Edge

[1] The prefix x refers to I-, O-, IAUX- or OAUX- for the full pin name

Table 16. Temperature Range

	Min	Typ	Max	Units
Specifications Guaranteed		25		°C
Functionality Guaranteed	–40		85	°C
Storage	–65		150	°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Table 17.

Parameter	Rating
DVDD to DGND and ODVDD to DGND	0 V to 4.6 V
AVDD to AGND	0 V to 4.6 V
Digital Inputs	DGND – 0.3 V to DVDD + 0.3 V
Analog Inputs	AGND – 0.3 V to AVDD + 0.3 V
AGND to DGND	–0.3 V to +0.3 V
Reference Voltage	Indefinite short circuit to ground
Soldering (10 s)	+300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

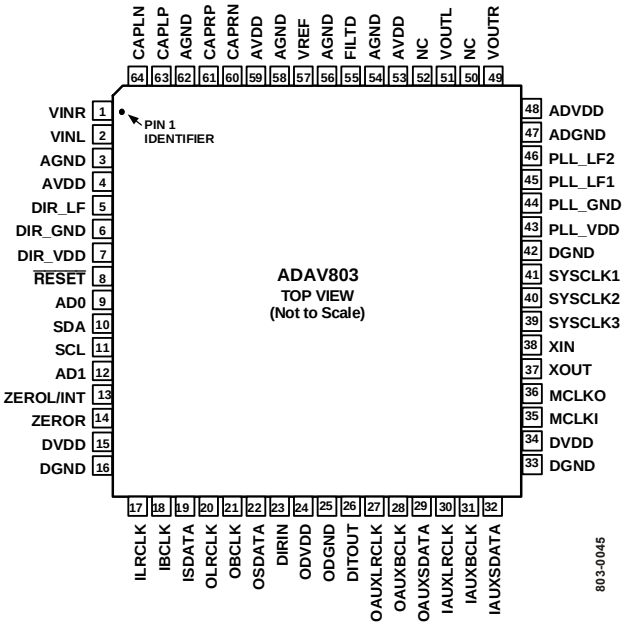

Figure 2. 64-Lead Plastic Quad Flatpack [LQFP] (ST-520)

Table 18. ADAV804 Pin Function Descriptions

Pin Number	Input/Output	Mnemonic	Description
1	INPUT	VINR	Analog Audio Input - Right Channel
2	INPUT	VINL	Analog Audio Input - Left Channel
3		AGND	Analog Ground
4		AVDD	Analog Voltage Supply
5		DIR_LF	DIR Phase Locked Loop (PLL) Loop Filter Pin
6		DIR_GND	Supply Ground for DIR Analog Section. This pin should be connected to AGND
7		DIR_VDD	Supply for DIR Analog Section. This pin should be connected to AVDD
8	INPUT	$\overline{\text{RESET}}$	Reset input (Active Low)
9	INPUT	AD0	I^2C Address LSB
10	INPUT/OUTPUT	SDA	Data Input/Output of I^2C compatible control interface
11	INPUT	SCL	Clock Input of I^2C compatible control interface
12	INPUT	AD1	I^2C Address MSB
13	OUTPUT	ZEROL/INT	Left Channel (Output) Zero Flag or Interrupt (Output) Flag. The function of this pin is determined by the INTRPT bin in DAC Control Register 4
14	OUTPUT	ZEROR	Right Channel (Output) Zero Flag
15		DVDD	Digital Voltage Supply
16		DGND	Digital Ground
17	INPUT/OUTPUT	ILRCLK	Sampling Clock (LRCLK) of Playback Digital Input Port
18	INPUT/OUTPUT	IBCLK	Serial Clock (BCLK) of Playback Digital Input Port
19	INPUT	ISDATA	Data Input of Playback Digital Input Port
20	INPUT/OUTPUT	OLRCLK	Sampling Clock (LRCLK) of Record Digital Output Port
21	INPUT/OUTPUT	OBCLK	Serial Clock (BCLK) of Record Digital Output Port
22	OUTPUT	OSDATA	Data Output of Record Digital Output Port

Pin Number	Input/Output	Mnemonic	Description
23	INPUT	DIRIN	Input to Digital Input Receiver (S/PDIF)
24		ODVDD	Interface Digital Voltage Supply
25		ODGND	Interface Digital Ground
26	OUTPUT	DITOUT	S/PDIF Output from DIT
27	INPUT/OUTPUT	OAUXLRCLK	Sampling Clock (LRCLK) of Auxiliary Digital Output Port
28	INPUT/OUTPUT	OAUXBCLK	Serial Clock (BCLK) of Auxiliary Digital Output Port
29	OUTPUT	OAUXSDATA	Data Output of Auxiliary Digital Output Port
30	INPUT/OUTPUT	IAUXLRCLK	Sampling Clock (LRCLK) of Auxiliary Digital Input Port
31	INPUT/OUTPUT	IAUXBCLK	Serial (BCLK) of Auxiliary Digital Input Port
32	INPUT	IAUXSDATA	Data Input of Auxiliary Digital Input Port
33		DGND	Digital Ground
34		DVDD	Digital Supply Voltage
35	INPUT	MCLKI	External MCLK Input
36	OUTPUT	MCLKO	Oscillator Output
37	INPUT	XOUT	Crystal Input
38	INPUT	XIN	Crystal or External MCLK Input
39	OUTPUT	SYSCLK3	System Clock 3 (from PLL 2)
40	OUTPUT	SYSCLK2	System Clock 2 (from PLL 2)
41	OUTPUT	SYSCLK1	System Clock 1 (from PLL 1)
42		DGND	Digital Ground
43		PLL_VDD	Supply for PLL Analog Section. This pin should be connected to AVDD
44		PLL_GND	Ground for PLL Analog Section. This pin should be connected to AGND
45		PLL_LF1	Loop Filter for PLL1
46		PLL_LF2	Loop Filter for PLL2
47		ADGND	Analog Ground (Mixed Signal)
48		ADVDD	Analog Voltage Supply (Mixed Signal). This pin should be connected to AVDD
49	OUTPUT	VOUTR	Right Channel Analog Output
50		NC	No Connect
51	OUTPUT	VOUTL	Left Channel Analog Output
52		NC	No Connect
53		AVDD	Analog Voltage Supply
54		AGND	Analog Ground
55		FILTD	Output DAC Reference Decoupling
56		AGND	Analog Ground
57		VREF	Voltage Reference Voltage
58		AGND	Analog Ground
59		AVDD	Analog Voltage Supply
60		CAPRN	ADC Modulator Input Filter Capacitor (Right Channel - Negative)
61		CAPRP	ADC Modulator Input Filter Capacitor (Right Channel - Positive)
62		AGND	Analog Ground
63		CAPLP	ADC Modulator Input Filter Capacitor (Left Channel - Positive)
64		CAPLN	ADC Modulator Input Filter Capacitor (Left Channel - Negative)

(*continued from Page 1*)

Operation of the ADAV804 is controlled via an I²C serial interface, which allows individual Control Register settings to be programmed. The ADAV804 operates from a single analog +3.3 V power supply - and a digital power supply of +3.3 V with optional digital interface range of 3.0 V to +3.6 V. It is housed in a 64-lead LQFP package and is characterized for operation over the commercial temperature range –40°C to 85°C.

FUNCTIONAL DESCRIPTION

ADC SECTION

The ADAV804's ADC section is implemented using a 2nd order multi-bit (5-bits) Sigma-Delta modulator. The modulator is sampled at either half the ADC MCLK rate (Modulator Clock = 128 × f_S) or a quarter of the ADC MCLK rate (Modulator Clock = 64 × f_S). The digital decimator consists of a Sinc^5 filter followed by a cascade of 3 half-band FIR filters. The Sinc decimates by a factor of 16 at 48 kHz and by 8 at 96 kHz. Each of the half-band filters decimates by a factor of 2. Figure 3 below shows the detail of the ADC section. The ADC can be clocked by a number of different clock sources to control the sample rate. MCLK selection for the ADC is set by Internal Clocking Control Register 1 (address = 0x76). The ADC provides an output word of up to 24 bits in resolution in 2s complement format. The output word can be routed to the output ports, to the sample rate converter or to the SPDIF digital transmitter.

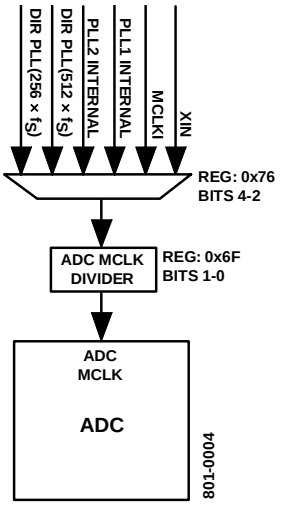

Figure 3. Clock Path Control on the ADC

Programmable Gain Amplifier (PGA)

The input of the record channel features a PGA which converts the single-ended signal to a differential signal which is applied to the analog sigma-delta modulator of the ADC. The PGA can be programmed to amplify a signal by up to 24dB in 0.5dB increments. Figure 4 details the structure of the PGA circuit.

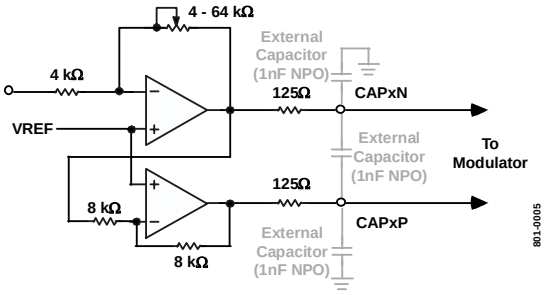

Figure 4. PGA Block Diagram

Analog Sigma Delta Modulator

The ADC features a 2nd order, multi-bit, Sigma-Delta modulator. The input features two integrators in cascade followed by a flash converter. This multi-bit output is directed to a scrambler, followed by a DAC for loop feedback. The Flash ADC output is also converted from "thermometer" coding to "binary" coding for input as a 5-bit word to the decimator. Figure 5 shows the ADC block diagram.

The ADC also features independent digital volume control for the left and right channels. The volume control consists of 256 linear steps with each step reducing the digital output codes by 0.39%. Each channel also has a peak detector which records the peak level of the input signal. The peak detector register is cleared by reading it.

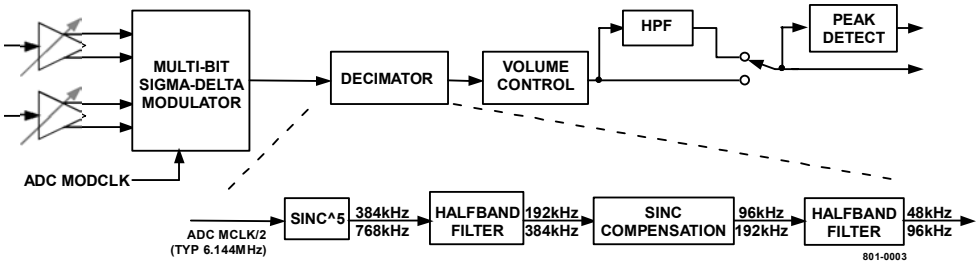

Figure 5. ADC Block Diagram

Selecting A Sample Rate

The sample rate of the ADC is always 256 × f_S. To facilitate different MCLKs the ADC block has a programmable divider which allows the MCLK to be divided by 1, 2 or 3 before being applied to the ADC. This allows for MCLKs of 256 × f_S, 512 × f_S or 768 × f_S to be applied to the ADC. To synchronize the data output port with the ADC the same divider setting should be applied to the Internal Clock (ICLK1 or ICLK2) which is controlling the output port. The Internal Clock dividers are shown in Figure 34. By default the ∑Δ modulator runs at ADC MCLK/2. The modulator is designed to run with a maximum clock rate of 6.144MHz,. For cases where higher sample rates would run the modulator at speeds higher than this the user can select divide the ADC MCLK by 4 before it is applied to the modulator. To compensate for this the modulator uses an alternate filter configuration. The divide setting is selected by the AMC bit in ADC Control Register 1.Automatic Level Control (ALC)

The ADC record channel features a programmable automatic level control block. This block monitors the level of the ADC output signal and will automatically reduce the gain if the signal at the input pins causes the ADC output to exceed a preset limit. This function can be useful to maximize the signal dynamic range when the input level is not well-defined. The PGA can be used to amplify the unknown signal and the ALC will reduce the gain until the ADC output is within the preset limits. This results in maximum front-end gain. Since the ALC block monitors the output of the ADC the volume control function should not be used. The ADC volume control scales the results from the ADC and any distortion caused by the input signal exceeding the input range of the ADC will still be present at the output of the ADC but scaled by a value determined by the volume control register. The ALC block consists of two functions, Attack Mode and Recovery Mode. The Recovery Mode consists of three settings, namely, No Recovery, Normal Recovery and Limited Recovery. Each of these modes in discussed in detail below. Figure 6 shows an overall flow diagram of the ALC block.

Attack Mode

When the absolute value of the ADC output exceeds the level set by the Attack Threshold bits in the ALC Control Register 2, Attack Mode is initiated. The PGA gain for both channels is reduced by one step (0.5dB). The ALC will then wait for a time determined by the Attack Timer bits before sampling the ADC output value again. If the ADC output is still above the threshold the PGA gain is reduced by a further step. This procedure continues until the ADC output is below the limit set by the Attack Threshold bits. The initial gains of the PGAs are defined by ADC Left PGA Gain Register and ADC Right PGA Gain Register and may be different values. The ALC simply adds or subtracts a common gain offset to these values. The ALC will preserve any gain difference in dB as defined by those registers. At no time will the PGA gains exceed their initial values. Therefore, the initial gain setting also serves as a maximum value.

The Limit Detection Mode bit in ALC Control Register 1 determines how the ALC should respond to an ADC output which exceeds the set limits. If this bit is a one then both channels must exceed the threshold before the gain is reduced. This mode can be used to prevent unnecessary gain reduction due to spurious noise on a single channel. If the Limit Detection Mode bit is a zero the gain will be reduced when either channel exceeds the threshold.

No Recovery Mode

By default there is no gain recovery. Once the gain has been reduced it will not be recovered until the ALC has been reset, by toggling the ALCEN bit in ALC Control Register 1 or by writing any value to ALC Control Register 3. The latter option is more efficient as it requires only one write operation to reset the ALC function. No Recovery Mode prevents volume modulation of the signal, caused by adjusting the gain, which can create undesirable artifacts in the signal. Since the gain can be reduced but not recovered, care should be taken that spurious signals do not interfere with the input signal as these may trigger a gain reduction unnecessarily.

Normal Recovery

This mode allows for the PGA gain to be recovered providing that the input signal meets certain criteria. Firstly, the ALC must not be in Attack Mode, i.e., the PGA gain has been reduced sufficiently such that the input signal is below the level set by the Attack Threshold bits. Secondly, the output result from the ADC must be below the level set by the Recovery Threshold bits in ALC Control Register. If both of these criteria are met the gain is recovered by one step (0.5dB). The gain is incrementally restored to its original value assuming the ADC output level is below the Recovery Threshold at intervals determined by the Recovery Time bits. Should the ADC output level exceed the Recovery Threshold while the PGA gain is being restored the PGA gain value will be held and will not continue restoration until the ADC output level is again below the Recovery Threshold. Once the PGA gain is restored to its original value it will not be changed again unless the ADC output value exceeds the Attack Threshold and the ALC then enters Attack Mode. Care should be exercised when using this mode to choose values for the Attack and Recovery thresholds to prevent excessive volume modulation caused by continuous gain adjustments.

Limited Recovery

Limited Recovery Mode offers a compromise between No Recovery and Normal Recovery Modes. If the output level of the ADC exceeds the Attack Threshold then Attack Mode is

initiated. When Attack Mode has reduced the PGA gain to suitable levels the ALC will attempt to recovery the gain to its original level. If the ADC output level exceeds the level set by the Recovery Threshold bits a counter is incremented (GAINCNTR). This counter is incremented, at intervals equal to the Recovery Time selection, if the ADC has any excursion above the Recovery Threshold. If the counter reaches its maximum value, determined by the GAINCNTR bits in ALC Control Register 1, the PGA gain is deemed suitable and no further gain recovery is attempted. If, at any time, the ADC output level exceeds the Attack Threshold, Attack Mode is reinitiated and the counter is reset

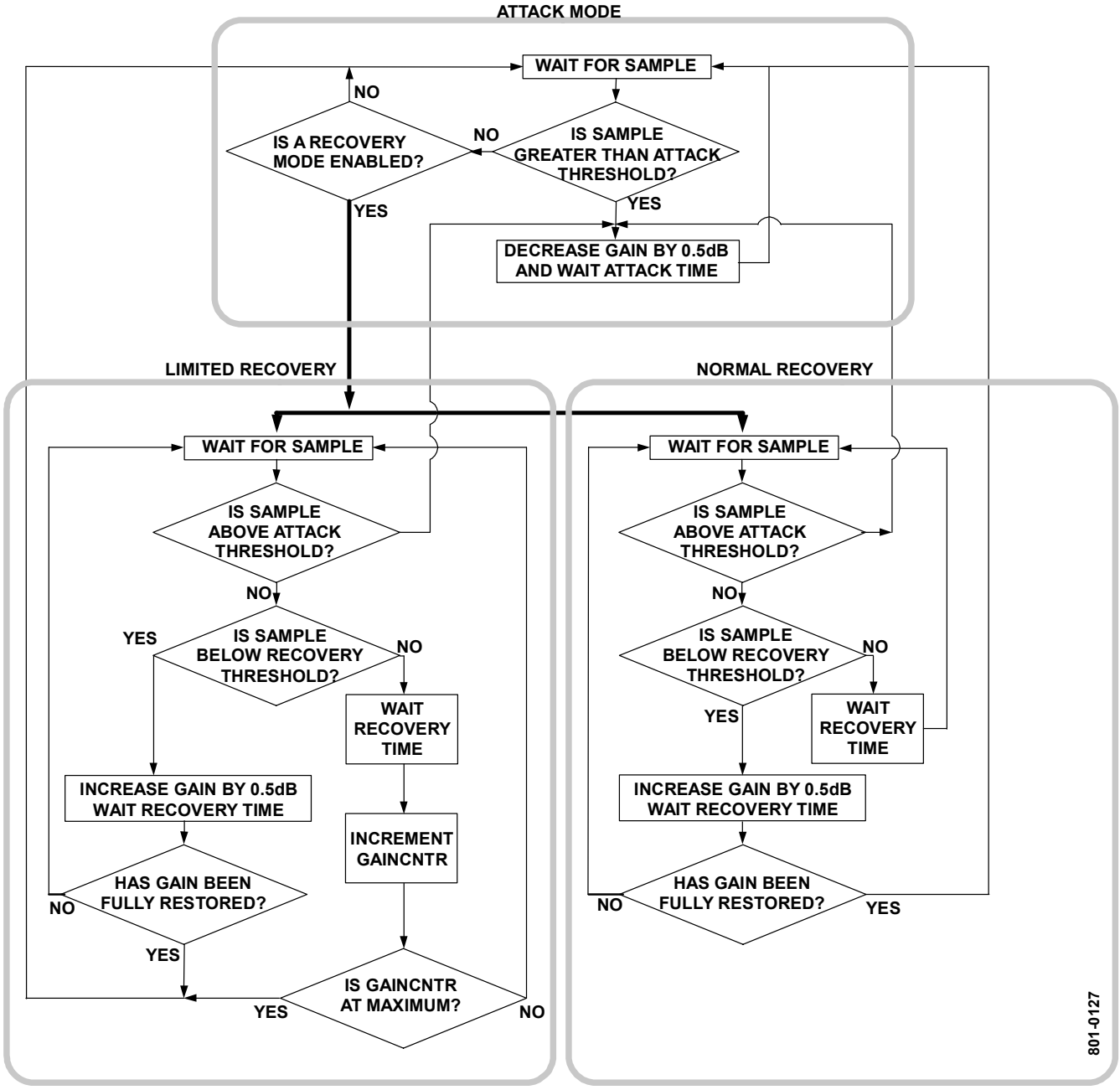

Figure 6. ALC Flow Diagram

DAC SECTION

The ADAV804 has two DAC channels arranged as a stereo pair with differential outputs. Each channel has its own independently programmable attenuator, adjustable in 128 steps of 0.375dB per step. The DAC can receive data from the playback or auxiliary input ports, the SRC, the ADC or the DIR. Each analog output pin sits at a dc level of VREF, and swings 1.0 Vrms for a 0dB digital input signal. A single op-amp third-order external low-pass filter is recommended to remove high-frequency noise present on the output pins. Note that the use of op amps with low slew rate or low bandwidth may cause high frequency noise and tones to fold down into the audio band; care should be exercised in selecting these components. The FILTD and FILTR pins should be bypassed by external capacitors to AGND. The FILTD pin is used to reduce the noise of the internal DAC bias circuitry, thereby reducing the DAC output noise. The voltage at the VREF pin, FILTR can be used to bias external op amps used to filter the output signals. For applications where the FILTR is required to drive external op amps which may draw more than 50μA or may have dynamic load changes extra buffering should be used to preserve the quality of the ADAV804 reference. The digital input data source for the DAC can be selected from a number of available sources. by programming the appropriate bits in the Datapath Control register. Figure 7 shows how the digital data source and MCLK source for the DAC are selected. Each DAC has an independent volume register giving 256 steps of control with each step giving approximately 0.375dB of attenuation. Each DAC also has a peak level register which records the peak value of the digital audio data. Reading the register clears the peak .

Selecting a Sample Rate

Correct operation of the DAC is dependant upon the data rate provided to the DAC, the master clock applied to the DAC and the selected interpolation rate. By default the DAC assumes that the MCLK rate is 256 times the sample rate which requires an 8 times oversampling rate. This combination is suitable for sample rates up to 48kHz. For the case of a 96kHz data rate which has a 24.576MHz MCLK (256 × f_S) associated with it the DAC MCLK divider should be set to divide the MCLK by 2. This will prevent the DAC engine being run too fast. To compensate for the reduced MCLK rate the interpolator should be selected to operate in 4 × (DAC MCLK = 128 × f_S). Similar combinations can be selected for different sample rates.

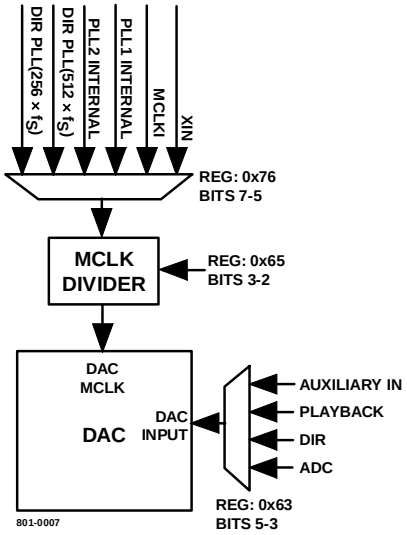

Figure 7. Clock and data Path Control on the DAC

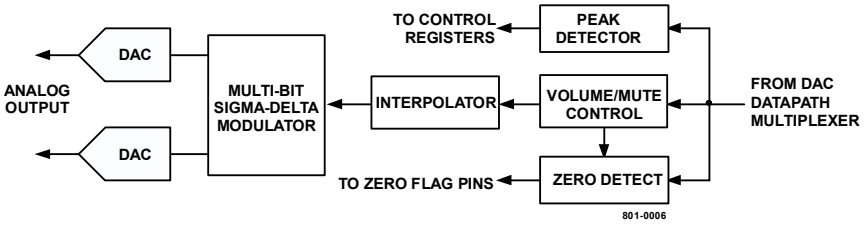

Figure 8. DAC Block Diagram

SRC FUNCTIONAL OVERVIEW

THEORY OF OPERATION

Asynchronous sample rate conversion is converting data from at the same or different sample rate. The simplest approach to an asynchronous sample rate conversion is the use of a zero-order hold between the two samplers shown in Figure 9 In an asynchronous system, T2 is never equal to T1 nor is the ratio between T2 and T1 rational. As a result, samples at fS_OUT will be repeated or dropped producing an error in the re-sampling process. The frequency domain shows the wide side lobes that result from this error when the sampling of fS_OUT is convolved with the attenuated images from the sin(x)/x nature of the zero-order hold. The images at fS_IN, dc signal images, of the zero-order holdare infinitely attenuated. Since the ratio of T2 to T1 is an irrational number, the error resulting from the re-sampling at fS_OUT can never be eliminated. However, the error can be significantly reduced through interpolation of the input data at fS_IN. The sample rate converter in the ADAV804/ is conceptually interpolated by a factor of 2^{20}.

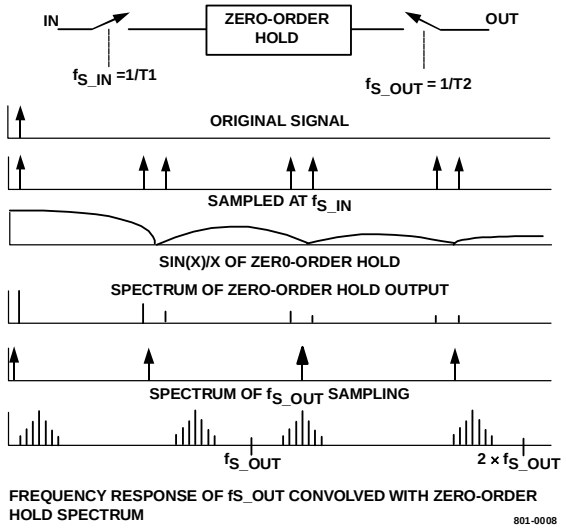

Figure 9. Zero Order Hold Being Used by fS OUT to Resample Data from fS_IN

CONCEPTUAL HIGH INTERPOLATION MODEL

Interpolation of the input data by a factor of 2^{20} involves placing (2^{20} –1) samples between each f_{S_IN} sample. Figure 10 shows both the time domain and the frequency domain of interpolation by a factor of 2^{20}. Conceptually, interpolation by 2^{20} would involve the steps of zero-stuffing (2^{20} –1) number of samples between each f_{S_IN} sample and convolving this interpolated signal with a digital low-pass filter to suppress the images. In the time domain, it can be seen that f_{S_OUT} selects the closest $f_{S\_IN} \times 2^{20}$ sample from the zero-order hold as opposed to the nearest f_{S_IN} sample in the case of no interpolation. This significantly reduces the re-sampling error.

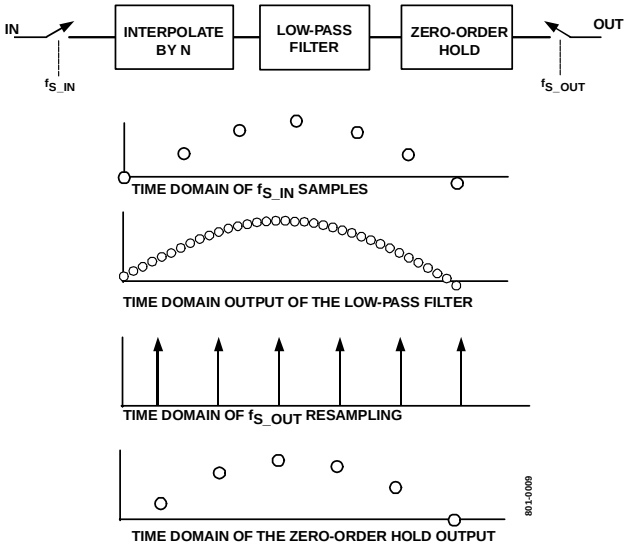

Figure 10. SRC Time Domain

In the frequency domain shown in Figure 11, the interpolation expands the frequency axis of the zero-order hold. The images from the interpolation can be sufficiently attenuated by a good low-pass filter. The images from the zero-order hold are now pushed by a factor of 2^{20} closer to the infinite attenuation point of the zero-order hold, which is $f_{S\_IN} \times 2^{20}$ The images at the zero-order hold are the determining factor for the fidelity of the output at f_{S_OUT}. The worst-case images can be computed from the zero-order hold frequency response, maximum image = sin ($\times$ F/f_{S_INTERP})/($\times$ F/f_{S_INTERP}). F is the frequency of the worst-case image that would be $2^{20} \times f_{S\_IN} \pm f_{S\_IN}/2$, and f_{S_INTERP} is $f_{S\_IN} \times 2^{20}$.

The following worst-case images would appear for f_{S_IN} = 192 kHz:

Image at f_{S_INTERP} − 96 kHz = –125.1 dB

Image at f_{S_INTERP} + 96 kHz = –125.1 dB

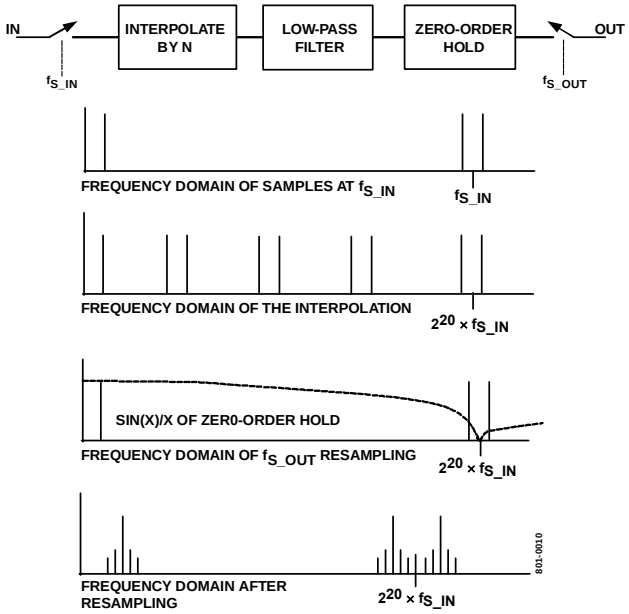

Figure 11. Frequency Domain of the Interpolation and Resampling

HARDWARE MODEL

The output rate of the low-pass filter of Figure 10 would be the interpolation rate, $2^{20} \times 192000$ kHz = 201.3 GHz. Sampling at a rate of 201.3 GHz is clearly impractical, not to mention the number of taps required to calculate each interpolated sample. However, since interpolation by 2^{20} involves zero-stuffing $2^{20}-1$ samples between each f_{S_IN} sample, most of the multiplies in the low-pass FIR filter are by zero. A further reduction can be realized by the fact that since only one interpolated sample is taken at the output at the f_{S_OUT} rate, only one convolution needs to be performed per f_{S_OUT} period instead of 2^{20} convolutions. A 64-tap FIR filter for each f_{S_OUT} sample is sufficient to suppress the images caused by the interpolation. The difficulty with the above approach is that the correct interpolated sample needs to be selected upon the arrival of f_{S_OUT}. Since there are 2^{20} possible convolutions per f_{S_OUT} period, the arrival of the f_{S_OUT} clock must be measured with an accuracy of 1/201.3 GHz = 4.96 ps. Measuring the f_{S_OUT} period with a clock of 201.3 GHz frequency is clearly impossible; instead, several coarse measurements of the f_{S_OUT} clock period are made and averaged over time.

Another difficulty with the above approach is the number of coefficients required. Since there are 2^{20} possible convolutions with a 64-tap FIR filter, there needs to be 2^{20} polyphase coefficients for each tap, which requires a total of 2^{26} coefficients. To reduce the amount of coefficients in ROM, the SRC stores small subset of coefficients and performs a high order interpolation between the stored coefficients. So far the above approach works for the case of $f_{S\_OUT} > f_{S\_IN}$. However, in the case when the output sample rate, f_{S_OUT}, is less than the input sample rate, f_{S_IN}, the ROM starting address, input data, and the length of the convolution must be scaled. As the input sample rate rises over the output sample rate, the anti-aliasing filter's cutoff frequency has to be lowered because the Nyquist frequency of the output samples is less than the Nyquist frequency of the input samples. To move the cutoff frequency of the antialiasing filter, the coefficients are dynamically altered and the length of the convolution is increased by a factor of (f_{S_IN}/f_{S_OUT}).

This technique is supported by the Fourier transform property that if f(t) is F(ω), then f(k × t) is F(ω/k). Thus, the range of decimation is simply limited by the size of the RAM.

THE SAMPLE RATE CONVERTER ARCHITECTURE

The architecture of the sample rate converter is shown in Figure 12. The sample rate converter's FIFO block adjusts the left and right input samples and stores them for the FIR filter's convolution cycle. The f_{S_IN} counter provides the write address to the FIFO block and the ramp input to the digital servo loop. The ROM stores the coefficients for the FIR filter convolution and performs a high order interpolation between the stored coefficients. The sample rate ratio block measures the sample rate for dynamically altering the ROM coefficients and scaling of the FIR filter length as well as the input data. The digital servo loop automatically tracks the f_{S_IN} and f_{S_OUT} sample rates and provides the RAM and ROM start addresses for the start of the FIR filter convolution.

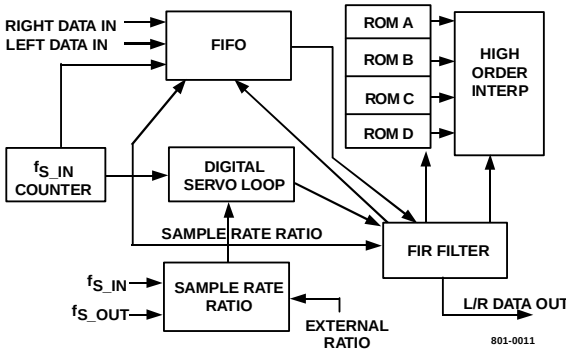

Figure 12. Architecture of the Sample Rate Converter

The FIFO receives the left and right input data and adjusts the amplitude of the data for both the soft muting of the sample rate converter and the scaling of the input data by the sample rate ratio before storing the samples in the RAM. The input data is scaled by the sample rate ratio because as the FIR filter length of the convolution increases, so does the amplitude of the convolution output. To keep the output of the FIR filter from saturating, the input data is scaled down by multiplying it by (f_{S_OUT}/f_{S_IN}) when $f_{S\_OUT} < f_{S\_IN}$. The FIFO also scales the input data for muting and unmuting of the SRC.

The RAM in the FIFO is 512 words deep for both left and right channels. An offset to the write address provided by the f_{S_IN} counter is added to prevent the RAM read pointer from ever overlapping the write address. The minimum offset on the SRC

is 16 samples. However, the Group Delay and Mute In register can be used to increase this offset. The number of input samples added to the write pointer of the FIFO on the SRC is 16 + Bits 6-0 of the Group Delay register. This feature is useful in vari-speed applications in order to prevent the read pointer to the FIFO running ahead of the write pointer. When set, bit 7 of the Group Delay and Mute In register will soft mute the sample rate. Increasing the offset of the write address pointer is useful for applications when small changes in the sample rate ratio between f_{S_IN} and f_{S_OUT} are expected. The maximum decimation rate can be calculated from the RAM word depth and the group delay as (512−16)/64 taps = 7.75 for short group delay and (512-64)/64 taps = 7 for long group delay.

The digital servo loop is essentially a ramp filter that provides the initial pointer to the address in RAM and ROM for the start of the FIR convolution. The RAM pointer is the integer output of the ramp filter while the ROM is the fractional part. The digital servo loop must be able to provide excellent rejection of jitter on the f_{S_IN} and f_{S_OUT} clocks as well as measure the arrival of the f_{S_OUT} clock within 4.97 ps. The digital servo loop will also divide the fractional part of the ramp output by the ratio of f_{S_IN}/f_{S_OUT} for the case when $f_{S\_IN} > f_{S\_OUT}$, to dynamically alter the ROM coefficients.

The digital servo loop is implemented with a multi-rate filter. To settle the digital servo loop filter more quickly upon startup or a change in the sample rate, a "fast mode" was added to the filter. When the digital servo loop starts up or the sample rate is changed, the digital servo loop kicks into "fast mode" to adjust and settle on the new sample rate. Upon sensing the digital servo loop settling down to some reasonable value, the digital servo loop will kick into "normal" or "slow mode."

During "fast mode" the MUTE_OUT bit in the Sample Rate Error register is asserted to let the user know clicks or pops may be present in the digital audio data. The output of the SRC can be muted, by asserting bit 7 of the Group Delay & Mute register until the SRC has changed to "slow mode". The MUTE_OUT bit can be set to generate an interrupt when the SRC changes to "slow mode" indicating that the data will be sample rate converted accurately. The frequency response of the digital servo loop for "fast mode" and "slow mode" are shown in Figure 14. The FIR filter is a 64-tap filter in the case of $f_{S\_OUT} \geq f_{S\_IN}$ and is $(f_{S\_IN}/f_{S\_OUT}) \times 64$ taps for the case when $f_{S\_IN} > f_{S\_OUT}$. The FIR filter performs its convolution by loading in the starting address of the RAM address pointer and the ROM address pointer from the digital servo loop at the start of the f_{S_OUT} period. The FIR filter then steps through the RAM by decrementing its address by 1 for each tap, and the ROM pointer increments its address by the $(f_{S\_OUT}T/f_{S\_IN}) \times 2^{20}$ ratio for $f_{S\_IN} > f_{S\_OUT}$ or 2^{20} for $f_{S\_OUT} \geq f_{S\_IN}$. Once the ROM address rolls over, the convolution is completed. The convolution is performed for both the left and right channels, and the multiply accumulate circuit used for the convolution is shared between the channels. The f_{S_IN}/f_{S_OUT} sample rate ratio circuit is used to dynamically alter the coefficients in the ROM for the case when $f_{S\_IN} > f_{S\_OUT}$. The ratio is calculated by comparing the output of an f_{S_OUT} counter to the output of an f_{S_IN} counter. If $f_{S\_OUT} > f_{S\_IN}$, the ratio is held at one. If $f_{S\_IN} > f_{S\_OUT}$, the sample rate ratio is updated if it is different by more than two f_{S_OUT} periods from the previous f_{S_OUT} to f_{S_IN} comparison. This is done to provide some hysteresis to prevent the filter length from oscillating and causing distortion.

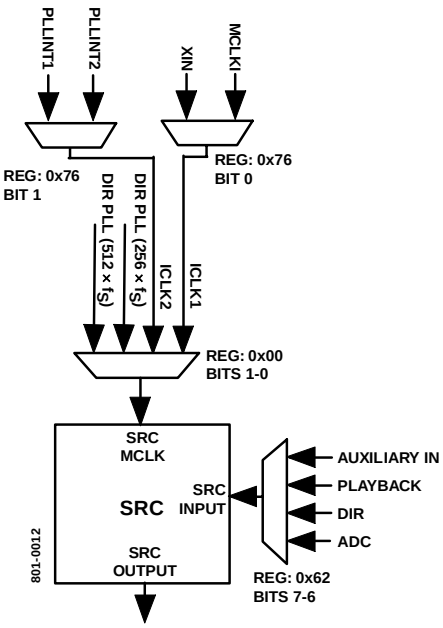

Figure 13. Clock and Data Path Control on the SRC

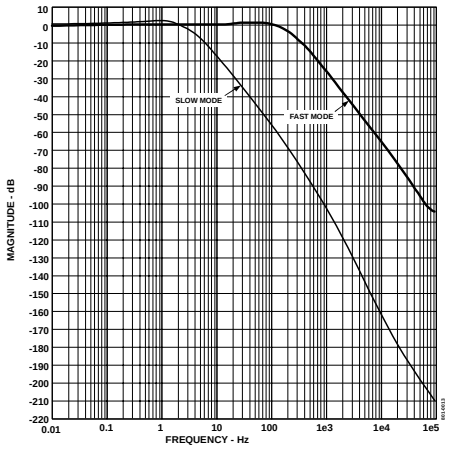

Figure 14. Frequency Response of the Digital Servo Loop. fS_IN is the X-Axis, fS_OUT = 192 KHz, Master Clock is 30 MHz

PLL SECTION

The ADAV804 features a dual PLL configuration to generate independent system clocks for asynchronous operation. Figure 17 shows the block diagram of the PLL section. The PLL generates the internal and system clocks from a 27MHz clock. This clock is generated either by a crystal connected between XIN and XOUT, as shown in Figure 15 or from an external

clock source connected directly to XIN. A 54MHz clock can also be used if the internal clock divider is used. Both PLLs (PLL1 and PLL2) can be programmed independently and cater for a range of sampling rates (32/44.1/48 kHz) with selectable system clock oversampling rates of 256 and 384. Higher oversampling rates can also be selected by enabling the doubling of the sampling rate to give 512 or 768 × f_S ratios. Note that this option also allows oversampling ratios of 256 or 384 at double sample rates of 64/88.2/96 kHz. The PLL outputs can be routed internally to act as clock sources for the other component blocks such as the ADC, DAC etc. The outputs of the PLLs are also available on the three SYSCLK pins. Figure 18 shows how the PLLs can be configured to provide the sampling clocks.

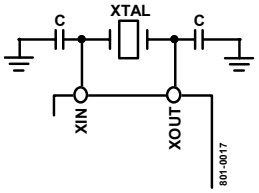

Figure 15. Crystal Connection

Table 19. PLL Frequency Selection Options

PLL	Sample Rate (f_S)	MCLK Selection Normal f_S	Double f_S
1	32/44.1/48 kHz	256/384×f_S	512/768×f_S
	64/88.2/96 kHz		256/384×f_S
2A	32/44.1/48 kHz	256/384×f_S	512/768×f_S
	64/88.2/96 kHz		256/384×f_S
2B	Same as f_S selected for PLL 2A	512×f_S 512×f_S	

The PLLs require a some external components to operate correctly. These components, shown in Figure 16 form a loop filter which integrates the current pulses from a charge pump and produces a voltage which is used to tune the VCO. Good quality capacitors, such as PPS film, are recommended .Figure 17 shows a block diagram of the PLL section including master clock selection. Figure 18 shows how the clock frequencies at the clock output pins, SYSCLK1-3 and the internal PLL clock values, PLL1 and PLL2 are selected. The clock nodes, PLL1 and PLL2, can be used as master clocks for the other blocks in the ADAV804 such as the DAC or ADC. The PLL has separate supply and ground pins and these should be as clean as possible to prevent electrical noise being converted into clock jitter by coupling onto the loop filter pins.

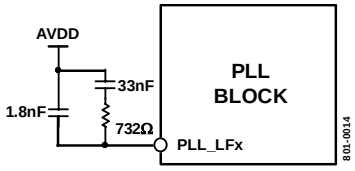

Figure 16. PLL L

F

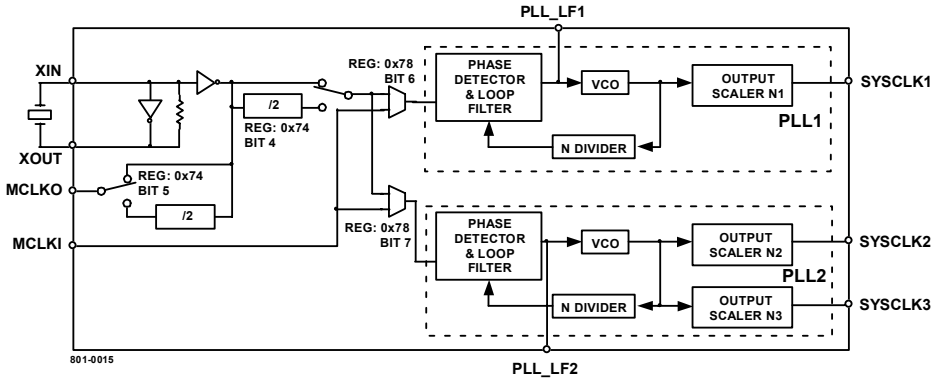

Figure 17. PLL Section Block Diagram

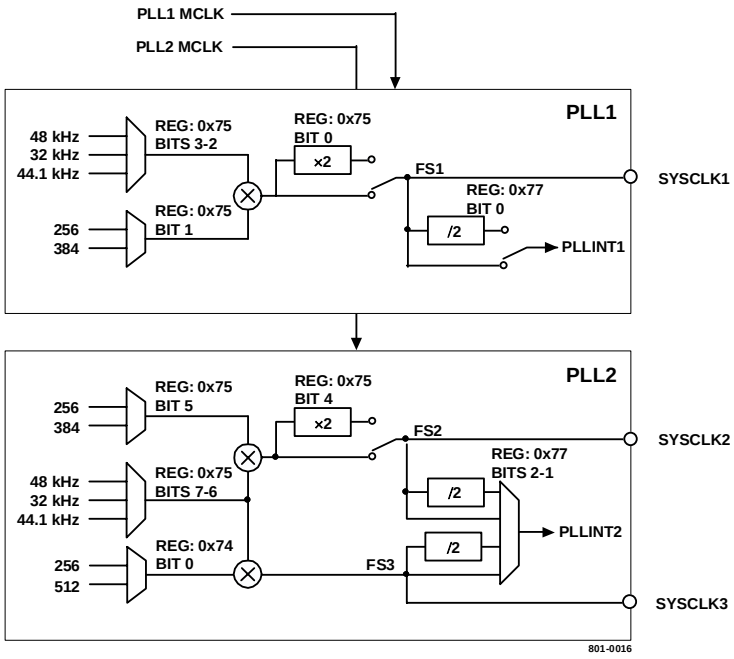

Figure 18. PLL Clocking Scheme

SPDIF TRANSMITTER AND RECEIVER

The ADAV804 contains an integrated SPDIF transmitter and receiver. The transmitter consists of a single output pin, DITOUT, on which the biphase encoded data appears. The SPDIF transmitter source can be selected from the different blocks making up the ADAV804. Additionally the clock source for the SPDIF transmitter can be selected from the various clock sources available in the ADAV804. The receiver uses two pins, DIRIN and DIR_LF. DIRIN accepts the SPDIF input data stream. The DIRIN pin can be configured to accept a digital input level as defined by Table 13 or an input signal with a peak to peak level of 200mV minimum as defined by the IEC60958-3 specification. DIR_LF is a loop filter pin required by the internal PLL which is used to recover the clock from the SPDIF data stream. The components shown in Figure 22 form a loop filter which integrates the current pulses from a charge pump and produces a voltage which is used to tune the VCO of the clock recovery PLL. The recovered audio data and audio clock can be routed to the different blocks of the ADAV801 as required. Figure 19shows a conceptual diagram of the DIRIN block.

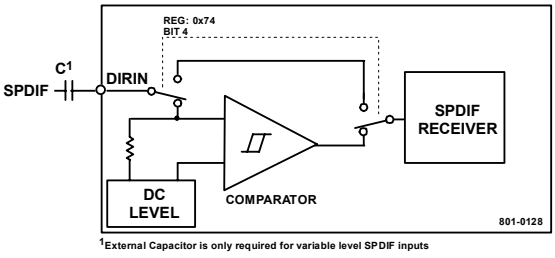

Figure 19. DIRIN Block

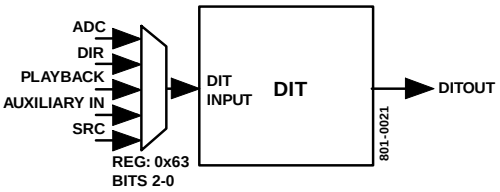

Figure 20. Digital Output Transmitter Block Diagram

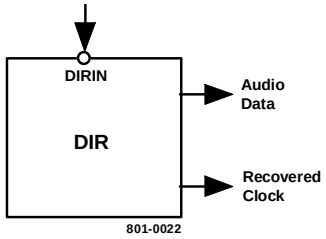

Figure 21. Digital Input Receiver Block Diagram

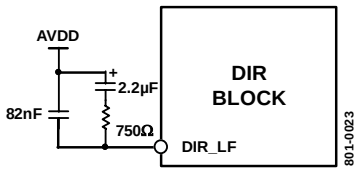

Figure 22. DIR loop Filter Components

Serial Digital Audio Transmission Standards

The ADAV804 can receive and transmit SPDIF, AES/EBU and IEC-958 serial streams. SPDIF is a consumer audio standard and AES/EBU is a professional audio standard. IEC-958 has both consumer and professional definitions. This data sheet is not intended to fully define or to provide a tutorial for these standards, please contact the international standards setting bodies for the full specifications.

All of these digital audio serial communication schemes encode audio data and audio control information using the biphase-mark method. This encoding method minimizes the dc content of the transmitted signal. As can be seen from Figure 23 ones in the original data end up with midcell transitions in the biphase-mark encoded data, while zeros in the original data do not. Note that the biphase-mark encoded data always has a transition between bit boundaries.

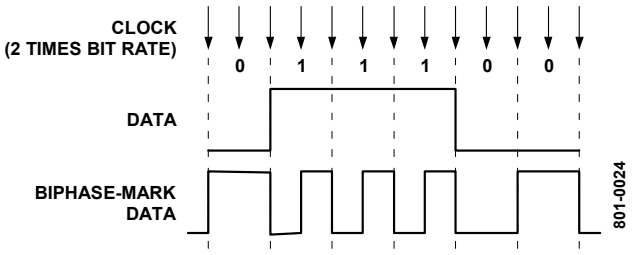

Figure 23. Biphase-Mark Encoding

Digital audio communication schemes use "preambles" to distinguish between channels (called "subframes") and between longer term control information blocks (called "frames"). Preambles are particular biphase-mark patterns, which contains encodeing violations that allow the receiver to uniquely recognize them. These patterns, and their relationship to frames and subframes, are shown in Figure 24 and Figure 25.

	BIPHASE PATTERNS	CHANNEL
X	11100010 OR 00011101	LEFT
Y	11100100 OR 00011011	RIGHT
Z	11101000 OR 00010111	LEFT AND C.S. BLOCKSTART

801-0025

Figure 24. Biphase-Mark Encoded Preambles

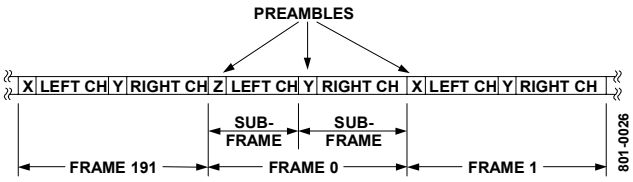

Figure 25. Preambles, Frames and Subframes

The biphase-mark encoding violations are shown in Figure 26. Note that all three preambles include encoding violations. Ordinarily, the biphase-mark encoding method results in a polarity transition between bit boundaries.

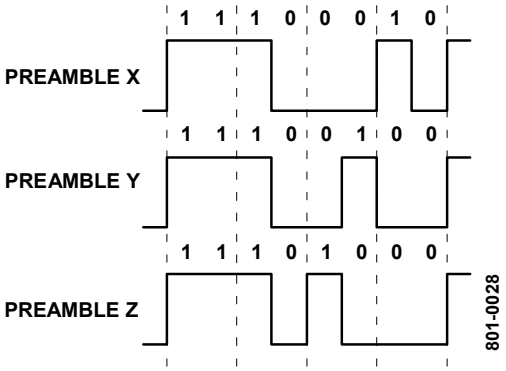

Figure 26. Preambles

The serial digital audio communication scheme are organized using a frame and subframe construction. There are two subframes per frame (ordinarily the left and right channel). Each subframe includes the appropriate four bit preamble, up to 24 bits of audio data, a "validity" (V) bit, a "user" (U) bit, a "channel status" (C) bit and an even "parity" (P) bit. The channel status bits and the user bits accumulate over many frames to convey control information. The channel status bits accumulate over a 192 frame period (called a channel status block). The user bits accumulate over 1176 frames when the interconnect is implementing the so-called "subcode" scheme (EIAJ CP-2401). The organization of the channel status block, frames and subframes are shown in Figure 27 and Figure 28.

	Data Bits							
Address	7	6	5	4	3	2	1	0
N	Channel Status		Emphasis			Copy-right	Non-Audio	Pro/Con =0
N+1	Category Code							
N+2	Channel Number					Source Number		
N+3	Reserved		Clock Accuracy			Sampling Frequency		
N+4	Reserved					Word Length		
(N+5) to (N+23)	Reserved							

801-0029

N = 0x20 for Receiver Channel Status Buffer
N = 0x38 for Transmitter Channel Status Buffer

Figure 27. Consumer

	Data Bits							
Address	7	6	5	4	3	2	1	0
N	Sample Frequency		Lock	Emphasis			Non-Audio	Pro/Con =1
N+1	User Bit Management			Channel Mode				
N+2	Alignment Level		Source Word Length			Use of Auxiliary Mode Sample Bits		
N+3	Channel Identification							
N+4	fs Scaling	Sample Frequency (fs)			Res-erved	Digital Audio Reference Signal		
N+5	Reserved							
N+6	Alphanumeric Channel Origin Data - First Character							
N+7	Alphanumeric Channel Origin Data							
N+8	Alphanumeric Channel Origin Data							
N+9	Alphanumeric Channel Origin Data - Last Character							
N+10	Alphanumeric Channel Destination Data - First Character							
N+11	Alphanumeric Channel Destination Data							
N+12	Alphanumeric Channel Destination Data							
N+13	Alphanumeric Channel Destination Data - Last Character							
N+14	Local Sample Address Code - LSW							
N+15	Local Sample Address Code							
N+16	Local Sample Address Code							
N+17	Local Sample Address Code - MSW							
N+18	Time Of Day Code - LSW							
N+19	Time Of Day Code							
N+20	Time Of Day Code							
N+21	Time Of Day Code - MSW							
N+22	Reliability Flags			Reserved				
N+23	Cyclic Redundancy Check Character (CRCC_							

801-0030

N = 0x20 for Receiver Channel Status Buffer
N = 0x38 for Transmitter Channel Status Buffer

Figure 28. Professional

The standards allow for the channel status bits in each subframe to be independent, but ordinarily the channel status bit in the two subframes of each frame are the same. The channel status bits are defined differently for the consumer audio standards and the professional audio standards. The 192 channel status bits are organized into 24 bytes and have the interpretations shown in Figure 27 and Figure 28.

The SPDIF transmitter and receiver have a comprehensive register set. The registers give the user full access to the functions of the SPDIF block such as detecting non-audio and validity bits, Q subcodes, preambles etc. The channel status bits as defined by the IEC60958 and AES3 specification are stored in register buffers for ease of use. An autobuffering function allows for channel status and user bits read by the receiver to be copied directly to the transmitter block removing the need for user intervention.

Receiver Section

The ADAV804 uses a double buffering scheme to handle reading Channel Status and User bit information. The Channel Status bits are available as a memory buffer taking up 24 consecutive register locations. The User bits are read using an indirect memory addressing scheme where the Receiver User Bit Indirect Address register is programmed with an offset to the User bit buffer and the Receiver User Bit Data register can be read to determine the User bits at that location. Reading the Receiver User Bit Data register automatically updates the Indirect Address Register to the next location in the buffer. Typically the Receiver User Bit Indirect Address register is programmed to zero, the start of the buffer, and the Receiver User Bit Data register is read repeatedly until all the buffers data has been read. Figure 29 and Figure 30 shows how receiving the Channel Status and User bits is implemented.

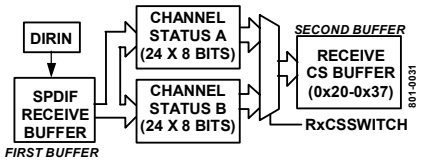

Figure 29. Channel Status Buffer

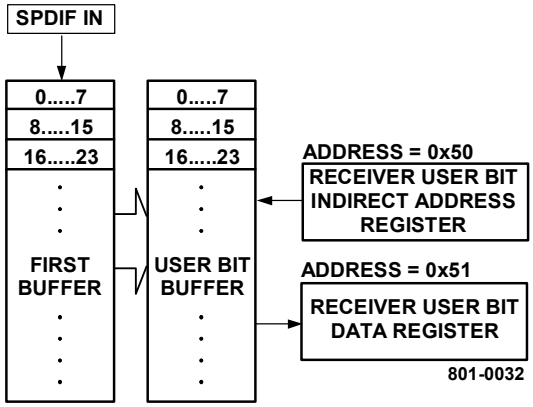

Figure 30. Receiver User Bit Buffer

The SPDIF receive buffer is updated continuously by the incoming SPDIF stream and once all of the channel status bits for the block, 192 for channel A and 192 for channel B, are received the bits are copied into the receiver channel status buffer. This buffer stores all 384 bits of channel status information and the RxCSSWITCH bit in the Channel Status Switch Buffer register determines whether the channel A or channel B status bits are required to be read. The receive channel status bit buffer is 24 bytes long and spans the address range from 0x20 to 0x37.

Since the Channel Status bits of an SPDIF stream rarely change a software interrupt/flag bit, RxCSBINT is provided to notify the host control that either a new block of channel status bits is available or that the first 5 bytes of channel status information

have changed from a previous block. The function of the RxCSBINT is controlled by the RxBCONF3 bit in the Receiver Buffer Configuration Register.

The size of the User bit buffer can be set using by programming the RxBCONF0 bit in the Receiver Buffer Configuration register as shown in Table 20.

Table 20. RxBCONF3 Functionality

RxBCONF0	Receiver User Bit Buffer Size
0	384 bits with Preamble Z as the start of the block
1	768 bits with Preamble Z as the start of the block

The updating of the User bit buffer is controlled by bits RxBCONF2-1 and bits 7 to 4 of the Channel Status as shown in Table 21 and Table 22.

Table 21. RxBCONF2-1 Functionality

RxBCONF		Receiver User Bit Buffer Configuration
Bit 2	Bit 1	
0	0	User bits are ignored
0	1	Update second buffer when first buffer is full
1	0	Format according to byte 1, bits 4-7 if PRO bit is set. Format according to IEC60958-3 if PRO bit is clear

Table 22. Automatic User Bit Configuration

Bits				Automatic Receiver User Bit Buffer Configuration
7	6	5	4	
0	0	0	0	User Bits are ignored
0	1	0	0	AES-18 format, the User bit buffer is treated in the same way as when RxBCONF2-1 = 0b01
1	0	0	0	User bit buffer is updated in the same way as when RxBCONF2-1 = 0b01 and RxBCONF0 = 0b00
1	1	0	0	User defined format, the User bit buffer is treated in the same way as when RxBCONF2-1 = 0b01

When the User bit buffer has been filled, the RxUBINT interrupt bit in the Interrupt Status register will be set, provided that the RxUBINT Mask bit is set, to indicate that the buffer has new information and can be read.

For the special case when the user data is formatted according to the IEC60958-3 standard into messages made of of information units, called IUs, the zeros stuffed between each IU and each message are removed and only the IUs are stored. Once the end of the message is sensed, by more that 8 zeros between IUs, the User bit buffer is updated with the complete message and the first buffer begins looking for the start of the next message. Each IU is stored as a byte consisting of 1, Q, R, S, T, U, V and W bits (see the IEC60958-3 specification for more information). For the case where 96IUs are received, the Q subcode of the IUs is stored in the Q subcode buffer consisting of 10 bytes. The Q subcode is the Q bits taken from each of the 96 IUs. The first 10 bytes, 80 bits, of the Q subcode contain information sent by CD, MD and DAT systems. The last 16 bits of the Q subcode are used to perform a CRC check of the Q subcode. If an error occurs in the CRC check of the Q subcode, the QCRCERROR bit will be set. This is a sticky bit and will remain high until the register is read.

Transmitter Operation

The SPDIF transmitter has a similar buffer structure to the receive section. The transmitter Channel Status buffer occupies 24 bytes of the register map. This buffer is long enough to store the 192 bits required for one channel of Channel Status information. Setting the TxCSSWITCH bit determines if the data loaded to the Transmitter Channel Status buffer is intended for channel A or channel B. In most cases the channel status bits for channel A and channel B are the same in which case setting the Tx_A/B_Same bit will read the data from the Transmitter Channel Status buffer and transmit it on both channels. Since the Channel Status information is rarely changed during transmission the information contained in the buffer is transmitted repeatedly. The Disable_Tx_Copy bit can be used to prevent the Channel Status bits from being copied from the Transmitter CS Buffer into the SPDIF Transmitter buffer until the user has finished loading the buffers. This feature is typically used if the channel A and channel B data is different. Setting the bit will prevent the data being copied and clearing the bit will allow the data to be copied and then transmitted. Figure 31 shows how the buffers are organized.

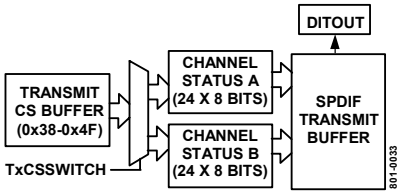

Figure 31. Transmitter Channel Status Buffer

As with the receiver section the transmitted User bits are also double buffered. This is required since, unlike the Channel Status bits, the User bits do not necessarily repeat themselves. The User bits can be buffered in various configuration as Table 23. Transmission of the user bits is determined by the state of the BCONF3 bit. If the bit is 0 the user bits will begin transmitting straight away without alignment to the Z preamble. If this bit is 1 the User bits will not start transmitting until a Z preamble occurs when the TxBCONF2-1 bits are 01.

Table 23. Transmitter User Bit Buffer Configurations

TxBCONF2-1		Transmitter User Bit Buffer Configuration
Bit2	Bit1	
0	0	Zeros are transmitted for the User bits
0	1	Host writes User bits to the buffer until it is full
1	0	Write the user bits to the buffer in IUs specified by IEC60958-3 and transmit them according to the standard
1	1	The first 10 bytes of the user bit buffer is configured to store a Q subcode

Table 24. Transmitter User Bit Buffer Size

TxBCONF0	Buffer Size
0	384 bits with Preamble Z as the start of the block
1	768 bits with Preamble Z as the start of the block

The transmit buffers can notify the host or micro-controller when the first user bit buffer has been updated and when the second transmit user bit buffer is full using sticky bits and interrupts. The sticky bit TxUBINT, is set when the transmit user buffer has been updated and the second transmit user bit buffer is ready to accept new user bits. The sticky bit, TxFBINT, is set whenever the second transmit user bit buffer is full and any new writes to this buffer will be ignored until the first transmit buffer is updated. These two bits are located in the Interrupt Status register. When the host reads the Interrupt Status register these bits will be cleared. Interrupts for the TxUBINT and TxFBINT sticky bits can be enabled by setting the TxUBMASK and TxFBMASK bits respectively in the Interrupt Status Mask register.

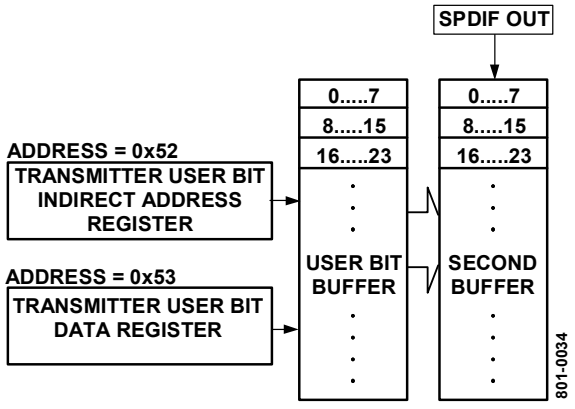

Figure 32.Transmitter User Bit Buffer

Autobuffering

The ADAV804 SPDIF receiver and transmitter sections have an autobuffering mode allowing the Channel Status and User bits to be copied automatically from the receiver to the transmitter without user intervention. The Channel Status and User bits can be independently selected for autobuffering using the Auto_CSBits and Auto_UBits bits in Autobuffer register respectively. When the receiver and transmitter are running at the same sample rate the transmitted Channel Status and User bits will be the same as the received Channel Status and User bits. However in many systems it is likely that the receiver and transmitter will not be running at the same frequency. When the transmitter sample rate is higher than receiver sample rate, the Channel Status and User bit block may be repeated sometimes. When the transmitter sample rate is lower than the receiver sample rate, the Channel Status and User bit blocks may be dropped. Since the first 5 bytes of the Channel Status are, typically, constant the can be repeated or dropped and no information is lost. However, if the PRO bit in the channel status is set and the local sample address code and time of day code bytes contain information, these bytes may be repeated or dropped in which case information can be lost. It is up to the user to determine how to handle this case. In the case of the user bits being transmitted according to the IEC60958-3 format the messages contained in the user bits can still be sent without dropping or repeating messages. Since zero-stuffing is allowed between IUs and messages, zeros can be added or subtracted to preserve the messages. For the case when the transmitter sample rate is greater than the receiver sample rate extra zeros are stuffed between the messages. When the sample rate of the transmitter is less than the sample rate of the receiver, the zeros stuffed between the messages will be subtracted. If there is not enough zeros between the messages to be subtracted, the zeros between IUs will be subtracted as well. The Zero_Stuff_IU bit in the Autobuffer register enables zeros to be added or subtracted between messages.

Interrupts

The ADAV804 provides interrupt bits to indicate the presence of certain conditions which may require attention. Reading the Interrupt Status register will allow the user to determine if any of the interrupts have be asserted. The bits of the Interrupt Status register will remain high, if set, until the register is read. Two bits, SRCError and RxError indicate interrupt conditions in the sample rate converter and an SPDIF receiver error respectively. Both of these condition require a read of the appropriate error register to determine the exact cause of the interrupt. Each interrupt in the Interrupt Status register has an associated mask bit in the Interrupt Status Mask register. The interrupt mask bit must be set for the corresponding interrupt to be generated. This feature allows the user to determine which functions should be responded to. The dual function pin ZEROL/INT can be set to indicate the presence of no audio data on the left channel or the presence of an interrupt being set in the Interrupt Status register. The function of this pin is selected by the INTRPT bit in DAC Control Register 4 as shown in Table 25.

Table 25. ZEROL/INT Pin Functionality

INTRPT	Pin Functionality
0	The pin functions as a ZEROL flag pin
1	The pin functions as an interrupt pin

SERIAL DATA PORTS

The ADAV804 contains four flexible serial ports (SPORTs) to allow data transfer to and from the codec. All four SPORTs are independent and can be configured as master or slave ports. In Slave Mode the xLRCLK and xBCLK signals are inputs to the serial ports. In Master Mode, the serial port generates the xLRCLK and xBCLK signals. The master clock for the SPORT can be selected from a number of sources, as shown in Figure 34 and care should be taken to ensure that the clock rate is appropriate for whatever block is connected to the serial port. For example if the ADC is running from the MCLKI input at $256 \times f_S$ then the master clock for the SPORT should also run run from the MCLKI input to ensure that the ADC and serial port are synchronised. The SPORTs can be set to transmit or receive data in I^2S, Left Justified or Right Justified formats with different word lengths by programming the appropriate bits in the Playback, Auxiliary Input Port, Record and Auxiliary Output Port Control Registers. Figure 33 shows a timing diagram of the serial data port formats.

CLOCKING SCHEME

The ADAV804 provides a flexible choice of on-chip and off-chip clocking sources. The on-chip oscillator with dual-PLLs is intended to offer complete system clocking requirements for use with available MPEG encoders, decoders or combination codecs. The oscillator function is designed for generation of a 27 MHz video clock from a 27 MHz crystal connected between XIN and XOUT pins. Capacitors are also required to be connected between these pins and DGND as shown in Figure 15. The capacitor values should be specified by the crystal manufacturer. A square-wave version of the crystal clock is output on the MCLKO pin. If the system has 27MHz clock available this can be connected directly to the XIN pin.

DATA PATH

The ADAV804 features a Digital Input/Output switching/multiplexing matrix which gives flexibility to the range of possible Input and Output connections. Digital Input ports include Playback and Auxiliary Input - both 3-wire digital - and S/PDIF (single wire to the on-chip receiver). Output ports include the Record and Auxiliary Output ports - both 3-wire digital - and the S/PDIF port (single wire from the on-chip transmitter). Internally the DIR and DIT are interfaced via 3-wire interfaces. The data path for each input and output port is selected by programming Datapath Control Registers 1 and 2. Figure 35 shows the internal data path structure of the ADAV804.

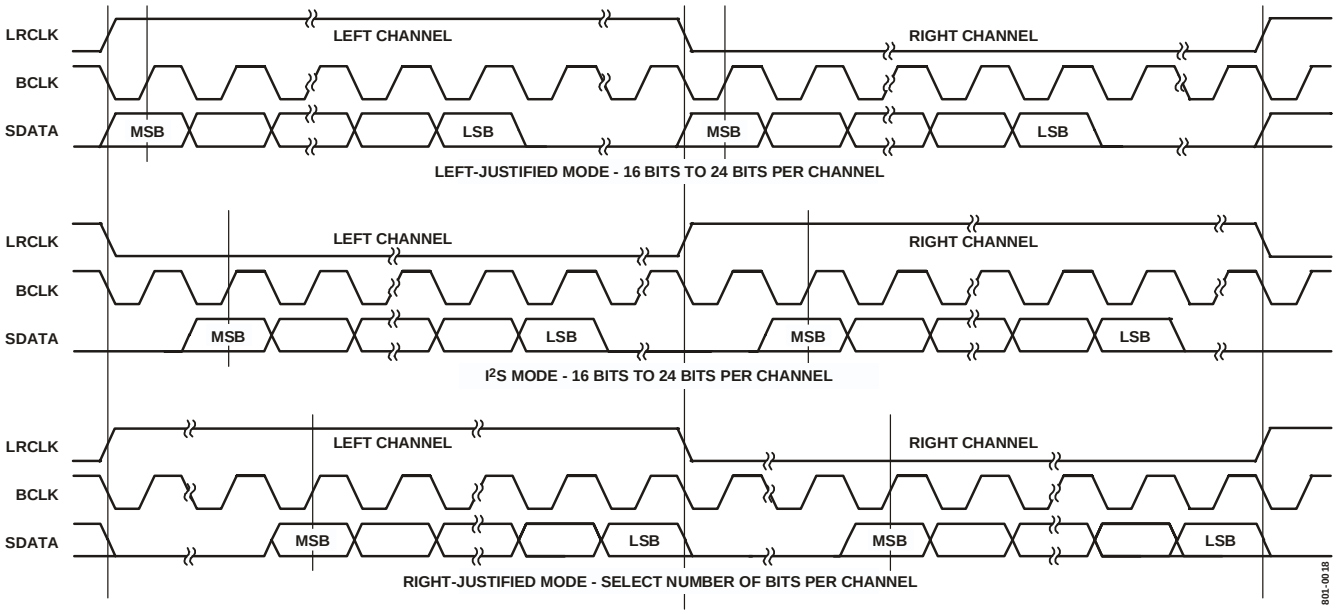

Figure 33. Serial Data Modes

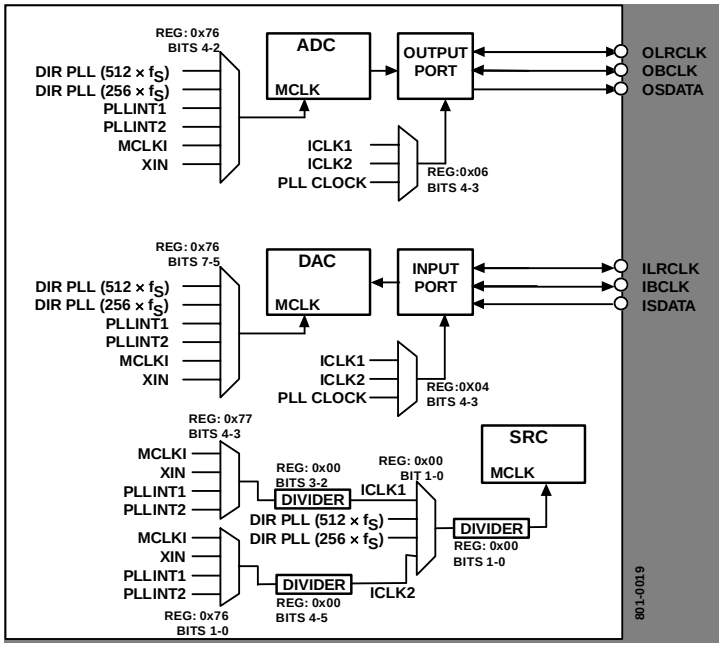

Figure 34. Sport Clocking Scheme

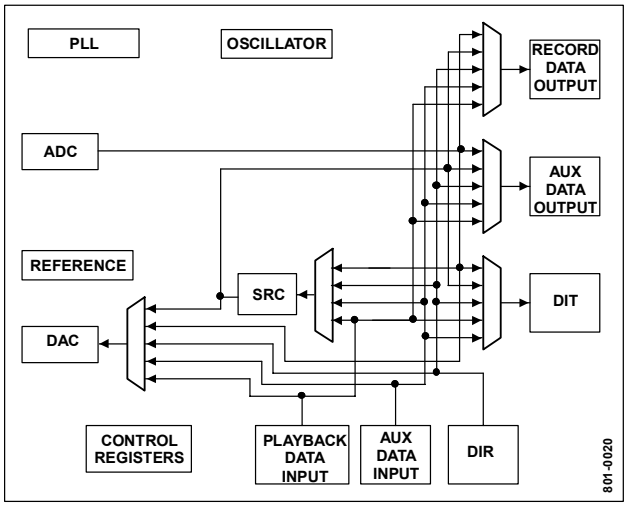

Figure 35. Data Path

INTERFACE CONTROL

The ADAV804 has a dedicated control port to allow the internal registers of the ADAV804 to be accessed. Each of the internal registers is 8 bits wide. Where bits are described as reserved (RES) these bits should be programmed as zero.

I²C Interface

The I²C interface of the ADAV804 is a two wire interface consisting of a clock line, SCL and a data line, SDA. SDA is bidirectional and the ADAV804 will drive SDA either to acknowledge the master, ACK, or to send data during a read operation. The SDA pin for the I²C port is an open drain collector and requires a 1KΩ pullup resistor. A write or read access occurs when the SDA line is pulled low while the SCL line is high indicated by START in the timing diagrams. SDA is only allowed to change when SCL is low except when a START or STOP condition occurs as shown in figures 36 and 37. The first eight bits of the access consist of the device address and the R/W bit. The device address consists of an internal built-in address (0b00100) and two address pins, AD1 and AD0. The two address pins allow up to four ADAV804s to be used in a system. Initiating a write operation to the ADAV804 involves sending a START condition and then sending the device address with the R/W set low. The ADAV804 will respond by issuing an ACK to indicate that it has been addressed. The user

then sends a second frame telling the ADAV804 which register is required to be written to. The 7 bit register address is left shifted to make the 8 bits that the frame requires. Another ACK is issued by the ADAV804. Finally the user can send another frame with the 8 data bits required to be written to the register. A third ACK is issued by the ADAV804 after which the user can send a STOP condition to complete the data transfer.

A read operation requires that the user first write to the ADAV804 to point to the correct register and then read the data. This is achieved by sending a START condition followed by the device address frame, with R/W low, and then the register address frame. Following the ACK from the ADAV804 the user must issue a REPEATED START condition. This is identical to a START condition. The next frame is the device address with R/W set high. On the next frame the ADAV804 will output the register data on the SDA line. A STOP condition completes the read operation. Figure 38 and Figure 39 show examples of writing to and reading from the DAC Left Volume Register (address = 0b1101000)

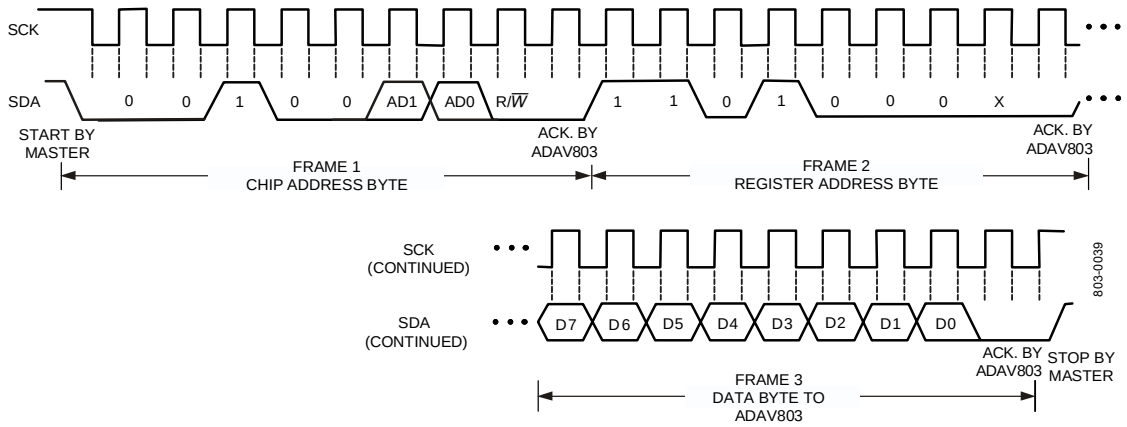

Figure 38. Writing to the ADAV804 inI²C

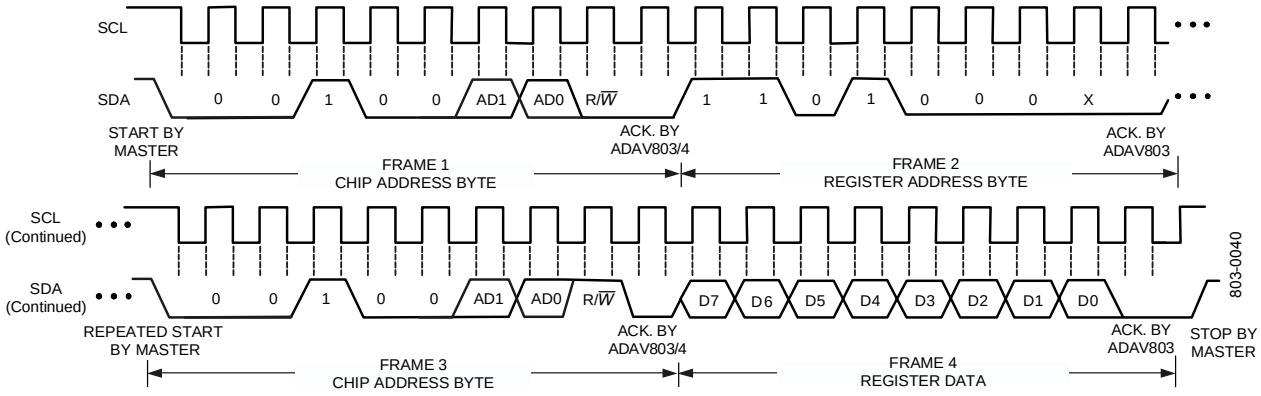

Figure 39. Reading From the DAC Leeft VolumeRegister in I²C

Block Reads and Writes

The ADAV804 provides the user with the ability to write to or read from a block of registers in one continuous operation. To use this feature the user simply has to continue providing data frames before the STOP condition. For a write operation the Register Address is automatically incremented with each additional frame and the register data is written to that register address. For a read operation the Register Address is automatically incremented with each additional frame and the register data is clocked out on that frame. Care should be exercised when using the block read or block write modes. For most cases block reading, or writing to, a register will automatically increment the register address to point to the next register. The exceptions to this case are the indirect memory address registers, Transmitter User Bit and Receiver User Bit

data buffers. Using a block read or write to access these registers will not update the absolute register address but rather will update the buffer address to provide the next value in the buffer.

Table 26. SRC & Clock Control Register

	SRCDIV1	SRCDIV	CLK2-DIV1	CLK2-DIV0	CLK1-DIV1	CLK1-DIV0	MCLK-SEL1	MCLK-SEL0
	7	6	5	4	3	2	1	0
ADDRESS = 0000000								
SRCDIV1-0	Divides the SRC Master Clock 00 = The SRC Master Clock is not divided 01 = The SRC Master Clock is divided by 1.5 10 = The SRC Master Clock is divided by 2 11= The SRC Master Clock is divided by 3							
CLK2DIV1-0	Clock Divider for Internal Clock 2 (ICLK2) 00 = Divide by 1 01 = Divide by 1.5 10 = Divide by 2 11 = Divide by 3							
CLK1DIV1-0	Clock Divider for Internal Clock 1 (ICLK1) 00 = Divide by 1 01 = Divide by 1.5 10 = Divide by 2 11 = Divide by 3							
MCLKSEL1-0	Clock Selection for the SRC Master Clock 00 = Internal Clock 1 01 = Internal Clock 2 10 = PLL Recovered Clock (512 × f_S) 11 = PLL Recovered Clock (256 × f_S)							

Table 27. SPDIF Loopback Control Register

	RES	RES	RES	RES	RES	RES	RES	TxMUX
	7	6	5	4	3	2	1	0
ADDRESS = 0000011								
TxMUX	Selects the source for SPDIF Output (DITOUT) 0 = SPDIF Transmitter - Normal Mode 1 = DIRIN - Loopback Mode							

Table 28. Playback Port Control Register

	RES	RES	RES	CLKSRC1	CLKSRC0	SPMODE2	SPMODE1	SPMODE0
	7	6	5	4	3	2	1	0
ADDRESS = 0000100								
CLKSRC1-0	Selects the Clock Source for generating the ILRCLK and IBCLK 00 = Input Port is a Slave 01 = Recovered PLL Clock 10 = Internal Clock 1 11 = Internal Clock 2							
SPMODE1-0	Selects the serial format of the Playback Port 000 = Left Justified 001 = I²S 100 = 24 Bit Right Justified 101 = 20 Bit Right Justified 110 = 18 Bit Right Justified 111 = 16 Bit Right Justified							

Table 29. Auxiliary Input Port Register

	RES	RES	RES	CLKSRC1	CLKSRC0	SPMODE2	SPMODE1	SPMODE0
	7	6	5	4	3	2	1	0
ADDRESS = 0000101								
CLKSRC1-0	Selects the Clock Source for generating the IAUXLRCLK and IAXUBCLK 00 = Input Port is a Slave 01 = Recovered PLL Clock 10 = Internal Clock 1 11 = Internal Clock 2							
SPMODE1-0	Selects the serial format of Auxiliary Input Port 000 = Left Justified 001 = I²S 100 = 24 Bit Right Justified 101 = 20 Bit Right Justified 110 = 18 Bit Right Justified 111 = 16 Bit Right Justified							

Table 30. Record Port Control Register

	RES	RES	CLKSRC1	CLKSRC0	WLEN1	WLEN0	SPMODE1	SPMODE0
	7	6	5	4	3	2	1	0
ADDRESS = 0000110								
RES	Reserved							
CLKSRC1-0	Selects the Clock Source for generating the OLRCLK and OBCLK							
	00 = Record Port is a Slave							
	01 = Recovered PLL Clock							
	10 = Internal Clock 1							
	11 = Internal Clock 2							
WLEN1-0	Selects the Serial Output Word Length							
	00 = 24 Bits							
	01 = 20 Bits							
	10 = 18 Bits							
	11 = 16 Bits							
SPMODE1-0	Selects the serial format of the Record Port							
	00 = Left Justified							
	01 = I^2S							
	10 = Reserved							
	11 = Right Justified							

Table 31. Auxiliary Output Port Register

	RES	RES	CLKSRC1	CLKSRC0	WLEN1	WLEN0	SPMODE1	SPMODE0
	7	6	5	4	3	2	1	0
ADDRESS = 0000111								
RES	Reserved							
CLKSRC1-0	Selects the Clock Source for generating the OAUXLRCLK and OAUXBCLK							
	00 = Auxiliary Record Port is a Slave							
	01 = Recovered PLL Clock							
	10 = Internal Clock 1							
	11 = Internal Clock 2							
WLEN1-0	Selects the Serial Output Word Length							
	00 = 24 Bit							
	01 = 20 Bits							
	10 = 18 Bits							
	11 = 16 Bits							
SPMODE1-0	Selects the serial format of the Auxiliary Record Port							
	00 = Left Justified							
	01 = I^2S							
	10 = Reserved							
	11 = Right Justified							

Table 32. Group Delay and Mute Register

	MUTE_SRC	GRPDLY6-0
	7	6,5,4,3,2,1,0
ADDRESS = 0001000		
MUTE_SRC	Soft Mutes the Output of theSample Rate Converter 0 = No Mute 1 = Soft Mute	
GRPDLY6-0	Adds delay to the Sample Rate Converter FIR filter by GRPDLY6-0 Input Samples 0000000 = No Delay 0000001 = 1 Sample Delay 0000010 = 2 Sample Delay 1111110 = 126 Sample Delay 1111111 = 127 Sample Delay	

Table 33. Receiver Configuration 1 Register

	NO- CLOCK	RXCLK1-0	AUTO_ DEEMPH	ERR1-0	LOCK1-0
	7	6,5	4	3,2	1,0
ADDRESS = 0001001					
NOCLOCK	Selects the source of the Receiver Clock when the PLL is not locked 0 = The Recovered PLL Clock is used 1 = ICLK1 is used				
RXCLK1-0	Determines the oversampling ratio of the Recovered Receiver Clock 00 = RxCLK is a 128 × f_S recovered clock 01 = RxCLK is a 256 × f_S recovered clock 10 = RxCLK is a 512 × f_S recovered clock 11 = Reserved				
AUTO_DEEMPH	Automatically de-emphasizes the data from the receiver based on the Channel Status Information 0 = Automatic De-emphasis is disabled 1 = Automatic De-emphasis is enabled				
ERR1-0	Defines what action the receiver should take if the receiver detects a parity or biphase error 00 = No action will be taken 01 = The last valid sample is held 10 = The invalid sample is replaced with zeros 11 = Reserved				
LOCK1-0	Defines what action the receiver should take if the PLL loses lock. 00 = No action will be taken 01 = The last valid sample will be held 10 = Zeros will be sent out after the last valid sample 11 = Soft Mute of the last valid audio sample				

Table 34. Receiver Configuration 2 Register

	RxMUTE	SP-PLL	SP_PLL_ SEL1-0	RES	RES	NO NON-AUDIO	NO_ VALIDITY
	7	6	5,4	3	2	1	0
ADDRESS = 0001010							
RxMUTE	Hard Mutes the Audio Output for the AES3/SPDIF Receiver 0 = AES3/SPDIF Receiver is not muted 1 = AES3/SPDIF Receiver is muted						
SP_PLL	The AES3/SPDIF Receiver PLL will accept a Left/Right Clock from one of the four serial ports as the PLL reference clock 0 = Left/Right Clock generated from the AES3/SPDIF preambles is the reference clock to the PLL 1 = Left/Right Clock from one of the serial ports is the reference clock to the PLL						
SP_PLL_SEL1-0	Selects one of the four serial ports as the reference clock to the PLL when SP_PLL is set 00 = Playback Port is selected 01 = Auxiliary Input Port is selected 10 = Record Port is selected 11 = Auxiliary Output Port is selected						
NO NONAUDIO	When the NONAUDIO bit is set, data from the AES3/SPDIF Receiver will not be allowed into the Sample Rate Converter (SRC). If the NONAUDIO data is due to DTS, AAC, etc. as defined by the IEC61937 standard, then the data from the AES3/SPDIF Receiver will not be allowed into the SRC regardless of the state of this bit 0 = AES3/SPDIF Receiver data will be sent to the SRC 1 = Data fro the AES3/SPDIF Receiver will not be allowed into the SRC if the NONAUDIO bit is set						
NO_VALIDITY	When the VALIDITY bit is set data from the AES3/SPDIF Receiver will not be allowed into the SRC 0 = AES3/SPDIF Receiver data will be sent to the SRC 1 = Data from the AES3/SPDIF Receiver will not be allowed into the SRC if the VALIDITY bit is set						

Table 35. Receiver Buffer Configuration Register

	RES	RES	RxBCONF5	RxBCONF4	RxBCONF3	RxBCONF2-1	RxBCONF0
	7	6	5	4	3	2,1	0
ADDRESS = 0001011							
RxBCONF5	If the user bits are formatted according to the IEC60958-3 standard and the DAT Category is detected, the User Bit interrupt is only enabled when there is a change in the Start (ID) bit. 0 = The User Bit interrupt is enabled in the normal mode. 1 = If the DAT category is detected, the User bit interrupt is only enabled if there is a change in the Start (ID) bit						
RxBCONF4	This bit determines whether Channel A and Channel B User Bits are stored in the buffer together or separated between A and B 0 = The User Bits are stored together 1 = The User Bits are stored separately						
RxBCONF3	Defines the function of RxCSBINT 0 = RxCSBINT will be set when a new block of receiver channel status is read, which is 192 audio frames 1 = RxCSBINT will be set only if the first five bytes of the receiver channel status block changes from the previous channel status block						
RxBCONF2-1	Defines the User Bit Buffer 00 = User Bits are ignored 01 = Update the second user bit buffer when the first user bit buffer is full 10 = Format the received user bits according to byte 1, bits 4-7, of the channel status if the PRO bit is set. If the PRO bit is not set format the user bits according to the IEC60958-3 standard 11 = Reserved						
RxBCONF0	Defines the User Bit buffer size if RxBCONF2-1 = 01 0 = 384 Bits with Preamble-Z as the start of the buffer 1 = 768 Bits with Preamble-Z as the start of the buffer						

Table 36. Transmitter Control Register

	RES	Tx-VALIDITY	Tx-RATIO2-0	TxCLK SEL1-0	Tx-ENABLE
	7	6	5,4,3	2,1	0
ADDRESS = 0001100					

TxVALIDITY	This bit is used to set or clear the VALIDITY bit in the AES3/SPDIF Transmit stream
	0 = Audio is suitable for D/A conversion
	1 = Audio is not suitable for D/A conversion
TxRATIO2-0	Determines the AES3/SPDIF Transmit to AES3/SPDIF Receiver ratio
	000 = Transmitter to Receiver Ratio is 1:1
	001 = Transmitter to Receiver Ratio is 1:2
	010 = Transmitter to Receiver Ratio is 1:4
	101 = Transmitter to Receiver Ratio is 2:1
	110 = Transmitter to Receiver Ratio is 4:1
TxCLKSEL1-0	Selects the clock source for the AES3/SPDIF Transmitter
	00 = Internal Clock 1 is the clock source for the Transmitter
	01 = Internal Clock 2 is the clock source for the Transmitter
	10 = The recovered PLL clock is the clock source for the Transmitter
	11 = Reserved
TxENABLE	Enables the AES3/SPDIF Transmitter
	0 = The AES3/SPDIF Transmitter is disabled
	1 = The AES3/SPDIF Transmitter is enabled

Table 37. Transmitter Buffer Configuration Register

	IU_Zeros3-0	TxBCONF3	TxBCONF2-1	TxBCONF0
	7,6,5,4	3	2,1	0
ADDRESS = 0001101				

IU_Zeros3-0	Determines the number of zeros to be stuffed between IUs in a message up to a maximum of 8
	0000 = 0
	0001 = 1
	.....
	0111 = 7
	1000 = 8
TxBCONF3	The Transmitter User Bits can be stored in separate buffers or stored together
	0 = The User Bits are stored together
	1 = The User Bits are stored seperately
TxBCONF2-1	Configures the Transmitter User Bit Buffer.
	00 = Zeros are transmitted for the User Bits
	01 = The transmitter User Bit buffer size is configured according to TxBCONF0
	10 = Write the User Bits to the transmit buffer in IUs specified by the IEC60958-3 standard
	11 = Reserved
TxBCONF0	Determines the buffer size of the transmitter user bits when TxBCONF2-1 is 01
	0 = 384 Bits with Preamble-Z as the start of the buffer
	1 = 768 Bits with Preamble-Z as the start of the buffer

Table 38. Channel Status Switch Buffer and Transmitter

	RES	RES	Tx_A/B Same	Disable_ Tx_Copy	RES	RES	TxCSSWITCH	RxCSSWITCH
	7	6	5	4	3	2	1	0
ADDRESS = 0001110								
Tx_A/B_Same	Transmitter Channel Status A and B are the same. The transmitter will only read from the Channel Status A buffer and place the data into the Channel Status B buffer 0 = Channel Status for A and B are separate 1 = Channel Status for A and B are the same							
Disable_Tx_Copy	Disables the copying of the Channel Status bits from Transmitter Channel Status Buffer to SPDIF Transmitter Buffer 0 = Copying Transmitter Channel Status is enabled 1 = Copying Transmitter Channel Status is disabled							
RES	Reserved							
RES	Reserved							
TxCSSWITCH	The toggle switch for the Transmit Channel Status Buffer 0 = The 24 byte Transmitter Channel Status A Buffer can be accessed at address locations 0x38 through 0x4F 1 = The 24 byte Transmitter Channel Status B Buffer can be accessed at address locations 0x38 through 0x4F							
RxCSSWITCH	The toggle switch for the Receive Channel Status Buffer 0 = The 24 byte Receiver Channel Status A Buffer can be accessed at address locations 0x20 through 0x37 1 = The 24 byte Receiver Channel Status B Buffer can be accessed at address locations 0x20 through 0x37							

Table 39. Transmitter Message Zeros Most Significant Byte

	MSBZeros7-0
	7,6,5,4,3,2,1,0
ADDRESS = 0001111	
MSBZero7-0	The most significant byte of the number of zeros to be stuffed between IEC60958-3 messages (packets) Default = 0x00

Table 40. Transmitter Message Zeros Least Significant Byte

	LSBZeros7-0
	7,6,5,4,3,2,1,0
ADDRESS = 0010000	
LSBZero7-0	The least significant byte of the number of zeros to be stuffed between IEC60958-3 messages (packets) Default = 0x09

Table 41. Autobuffer Register

	RES	Zero_Stuff_IU	Auto_Ubits	Auto_CSBits	IU_Zeros3-0
	7	6	5	4	3,2,1,0
ADDRESS = 0010001					
Zero_Stuff_IU	Enables the addition or subtraction of zeros between IUs during autobuffering of the user bits in IEC60958-3 format 0 = No Zeros added or subtracted 1 = Zeros can be added or subtracted between IUs				
Auto_UBits	Enables the User Bits to be autobuffered between the AES3/SPDIF receiver and transmitter 0 = The User Bits are not autobuffered 1 = The User Bits are autobuffered				
Auto_CSBits	Enables the Channel Status bits to be autobuffered between the AES3/SPDIF receiver and transmitter 0 = The Channel Status bits are not autobuffered 1 = The Channel Status bits are autobuffered				
IU_Zeros3-0	Sets the maximum number of zero stuffing to be added between IUs while autobuffering up to a maximum of 8 0000 = 0 0001 = 1 ..... 0111 = 7 1000 = 8				

Table 42. Sample Rate Ratio MSB Register (Read Only)

	RES	SRCRATIO14-SRCRATIO08
	7	6,5,4,3,2,1,0
ADDRESS = 0010010		
SRCRATIO14-08	The seven most significant bits of the fifteen bit sample rate ratio	

Table 43. Sample Rate Ratio LSB Register (Read Only)

	SRCRATIO07-SRCRATIO01
	7,6,5,4,3,2,1,0
ADDRESS = 0010011	
SRCRATIO07-00	The eight least significant bits of the fifteen bit sample rate ratio

Table 44. Preamble-C MSB Register (Read Only)

	PRE_C15-PRE_08
	7,6,5,4,3,2,1,0
ADDRESS = 0010100	
PRE_C15-08	The eight most significant bits of the sixteen bit Preamble-C when Nonaudio data is detected according to the IEC60937 standard, otherwise bits show zeros

Table 45. Preamble-C LSB Register (Read Only)

	PRE_C07-PRE_C00
	7,6,5,4,3,2,1,0
ADDRESS = 0010101	
PRE_C07-00	The eight least significant bits of the sixteen bit Preamble-C when Nonaudio data is detected according to the IEC60937 standard, otherwise bits show zeros

Table 46. Preamble-D MSB Register (Read Only)

	PRE_D15-PRE_D08
	7,6,5,4,3,2,1,0
ADDRESS = 0010110	
PRE_D15-08	The eight most significant bits of the sixteen bit Preamble-D when Nonaudio data is detected according to the IEC60937 standard, otherwise bits show zeros. When subframe Nonaudio is used this becomes the 8 most significant bits of the 16 bit Preamble-C of Channel B

Table 47. Preamble-D LSB Register (Read Only)

	PRE_D07-PRE_D00
	7,6,5,4,3,2,1,0
ADDRESS = 0010111	
PRE_D07-00	The eight least significant bits of the sixteen bit Preamble-D when Nonaudio data is detected according to the IEC60937 standard, otherwise bits show zeros When subframe Nonaudio is used this becomes the 8 most significant bits of the 16 bit Preamble-C of Channel B

Table 48. Receiver Error Register (Read Only)

	RxValidity	Emphasis	Non-Audio	NonAudio Preamble	CRC-Error	No-Stream	BiPhase/Parity	Lock
	7	6	5	4	3	2	1	0
ADDRESS = 0011000								
RxValidity	This is the VALIDITY bit in the AES3 Received stream							
Emphasis	This bit will be set if the audio data is preemphasized. Once it has been read it will remain high and not generate an interrupt unless it changes state							
NonAudio	This bit will be set when Channel Status Bit 1 (Nonaudio) is set. Once it has been read it will not generate another interrupt unless the data becomes audio or the type of nonaudio data changes							
NonAudio Preamble	This bit will be set if the audio data is nonaudio due to the detection of a Preamble. The NonAudio Preamble Type register will indicate what type of preamble was detected. Once read it will remain in its state and not generate an interrupt unless it has changed state							
CRCError	This bit is the error flag for the channel status CRC error check. This bit will not clear until the Receiver Error Register is read							
NoStream	This bit will be set if there is no AES3/SPDIF stream present at the AES3/SPDIF receiver. Once read it will remain high and not generate an interrupt unless its changes state.							
BiPhase/Parity	This bit will be set if a biphase or parity error occurred in the AES3/SPDIF stream. This bit will not be cleared until the register is read.							
Lock	This bit will be set if the PLL has locked or cleared when the PLL loses lock. Once read it will remain in its state and not generate an interrupt unless it has changed state.							

Table 49. Receiver Error Mask Register

	RxValidity Mask	Emphasis Mask	Nonaudio Mask	NonAudio Preamble Mask	CRC Error Mask	Nostream Mask	BiPhase/ Parity Mask	Lock Mask
	7	6	5	4	3	2	1	0
ADDRESS = 0011001								

RxValidity Mask	Masks the RxValidity bit from generating an interrupt 0= The RxValidity bit will not generate an interrupt 1 = The RxVvalidity bit will generate and interrupt
Emphasis Mask	Masks the Emphasis bit from generating an interrupt 0 = The Emphasis bit will not generate an interrupt 1 = The Emphasis bit will generate and interrupt
NonAudio Mask	Masks the NonAudio bit from generating an interrupt 0 = The NonAudio bit will not generate an interrupt 1 = The NonAudio bit will generate and interrupt
NonAudioPreamble Mask	Masks the NonAudio Preamble bit from generating an interrupt 0 = The NonAudio Preamble bit will not generate an interrupt 1 = The NonAudio Preamble bit will generate and interrupt
CRCError Mask	Masks the CRC Error bit from generating an interrupt 0 = The CRC Error bit will not generate an interrupt 1 = The CRC Error bit will generate and interrupt
NoStream Mask	Masks the NoStream bit from generating an interrupt 0 = The NoStream bit will not generate an interrupt 1 = The NoStream bit will generate an interrupt
BiPhase/Parity Mask	Masks the BiPhase/Parity bit from generating an interrupt 0 = The BiPhase/Parity bit will not generate an interrupt 1 = The BiPhase/Parity bit will generate an interrupt
Lock Mask	Masks the Lock bit from generating an interrupt 0 = The Lock bit will not generate an interrupt 1 = The Lock bit will generate an interrupt

Table 50. Sample Rate Converter Error Register (Read Only)

	RES	RES	RES	RES	TOO_SLOW	OVRL	OVRR	MUTE_IND
	7	6	5	4	3	2	1	0
ADDRESS = 0011010								

TOO_SLOW	This bit is set when the clock to the SRC is too slow, i.e. there are not enough clock cycles to complete the internal convolution.
OVRL	This bit will be set when the Left Output Data of the sample rate converter has gone over the full-scale range and has been clipped. This bit will not be cleared until the register is read.
OVRR	This bit will be set when the Right Output Data of the sample rate converter has gone over the full-scale range and has been clipped. This bit will not be cleared until the register is read.
MUTE_IND	Mute Indicated. This bit is set when the SRC is in Fast Mode and clicks or pops may be heard in the SRC output data. The output of the SRC can be muted, if required, until the SRC is in Slow Mode. Once read this bit will remain in its state and not generate an interrupt until it has changed state.

Table 51. Sample Rate Converter Error Mask Register

	RES	RES	RES	RES	RES	OVRL Mask	OVRR Mask	MUTE_IND MASK
	7	6	5	4	3	2	1	0
ADDRESS = 0011011								
OVRL Mask	Masks the OVRL from generating an interrupt 0 = The OVRL bit will not generate an interrupt 1 = The OVRL bit will generate an interrupt							
OVRR Mask	Masks the OVRR from generating an interrupt 0 = The OVRR bit will not generate an interrupt 1 = The OVRR bit will generate an interrupt Reserved							
MUTE_IND MASK	Masks the MUTE_IND from generating an interrupt 0 = The MUTE_IND bit will not generate an interrupt 1 = The MUTE_IND bit will generate an interrupt							

Table 52. Interrupt Status Register

	SRC Error	TxCST-INT	TxUB-INT	TxCS-INT	RxCS-DIFF	RxUB-INT	RxCS-BINT	Rx-ERROR
	7	6	5	4	3	2	1	0
ADDRESS = 0011100								
SRCERROR	This bit will be set if one of the sample rate converter interrupts is asserted, and the host should immediately read the Sample Rate Converter Error register. This bit will remain high until the Interrupt Status register is read							
TxCSTINT	This bit will be set if a write to the transmitter channel status buffer was made while transmitter channel status bits were being copied from transmitter CS buffer to SPDIF Transmit buffer							
TxUBINT	This bit will be set if the SPDIF Transmit buffer is empty. This bit will remain high until the Interrupt Status register is read.							
TxCSINT	This bit will be set if the transmitter channel status bit buffer has transmitted its block of channel status. This bit will remain high until the Interrupt Status register is read							
RxCSDIFF	This bit will be set if the receiver Channel Status A block is different from the receiver Channel Status B clock. This bit will remain high until read but does not generate an interupt							
RxUBINT	This bit will be set if the Receiver User bit buffer has a new block or message. This bit will remain high until the Interrupt Status register is read.							
RxCSBINT	This bit will be set if a new block of channel status is read when RxBCONF3 = 0 or if the channel status has changed when RxBCONF3 = 1. This bit will remain high until the Interrupt Status register is read.							
RxERROR	This bit will be set if one of the AES3/SPDIF receiver interrupts is asserted and the host should immediately read the Receiver Error register. This bit will remain high until the Interrupt Status register is read.							

Table 53. Interrupt Status Mask Register

	SRCError Mask	TxCSTINT Mask	TxUBINT Mask	TxCSBINT Mask	RES	RxUBINT Mask	RxCSBINT Mask	RxError Mask
	7	6	5	4	3	2	1	0
ADDRESS = 0011101	**DEFAULT VALUE = 0x00**							
SRCError Mask	Masks the SRCError bit from generating an interrupt 0 = The SRCError bit will not generate an interrupt 1 = The SRCError bit will generate and interrupt							
TxCSTINT Mask	Masks the TxCSTBINT bit from generating an interrupt 0 = The TxSCTINT bit will not generate an interrupt 1 = The TxCSTINT bit will generate and interrupt							
TxUBINT Mask	Masks the TxUBINT bit from generating an interrupt 0 = The TxUBINT bit will not generate an interrupt 1 = The TxUBINT bit will generate and interrupt							
RxUBINT Mask	Masks the RxUBINT bit from generating an interrupt 0 = The RxUBINT bit will not generate an interrupt 1 = The RxUBINT bit will generate and interrupt							
RxCSBINT Mask	Masks the RxCSBINT bit from generating an interrupt 0 = The RxCSBINT bit will not generate an interrupt 1 = The RxCSBINT bit will generate an interrupt							
RxError Mask	Masks the RxError bit from generating an interrupt 0 = The RxError bit will not generate an interrupt 1 = The RxError bit will generate an interrupt							

Table 54. Mute and Deemphasis Register

	RES	RES	TxMUTE	RES	RES	SRC_DEEM1-0	RES
	7	6	5	4	3	2,1	0
ADDRESS = 0011110	**DEFAULT VALUE = 0x00**						
TxMUTE	Mutes the AES3/SPDIF Transmitter 0 = The Transmitter is not muted 1 = The Transmitter is muted						
SRC_DEEM1-0	Selects the Deemphasis Filter for the input data to the Sample Rate Converter 00 = No Deemphasis 01 = 32 kHz Deemphasis 10 = 44.1 kHz Deemphasis 11 = 48 kHz Deemphasis						

Table 55. NonAudio Preamble Type Register (Read Only)

	RES	**RES**	**RES**	**DTS-CD RES**	**Non Audio Preamble**	**Non Audio Frame**	**Non Audio Subframe_A**	**Non Audio Subframe_B**
	7	6	5	4	3	2	1	0
ADDRESS = 0011111			**DEFAULT VALUE = 0x**					
DTS-CD Preamble	Will be set if the DTS-CD Preamble is detect							
NonAudio Frame	This bit will be set if the data received through the AES3/SPDIF Receiver is nonaudio data according to the IEC61937 standard or nonaudio data according to SMPTE337M							
NonAudio Subframe_A	This bit will be set if the data received through Channel A of the AES3/SPDIF Receiver is subframe nonaudio data according to SMPTE337M							
NonAudio Subframe_B	This bit will be set if the data received through Channel B of the AES3/SPDIF Receiver is subframe nonaudio data according to SMPTE337M							

Table 56. Receiver Channel Status Buffer

	RCSB7	**RCSB6**	**RCSB5**	**RCSB4**	**RCSB3**	**RCSB2**	**RCSB1**	**RCSB0**
	7	6	5	4	3	2	1	0
ADDRESS = 0100000 to 0110111								
This is the 24 byte Receiver Channel Status Buffer. The PRO bit is stored at address location 0x20, bit 0. This buffer is read only if the channel status is not autobuffered between the receiver and transmitter.								

Table 57. Transmitter Channel Status Buffer

	TCSB7	**TCSB6**	**TCSB5**	**TCSB4**	**TCSB3**	**TCSB2**	**TCSB1**	**TCSB0**
	7	6	5	4	3	2	1	0
ADDRESS = 0111000 to 1001111								
This is the 24 byte Transmitter Channel Status Buffer. The PRO bit is stored at address location 0x38, bit 0. This buffer is disabled when autobuffering between the receiver and transmitter is enabled.								

Table 58. Receiver User Bit Buffer Indirect Address Register

	RxUBADDR07-RxUBADDR00
	7,6,5,4,3,2,1,0
ADDRESS = 1010000	
RxUBADDR07-00	Indirect Address pointing to the address location in the Receiver User Bit buffer

Table 59. Receiver User Bit Buffer Data Registe

	RxUBDATA07-RxUBDATA00
	7,6,5,4,3,2,1,0
ADDRESS = 1010001	
RxUBDATA07-00	A read from this register will read 8 bits of user data from the Receiver User bit buffer pointed to by RxUBADDR7-0. This buffer can be written to when autobuffering of the user bits is enabled otherwise it is a read only buffer

Table 60. Transmitter User Bit Buffer Indirect Address Register

	TxUBADDR07-TxUBADDR00
	7,6,5,4,3,2,1,0
ADDRESS = 1010010	
TxUBADDR07-00	Indirect Address pointing to the address location in the Transmitter User Bit buffer

Table 61. Transmitter User Bit Buffer Data Register

	TxUBDATA07-TxUBDATA00
	7,6,5,4,3,2,1,0
ADDRESS = 1010011	
TxUBDATA07-00	A write to this register will write 8 bits of user data to the Transmit User bit buffer pointed to by TxUBADDR7-0. When User Bit autobuffering is enabled this buffer is disabled.

Table 62. Q Subcode CRC Error Status Register (Read Only)

	RES	RES	RES	RES	RES	RES	QCRCERROR	QSUB
	7	6	5	4	3	2	1	0
ADDRESS = 1010100								
QCRCERROR	This bit will be set if the CRC check of the Q Subcode fails. This bit will remain high but will not generate an interrupt. This bit will be cleared once the register is read.							
QSUB	This bit will be set if a Q subcode has been read into the Q subcode buffer							

Table 63. Q Subcode Buffe

ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x55	Address	Address	Address	Address	Control	Control	Control	Control
0x56	Track Number	Track Number	Track Number	Track Number	Track Number	Track Number	Track Number	Track Number
0x57	Index	Index	Index	Index	Index	Index	Index	Index
0x58	Minute	Minute	Minute	Minute	Minute	Minute	Minute	Minute
0x59	Second	Second	Second	Second	Second	Second	Second	Second
0x5A	Frame	Frame	Frame	Frame	Frame	Frame	Frame	Frame
0x5B	Zero	Zero	Zero	Zero	Zero	Zero	Zero	Zero
0x5C	Absolute Minute	Absolute Minute	Absolute Minute	Absolute Minute	Absolute Minute	Absolute Minute	Absolute Minute	Absolute Minute
0x5D	Absolute Second	Absolute Second	Absolute Second	Absolute Second	Absolute Second	Absolute Second	Absolute Second	Absolute Second
0x5E	Absolute Frame	Absolute Frame	Absolute Frame	Absolute Frame	Absolute Frame	Absolute Frame	Absolute Frame	Absolute Frame

Table 64. Datapath Control Register 1

	SRC1	SRC0	REC2	REC1	REC0	AUXO2	AUXO1	AUXO0
	7	6	5	4	3	2	1	0
ADDRESS = 1100010								
SRC1-0	Datapath Source Select for Sample Rate Converter(SRC) 00 = ADC 01 = DIR 10 = Playback 11 = Auxiliary In							
REC2-0	Datapath Source Select for Record Output Port 000 = ADC 001 = DIR 010 = Playback 011 = Auxiliary In 100 = SRC							
AUXO2-0	Datapath Source Select for Auxiliary Output Port 000 = ADC 001 = DIR 010 = Playback 011 = Auxiliary In 100 = SRC							

Table 65. Datapath Control Register 2

	RES	RES	DAC2	DAC1	DAC0	DIT2	DIT1	DIT0
	7	6	5	4	3	2	1	0
ADDRESS = 1100011								
DAC2-0	Datapath Source Select for DAC 000 = ADC 001 = DIR 010 = Playback 011 = Auxiliary In 100 = SRC							
DIT2-0	Datapath Source Select for DIT 000 = ADC 001 = DIR 010 = Playback 011 = Auxiliary In 100 = SRC							

Table 66. DAC Control Register 1

	DR_ALL	DR_DIG	CHSEL1	CHSEL0	POL1	POL0	MUTER	MUTEL
	7	6	5	4	3	2	1	0
ADDRESS = 1100100								

DR_ALL	Hard Reset and Powerdown
	0 = Normal, Output pins go to V_{REF} Level
	1 = Hard Reset & Low Power, Output pins go to AGND
DR_ALL	DAC Digital Reset
	0 = Normal
	1 = Reset All except registers
CHSEL1-0	DAC Channel Select
	00 = Normal Left-Right
	01 = Both Right
	10 = Both Left
	11 = Swapped, Right-Left
POL1-0	DAC Channel Polarity
	00 = Both Positive
	01 = Left Negative
	10 = Right Negative
	11 = Both Negative
MUTER	Mute Right Channel
	0 = Normal
	1 = Mute
MUTEL	Mute Left Channel
	0 = Normal
	1 = Mute

Table 67. DAC Control Register 2

	RES	RES	DMCLK1	DMCLK0	DFS	DFS0	DEEM1	DEEM0
	7	6	5	4	3	2	1	0
ADDRESS = 1100101								

DMCLK1-0	DAC MCLK Divider
	00 = MCLK
	01 = MCLK/1.5
	10 = MCLK/2
	11 = MCLK/3
DFS1-0	DAC Interpolator Select
	00 = 8 × (MCLK = 256 × f_S)
	01 = 4 × (MCLK = 128 × f_S)
	10 = 2 × (MCLK = 64 × f_S)
	11 = Reserved
DEEM1-0	DAC De-emphasis Select 00 = None
	01 = 44.1 kHz
	10 = 32 kHz
	11 = 48 kHz

Table 68. DAC Control Register 3

	RES	RES	RES	RES	RES	ZFVOL	ZFDATA	ZFPOL
	7	6	5	4	3	2	1	0
ADDRESS = 1100110								
ZFVOL	DAC Zero Flag on Mute and Zero Volume 0 = Enabled 1 = Disabled							
ZFDATA	DAC Zero Flag on Zero Data Disable 0 = Enabled 1 = Disabled							
ZFPOL	DAC Zero Flag Polarity 0 = Active High 1 = Active Low							

Table 69. DAC Control Register 4

	RES	INTRPT	ZEROSEL1	ZEROSEL0	RES	RES	RES	RES
	7	6	5	4	3	2	1	0
ADDRESS = 1100111								
INTRPT	This bit selects the functionality of the ZEROL/INT pin 0 = The pin functions as a ZEROL flag pin 1 = The pin functions as an interrupt pin							
ZEROSEL1-0	These bits control the functionality of the ZEROR pin when the ZEROL/INT pin is used as an interrupt 00 = The pin functions as a ZEROR flag pin 01 = The pin functions as a ZEROL flag pin 10 = The pin is asserted when either the Left or Right channel is zero 10 = The pin is asserted when both the Left and Right channels are zero							

Table 70. DAC Left Volume Register

	DVOLL7	DVOLL6	DVOLL5	DVOLL4	DVOLL3	DVOLL2	DVOLL1	DVOLL0
	7	6	5	4	3	2	1	0
ADDRESS = 1101000								
DVOLL7-0	DAC Left Channel Volume Control 1111111 = 0dBFS 1111110 = -0.375dBFS 0000000 = -95.625dBFS							

Table 71. DAC Right Volume Register

	DVOLR7	DVOLR6	DVOLR5	DVOLR4	DVOLR3	DVOLR2	DVOLR1	DVOLR0
	7	6	5	4	3	2	1	0
ADDRESS = 1101001								
DVOLL7-0	DAC Right Channel Volume Control 1111111 = 0dBFS 1111110 = -0.375dBFS 0000000 = -95.625dBFS							

Table 72. DAC Left Peak Volume Register

	RES	RES	DLP5	DLP4	DLP3	DLP2	DLP1	DLP0
	7	6	5	4	3	2	1	0
ADDRESS = 1101010								
DLP5-0	DAC Left Channel Peak Volume Detection 000000 = 0dBFS 000001 = -1dBFS 111111 = -63dBFS							

Table 73. DAC Right Peak Volume Register

	RES	RES	DRP5	DRP4	DRP3	DRP2	DRP1	DRP0
	7	6	5	4	3	2	1	0
ADDRESS = 1101011								
DRP5-0	DAC Right Channel Peak Volume Detection 000000 = 0dBFS 000001 = -1dBFS 111111 = -63dBFS							

Table 74. ADC Left Channel PGA Gain Register

	RES	RES	AGL5	AGL4	AGL3	AGL2	AGL1	AGL0
	7	6	5	4	3	2	1	0
ADDRESS = 1101100								
AGL5-0	PGA Left Channel Gain Control 000000 = 0 dB 000001 = +0.5 dB ..... 101111 = +23.5 dB 110000 = +24 dB ..... 111111 = +24 dB							

Table 75. ADC Right Channel PGA Gain Register

	RES	RES	AGR5	AGR4	AGR3	AGR2	AGR1	AGR0
	7	6	5	4	3	2	1	0
ADDRESS = 1101101								
AGR5-0	PGA Right Channel Gain Control 000000 = 0 dB 000001 = +0.5 dB ..... 101111 = +23.5 dB 110000 = +24 dB ..... 111111 = +24 dB							

Table 76. ADC Control Register 1

	AMC	HPF	PWRDWN	AND_PD	MUTER	MUTEL	PLPD	PRPD
	7	6	5	4	3	2	1	0
ADDRESS = 1101110								
AMC	ADC Modulator Clock							
	0 = ADC MCLK/2 (128 × f_S)							
	1 = ADC MCLK/4 (64 × f_S)							
HPF	High Pass Filter Enable							
	0 = Normal							
	1 = HPF Enabled							
PWRDWN	ADC Powerdown							
	0 = Normal							
	1 = Powerdown							
ANA_PD	ADC Analog Section Powedown							
	0 = Normal							
	1 = Powedown							
MUTER	Mute ADC Right Channel							
	0 = Normal							
	1 = Muted							
MUTEL	Mute ADC Left Channel							
	0 = Normal							
	1 = Muted							
PLPD	PGA Left Powerdown							
	0 = Normal							
	1 = Powerdown							
PRPD	PGA Right Powerdown							
	0 = Normal							
	1 = Powerdown							

Table 77. ADC Control Register 2

	RES	RES	RES	BUF_PD	RES	RES	MCD1	MCD0
	7	6	5	4	3	2	1	0
ADDRESS = 1101111								
BUF_PD	Reference Buffer Powerdown Control							
	0 = Normal							
	1 = Powerdown							
MCD1-0	ADC Master Clock Divider							
	00 = Divide by 1							
	01 = Divide by 2							
	10 = Divide by 3							
	11 = Divide by 1							

Table 78. ADC Left Volume Register

	AVOLL7	AVOLL6	AVOLL5	AVOLL4	AVOLL3	AVOLL2	AVOLL1	AVOLL0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADDRESS = 1110000								
AVOLL7-0	ADC Left Channel Volume Control							
	1111111 = 1.0 (0dBFS)							
	1111110 = 0.996 (-0.00348dBFS)							
	1000000 = 0.5 (-6dBFS)							
	0111111 = 0.496 (-6.09dBFS)							
	0000000 = 0.0039 (-48.18dBFS)							

Table 79. ADC Right Volume Register

	AVOLR7	AVOLR6	AVOLR5	AVOLR4	AVOLR3	AVOLR2	AVOLR1	AVOLR0
	7	6	5	4	3	2	1	0
ADDRESS = 1110001								
AVOLR7-0	ADC Right Channel Volume Control 1111111 = 1.0 (0dBFS) 1111110 = 0.996 (-0.00348dBFS) 1000000 = 0.5 (-6dBFS) 0111111 = 0.496 (-6.09dBFS) 0000000 = 0.0039 (-48.18dBFS)							

Table 80. ADC Left Peak Volume Register

	RES	RES	ALP5	ALP4	ALP3	ALP2	ALP1	ALP0
	7	6	5	4	3	2	1	0
ADDRESS = 1110010								
ALP5-0	ADC Left Channel Peak Volume Detection 000000 = 0dBFS 000001 = -1dBFS 111111 = -63dBFS							

Table 81. ADC Right Peak Volume Register

	RES	RES	ARP5	ARP4	ARP3	ARP2	ARP1	ARP0
	7	6	5	4	3	2	1	0
ADDRESS = 1110011								
ARP5-0	ADC Right Channel Peak Volume Detection 000000 = 0dBFS 000001 = -1dBFS 111111 = -63dBFS							

Table 82. PLL Control Register 1

	RES	RES	MCLKODIV	PLLDIV	PLL2PD	PLL1PD	XTLPD	SYSCLK3
	7	6	5	4	3	2	1	0
ADDRESS = 1110100								
MCLKODIV	Divide Input MCLK by 2 to generate MCLKO 0 = Disabled 1 = Enabled							
PLLDIV	Divide XIN by 2 to generate the PLL master clock 0 = Disabled 1 = Enabled							
PLL2PD	Powerdown PLL2 0 = Normal 1 = Powerdown							
PLL1PD	Powerdown PLL1 0 = Normal 1 = Powerdown							
XTLPD	Powerdown XTAL Oscillator 0 = Normal 1 = Powerdown							
SYSCLK3	Clock Output for SYSCLK3 0 = 512 × f_S 1 = 256 × f_S							

Table 83. PLL Control Register 2

	FS2-1	FS2-1	SEL2	DOUB2	FS1-1	FS1-0	SEL1	DOUB1
	7	6	5	4	3	2	1	0
ADDRESS = 1110101								
FS2_1-0	Sample Rate Select for PLL2 00 = 48 kHz 01 = Reserved 10 = 32 kHz 11 = 44.1 kHz							
SEL2	Oversample Ratio Select for PLL2 0 = 256 × f_S 1 = 384 × f_S							
DOUB2	Double Selected Sample Rate on PLL2 0 = Disabled 1 = Enabled							
FS1-0	Sample Rate Select for PLL1 00 = 48 kHz 01 = Reserved 10 = 32 kHz 11 = 44.1 kHz							
SEL1	Oversample Ratio Select for PLL1 0 = 256 × f_S 1 = 384 × f_S							
DOUB1	Double Selected Sample Rate on PLL1 0 = Disabled 1 = Enabled							

Table 84 .Internal Clocking Control Register 1

	DCLK2	DCLK1	DCLK0	ACLK2	ACLK1	ACLK0	ICLK2-1	ICLK2-0
	7	6	5	4	3	2	1	0
ADDRESS = 1110110								
DCLK2-0	DAC Clock Source Select 000 = XIN 001 = MCLKI 010 = PLLINT1 011 = PLLINT2 100 = DIR PLL (512 × f_s) 101 = DIR PLL (256 × f_s) 110 = XIN 111 = XIN							
ACLK2-0	ADC Clock Source Select 000 = XIN 001 = MCLKI 010 = PLLINT1 011 = PLLINT2 100 = DIR PLL (512 × f_s) 101 = DIR PLL (256 × f_s) 110 = XIN 111 = XIN							
ICLK2	Source Selector for Internal Clock ICLK2 00 = XIN 01 = MCLKI 10 = PLLINT1 11 = PLLINT2							

Table 85. Internal Clocking Control Register 2

	RES	RES	RES	ICLK1-1	ICLK1-0	PLL2INT1	PLL2INT0	PLL1INT
	7	6	5	4	3	2	1	0
ADDRESS = 1110111								
Iclk1-0	Source Selector for Internal Clock ICLK1							
	00 = XIN							
	01 = MCLKI							
	10 = PLLINT1							
	11 = PLLINT2							
PLL2INT1-0	PLL2 Internal Selector (See Figure 18)							
	00 = FS2							
	01 = FS2/2							
	10 = FS3							
	11 = FS3/2							
PLL1INT	PLL1 Internal Selector							
	0 = FS1							
	1 = FS1/2							

Table 86. PLL Clock Source Register

	PLL1_Source	PLL2_Source	RES	RES	RES	RES	RES	RES
	7	6	5	4	3	2	1	0
ADDRESS = 1111000								
PLL1_Source	Selects the clock source for PLL1							
	0 = XIN							
	1 = MCLKI							
PLL2_Source	Selects the clock source for PLL2							
	0 = XIN							
	1 = MCLKI							

Table 87. PLL Output Enable Register

	RES	RES	RES	DIRIN_PIN	RES	SYSCLK1	SYSCLK2	SYSCLK3
	7	6	5	4	3	2	1	0
ADDRESS = 1111010								
DIRIN_PIN	This bit determines the input levels of the DIRIN pin							
	0 = The DIRIN will accept input signals down to 200mV according to AES3 requirements							
	1 = The DIRIN will accept input signals as defined in Table 13							
SYSCLK1	Enables the SYSCLK1 Output							
	0 = Enabled							
	1 = Disabled							
SYSCLK2	Enables the SYSCLK2 Output							
	0 = Enabled							
	1 = Disabled							
SYSCLK3	Enables the SYSCLK3 Output							
	0 = Enabled							
	1 = Disabled							

Table 88. ALC Control Register 1

	FSSEL1-0	GAINCNTR1-0	RECMODE1-0	LIMDET	ALCEN
	7,6	5,4	3,2	1	0
ADDRESS = 1111011		**Default = 0x00**			
FSSEL1-0	These bits should equal the sample rate of the ADC				
	00 = 96 kHz				
	01 = 48 kHz				
	10 = 32 kHz				
	11 = Reserved				
GAINCNTR1-0	These bits determine the limit of the counter used in Limited Recovery Mode				
	00 = 3				
	01 = 7				
	10 = 15				
	11 = 31				
RECMODE1-0	These bits determine which recovery mode is used by the ALC section				
	00 = No Recovery				
	01 = Normal Recovery				
	10 = Limited Recovery				
	11 = Reserved				
LIMDET	Limit Detect Mode				
	0 = ALC is used when either channel exceeds the set limit				
	1 = ALC is used only when both channels exceed the set limit				
ALCEN	ALC Enable				
	0 = Disable ALC				
	1 = Enable ALC				

Table 89. ALC Control Register 2

	RES	RECTH1-0	ATKTH1-0	RECTIME1-0 ATKTIME	
	7	6,5	4,3	2,1	0
ADDRESS = 1111100		**Default = 0x52**			
RECTH1-0	Recovery Threshold				
	00 = -2 dB				
	01 = -3 dB				
	10 = -4 dB				
	11 = -6 dB				
ATKTH1-0	Attack Theshold				
	00 = 0 dB				
	01 = -1 dB				
	10 = -2 dB				
	11 = -4 dB				
RECTIME1-0	Recovery Time Selection				
	00 = 32 ms				
	01 = 64 ms				
	10 = 128 ms				
	11 = 256 ms				
ATKTIME	Attack Timer Selection				
	0 = 1 ms				
	1 = 4 ms				

Table 90. ALC Control Register 3

	ALC RESET
	7,6,5,4,3,2,1,0
ADDRESS = 1111101	**Default = 0x00**
ALC RESET	A write to this register will restart the ALC operation. The value written to this register is irrelevant. A read from this register will give the gain reduction factor.

OUTLINE DIMENSIONS

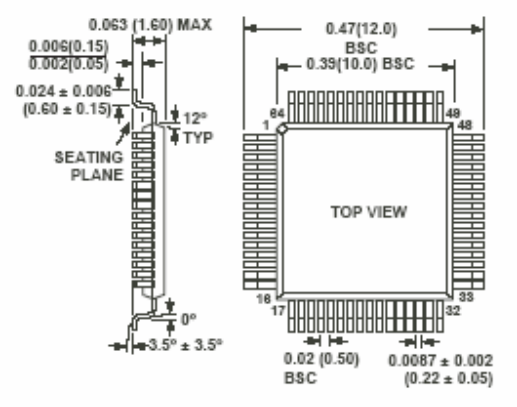

Figure 40. 64-Lead Plastic Quad Flatpack [LQFP]
(ST-64)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Control Interface	DAC Outputs	Package Options
ADAV804AST	–40°C to +85°C	I^2C	Differential	ST-64

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