MOTOROLA

MC33077

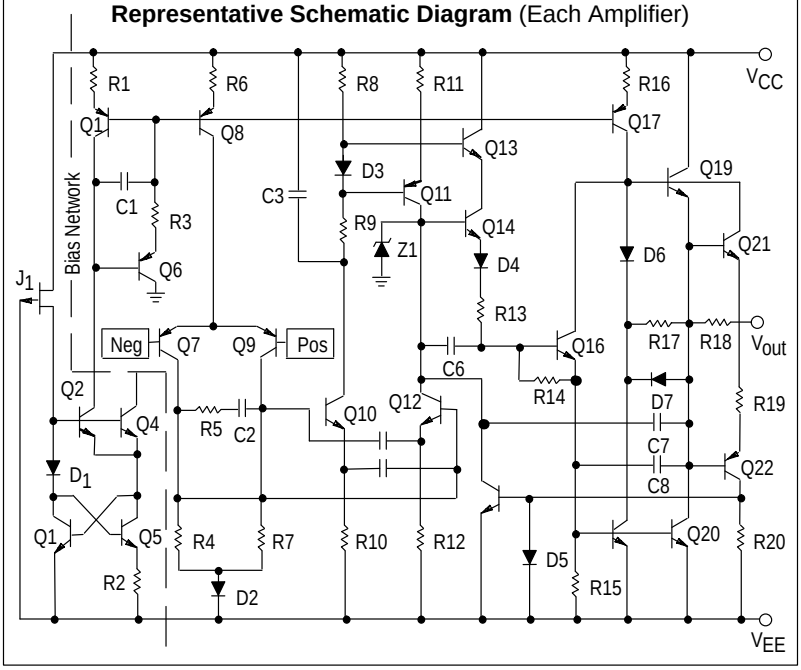
Dual, Low Noise Operational Amplifier

The MC33077 is a precision high quality, high frequency, low noise monolithic dual operational amplifier employing innovative bipolar design techniques. Precision matching coupled with a unique analog resistor trim technique is used to obtain low input offset voltages. Dual–doublet frequency compensation techniques are used to enhance the gain bandwidth product of the amplifier. In addition, the MC33077 offers low input noise voltage, low temperature coefficient of input offset voltage, high slew rate, high AC and DC open loop voltage gain and low supply current drain. The all NPN transistor output stage exhibits no deadband cross–over distortion, large output voltage swing, excellent phase and gain margins, low open loop output impedance and symmetrical source and sink AC frequency performance.

The MC33077 is tested over the automotive temperature range and is available in plastic DIP and SO–8 packages (P and D suffixes).

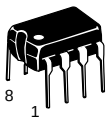
- Low Voltage Noise: 4.4 nV/$\sqrt{Hz}$ @ 1.0 kHz
- Low Input Offset Voltage: 0.2 mV
- Low TC of Input Offset Voltage: 2.0 μV/°C
- High Gain Bandwidth Product: 37 MHz @ 100 kHz
- High AC Voltage Gain: 370 @ 100 kHz
  1850 @ 20 kHz
- Unity Gain Stable: with Capacitance Loads to 500 pF
- High Slew Rate: 11 V/μs
- Low Total Harmonic Distortion: 0.007%
- Large Output Voltage Swing: +14 V to –14.7 V
- High DC Open Loop Voltage Gain: 400 k (112 dB)
- High Common Mode Rejection: 107 dB
- Low Power Supply Drain Current: 3.5 mA
- Dual Supply Operation: ±2.5 V to ±18 V

Representative Schematic Diagram (Each Amplifier)



DUAL, LOW NOISE OPERATIONAL AMPLIFIER

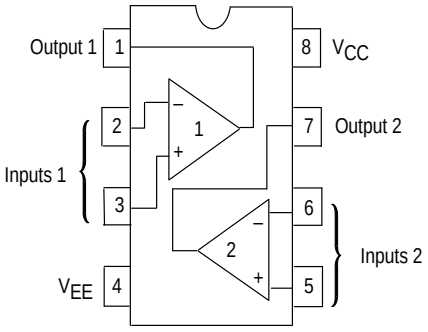
SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33077D	T_A = – 40° to +85°C	SO–8
MC33077P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	–60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE} (See Applications Information).
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (See power dissipation performance characteristic, Figure 1).

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = –40° to +85°C	$\|V_{IO}\|$	 — —	 0.13 —	 1.0 1.5	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = –40° to +85°C	$\Delta V_{IO}/\Delta T$	—	2.0	—	μV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = –40° to +85°C	I_{IB}	 — —	 280 —	 1000 1200	nA
Input Offset Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = –40° to +85°C	I_{IO}	 — —	 15 —	 180 240	nA
Common Mode Input Voltage Range (ΔV_{IO} ,= 5.0 mV, V_O = 0 V)	V_{ICR}	±13.5	±14	—	V
Large Signal Voltage Gain (V_O = ±1.0 V, R_L = 2.0 kΩ) T_A = +25°C T_A = –40° to +85°C	A_{VOL}	 150 k 125 k	 400 k —	 — —	V/V
Output Voltage Swing (V_{ID} = ±1.0 V) R_L = 2.0 kΩ R_L = 2.0 kΩ R_L = 10 kΩ R_L = 10 kΩ	 V_{O+} V_{O-} V_{O+} V_{O-}	 +13.0 — +13.4 —	 +13.6 –14.1 +14.0 –14.7	 — –13.5 — –14.3	V
Common Mode Rejection (V_{in} = ±13 V)	CMR	85	107	—	dB
Power Supply Rejection (Note 3) V_{CC}/V_{EE} = +15 V/ –15 V to +5.0 V/ –5.0 V	PSR	80	90	—	dB
Output Short Circuit Current (V_{ID} = ±1.0 V, Output to Ground) Source Sink	I_{SC}	 +10 –20	 +26 –33	 +60 +60	mA
Power Supply Current (V_O = 0 V, All Amplifiers) T_A = +25°C T_A = –40° to +85°C	I_D	 — —	 3.5 —	 4.5 4.8	mA

NOTE: 3. Measured with V_{CC} and V_{EE} simultaneously varied.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = –10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0)	SR	8.0	11	—	V/μs
Gain Bandwidth Product (f = 100 kHz)	GBW	25	37	—	MHz
AC Voltage Gain (R_L = 2.0 kΩ, V_O = 0 V) f = 100 kHz f = 20 kHz	A_{VO}	 — —	 370 1850	 — —	V/V
Unity Gain Frequency (Open Loop)	f_U	—	7.5	—	MHz
Gain Margin (R_L = 2.0 kΩ, C_L = 10 pF)	A_m	—	10	—	dB
Phase Margin (R_L = 2.0 kΩ, C_L = 10 pF)	$\varnothing_m$	—	55	—	Degrees
Channel Separation (f = 20 Hz to 20 kHz, R_L = 2.0 kΩ, V_O = 10 V_{pp})	CS	—	–120	—	dB
Power Bandwidth (V_O = 27$_{p-p}$, R_L = 2.0 kΩ, THD ≤ 1%)	BW_p	—	200	—	kHz
Distortion (R_L = 2.0 kΩ) A_V = +1.0, f = 20 Hz to 20 kHz V_O = 3.0 V_{rms} A_V = 2000, f = 20 kHz V_O = 2.0 V_{pp} V_O = 10 V_{pp} A_V = 4000, f = 100 kHz V_O = 2.0 V_{pp} V_O = 10 V_{pp}	THD	 — — — — —	 0.007 0.215 0.242 0.3.19 0.316	 — — — — —	%
Open Loop Output Impedance (V_O = 0 V, f = f_U)	$\|Z_O\|$	—	36	—	Ω
Differential Input Resistance (V_{CM} = 0 V)	R_{in}	—	270	—	kΩ
Differential Input Capacitance (V_{CM} = 0 V)	C_{in}	—	15	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω) f = 10 Hz f = 1.0 kHz	e_n	 — —	 6.7 4.4	 — —	nV/√Hz
Equivalent Input Noise Current (f = 1.0 kHz) f = 10 Hz f = 1.0 kHz	i_n	 — —	 1.3 0.6	 — —	pA/√Hz

Figure 1. Maximum Power Dissipation versus Temperature

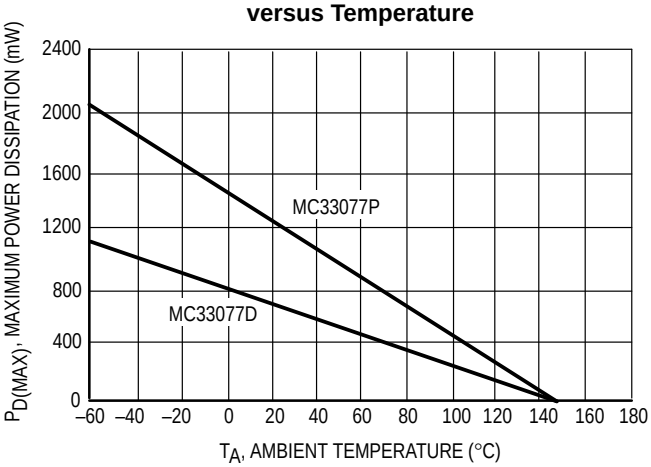


Figure 2. Input Bias Current versus Supply Voltage

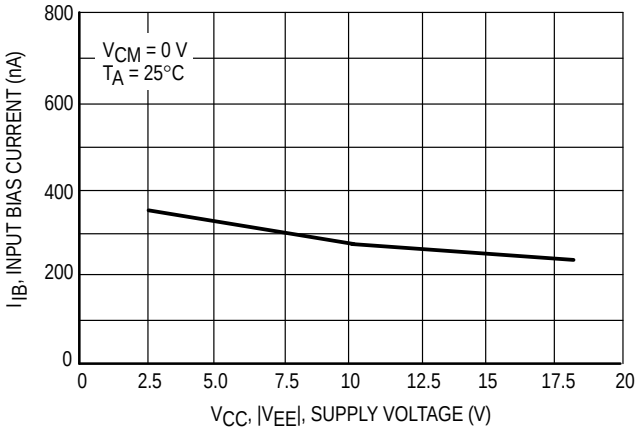


Figure 3. Input Bias Current versus Temperature

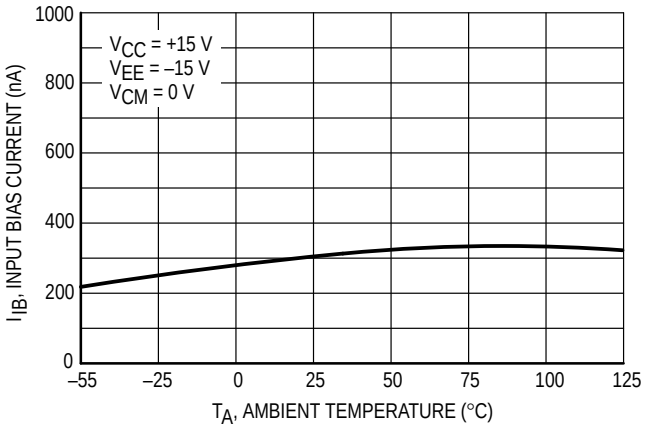


Figure 4. Input Offset Voltage versus Temperature

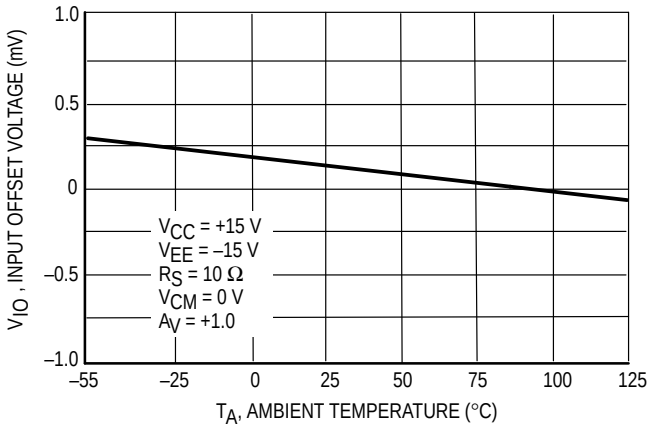


Figure 5. Input Bias Current versus Common Mode Voltage

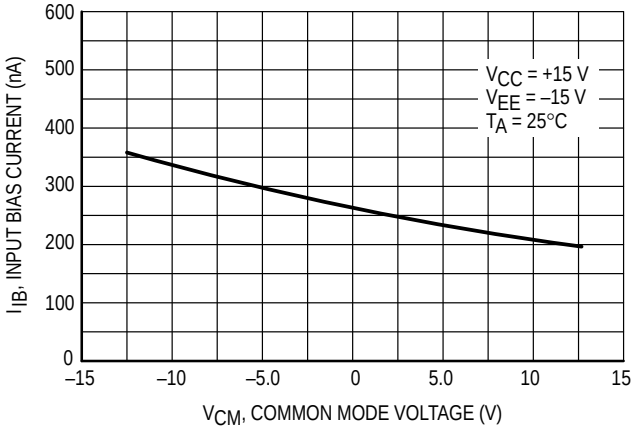


Figure 6. Input Common Mode Voltage Range versus Temperature

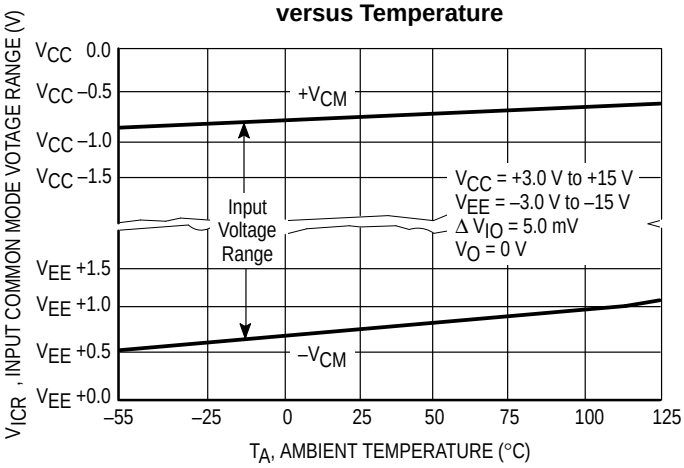


Figure 7. Output Saturation Voltage versus Load Resistance to Ground

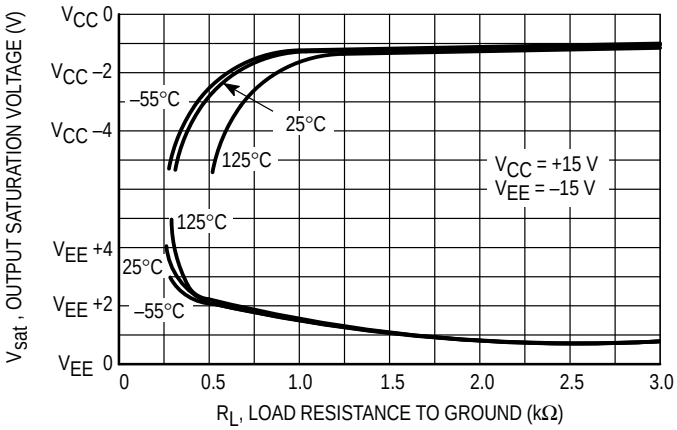


Figure 8. Output Short Circuit Current versus Temperature

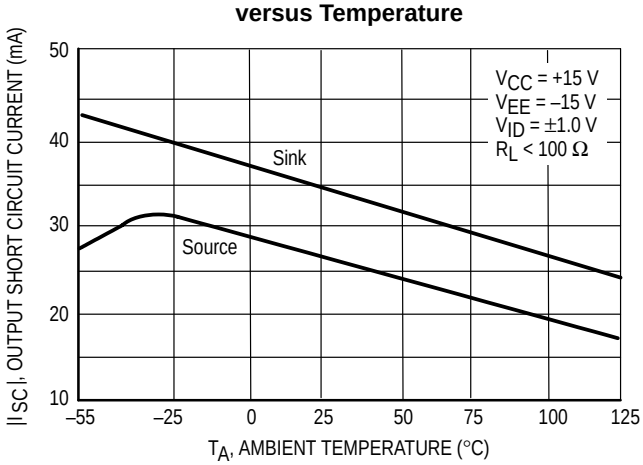


Figure 9. Supply Current versus Temperature

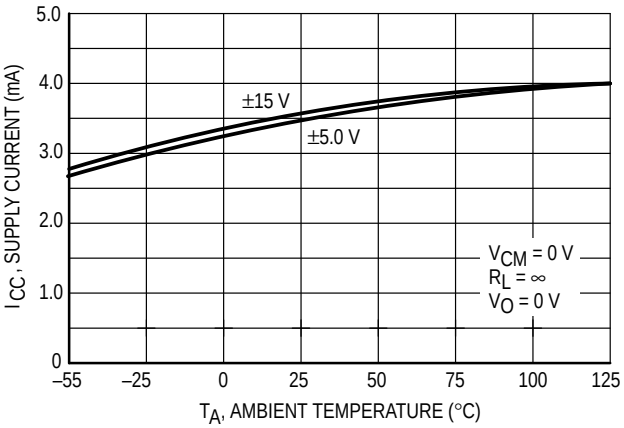


Figure 10. Common Mode Rejection versus Frequency

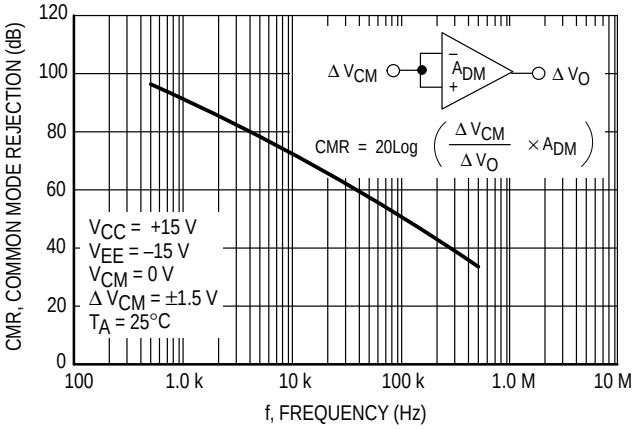


Figure 11. Power Supply Rejection versus Frequency

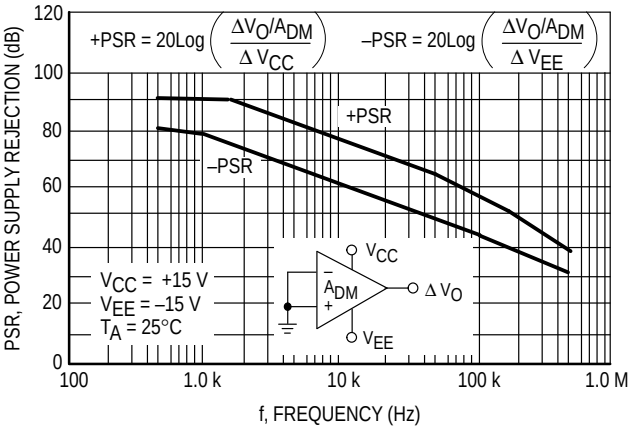


Figure 12. Gain Bandwidth Product versus Supply Voltage

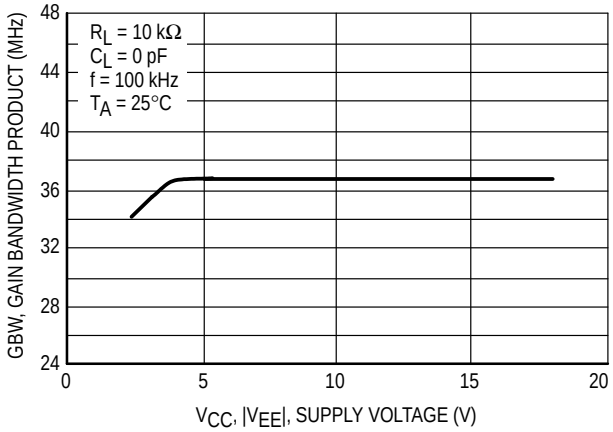


Figure 13. Gain Bandwidth Product versus Temperature

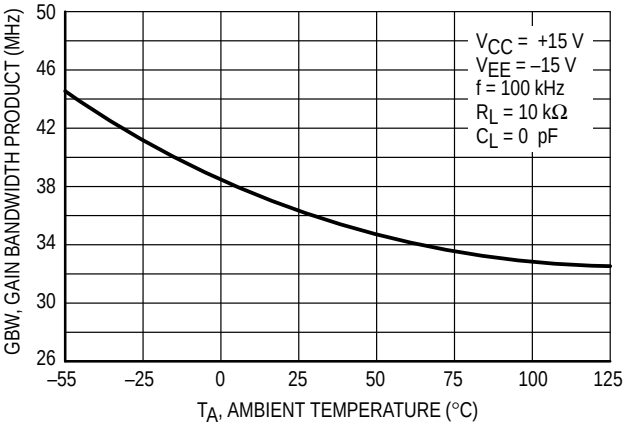


Figure 14. Maximum Output Voltage versus Supply Voltage

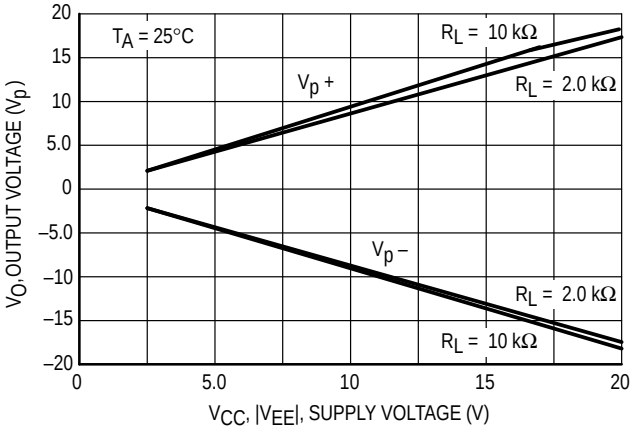


Figure 15. Output Voltage versus Frequency

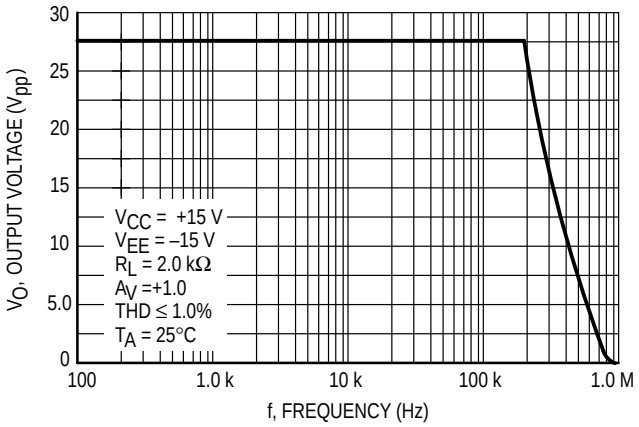


Figure 16. Open Loop Voltage Gain versus Supply Voltage

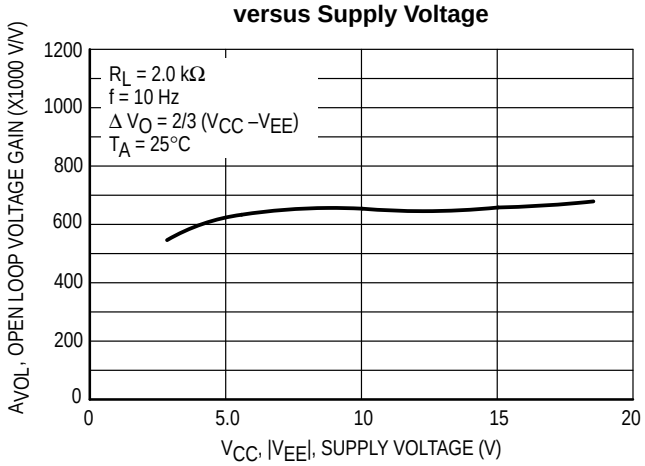


Figure 17. Open Loop Voltage Gain versus Temperature

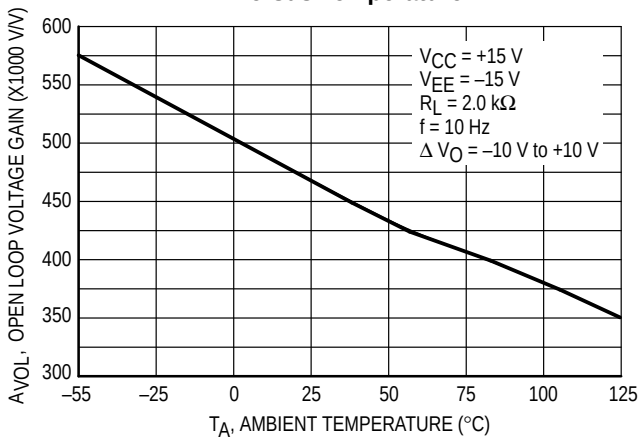


Figure 18. Output Impedance versus Frequency

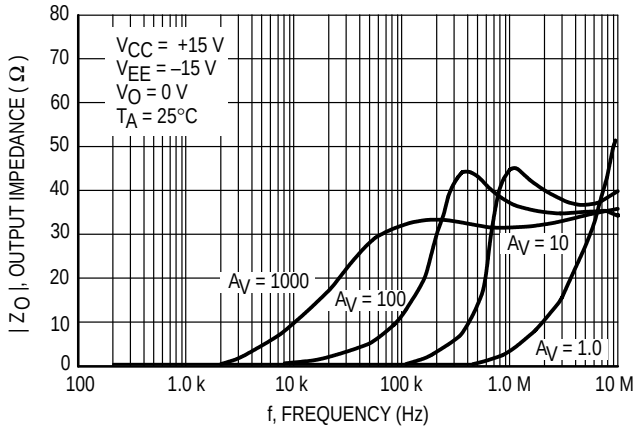


Figure 19. Channel Separation versus Frequency

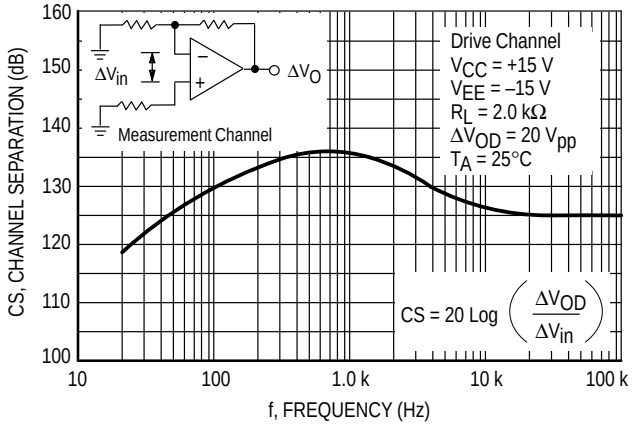


Figure 20. Total Harmonic Distortion versus Frequency

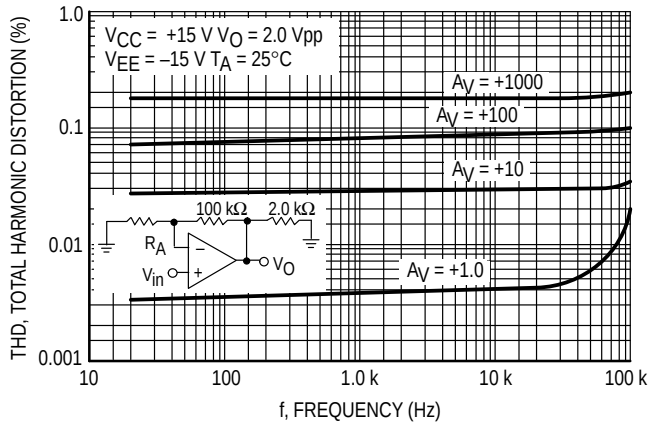


Figure 21. Total Harmonic Distortion versus Frequency

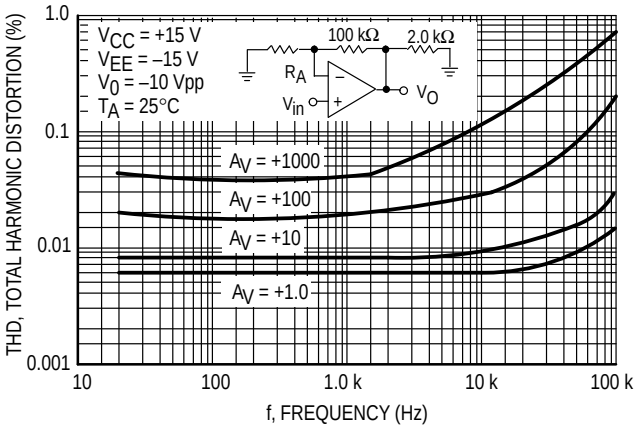


Figure 22. Total Harmonic Distortion versus Output Voltage

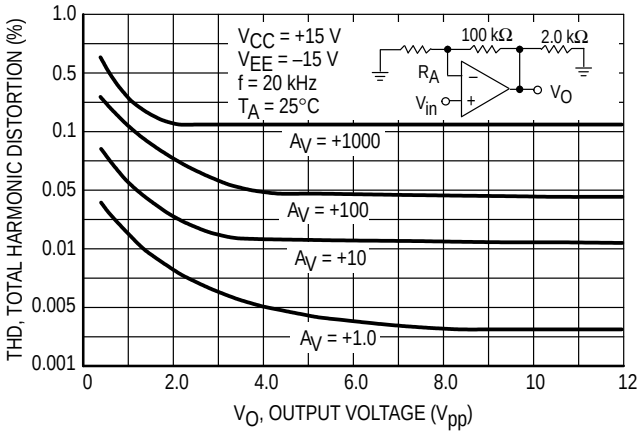


Figure 23. Slew Rate versus Supply Voltage

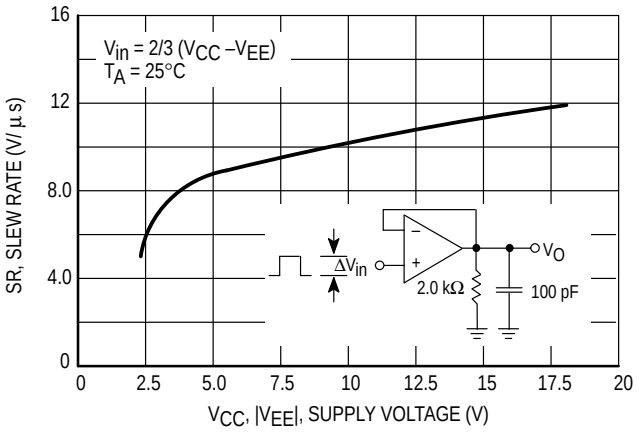


Figure 24. Slew Rate versus Temperature

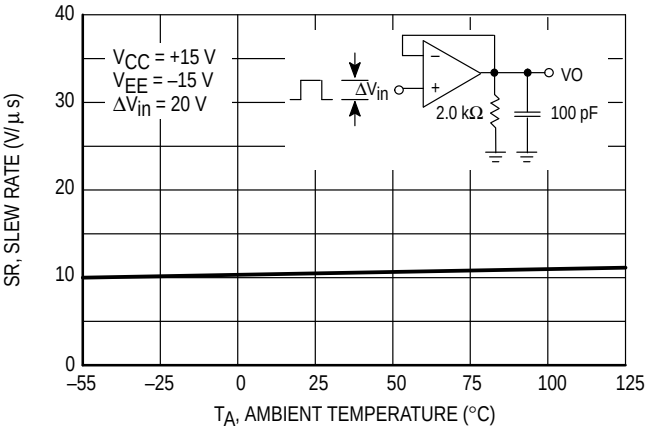


Figure 25. Voltage Gain and Phase versus Frequency

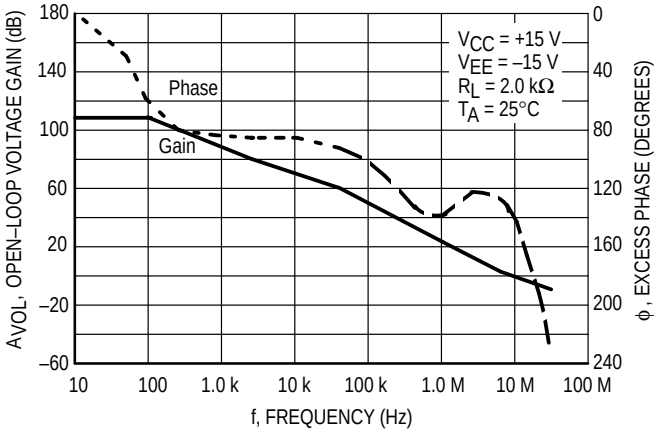


Figure 26. Open Loop Gain Margin and Phase Margin versus Output Load Capacitance

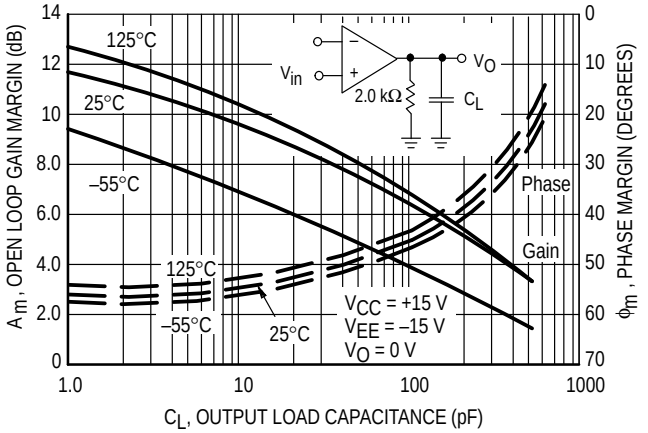


Figure 27. Phase Margin versus Output Voltage

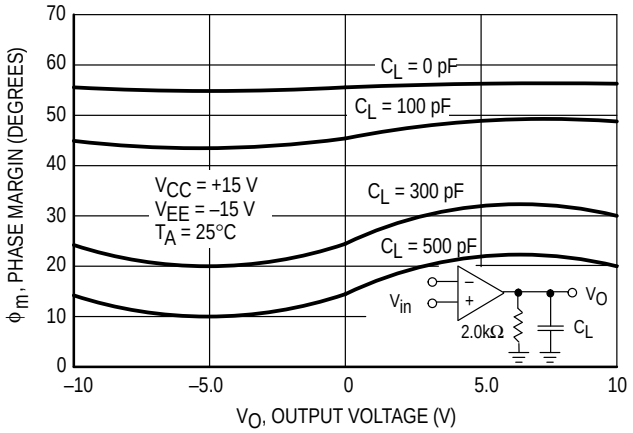


Figure 28. Overshoot versus Output Load Capacitance

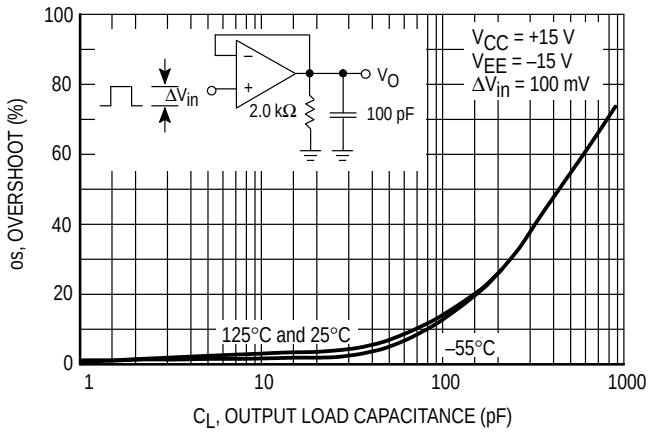


Figure 29. Input Referred Noise Voltage and Current versus Frequency

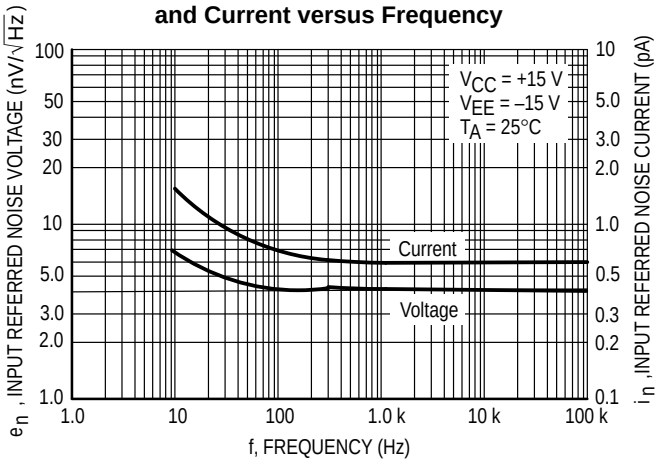


Figure 30. Total Input Referred Noise Voltage versus Source Resistant

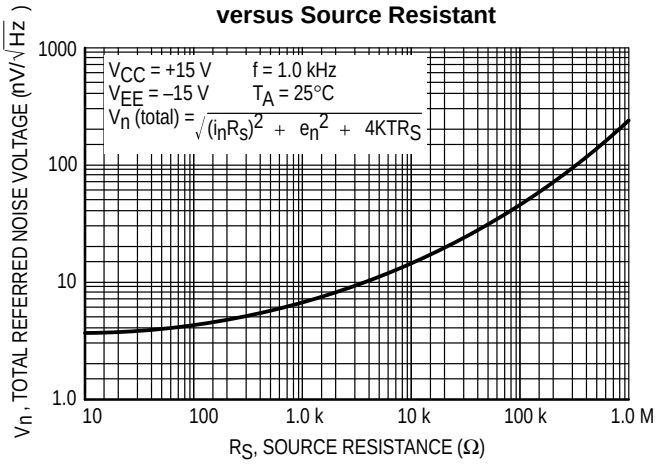


Figure 31. Phase Margin and Gain Margin versus Differential Source Resistance

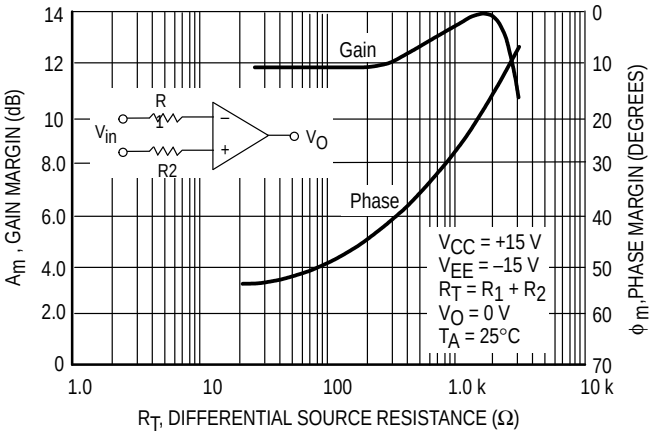


Figure 32. Inverting Amplifer Slew Rate

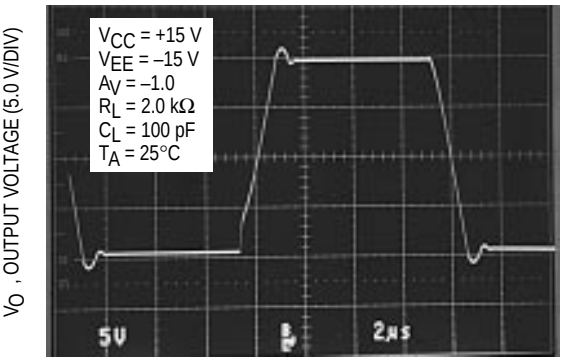


Figure 33. Noninverting Amplifier Slew Rate

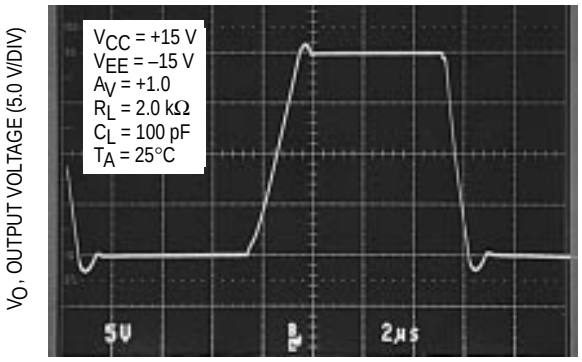


Figure 34. Noninverting Amplifier Overshoot

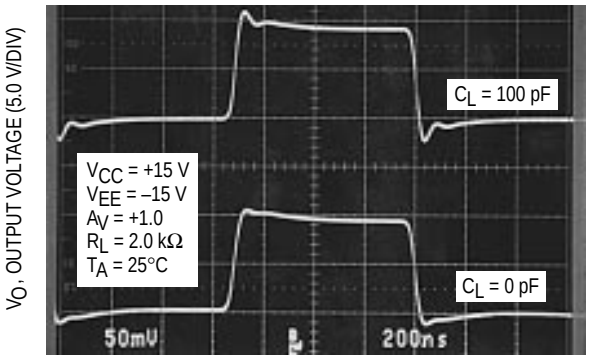
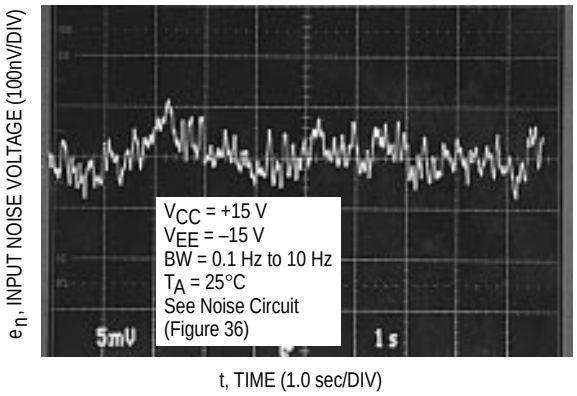


Figure 35. Low Frequency Noise Voltage versus Time



APPLICATIONS INFORMATION

The MC33077 is designed primarily for its low noise, low offset voltage, high gain bandwidth product and large output swing characteristics. Its outstanding high frequency gain/phase performance make it a very attractive amplifier for high quality preamps, instrumentation amps, active filters and other applications requiring precision quality characteristics.

The MC33077 utilizes high frequency lateral PNP input transistors in a low noise bipolar differential stage driving a compensated Miller integration amplifier. Dual–doublet frequency compensation techniques are used to enhance the gain bandwidth product. The output stage uses an all NPN transistor design which provides greater output voltage swing and improved frequency performance over more conventional stages by using both PNP and NPN transistors (Class AB). This combination produces an amplifier with superior characteristics.

Through precision component matching and innovative current mirror design, a lower than normal temperature coefficient of input offset voltage (2.0 μV/°C as opposed to 10 μV/°C), as well as low input offset voltage, is accomplished.

The minimum common mode input range is from 1.5 V below the positive rail (V_{CC}) to 1.5 V above the negative rail (V_{EE}). The inputs will typically common mode to within 1.0 V of both negative and positive rails though degradation in offset voltage and gain will be experienced as the common mode voltage nears either supply rail. In practice, though not recommended, the input voltage may exceed V_{CC} by approximately 30 V and decrease below the V_{EE} by approximately 0.6 V without causing permanent damage to the device. If the input voltage on either or both inputs is less than approximately 0.6 V, excessive current may flow, if not limited, causing permanent damage to the device.

The amplifier will not latch with input source currents up to 20 mA, though in practice, source currents should be limited to 5.0 mA to avoid any parametric damage to the device. If both inputs exceed V_{CC}, the output will be in the high state and phase reversal may occur. No phase reversal will occur if the voltage on one input is within the common mode range and the voltage on the other input exceeds V_{CC}. Phase reversal may occur if the input voltage on either or both inputs is less than 1.0 V above the negative rail. Phase reversal will be experienced if the voltage on either or both inputs is less than V_{EE}.

Through the use of dual–doublet frequency compensation techniques, the gain bandwidth product has been greatly enhanced over other amplifiers using the conventional single pole compensation. The phase and gain error of the amplifier remains low to higher frequencies for fixed amplifier gain configurations.

With the all NPN output stage, there is minimal swing loss to the supply rails, producing superior output swing, no crossover distortion and improved output phase symmetry with output voltage excursions (output phase symmetry being the amplifiers ability to maintain a constant phase relation independent of its output voltage swing). Output phase symmetry degradation in the more conventional PNP and NPN transistor output stage was primarily due to the inherent cut–off frequency mismatch of the PNP and NPN transistors used (typically 10 MHz and 300 MHz, respectively), causing considerable phase change to occur as the output voltage changes. By eliminating the PNP in the output, such phase change has been avoided and a very significant improvement in output phase symmetry as well as output swing has been accomplished.

The output swing improvement is most noticeable when operation is with lower supply voltages (typically 30% with ± 5.0 V supplies). With a 10 k load, the output of the amplifier can typically swing to within 1.0 V of the positive rail (V_{CC}), and to within 0.3 V of the negative rail (V_{EE}), producing a 28.7 V_{pp} signal from ±15 V supplies. Output voltage swing can be further improved by using an output pull–up resistor referenced to the V_{CC}. Where output signals are referenced to the positive supply rail, the pull–up resistor will pull the output to V_{CC} during the positive swing, and during the negative swing, the NPN output transistor collector will pull the output very near V_{EE}. This configuration will produce the maximum attainable output signal from given supply voltages. The value of load resistance used should be much less than any feedback resistance to avoid excess loading and allow easy pull–up of the output.

Output impedance of the amplifier is typically less than 50 Ω at frequencies less than the unity gain crossover frequency (see Figure 18). The amplifier is unity gain stable with output capacitance loads up to 500 pF at full output swing over the –55° to +125°C temperature range. Output phase symmetry is excellent with typically 4°C total phase change over a 20 V output excursion at 25°C with a 2.0 kΩ and 100 pF load. With a 2.0 kΩ resistive load and no capacitance loading, the total phase change is approximately one degree for the same 20 V output excursion. With a 2.0 kΩ and 500 pF load at 125°C, the total phase change is typically only 10°C for a 20 V output excursion (see Figure 27).

As with all amplifiers, care should be exercised to insure that one does not create a pole at the input of the amplifier which is near the closed loop corner frequency. This becomes a greater concern when using high frequency amplifiers since it is very easy to create such a pole with relatively small values of resistance on the inputs. If this does

occur, the amplifier's phase will degrade severely causing the amplifier to become unstable. Effective source resistances, acting in conjunction with the input capacitance of the amplifier, should be kept to a minimum to avoid creating such a pole at the input (see Figure 31). There is minimal effect on stability where the created input pole is much greater than the closed loop corner frequency. Where amplifier stability is affected as a result of a negative feedback resistor in conjunction with the amplifier's input capacitance, creating a pole near the closed loop corner frequency, lead capacitor compensation techniques (lead capacitor in parallel with the feedback resistor) can be employed to improve stability. The feedback resistor and lead capacitor RC time constant should be larger than that of the uncompensated input pole frequency. Having a high resistance connected to the noninverting input of the amplifier can create a like instability problem. Compensation for this condition can be accomplished by adding a lead capacitor in parallel with the noninverting input resistor of such a value as to make the RC time constant larger than the RC time constant of the uncompensated input resistor acting in conjunction with the amplifiers input capacitance.

For optimum frequency performance and stability, careful component placement and printed circuit board layout should be exercised. For example, long unshielded input or output leads may result in unwanted input output coupling. In order to reduce the input capacitance, the body of resistors connected to the input pins should be physically close to the input pins. This not only minimizes the input pole creation for optimum frequency response, but also minimizes extraneous signal "pickup" at this node. Power supplies should be decoupled with adequate capacitance as close as possible to the device supply pin.

In addition to amplifier stability considerations, input source resistance values should be low to take full advantage of the low noise characteristics of the amplifier. Thermal noise (Johnson Noise) of a resistor is generated by thermally–charged carriers randomly moving within the resistor creating a voltage. The rms thermal noise voltage in a resistor can be calculated from:

$$E_{nr} = \sqrt{4k\,TR \times BW}$$

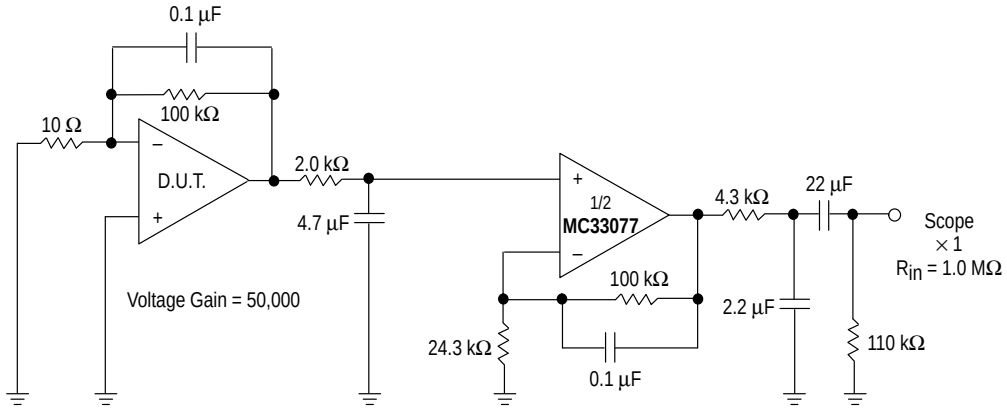
where:

k = Boltzmann's Constant (1.38×10^{-23} joules/k)
T = Kelvin temperature
R = Resistance in ohms
BW = Upper and lower frequency limit in Hertz.

By way of reference, a 1.0 kΩ resistor at 25°C will produce a 4.0 $nV/\sqrt{Hz}$ of rms noise voltage. If this resistor is connected to the input of the amplifier, the noise voltage will be gained–up in accordance to the amplifier's gain configuration. For this reason, the selection of input source resistance for low noise circuit applications warrants serious consideration. The total noise of the amplifier, as referred to its inputs, is typically only 4.4 $nV/\sqrt{Hz}$ at 1.0 kHz.

The output of any one amplifier is current limited and thus protected from a direct short to ground, However, under such conditions, it is important not to allow the amplifier to exceed the maximum junction temperature rating. Typically for ±15 V supplies, any one output can be shorted continuously to ground without exceeding the temperature rating.

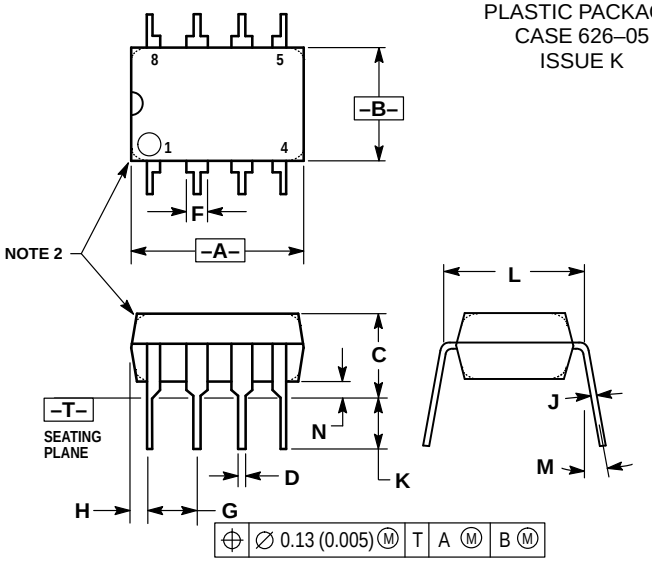
Figure 36. Voltage Noise Test Circuit (0.1 Hz to 10 Hz_{p-p})



Note: All capacitors are non–polarized.

OUTLINE DIMENSIONS

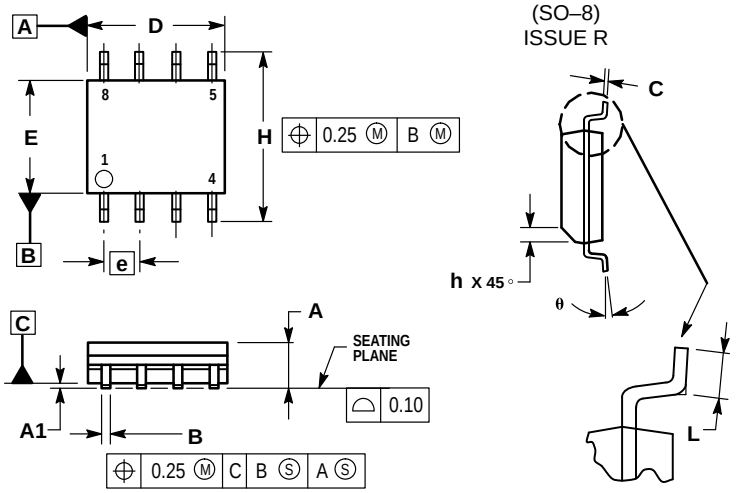
P SUFFIX
PLASTIC PACKAGE
CASE 626–05
ISSUE K



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

D SUFFIX
PLASTIC PACKAGE
CASE 751–05
(SO–8)
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

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