AN130
Configuring the PDSP16256
Application Note

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1. INTRODUCTION

The PDSP16256 is a digital finite impulse response (FIR) filter capable of providing between 16 and 128 digital filtering stages at sampling rates from 3.125MHz for a 128 stage filter up to 25MHz for 16 stages. The device contains 16 multiplier-accumulator circuits which are multi-cycled to produce filters of greater than 16 stages. Input data and coefficents are both represented by 16 bit two's complement numbers with coefficients converted internally to 12 bits.

The PDSP16256 is designed such that devices may be easily cascaded. This allows filter lengths to be increased above the nominal 128 stages offered by a single device. Cascading may also be used to raise the filter sampling rate in those cases where a single device is unable to offer the required performance. For example, a single PDSP16256, when configured as a 64 stage filter, offers a maximum sampling rate of 6.25MHz. Using two devices in cascade, each configured as a 32 stage filter, offers a sampling rate of 12.5MHz. Expansion buses ensure that no loss of accuracy occurs when devices are connected in this configuration. If a system contains a number of PDSP16256 devices which each comprise separate unrelated filters, the inherent cascading features of the device may still be used in order to allow all of the devices to be configured from a single EPROM, thereby simplifying the system design.

The PDSP16256 contains a single 16 bit control register which determines the mode and speed of operation, along with other control functions. The filter coefficients are 12 bits wide, with one coefficient being required for each stage of the filter.

The data presented to the 16 bit coefficient input bus is automatically rounded to yield a 12 bit coefficient during device configuration. The rounding scheme employed is described in detail in the PDSP16256 data sheet.

For filters with 64 (single filter mode only), 32 and 16 stages the PDSP16256 offers the coefficient bank swap feature. If enabled, bank swapping allows one set of coefficients to be replaced by an alternative set without the need to load these from an external source.

Before filtering operations may commence, it is necessary to load the device with both the filter coefficients and the control register word. This may be accomplished in one of two ways;

- by loading the data from a local memory device (e.g. EPROM)
- via a system data bus under the control of an intelligent master device (e.g. a microprocessor)

The former has the advantage of providing a stand-alone system which is able to load the required data on system boot-up whilst using the minimum number of external components. The latter allows much greater flexibility in the types of filtering systems which may be implemented. Remote master mode could be used, for example, to implement an adaptive filtering system in which the filter coefficients are changed, depending on prevailing conditions, thus maximizing the performance of the filter at all times.

This application brief gives detailed information which will allow users to determine how to interface to the PDSP16256 in order to load coefficient and control information. This brief covers the use of the device in both automatic EPROM load and remote master modes. Information on cascading devices in both modes is also included.

2. TIMING

The PDSP16256 uses registers on all inputs and outputs to ensure that signals are synchronous with the system clock. This scheme ensures that all setup and hold times for incoming signals are the same. Similarly, all clock to data valid delays for output signals are also identical.

The PDSP16256 datasheet in this handbook lists these delays for the PDSP16256 as :

Parameter	Min	Max
Input signal setup	8	-
Input signal hold	4	-
SCLK to output valid	5	26

(All times in nanoseconds)

There is an exception to this rule; the output circuitry. Here, the delay from activating the output enable to the data being available on the pins is not the same as the value given above for other output signals. Similarly, the delays in changing from a high- to a low-impedance output state, and vice-versa, are also different. The values of these delays may be found by referring to the DSP IC Handbook.

3. AUTOMATIC EPROM LOAD MODE

The PDSP16256 generates all the required signals to interface directly to an EPROM and load the required data automatically without the need for external glue logic in this mode. Tying the EPROM input to ground selects this mode of operation. It is assumed that all data loaded consists of 8 bit bytes. The data load sequence is initiated by the RESET input to the PDSP16256. RESET, which is active low, should be held low for 16 cycles of the system clock, SCLK. After the sixth SCLK cycle, the BUSY signal will go high, signalling to other devices in the system that the PDSP16256 is performing a data load function. All output data is invalid while the BUSY signal is active. BUSY returns to its inactive state once all the required coefficient and control register data has been loaded.

The address bus used to access the EPROM is 8 bits wide. This allows a maximum of 256 data bytes to be read. For a digital filter containing the maximum 128 stages, 256 bytes will be required to store the coefficients as each one requires two bytes of storage. The byte held in the lower address of each byte-pair should be the least significant byte. If a smaller filter is to be implemented, 32 taps for example, then some of the address lines are redundant and will remain low at all times. These redundant address lines should not be connected to the EPROM when a number of PDSP16256 devices are to be cascaded. A further two bytes are required to store the 16 bit control register word. The control word always resides above the filter coefficients in the EPROM memory map.

The coefficient control pin, CCS, is used to determine whether the control register or filter coefficients are to be loaded. When CCS is high, the control register is loaded and when low, the filter coefficients are loaded. CCS is effectively used as the most significant address line in addition to the address bus A7:0. Hence, when CCS is high, the EPROM address that will be referenced is 256+A7:0, assuming that all eight address lines are in use. In order to load the control register, A7:0 takes the values 0 and 1 whilst CCS is held high, thereby accessing addresses 256 and 257 in 128 stage filter systems.

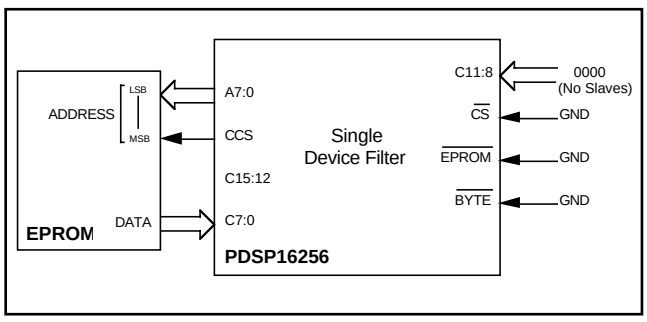


Fig.1 Diagram of standalone EPROM system

Once the control register has been loaded, A7:0 starts counting upwards from address 0. As CCS has now returned low, the EPROM addresses will be in the range 0 to 255. Bits 12, 13 and 14 of the control register define the number of digital stages in the filter and whether the decimate option is enabled. This defines the number of coefficients required and is used to regulate the number of bytes loaded from the EPROM. Every 4 SCLK cycles a new address is generated and a new byte loaded using the 8 least significant bits of the coefficient input bus, C15:0. If only one PDSP16256 device is contained in a filtering system (i.e. devices are not being cascading), then bits C11:8 should all be tied to ground and C15:12 should be left unconnected. The reasons for this will become apparent after reading section 3.2.

3.1 Timing Information

Each address is held on the A7:0 outputs for four SCLK cycles. On the fourth cycle, the data presented to the lower 8 bits of the C15:0 input bus is loaded into the device. Using this information the type of EPROM required to correctly interface to a PDSP16256 may be specified.

The EPROM access time is calculated by subtracting the output delay between SCLK and A7:0 and the setup time required to correctly load data into the PDSP16256 from four SCLK periods. Hence,

EPROM Access Time = 4.T - Output Delay - Setup Time

(where T is the SCLK period)

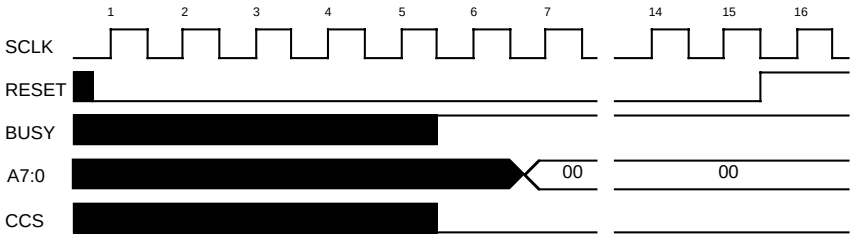
We know that the output delay has a maximum value of 26ns and that the setup time is 8ns. Therefore,

EPROM Access Time = 4.T - 26 - 8 = 4T - 34

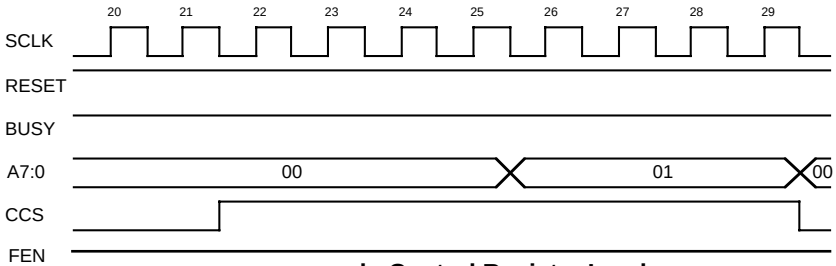
For a typical application where SCLK is running at 25MHz (T=40ns), it can be seen that the EPROM access time will be 126ns. This means that to correctly load data with SCLK running at 25MHz, an EPROM with an access time of 126ns, or less, is required.

3.2 Cascading devices in EPROM mode

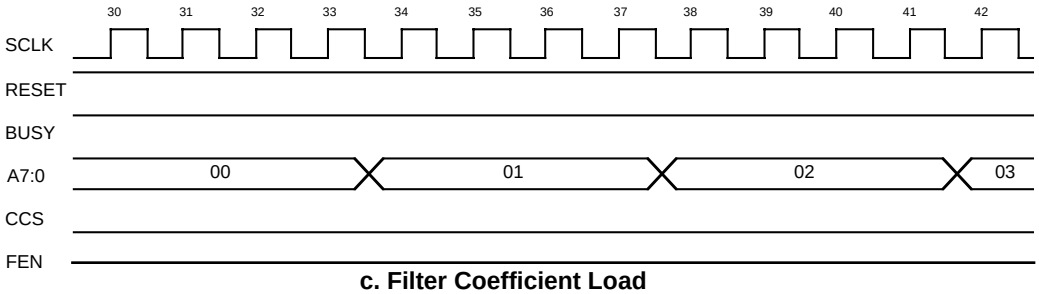
An arbitrary number of PDSP16256 devices may be cascaded to form a given filtering system. However, only a maximum of 16 devices may access the same EPROM to load configuration data. Hence, if more than 16 devices are to be cascaded, these should be subdivided into blocks of 16 for configuration purposes, with each 16 device block having access to a separate EPROM.



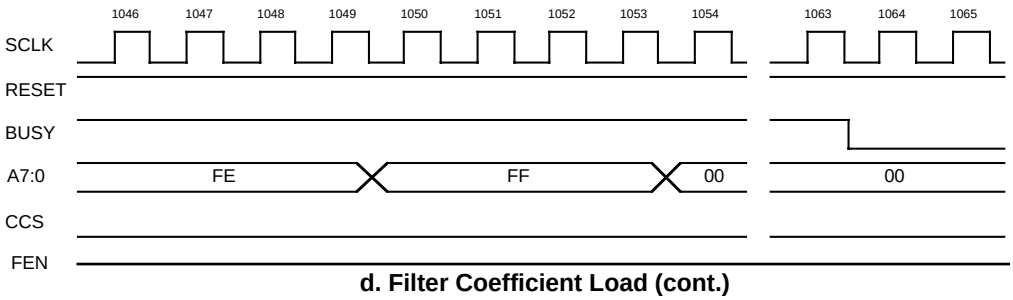
a. Reset Sequence



b. Control Register Load



c. Filter Coefficient Load



d. Filter Coefficient Load (cont.)

Fig.2 Reset & coefficient load sequences.

When several devices are connected in cascade, one of these devices is nominated the master (this should not be confused with a remote master discussed elsewhere in this application brief). The master device is responsible for controlling the loading of data for all devices to which it is connected. The master is identified by the fact that its EPROM input is grounded; all other cascaded devices, termed slaves, have their EPROM inputs connected to +5V. The master provides address, Write Enable, CCS and device decoding signals for all slave devices as well as for itself.

Only 8 of the 16 bits of the coefficient input bus, C15:0, are used in automatic EPROM load mode. The remaining eight lines are used to provide device decoding information. These signals help pass the required coefficient and control data to the correct device under the control of the master. The four bits C11:8, which are programmed as inputs on both slave and master devices, are used to assign a unique code to each slave. The first slave should have C11:8=0001, the second, C11:8=0010 and so on. The master device is therefore implicitly labelled 0000. The master uses C11:8 inputs to identify the total number of slaves contained in the cascaded system. If four devices are to be cascaded, for example, these will comprise one master and three slaves. Therefore, the C11:8 inputs on the master would be set to 0011.

The four bits C15:12 are programmed as outputs on the master and inputs on all slaves. Only when the value indicated on C15:12 is equal to the slave device code defined by C11:8 will the slave in question load the data passed to it via the coefficient input bus. This arrangement effectively provides a unique decode signal for each slave device in turn. The Chip Select signal, CS, should be tied to ground on all devices; slaves and master. C15:12 are used in conjunction wth A7:0 and CCS to access different pages of the EPROM, as shown by the timing diagram, fig. 4.

3.3 EPROM Memory Requirement

When the PDSP16256 loads coefficient data, if the filter length is such that bank swapping is possible, the device will always attempt to load a second bank of coefficients, irrespective of whether the bank swapping option has been enabled in the control word or not. Hence, in single filter mode, the amount of EPROM space required for each of the filter lengths, in bytes, is:

Filter Length	EPROM Space
128	512
64	512
32	256
16	128

In dual filter mode, the EPROM memory requirements are as follows:

Filter Length	EPROM Space
64	512
32	512
16	256
8	128

If n devices are connected in cascade, with each device implementing the same size of filter, then the EPROM space required is simply the product of the space required by a single device and the number of devices.

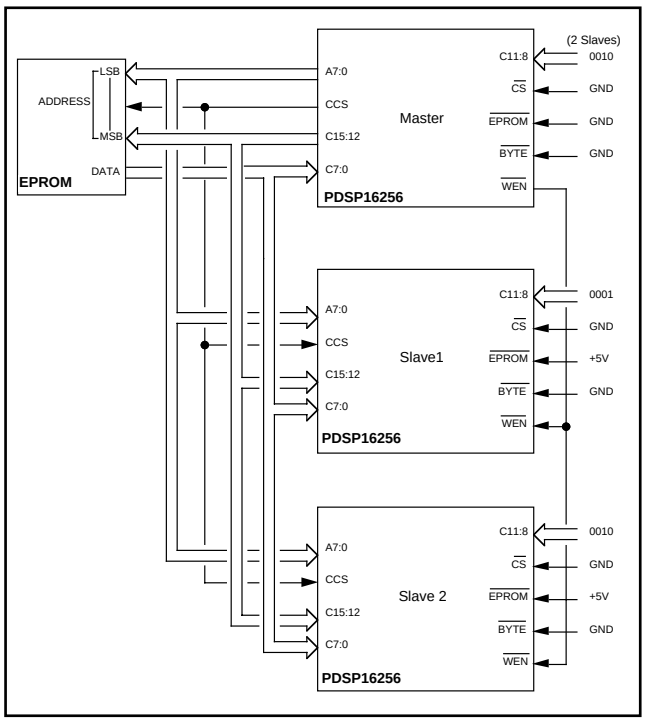


Fig.3 Cascaded system

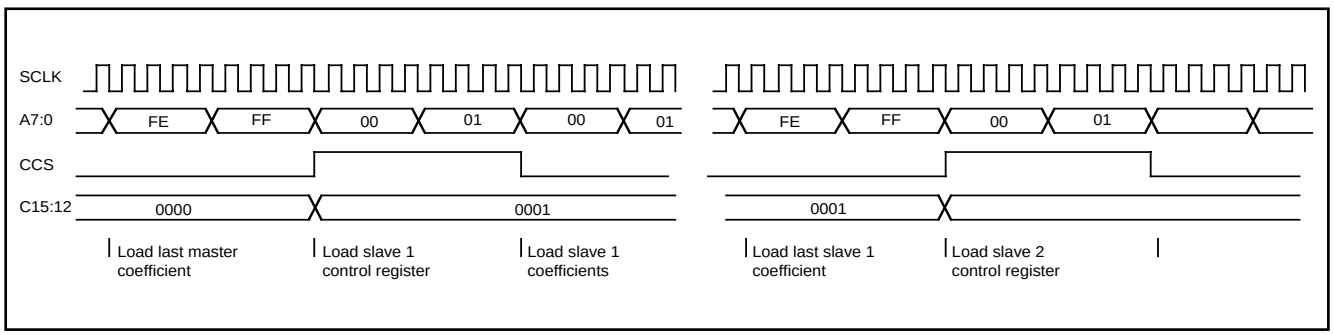


Fig.4 Load sequence for a cascaded system

Consider a system which contains four devices each of which contains a single 128 stage filter. In order to configure all four devices, an EPROM containing a total of

4 x 512 = 2048 bytes

will be required. The memory map for this EPROM is shown in Fig.5. The diagram shows the values of C15:12, CCS and A7:0 required to access each different area of the EPROM.

4. REMOTE MASTER MODE

In this mode, the remote master, is charged with supplying the address and data buses to the PDSP16256 via a synchronous peripheral interface. This mode allows all or selected coefficients to be updated under the control of the remote master whenever conditions dictate. Remote master mode is selected by tying the EPROM input pin of the PDSP16256 to +5V.

A filter initialisation sequence, where both the control register and filter coefficients are loaded, is initiated by a RESET sequence. RESET should be held low for 16 cycles of SCLK. After the sixth SCLK cycle the BUSY signal goes high, indicating that the device is performing internal initialisation operations. BUSY will remain active for 31 SCLK cycles. Only when it goes low can data be written to the device. A RESET sequence, as described above, is not needed when filter coefficients alone are to be updated.

When valid data appears on the address and data bus, this data is written to the PDSP16256 by the application of synchronous Chip Select (CS) and Write Enable (WEN) signals. Data may be written to the PDSP16256 either in 8 bit bytes or 16 bit words, the data width being selected by the BYTE input pin.

If BYTE is tied low, data is loaded as 8 bit bytes, and if high, as 16 bit words. The comparison that is made in automatic EPROM load mode between C15:12 and C11:8 is also made in byte mode, irrespective of the fact that remote master mode is selected. Hence, to satisfy this comparison, pins C15:8 should all be tied to ground when using 8 bit data transfers. In byte mode, the least significant byte (which is accessed when A0=0) should be written first, followed by the most significant (accessed when A0=1). If the device is operating in byte mode, it is necessary to hold CS low for an extra two SCLK cycles once all the coefficients have been loaded. This can be clearly seen in fig. 8c.

When 16 bit words are used, a maximum of 128 transfers are required to load all the required filter coefficients. Hence, only 7 address lines are needed and A7 is therefore redundant in word mode. Unlike automatic EPROM load mode, new data may be written to the device on every SCLK cycle, if required, as long as the timing constraints are honoured.

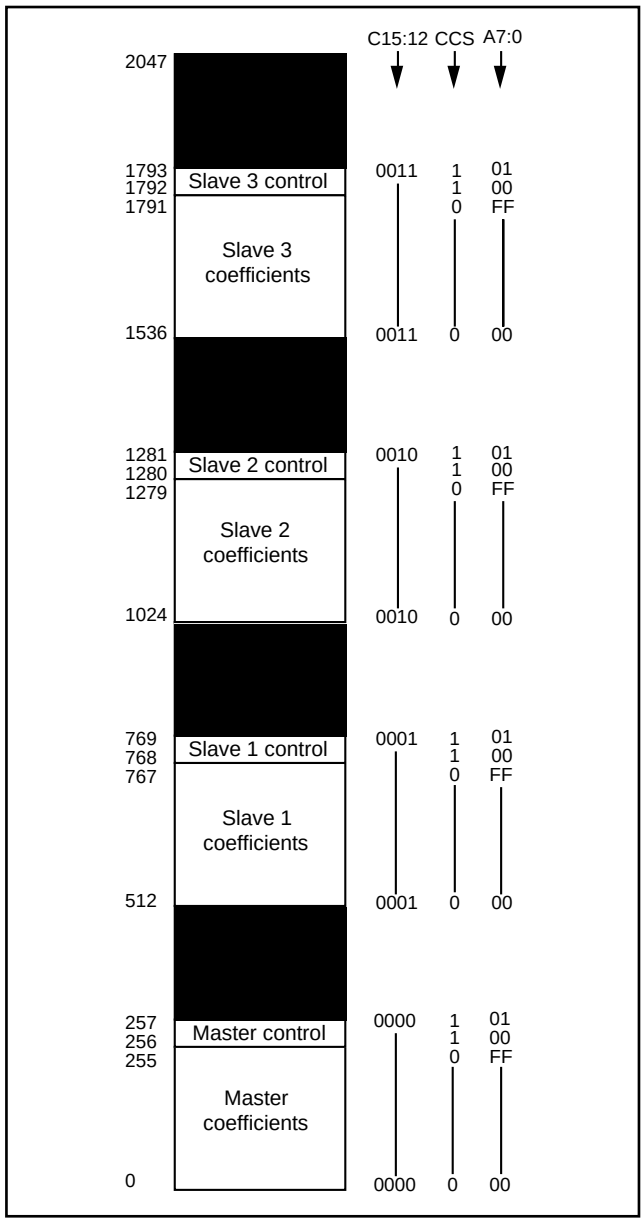


Fig.5 EPROM memory map for a four device system

As with automatic EPROM load mode, the control register should be loaded first, followed by the filter coefficients. A delay of at least two clock cycles needs to be inserted after the control register has been loaded and before any filter coefficents are written to the device. CS needs to be held low for a total of three clock cycles when loading the control register, as shown in fig. 8a. CCS becomes an input to the PDSP16256 in this mode and, when high, indicates that a load to the control register is to take place. Hence, as with automatic EPROM load mode, CCS is used as the most significant address line in conjunction with A7:0. The filter coefficients may be addressed at random, i.e. they need not be loaded in address order, and an arbitrary number may be modified under the control of the remote master at any time. It must be borne in mind that one of the effects of loading new coefficients will be that mathematically correct results will not

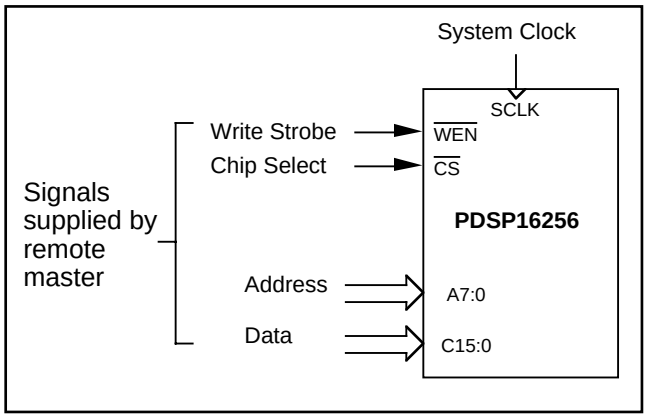


Fig.6 Remote Master standalone system

be obtained for a number of cycles, the exact number depending upon which coefficients were modified and the length of the filter. This is due to the effect of partial results, calculated using the old coefficients, being propagated through the device. It is not recommended that the control register be modified whilst the device is operating. The control register should only be loaded after a reset sequence, as described above.

The PDSP16256 is a synchronous device. This means that all external signals are assumed to be synchronous to the system clock. In general, the remote master's Write Enable and Chip Select signals will be asynchronous to the PDSP16256 system clock. Hence, the signals supplied to the PDSP16256 should be synchronised to SCLK and care taken to ensure that all setup and hold times are honoured. Double buffering the signals generated by the remote master, as shown in fig. 7a, will ensure that these constraints are met, whilst at the same time minimizing metastability problems.

The diagram below shows one possible implementation of a system that will ensure that all timing constraints are met when operating in remote master mode. The coefficient load state machine is used to generate the WEN and CS signals. As can be seen in fig. 7b, WEN is low only for the required one clock edge period. In more complicated systems this state machine could be used to perform other functions such as device decodes etc.

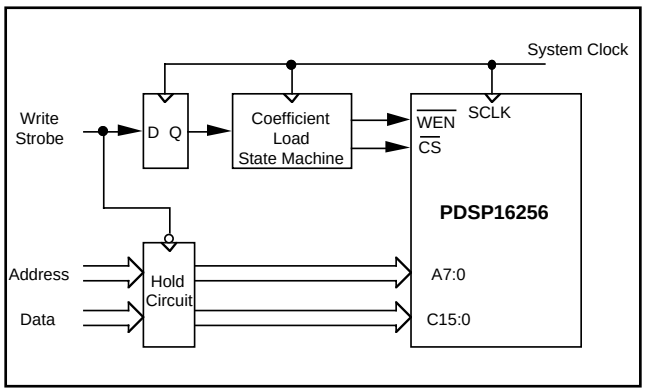


Fig.7a Remote master interface

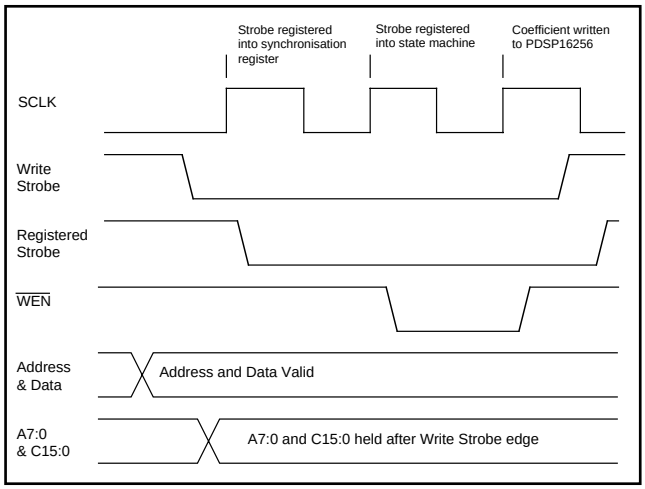


Fig.7b Remote master signal synchronisation

4.1 Timing

Figs. 8a and 8b show the setup and hold constraints which must be met if data is to be loaded correctly. The setup and hold time values are as listed in section 2 above. Fig. 9 shows examples of reset and load sequences for both byte and word modes.

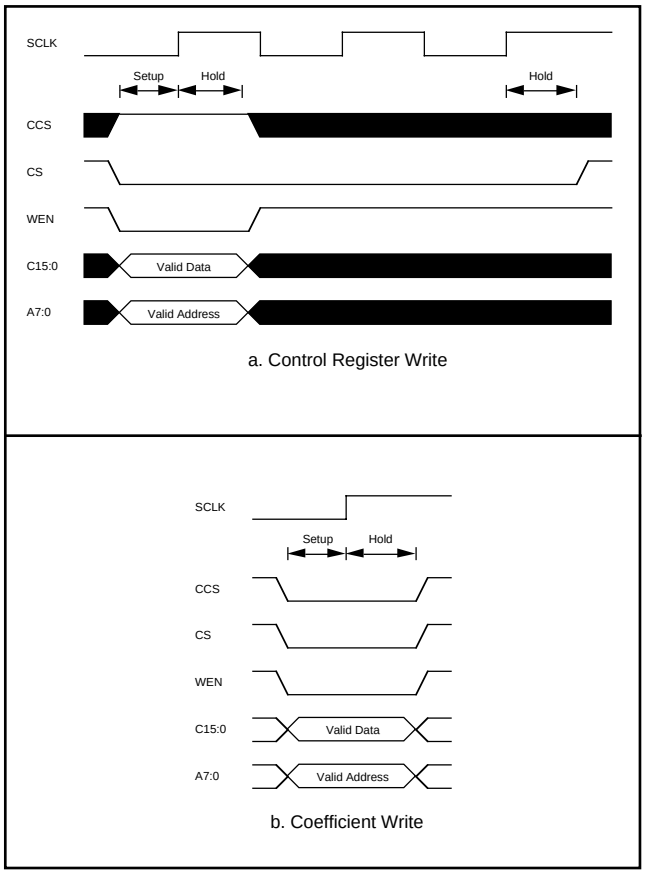


Fig.8a,b Remote master timing constraints

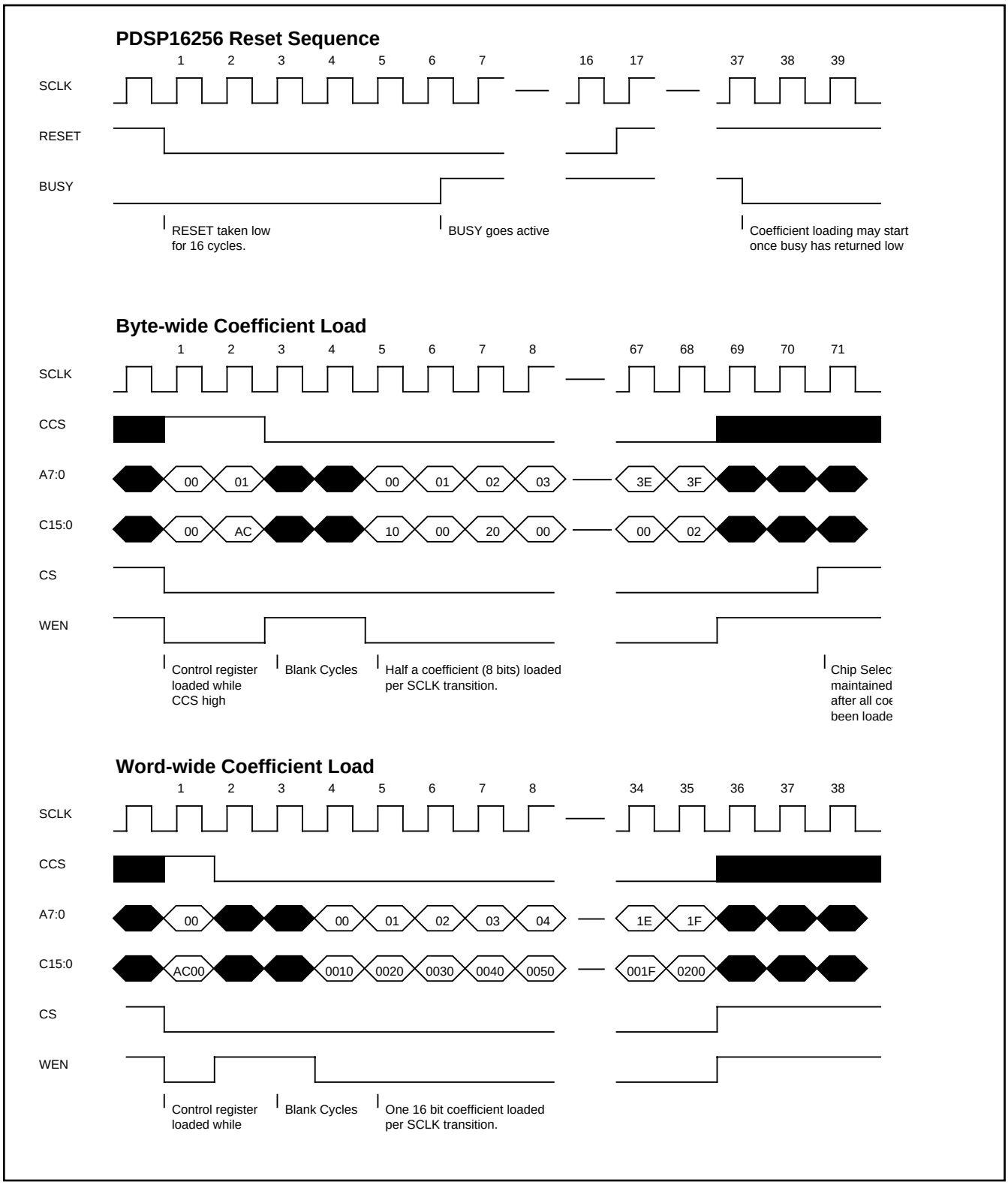


Fig.9 Reset & coefficient load sequences

4.2 Cascading in Remote Master mode

When devices are cascaded in this mode, the master-slave distinction that is evident in automatic EPROM load mode is not necessary as all devices are treated in the same way. Chip Select and Write Enable signals are used to selectively enable the required device and to write to it the relevant data. In many ways, the method used to write data to a series of PDSP16256 devices is analogous to the process of writing to a bank of RAM devices. Fig. 10 shows a typical cascade configuration for this mode.

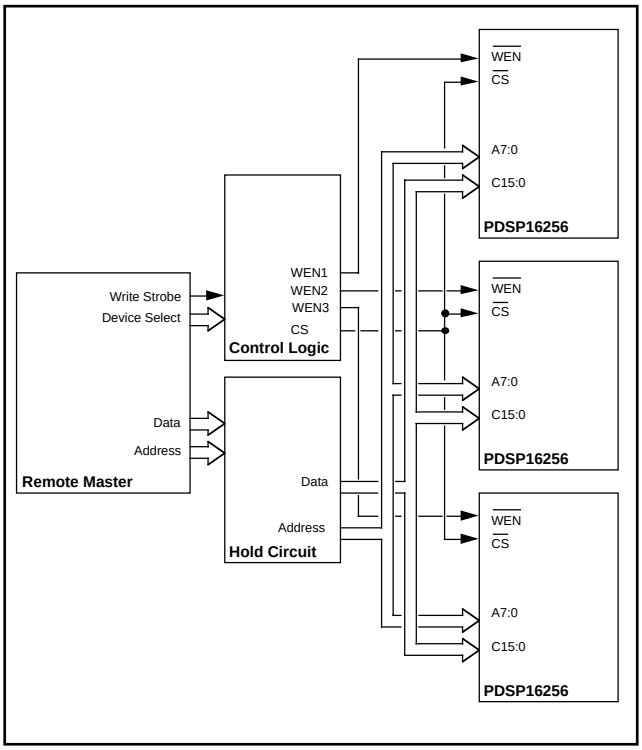


Fig.10 Cascaded remote master system

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