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Integrated GPS Downconverter

This integrated circuit is intended for GPS receiver applications. The dual conversion design is implemented in Motorola's low–cost, high–performance MOSAIC 5™ silicon bipolar process and is packaged in a low–cost surface mount LQFP–48 package. In addition to the mixers, a VCO, PLL, Crystal Oscillator, A/D converter and a loop filter are integrated on–chip. Output IF is nominally 4.1 MHz.

- 105 dB Typical Conversion Gain
- 2.7 V Operation
- 28 mA Typical Current Consumption
- Low-Cost, Low-Profile Plastic LQFP Package

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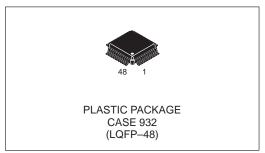
ORDERING INFORMATION

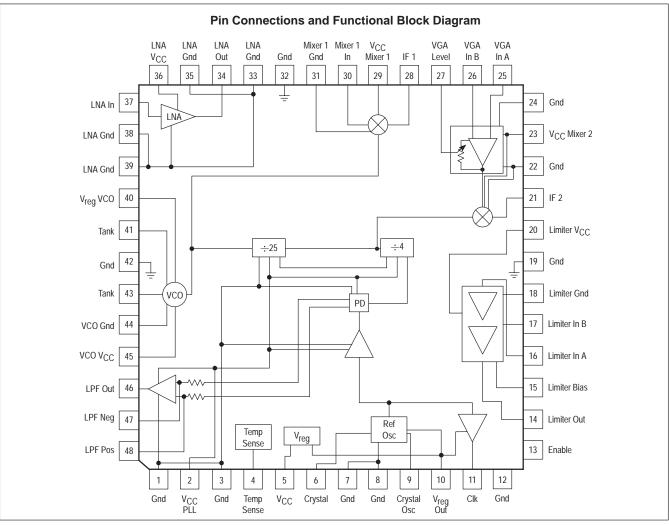
Device	Operating Temperature Range	Package
MRFIC1504R2	$T_A = -40 \text{ to } 85^{\circ}\text{C}$	LQFP-48

MRFIC1504

1.575 GHz GPS DOWNCONVERTER

SEMICONDUCTOR TECHNICAL DATA





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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	5.0	Vdc
DC Supply Current	I _{DD}	60	mA
Operating Ambient Temperature	T _A	-40 to 85	°C
Storage Temperature Range	T _{Stg}	-65 to 150	°C
Lead Soldering Temperature Range (10 seconds)	-	260	°C

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 2.7 \text{ to } 3.3 \text{ V}; T_A = -40 \text{ to } 85^{\circ}\text{C}; \text{ Enable} = 2.7 \text{ V} \text{ unless otherwise noted}$)

Characteristic	Symbol	Min	Тур	Max	Unit
TOTAL DEVICE	<u>'</u>		<u> </u>		
Supply Voltage	Vcc	2.7	3.0	3.3	V
Supply Current $(T_A = 25^{\circ}C, V_{CC} = 2.7 \text{ V}, \text{ Enable} = 2.7 \text{ V})$	lcc	_	28	36	mA
Supply Current (T _A = 25°C, V _{CC} = 2.7 V, Enable = 0 V)	lcc	_	2.0	4.0	mA
RF AMPLIFIER					
RF Input Frequency	f _{in}	-	1575.42	_	MHz
Input Impedance	z _{in}	_	50	_	Ω
Input VSWR	VSWRin	_	2.0	_	_
Gain	G	13	15	-	dB
Noise Figure	NF	-	2.0	_	dB
1.0 dB Compression (Measured at Output)	P _{1dB}	-	1.0	-	dBm
FIRST MIXER					•
Input Frequency	fin	-	1575.42	-	MHz
Gain	G	10	14	_	dB
Noise Figure	NF	-	13	_	dB
1.0 dB Compression (Measured at Output)	P _{1dB}	-	-13	-	dBm
First Local Oscillator Frequency	fLO1	-	1636.8	_	MHz
First Intermediate Frequency	fIF1	-	61.38	-	MHz
LO Leakage at IF Port	_	_	-40	_	dBm
LO Leakage at RF Port	_	_	-50	_	dBm
Output Impedance	Z _{out}	_	50	_	Ω
FIRST IF AMPLIFIER and SECOND MIXER	•		<u>'</u>		'
Input Frequency	f _{in}	-	61.38	-	MHz
Imput Impedance	Z _{in}	_	230	_	Ω
Output Impedance	Z _{out}	_	50	_	Ω
Second Local Oscillator Frequency	fLO2	_	65.47	_	MHz
Second Intermediate Frequency	f _{IF2}	_	4.092	_	MHz
LO Leakage at IF Port	_	_	-40	_	dBm
Gain	G	40	43	_	dB
Cascaded Noise Figure	NF	_	9.3	_	dB
1.0 dB Compression Point (Measured at Output)	P _{1dB}	_	-13	_	dBm

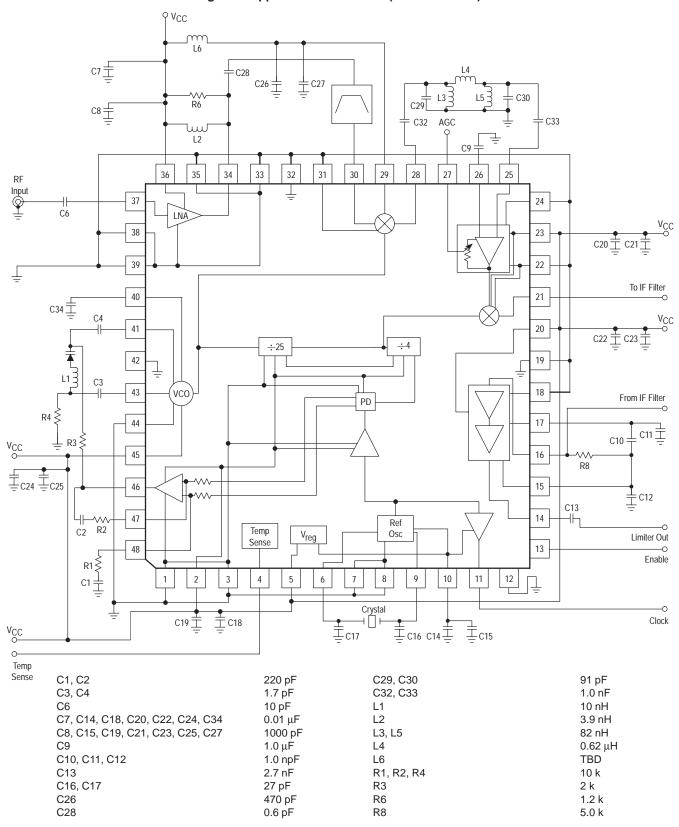
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ELECTRICAL CHARACTERISTICS — continued ($V_{CC} = 2.7 \text{ to } 3.3 \text{ V}$; $T_A = -40 \text{ to } 85^{\circ}\text{C}$; Enable = 2.7 V unless otherwise noted)

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Characteristic	Symbol	Min	Тур	Max	Unit
LIMITING AMPLIFIER					
Second Intermediate Frequency	fIF2	_	4.092	-	MHz
Input Signal Level	-	4.0	11	31	mV
Output Voltage Swing (Into 10 pf 100 kΩ)	V _{out}	800	-	-	mVpp
DC Output Level	_	_	1.4	-	V
Gain	G	_	50	-	dB
REFERENCE OSCILLATOR		•		•	
Reference Frequency	f _r	-	16.368	-	MHz
Reference Frequency Input Level (Crystal Output Pin)	-	-	500	-	mVpp
Reference Oscillator Output Voltage Level (Into 15 pF 10 kΩ)	-	750	-	-	mVpp
Reference Clock Input Drive Level	-	400	800	1500	mVpp
PLL		•			
First Local Oscillator Frequency	fLO1	-	1636.8	-	MHz
Second Local Oscillator Frequency	f _{LO2}	-	65.47	-	MHz
VCO C/N (at 10 kHz Offset)	-	_	-80	-	dBc/Hz
VCO Gain (TBD Varactor)	-	-	20	-	MHz/V
ENABLE		•			
Enable Active Level	-	0.8 × V _{CC}	VCC	-	V
Disable Active Level	-	-	0	0.2 × V _{CC}	V
VOLTAGE REGULATOR					
Regulator Output Voltage $(V_{CC} = 2.7 \text{ to } 3.3 \text{ V}, I_{out} = 3.0 \text{ mA})$	Vo	2.1	2.3	2.5	V
TEMPERATURE SENSE SPECS					
Temperature Sensor Output Voltage @ 25°C	_	1.2	1.28	1.375	V
Temperature Sensor Slope over Temperature	-	_	5.0	-	mV/°C

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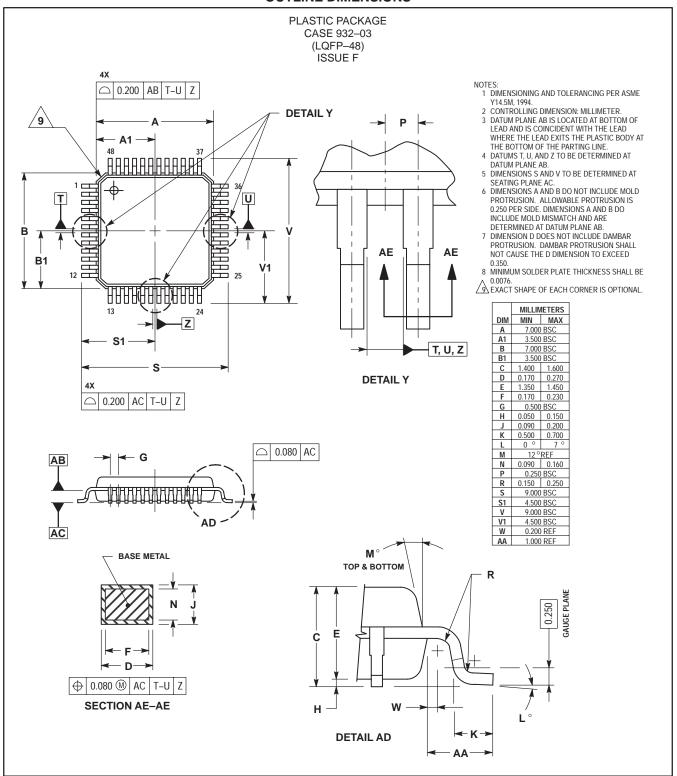
Figure 1. Applications Schematic (1636.8 MHz LO)



NOTES: 1. R8 must be set to match your 2nd IF filter impedance.

^{2.} Layout of capacitors C10, C11, C12 is critical for stability of Limiter.

OUTLINE DIMENSIONS



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NOTES

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