



Additional Features of the M50FW080 8 Mbit Firmware Hub

INTRODUCTION

The M50FW080 is an addition to the family of leading-edge Flash Memories from STMicroelectronics suited for use in PC Bios applications. The M50FW080 interfaces to chipsets which use the firmware hub protocol. It is manufactured using the same 0.18 μ m process as the M50FW040 FWH memory.

DIFFERENCES WITH RESPECT TO THE M50FW040 4 MBIT FWH

The M50FW080 is basically the same as the M50FW040 but with double the number of memory blocks. The M50FW080 has sixteen 64KByte blocks while the M50FW040 has eight 64KByte blocks.

The M50FW080 has an additional feature which is the possibility to perform chip erase operations when in A/A Mux mode. The internal chip erase algorithm allows a faster chip erase time when compared to separate block erase operations and may be useful for third party programmers and for factory re-programming. This feature is valid for V_{PP} at 12V. Chip erase is not available in FWH mode.

The M50FW080 has an additional feature of quadruple byte programming in A/A Mux mode which may be useful for third party programmers and for factory programming. The object is to reduce the overall chip program time with respect to the standard single byte method. See the section on fast programming and erase considerations for more details. Quadruple byte programming is not available in FWH mode.

The M50FW080 has a device code 2Dh; the M50FW040 has a device code 2Ch.

DIFFERENCES WITH RESPECT TO THE INTEL 8 MBIT FWH

The random number generator (RNG) documented in the Intel 8Mb FWH 82802AC datasheet is not available in the STMicroelectronics M50FW080. If your application requires a RNG within the firmware hub memory then you will not be able to use the M50FW080.

The manufacturer code (20h) and device code (2Dh) of the STMicroelectronics M50FW080 are different from those of the Intel 82802AC. Note that when reading the Electronic Signature, the correct addresses must be used with this command (ie. 00000h for Manufacturer Code and 00001h for Device Code). All other functional features of the 82802AC are believed to be included in the M50FW080 (except for RNG as already mentioned).

The M50FW080 has the additional features of chip erase in A/A Mux mode and quadruple byte programming in A/A Mux mode.

FAST PROGRAMMING AND ERASE CONSIDERATIONS

The quadruple byte program command in A/A Mux mode with V_{PP} at 12V can be used to effectively reduce programming time to a quarter of the single byte programming time.

This could be useful during factory programming or with third party programmers. Note that quadruple byte requires that the only addresses which change in the four bytes are A0 and A10. A typical chip program time with quadruple byte is about 2.5s compared with 10s which using single byte. The chip programming times quoted exclude any system overheads.

During quadruple byte programming if only A0 is changed within the four bytes (i.e: two of the bytes will have the same address and the same data) then it is possible to program two bytes (using the quadruple byte command) and effectively halve the chip programming time. For example if a quadruple byte command is issued with (Ax address, Dx data), (Ax address, Dx data), (Ay address, Dy data), (Ay address, Dy

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data) then result is to program the two bytes. If the order of the bytes and addresses is exchanged within the quadruple byte command then the result is still the same.

The chip erase command in A/A Mux mode with V_{PP} at 12V can be used to give a chip erase time which is faster than erasing all the blocks separately. The typical time for chip erase is about 9s (at 25°C and 3.3V) while the typical time for chip erase using separate blocks is about 15s (at 25°C and 3.3V). Note that STMicroelectronics delivers the device with all bits erased so a chip erase command might be useful only during a factory re-programming operation and not the first time the device is programmed.

When using the block erase command, if the V_{PP} pin is connected to 12V then the erase time is faster by approximately 0.2s per block (same as M50FW040).

When using the single byte program command the program time is not any faster if V_{PP} is at 12V. The V_{PP} at 12V is essential for quadruple byte commands.

Note that the M50FW080 has three V_{CC} pins and two V_{SS} pins. All these pins must be connected in order for the device to work correctly even in third party programmers in A/A Mux mode. The pins are not necessarily internally connected to each other within the device; in fact there are separate supplies of V_{CC} and V_{SS} to the FWH PCI compatible buffers.

CONCLUSIONS

The M50FW080 is an addition to the family of leading-edge Flash Memories from STMicroelectronics. It has been designed to be as near as possible a direct replacement of the existing 8Mb FWH from Intel. Additional features have been added to greatly improve factory programming throughput. It is manufactured on a 0.18µm process to ensure an excellent cost structure and a long production lifetime.

Table 1. Revision History

Date	Version	Revision Details
May 2001	-01	First Issue
June 2001	-02	"Differences with Respect to the M50FW040 4 Mbit FWH" and "Differences with Respect to the Intel 8 Mbit FWH" chapters changed
August 2001	-03	Added note on Electronic Signature in "Differences with Respect to the Intel 8Mb FWH".

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