

Application Note

Jitter Testing Procedures for Compliance with AT&T 62411

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Introduction

This application note presents guidelines for measuring whether a design is compliant with AT&T 62411 jitter tolerance, jitter generation and jitter attenuation requirements. 62411 compliance is a necessary requirement for *CPE* (Customer Premises Equipment) which is connected to T1 lines provided by AT&T. These T1 lines may be either private-line or central-office access lines. 62411 may not apply to equipment sold to telephone companies, equipment used within a campus environment or equipment used to access an alternative long-distance carrier.

AT&T 62411 jitter testing can be performed using the test equipment listed in Table 1. Other equipment with jitter generation and measurement capability is available from a number of vendors, but these systems commonly lack the performance required for 62411 in two areas. First, many do not have the ability to generate and measure the large amplitude (>28 UIpp) jitter below 300 Hz which is required by AT&T 62411. Also, many do not have the dynamic range to make the narrow-bandwidth, low amplitude jitter measurements required for measuring 62411 high frequency jitter transfer beyond 40 dB. The equipment and procedures shown here are based upon those used during AT&T conformance testing.

The HP 3785B is a powerful and flexible jitter test set which provides sinusoidal jitter generation and demodulation. The HP 3785B receiver features a front-panel meter which can display the broadband input jitter amplitude as well as the amplitude in the passband of one of its three internal filters. The HP 3785B also provides a demodulator output signal which can be input to a spectrum analyzer to make accurate narrow-bandwidth, high frequency jitter transfer measurements. However, the HP 3785B cannot generate or measure jitter larger than 10 UIpp.

Characterizing large amplitude jitter performance requires an RF signal generator with FM modulation capability. The HP 8656B accepts an externally generated modulating signal (from an audio oscillator) while the HP 8644A provides an internal modulation synthesizer. The RF generator's output is connected to a 50 Ω buffer which produces a logic level clock suitable for the pattern generator external clock input.

HP 3785B	Jitter Generator/Receiver
Phoenix 5500 or HP 3780A	QRTS Pattern Generator and Error Detector
HP 3585A	Spectrum Analyzer
HP8656B and Khron-Hite 5500A or HP 8644A	RF Signal Generator Audio Oscillator RF Signal Generator with Modulation Synthesizer
HP 5372A	Time Interval Analyzer

Table 1. Equipment Used for Jitter Testing

Jitter Tolerance Measurements

The basic test setup is shown in Figure 1. The RF generator creates a 1.544 MHz jittered clock which clocks the Pattern Generator producing the AMI-encoded QRTS data. The Pattern Generator output connects to the T1 trunk card under test using a twisted pair cable. The signal is routed through the T1 trunk card and synchronizer and back through the trunk card to the data input of the Pattern Receiver. The Pattern Receiver is then used to measure bit errors. The jitter tolerance of a receiver will vary with the width of the AMI pulses. It is very important that the pattern generators used have consistent pulse widths. (The pulses should meet DSX-1 type pulse requirements as identified in CB-119.)

The jitter frequencies typically checked are: 3, 10, 30, 100, 1k, 2k, 4k, 8k, 16k, 32k, 64k and 100k Hz. The normal procedure is to select a jitter frequency, and then increase the jitter amplitude until the onset of bit-errors (for DTE testing) or synchronization loss (for synchronizer testing). The jitter frequency is set with the audio oscillator connected to the HP 8656B modulation input. The

jitter amplitude is set by entering the peak frequency deviation (in kHz) on the front panel of the HP 8656B. Given the frequency deviation, the jitter amplitude in UIpp can be calculated using Equation 1 below.

$$UI_{pp} = \frac{\Delta f}{\pi F_j} \tag{1}$$

where,

Δf is the frequency deviation in Hz, and
 F_j is the jitter frequency in Hz.

It is important to determine how much the system exceeds the minimum 62411 jitter tolerance requirements since the later attenuation tests are made with three-quarters of the observed tolerance of the system. Larger tolerance levels have the benefit of raising the floor on the acceptable output jitter level during the attenuation tests.

AT&T 62411 testing calls for measuring jitter tolerance using a QRTS data pattern, which is representative of live traffic on the network. But the key to guaranteeing jitter tolerance is to test

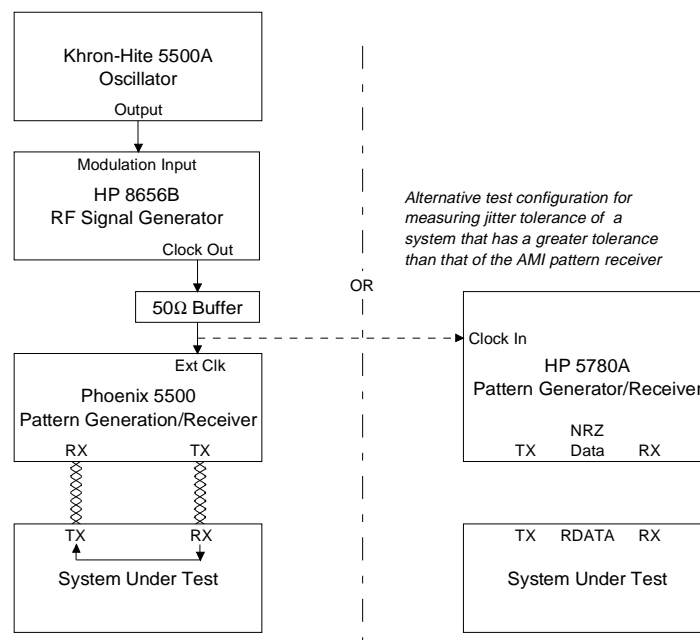


Figure 1 - Test Setup for Jitter Tolerance Measurements

receiver performance using a data pattern which is representative of the worst case conditions within the QRTS pattern. The most stressful jitter case for a receiver occurs when the maximum deviation from the ideal arrival time occurs between two ones which are separated by a string of zeros. For example, two ones separated by seven zeros can have maximum deviation from ideal arrival time at a jitter frequency of 96,500Hz. (Maximum phase deviation occurs in 1/2 of a jitter period; eight bit periods take 5181.4ns.) Still, this maximum jitter hit is dependant on the relationship of the phase of the jitter with respect to the occurrence of the string of zeros.

To trully measure jitter tolerance, one must guarantee that the maximum phase deviation between two consecutive ones separated by zeros will occur (assuming that the maximum allowable consecutive zeros is not exceeded). When using a quasi-random data pattern, it is unlikely that the jittered clock and the zero string in the data pattern will align to produce a maximum phase hit between successive ones unless the condition is tested for a long time. To guarantee 0.4 UI of jitter tolerance at jitter frequencies above 50 kHz, it is best to use a short pattern with repeating strings of 7 to 14 zeros to significantly increase the likelihood of a maximum jitter hit. Tests at Crystal Semiconductor have shown that repeating a data pattern similiar to:

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AA AA AA AA 33 33 33 33 33 33 03 00 03  
00 03 hex
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gives good correlation to the QRTS pattern. This pattern is considerably shorter than QRTS (which is $2^{20} - 1$ bits long) so the strings of fourteen zeros occur often enough for a robust test of jitter tolerance at 51.4 kHz (the worst case jitter frequency for ones separated by 14 zeros). In addition, this pattern has sections of 50% ones, to avoid placing undue strain on the clock recovery circuit. This pattern can be modified or extended for testing different zero strings at different frequencies.

The maximum jitter frequency at which the HP 3785B operates is 77kHz, however 62411 specifies jitter performance to 100kHz. Generally, the jitter tolerance performance of a receiver will have flattened out by 77kHz, so one can assume that if the jitter tolerance curve has flattened out, and if it passes a difficult data pattern such as 2 in 16 at 77kHz, that it will also pass at 100kHz. Hewlett Packard does make a CCITT version of the HP 3785B, the HP 3785A, which can produce jitter to beyond 100kHz and is available with a T1 option.

A word of caution: not all jitter (and pattern) generators have enough jitter tolerance to recover jitter amplitudes as large as they can generate. A pattern generator's receiver which is looking for bit errors in a retransmitted (looped back) signal which has not been jitter attenuated may itself make errors in data recovery leading the tester to falsely believe that the equipment being tested is making errors. Many pattern generators (like the HP 3780A) have a provision for accepting recovered clock and NRZ data. A test configuration such as shown on the right hand side of Figure 1 is highly recommended for measuring jitter tolerance of equipment which does not provide jitter attenuation.

Output Jitter Measurements

The basic test setup is shown in Figure 2. The measurement looks at jitter in specific frequency bands:

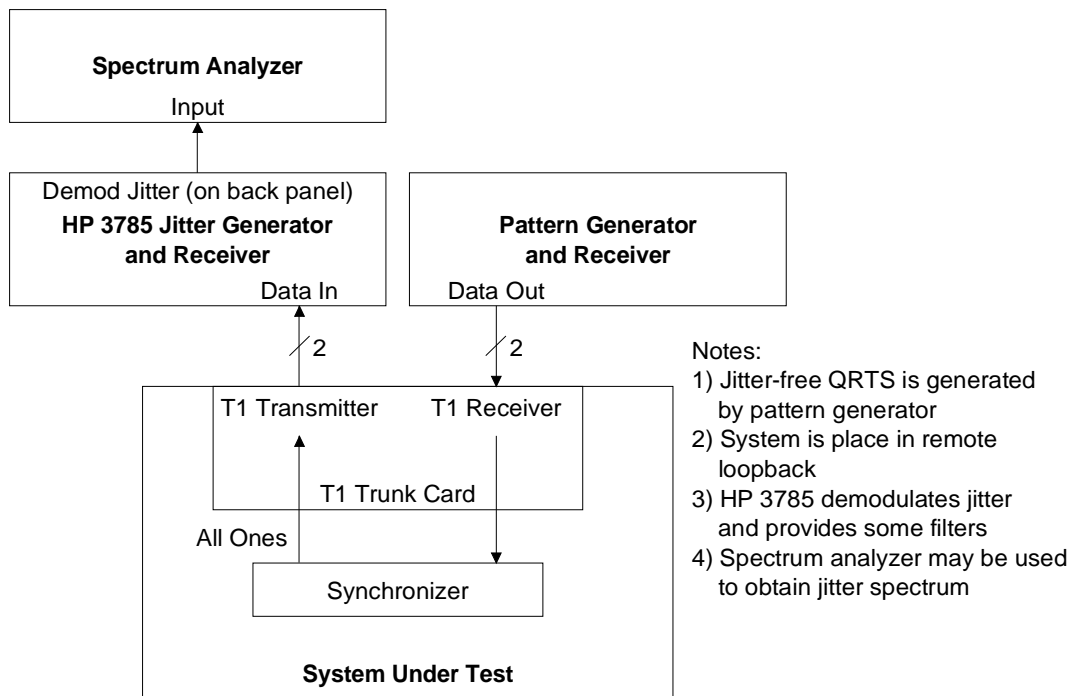
- 1) broadband; 0.05 UI,
- 2) using 10 Hz to 40 kHz filter; 0.025 UI,
- 3) using 8 kHz to 40 kHz filter; 0.025 UI,
- and
- 4) using 10 Hz to 8 kHz filter; 0.020 UI.

The first three of the frequency bands are selected using the filters available on the front panel of the HP 3785B. The output jitter levels are measured using the Received Jitter meter on the HP 3785B. For these measurements, the HP 3785B should be set to its "1" range which is its most sensitive scale. It is important to note that the HP 3785B's published accuracy is 4% + (0.035 UI) for input data patterns, and 4% + (0.025 UI) for input clocks.

Because the published accuracy of the instrument is not sufficient to measure to the small jitter levels required, it is advisable to do some sanity checks. Have the jitter receiver measure the jitter from the jitter free pattern generator. This will provide a "feel" for the HP 3785's measurement floor. It may be appropriate to subtract this result from subsequent measurements.

Furthermore, using an all ones data pattern will improve the instruments accuracy slightly (approaching that for input clocks). If the system under test has a transmit all ones capability, select this function for testing transmitted jitter. The transmit clock used in this case should be same as for normal operation or remote loopback.

Observing the DEMOD JITTER output (available from the back of the HP 3785) on a spectrum analyzer may also prove enlightening. While the sum of the jitter over a frequency band is not readily available, one can observe the jitter spectrum of the demodulated signal, look for jitter spikes ris-



- Notes:
- 1) Jitter-free QRTS is generated by pattern generator
 - 2) System is place in remote loopback
 - 3) HP 3785 demodulates jitter and provides some filters
 - 4) Spectrum analyzer may be used to obtain jitter spectrum

Note: Measurement is much more accurate if All Ones are transmitted to the HP 3785 using the recovered clock.

Figure 2 - Test Setup for Output (Added) Jitter Measurements

ing out of the noise floor, and most importantly, compare the spectrum of the jitter free pattern's source to the transmitter's output, watching for artifacts that may be present in the source or created by the HP 3785 itself.

The HP 3785 does not have internal filters for measuring jitter from 10 Hz to 8 kHz, so measuring jitter in this band requires additional work. Obviously, if the jitter from 10 Hz to 40 kHz is less than 0.020 UI, so is the jitter from 10 Hz to 8 kHz. Jitter in the 10 Hz to 8 kHz band can be mathematically approximated by measuring the jitter in the band from 10 Hz to 40 kHz and jitter and the band from 8 kHz to 40 kHz by using Equation 2.

$$b = \sqrt{c^2 - a^2} \tag{2}$$

where

- b = jitter from 10 Hz to 8 kHz
- c = jitter from 10 Hz to 40 kHz, and
- a = jitter from 8 kHz to 40 kHz.

Jitter in different bands will add as the sum of the squares. The most rigorous method is to build a band-pass filter which rolls off at 6dB / octave below 10 Hz and above 8 kHz. This filter is placed between the Demodulated Jitter Output and Measurement Input (both on the rear panel) of the HP 3785.

Jitter Transfer Measurements

The basic test setup is shown in Figure 3. The HP 3785B generates jitter at selected frequencies (the same frequencies at which jitter tolerance was measured, up to 32 kHz). The jitter amplitude that is input to the system should be 75% of the system's measured jitter tolerance.

Jitter attenuation is determined by comparing the amount of jitter in the signal output from the pattern generator (configuration "a") to the amount of jitter contained in the looped-back signal from the system under test (configuration "b"). The amount of jitter output from the jitter generator at each frequency should be 75% of the receiver's jitter tolerance at that frequency. The range scale used on the HP 3785 jitter receiver should be the same for both measurements.

When the input jitter is large (> 1 UI) *and* the output jitter from the system under test is greater than about 0.1 UI, the value shown on the Received Jitter display is sufficiently accurate. When the received jitter gets small (< 0.1 UI), it becomes necessary to use a spectrum analyzer to determine the jitter attenuation.

A spectrum analyzer must be used for two reasons. First, the accuracy of the jitter receiver is only 4% + (0.035 UI). Second, the value displayed by the jitter receiver is representative of the jitter over the selected bandwidth, not the jitter at the frequency being tested. Figure 4 shows a spectrum analysis display representing jitter attenuation. The upper curve shows the demodulated jitter present in the AMI data pattern output from the pattern generator. The lower curve shows the demodulated jitter present in the signal from the system under test. The attenuation is the difference in the amplitude of the two curves at the frequency of interest (shown at the top/center of the display).

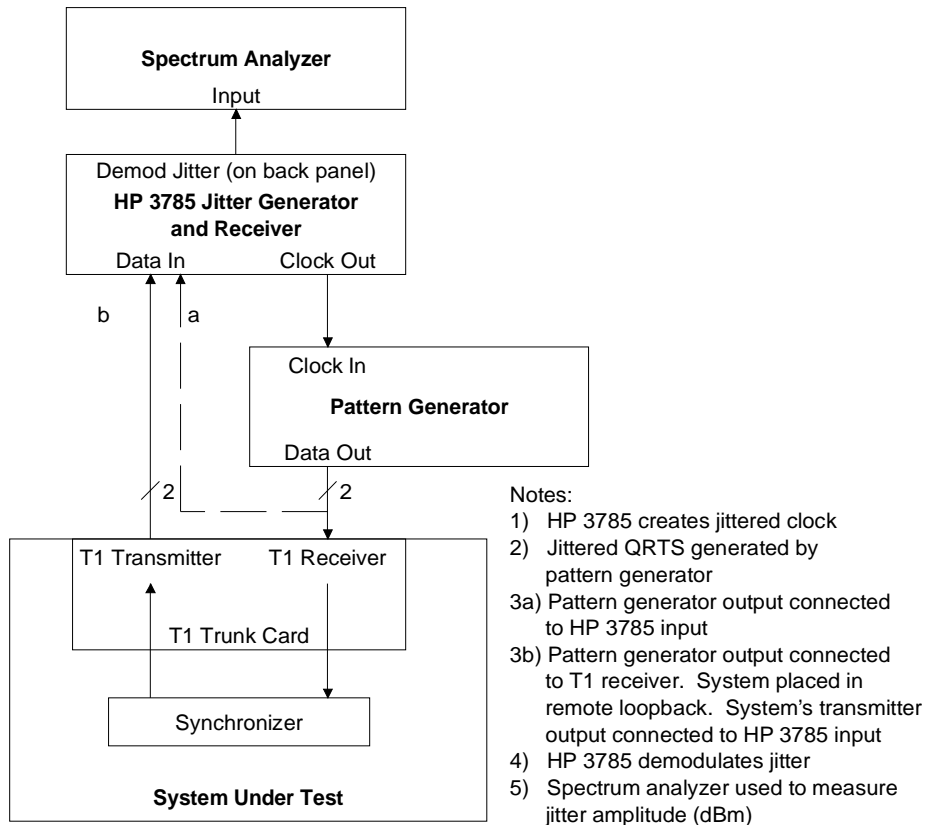


Figure 3 - Measuring Input and Output Jitter Amplitudes

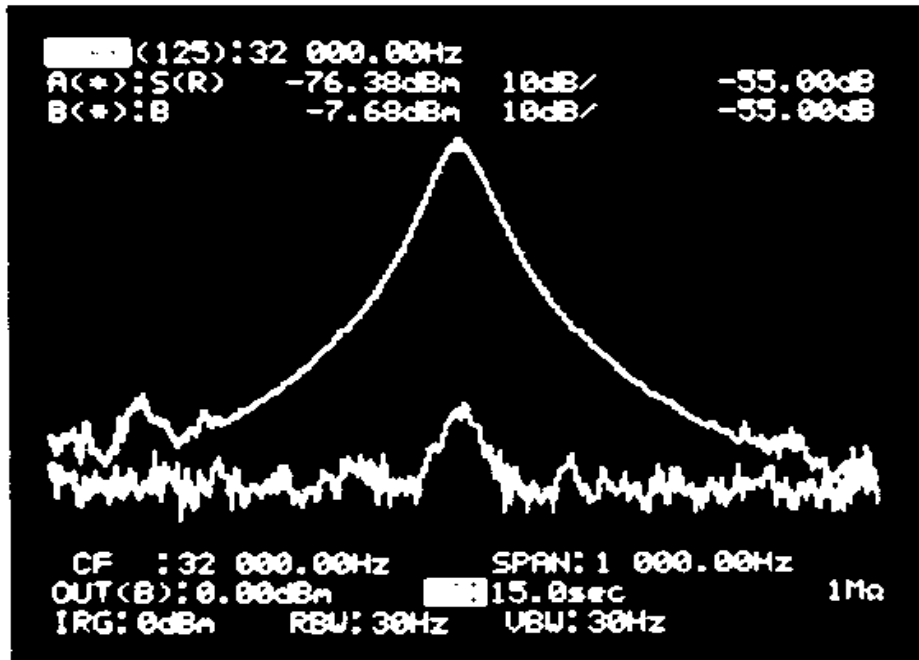


Figure 4 - Spectrum analyzer photograph showing 68.7dB of jitter attenuation at 32kHz.

Additional Considerations

When testing for compliance to 62411 it is often a good idea to expand the scope of some of the tests slightly to look for anomalous behavior of the system under test, and evaluate the robustness of the system's design. Here are some suggestions: Evaluate the system's performance as power supply and temperature are varied. ICs using external components (inductors, capacitors, and quartz crystals) may be particularly susceptible to temperature or supply variations.

It is prudent to check performance over the T1 frequency range allowed by the system. AT&T 62411 specifies a frequency tolerance of 75Hz (50 ppm). Some circuits will have sensitivity to frequency, and that sensitivity might be amplified by variations in temperature or supply. Verify that the frequency tolerance of the receiver exceeds 50 ppm, and check for anomalous behavior of the jitter attenuator as the T1 frequency is varied.

Testing for frequency dependence generally requires a frequency source which can be set to within a few Hertz of a desired frequency. The HP 3780A Pattern Generator / Error Detector has an option which allows the user to adjust the output clock frequency with great accuracy to frequencies within 50ppm of 1.544MHz. This clock can be used to externally clock a jitter generator, another pattern generator, or to simply vary the frequency at which the HP 3780A outputs a data pattern.

Verify that the receiver will readily acquire lock on to a data stream which is presented while the receiver is in a "loss of signal" state. This test will show how well the receiver locks on to a T1 signal when it is first input, or recovers from momentary interruption in the signal. Also see if the receiver will false lock when initially presented with a data pattern with low ones density such as a 1 of 8 or 1 of 16 pattern. A good design should

immediately lock on to any valid input signal, even one with low ones density.

When characterizing jitter transfer and generated jitter performance, it is wise to observe the output clock of the jitter attenuator in the time domain using an oscilloscope or a Frequency and Time Interval Analyzer like the HP 5372A. With a fast analog oscilloscope, this can be done by triggering the oscilloscope with the jitter free clock source, and observing edges of the jitter attenuated clock in the 1 ns to 5 ns time domain. Observations on a spectrum analyzer focus only on a narrow bandwidth. Anomalies created by the jitter attenuator that may appear at other frequencies would go unnoticed on the spectrum analyzer but the oscilloscope might indicate that more jitter is present. For example if input jitter of 0.3 UI is attenuated by 60dB, the output jitter should be 0.003 UI, which corresponds to about 2ns of time domain jitter. If the oscilloscope indicates something different, further investigation is warranted.

For loop-timed applications, it may also be important to evaluate the receiver's loss-of-signal, LOS, response. Check the receive circuit's LOS criteria: how many consecutive zeros, or how much pulse amplitude decay before LOS is declared? More importantly, test the circuit's recovered clock output. The recovered clock should smoothly transition to a reference clock when LOS is declared to ensure that no anomalies propagate to the system's backplane timing.

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