

P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^{a, e}	Q_g (Typ.)
- 20	0.100 at $V_{GS} = - 4.5$ V	- 3.7	9.5 nC
	0.118 at $V_{GS} = - 2.5$ V	- 3.4	
	0.140 at $V_{GS} = - 1.8$ V	- 3.1	
	0.205 at $V_{GS} = - 1.5$ V	- 2	

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- Compliant to RoHS Directive 2002/95/EC



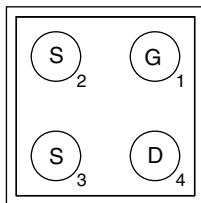
RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

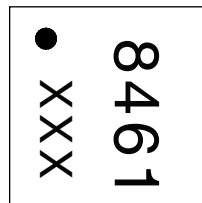
- Load Switch
- Battery Switch
- Charger Switch

MICRO FOOT

Bump Side View

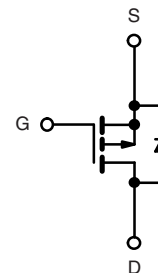


Backside View



Device Marking: 8461

xxx = Date/Lot Traceability Code



P-Channel MOSFET

Ordering Information: Si8461DB-T2-E1 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 20	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_A = 25$ °C	- 3.7 ^a
		$T_A = 70$ °C	- 3 ^a
		$T_A = 25$ °C	- 2.5 ^b
		$T_A = 70$ °C	- 1.9 ^b
Pulsed Drain Current	I_{DM}	- 20	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	
		$T_A = 25$ °C	- 0.65 ^b
Maximum Power Dissipation	P_D	$T_A = 25$ °C	1.8 ^a
		$T_A = 70$ °C	1.1 ^a
		$T_A = 25$ °C	0.78 ^b
		$T_A = 70$ °C	0.5 ^b
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Package Reflow Conditions ^c	VPR	260	
	IR/Convection	260	

Notes:

- Surface mounted on 1" x 1" FR4 board with full copper, $t = 10$ s.
- Surface mounted on 1" x 1" FR4 board with minimum copper, $t = 10$ s.
- Refer to IPC/JEDEC (J-STD-020C), no manual or hand soldering.
- In this document, any reference to case represents the body of the MICRO FOOT device and foot is the bump.
- Based on $T_A = 25$ °C.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	t = 10 s	R _{thJA}	55	70	°C/W
Maximum Junction-to-Ambient ^{c, d}	t = 10 s		125	160	

Notes:

- a. Surface mounted on 1" x 1" FR4 board with full copper.
b. Maximum under steady state conditions is 100 °C/W.
c. Surface mounted on 1" x 1" FR4 board with minimum copper.
d. Maximum under steady state conditions is 190 °C/W.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 20			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 12		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J		2.5			
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 0.4		- 1.0	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 20 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 20 V, V _{GS} = 0 V, T _J = 70 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ - 5 V, V _{GS} = - 4.5 V	- 10			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 1.5 A		0.083	0.100	Ω
		V _{GS} = - 2.5 V, I _D = - 1.5 A		0.098	0.118	
		V _{GS} = - 1.8 V, I _D = - 1 A		0.115	0.140	
		V _{GS} = - 1.5 V, I _D = - 0.5 A		0.136	0.205	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 10 V, I _D = - 1 A		7		S
Dynamic^b						
Input Capacitance	C _{iss}	V _{DS} = - 10 V, V _{GS} = 0 V, f = 1 MHz		610		pF
Output Capacitance	C _{oss}		120			
Reverse Transfer Capacitance	C _{rss}		95			
Total Gate Charge	Q _g	V _{DS} = - 10 V, V _{GS} = - 8 V, I _D = - 1 A		16	24	nC
				9.5	15	
Gate-Source Charge	Q _{gs}	V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = 1 A		0.9		
Gate-Drain Charge	Q _{gd}		2.6			
Gate Resistance	R _g	V _{GS} = - 0.1 V, f = 1 MHz		6.5		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 10 V, R _L = 10 Ω I _D ≅ - 1 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		15	25	ns
Rise Time	t _r		25	40		
Turn-Off Delay Time	t _{d(off)}		35	55		
Fall Time	t _f		10	15		
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 10 V, R _L = 10 Ω I _D ≅ - 1 A, V _{GEN} = - 8 V, R _g = 1 Ω		7	15	
Rise Time	t _r		12	20		
Turn-Off Delay Time	t _{d(off)}		32	50		
Fall Time	t _f		12	20		



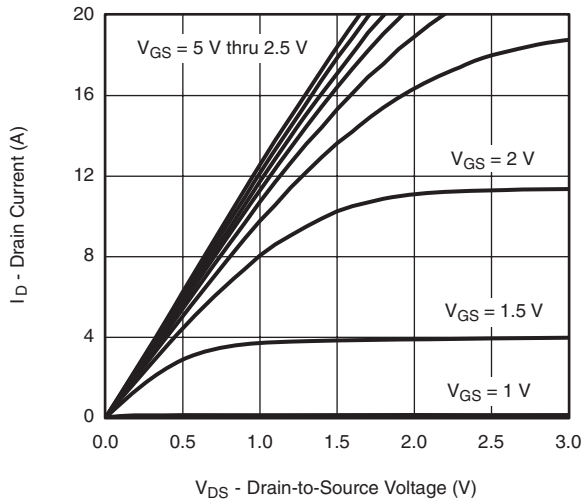
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_A = 25\text{ }^\circ\text{C}$			- 1.5	A
Pulse Diode Forward Current	I_{SM}				- 20	
Body Diode Voltage	V_{SD}	$I_S = - 1\text{ A}, V_{GS} = 0\text{ V}$		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = - 1\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		15	30	ns
Body Diode Reverse Recovery Charge	Q_{rr}			10	20	nC
Reverse Recovery Fall Time	t_a			9		ns
Reverse Recovery Rise Time	t_b			6		

Notes:

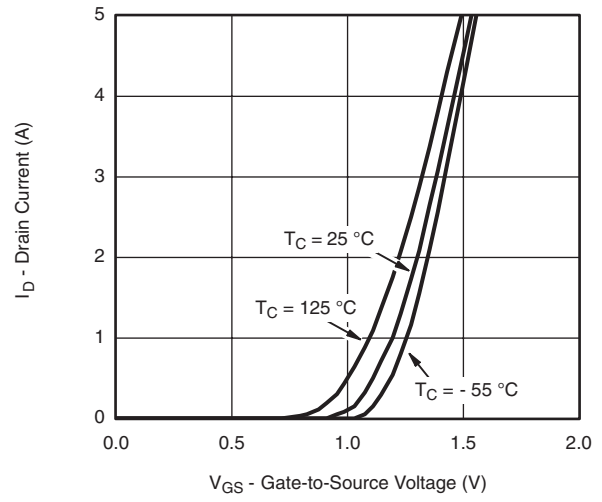
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

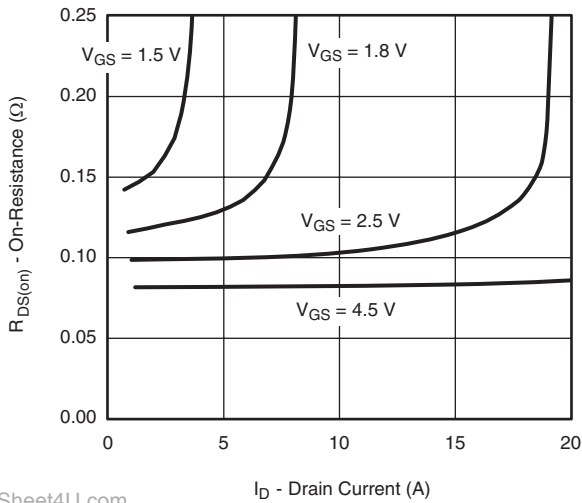
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



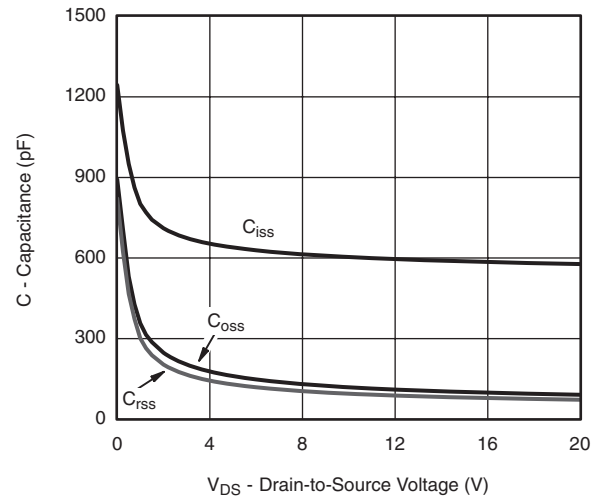
Output Characteristics



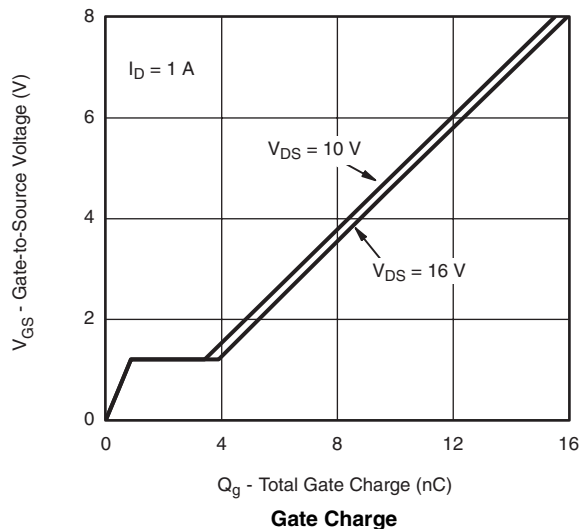
Transfer Characteristics



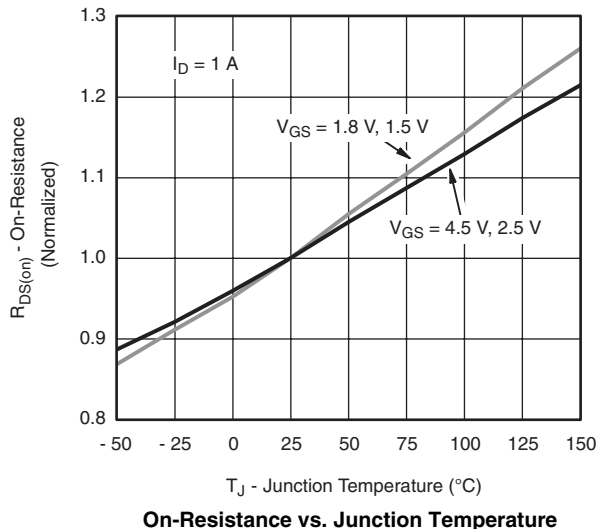
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



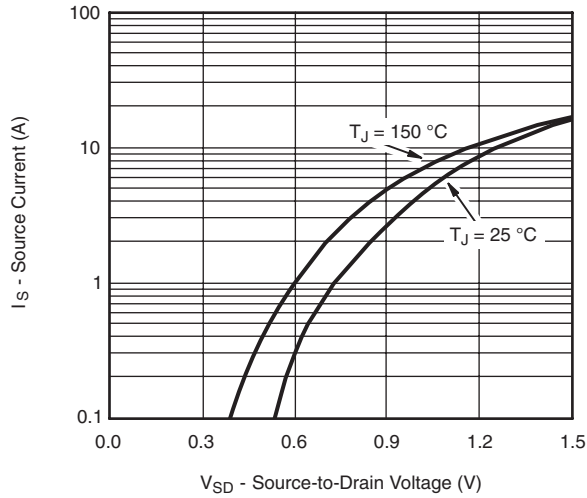
Gate Charge



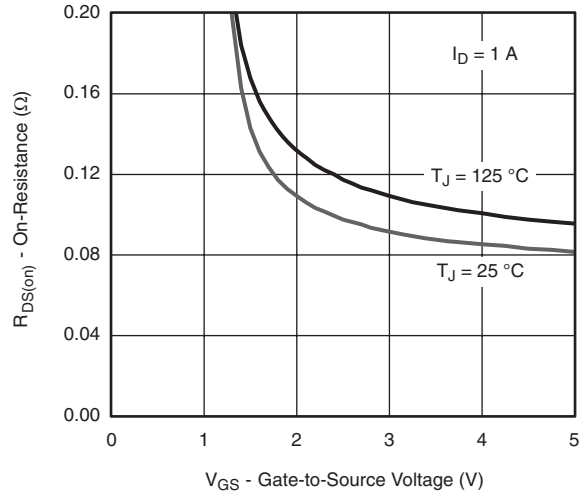
On-Resistance vs. Junction Temperature

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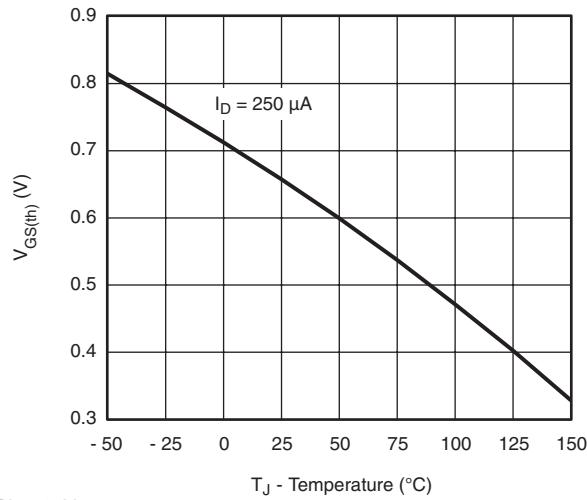
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



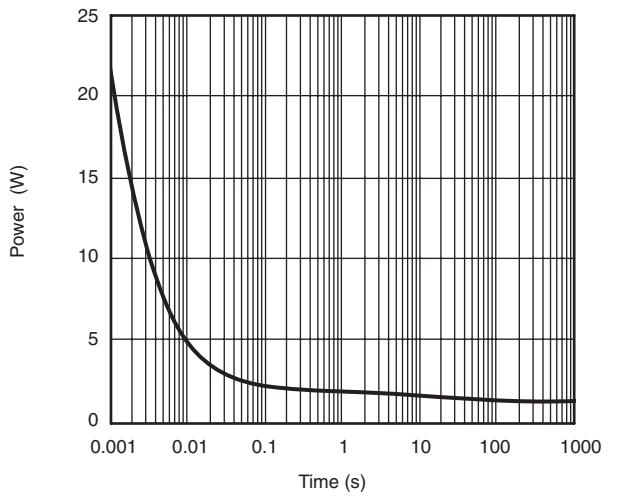
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

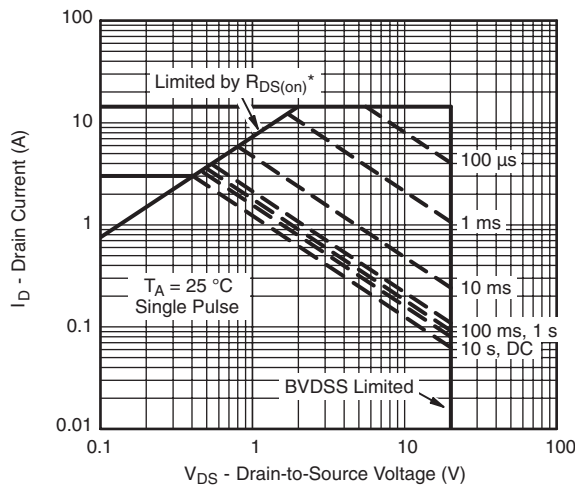


Threshold Voltage



Single Pulse Power, Junction-to-Ambient

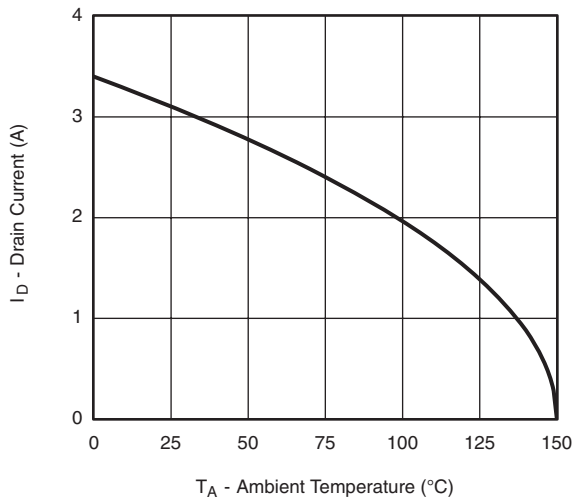
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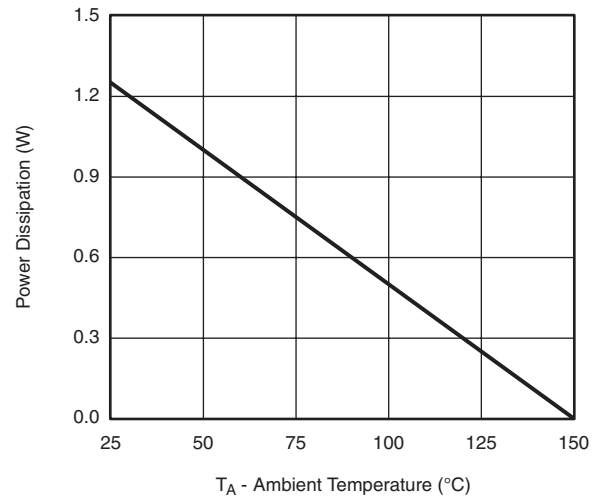
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



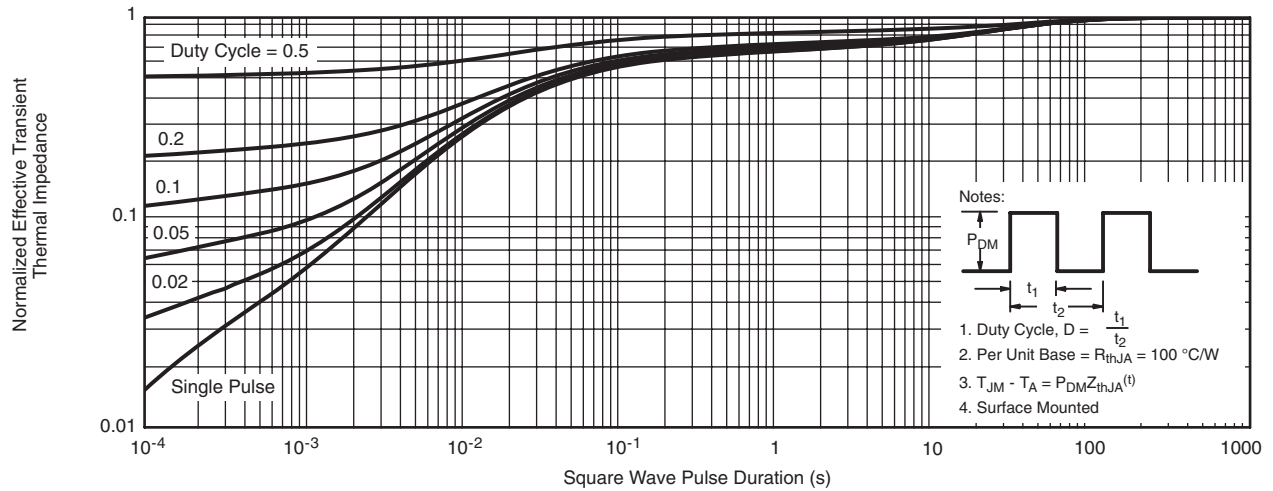
Power Derating

Note:

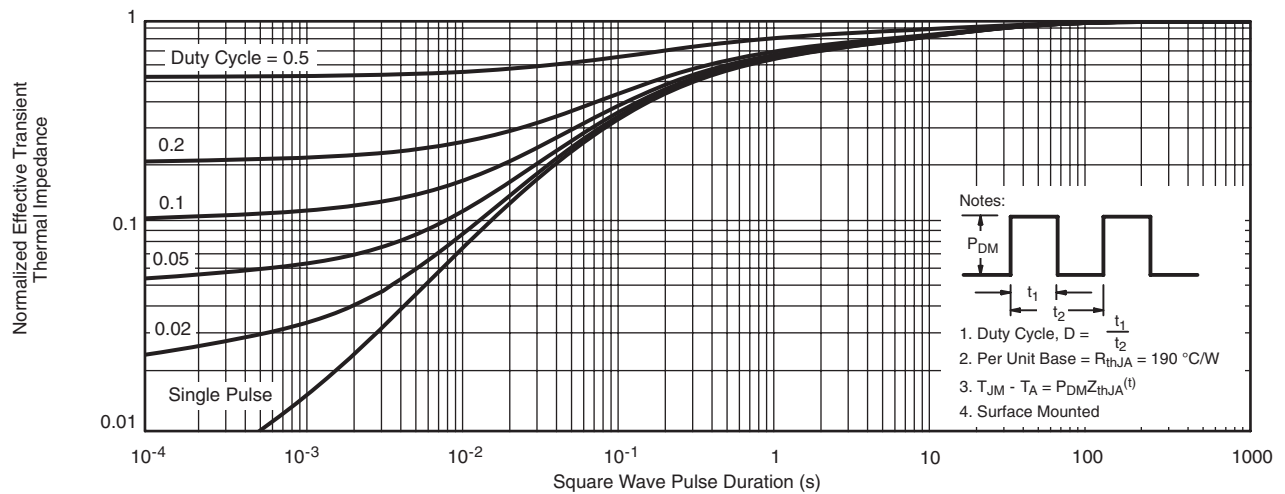
When Mounted on 1" x 1" FR4 with Full Copper.

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



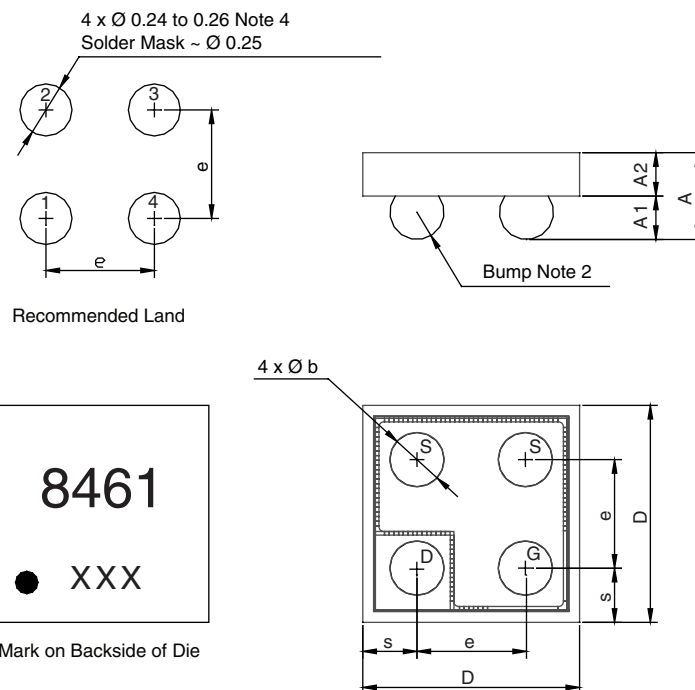
Normalized Thermal Transient Impedance, Junction-to-Ambient (1" x 1" FR4 Board with Full Copper)



Normalized Thermal Transient Impedance, Junction-to-Ambient (1" x 1" FR4 Board with Minimum Copper)

PACKAGE OUTLINE

MICRO FOOT: 4-BUMP (2 x 2, 0.5 mm PITCH)



Notes (Unless otherwise specified):

1. All dimensions are in millimeters.
2. Four (4) solder bumps are lead (Pb)-free 95.5Sn/3.8Ag/0.7Cu with diameter $\text{Ø } 0.30 \text{ mm to } 0.32 \text{ mm}$.
3. Backside surface is coated with a Ti/Ni/Ag layer.
4. Non-solder mask defined copper landing pad.
5. • is location of pin 1.

Dim.	Millimeters ^a			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.462	0.505	0.548	0.0181	0.0198	0.0215
A ₁	0.220	0.250	0.280	0.0086	0.0098	0.0110
A ₂	0.242	0.255	0.268	0.0095	0.0100	0.0105
b	0.300	0.310	0.320	0.0118	0.0122	0.0126
e	0.500			0.0197		
s	0.230	0.250	0.270	0.0090	0.0098	0.0106
D	0.920	0.960	1.000	0.0362	0.0378	0.0394

Notes:

- a. Use millimeters as the primary measurement.

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