

# 4/3/2/1-Phase PWM Controller for High-Density Power Supply

## General Description

The RT8841 is a 4/3/2/1-phase synchronous buck controller with 2 integrated MOSFET drivers for VR11 CPU power application. RT8841 uses differential inductor DCR current sense to achieve phase current balance and active voltage positioning. Other features include adjustable operating frequency, adjustable soft start, power good indication, external error-amp compensation, over voltage protection, over current protection and enable/shutdown for various applications. RT8841 comes to a small footprint with WQFN-40L 6x6 package

## Applications

- Desktop CPU Core Power
- Low Voltage, High Current DC/DC Converter

## Ordering Information

RT8841 □ □

- Package Type  
QW : WQFN-40L 6x6 (W-Type)
- Operating Temperature Range  
P : Pb Free with Commercial Standard  
G : Green (Halogen Free with Commercial Standard)

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### Note:

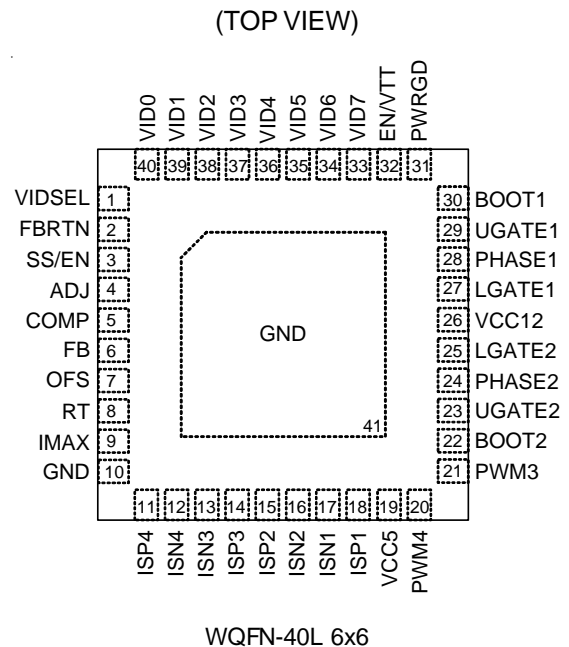
Richtek Pb-free and Green products are :

- ▶RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶Suitable for use in SnPb or Pb-free soldering processes.
- ▶100% matte tin (Sn) plating.

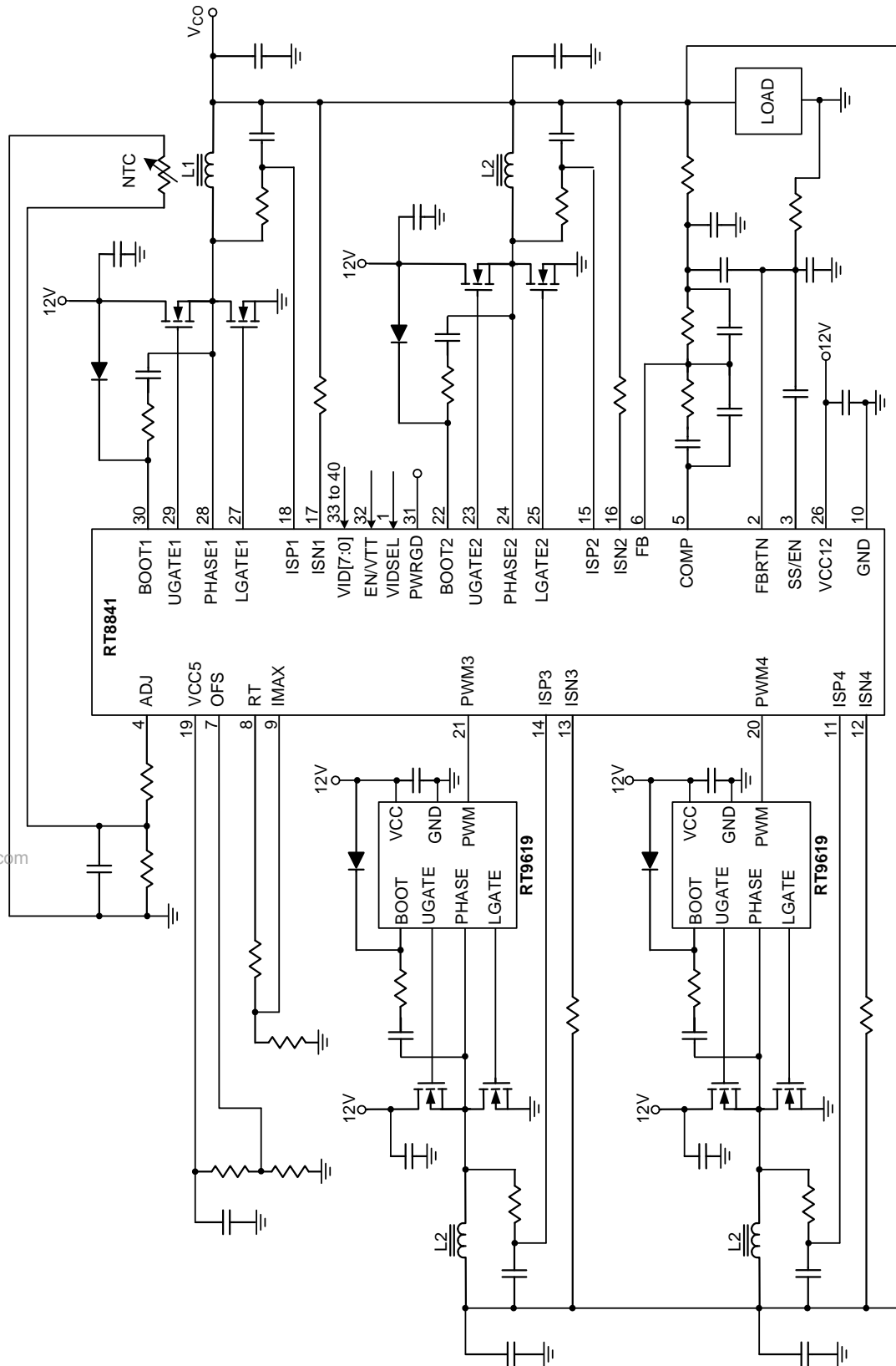
## Features

- 12V Power Supply Voltage
- 4/3/2/1-Phase Power Conversion
- 2 Embedded MOSFET Drivers
- Internal Regulated 5V Output
- VID Tables for Intel VRD11/VRD10.x and AMD K8, K8\_M2 CPUs
- Continuous Differential Inductor DCR Current Sense
- Adjustable Soft Start
- Adjustable Frequency
- Power Good Indication
- Adjustable Over Current Protection
- Over Voltage Protection
- Small 40-Lead WQFN Package
- RoHS Compliant and 100% Lead(Pb)-Free

## Pin Configurations



Typical Application Circuit



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**Table 1. Output Voltage Program (VRD10.x + VID6)**

Pin Name							Nominal Output Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	VID5	VID6	
0	1	0	1	0	1	1	1.60000V
0	1	0	1	0	1	0	1.59375V
0	1	0	1	1	0	1	1.58750V
0	1	0	1	1	0	0	1.58125V
0	1	0	1	1	1	1	1.57500V
0	1	0	1	1	1	0	1.56875V
0	1	1	0	0	0	1	1.56250V
0	1	1	0	0	0	0	1.55625V
0	1	1	0	0	1	1	1.55000V
0	1	1	0	0	1	0	1.54375V
0	1	1	0	1	0	1	1.53750V
0	1	1	0	1	0	0	1.53125V
0	1	1	0	1	1	1	1.52500V
0	1	1	0	1	1	0	1.51875V
0	1	1	1	0	0	1	1.51250V
0	1	1	1	0	0	0	1.50625V
0	1	1	1	0	1	1	1.50000V
0	1	1	1	0	1	0	1.49375V
0	1	1	1	1	0	1	1.48750V
0	1	1	1	1	0	0	1.48125V
0	1	1	1	1	1	1	1.47500V
0	1	1	1	1	1	0	1.46875V
1	0	0	0	0	0	1	1.46250V
1	0	0	0	0	0	0	1.45625V
1	0	0	0	0	1	1	1.45000V
1	0	0	0	0	1	0	1.44375V
1	0	0	0	1	0	1	1.43750V
1	0	0	0	1	0	0	1.43125V
1	0	0	0	1	1	1	1.42500V
1	0	0	0	1	1	0	1.41875V
1	0	0	1	0	0	1	1.41250V
1	0	0	1	0	0	0	1.40625V
1	0	0	1	0	1	1	1.40000V
1	0	0	1	0	1	0	1.39375V
1	0	0	1	1	0	1	1.38750V
1	0	0	1	1	0	0	1.38125V
1	0	0	1	1	1	1	1.37500V
1	0	0	1	1	1	0	1.36875V
1	0	1	0	0	0	1	1.36250V

To be continued

Table 1. Output Voltage Program (VRD10.x + VID6)

Pin Name							Nominal Output Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	VID5	VID6	
1	0	1	0	0	0	0	1.35625V
1	0	1	0	0	1	1	1.35000V
1	0	1	0	0	1	0	1.34375V
1	0	1	0	1	0	1	1.33750V
1	0	1	0	1	0	0	1.33125V
1	0	1	0	1	1	1	1.32500V
1	0	1	0	1	1	0	1.31875V
1	0	1	1	0	0	1	1.31250V
1	0	1	1	0	0	0	1.30625V
1	0	1	1	0	1	1	1.30000V
1	0	1	1	0	1	0	1.29375V
1	0	1	1	1	0	1	1.28750V
1	0	1	1	1	0	0	1.28125V
1	0	1	1	1	1	1	1.27500V
1	0	1	1	1	1	0	1.26875V
1	1	0	0	0	0	1	1.26250V
1	1	0	0	0	0	0	1.25625V
1	1	0	0	0	1	1	1.25000V
1	1	0	0	0	1	0	1.24375V
1	1	0	0	1	0	1	1.23750V
1	1	0	0	1	0	0	1.23125V
1	1	0	0	1	1	1	1.22500V
1	1	0	0	1	1	0	1.21875V
1	1	0	1	0	0	1	1.21250V
1	1	0	1	0	0	0	1.20625V
1	1	0	1	0	1	1	1.20000V
1	1	0	1	0	1	0	1.19375V
1	1	0	1	1	0	1	1.18750V
1	1	0	1	1	0	0	1.18125V
1	1	0	1	1	1	1	1.17500V
1	1	0	1	1	1	0	1.16875V
1	1	1	0	0	0	1	1.16250V
1	1	1	0	0	0	0	1,15625V
1	1	1	0	0	1	1	1.15000V
1	1	1	0	0	1	0	1.14375V
1	1	1	0	1	0	1	1.13750V
1	1	1	0	1	0	0	1.13125V
1	1	1	0	1	1	1	1.12500V
1	1	1	0	1	1	0	1.11875V

To be continued

**Table 1. Output Voltage Program (VRD10.x + VID6)**

Pin Name							Nominal Output Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	VID5	VID6	
1	1	1	1	0	0	1	1.11250V
1	1	1	1	0	0	0	1.10625V
1	1	1	1	0	1	1	1.10000V
1	1	1	1	0	1	0	1.09375V
1	1	1	1	1	0	1	OFF
1	1	1	1	1	0	0	OFF
1	1	1	1	1	1	1	OFF
1	1	1	1	1	1	0	OFF
0	0	0	0	0	0	1	1.08750V
0	0	0	0	0	0	0	1.08125V
0	0	0	0	0	1	1	1.07500V
0	0	0	0	0	1	0	1.06875V
0	0	0	0	1	0	1	1.06250V
0	0	0	0	1	0	0	1.05625V
0	0	0	0	1	1	1	1.05000V
0	0	0	0	1	1	0	1.04375V
0	0	0	1	0	0	1	1.03750V
0	0	0	1	0	0	0	1.03125V
0	0	0	1	0	1	1	1.02500V
0	0	0	1	0	1	0	1.01875V
0	0	0	1	1	0	1	1.01250V
0	0	0	1	1	0	0	1.00625V
0	0	0	1	1	1	1	1.00000V
0	0	0	1	1	1	0	0.99375V
0	0	1	0	0	0	1	0.98750V
0	0	1	0	0	0	0	0.98125V
0	0	1	0	0	1	1	0.97500V
0	0	1	0	0	1	0	0.96875V
0	0	1	0	1	0	1	0.96250V
0	0	1	0	1	0	0	0.95625V
0	0	1	0	1	1	1	0.95000V
0	0	1	0	1	1	0	0.94375V
0	0	1	1	0	0	1	0.93750V
0	0	1	1	0	0	0	0.93125V
0	0	1	1	0	1	1	0.92500V
0	0	1	1	0	1	0	0.91875V
0	0	1	1	1	0	1	0.91250V
0	0	1	1	1	0	0	0.90625V
0	0	1	1	1	1	1	0.90000V

To be continued

Table 1. Output Voltage Program (VRD10.x + VID6)

Pin Name							Nominal Output Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	VID5	VID6	
0	0	1	1	1	1	0	0.89375V
0	1	0	0	0	0	1	0.88750V
0	1	0	0	0	0	0	0.88125V
0	1	0	0	0	1	1	0.87500V
0	1	0	0	0	1	0	0.86875V
0	1	0	0	1	0	1	0.86250V
0	1	0	0	1	0	0	0.85625V
0	1	0	0	1	1	1	0.85000V
0	1	0	0	1	1	0	0.84375V
0	1	0	1	0	0	1	0.83750V
0	1	0	1	0	0	0	0.83125V

**Table 2. Output Voltage Program (VRD11)**

Pin Name	Nominal Output Voltage
HEX	DACOUT
00	OFF
01	OFF
02	1.60000V
03	1.59375V
04	1.58750V
05	1.58125V
06	1.57500V
07	1.56875V
08	1.56250V
09	1.55625V
0A	1.55000V
0B	1.54375V
0C	1.53750V
0D	1.53125V
0E	1.52500V
0F	1.51875V
10	1.51250V
11	1.50625V
12	1.50000V
13	1.49375V
14	1.48750V
15	1.48125V
16	1.47500V
17	1.46875V
18	1.46250V
19	1.45625V
1A	1.45000V
1B	1.44375V
1C	1.43750V
1D	1.43125V
1E	1.42500V
1F	1.41875V
20	1.41250V
21	1.40625V
22	1.40000V
23	1.39375V
24	1.38750V
25	1.38125V
26	1.37500V

Pin Name	Nominal Output Voltage DACOUT
HEX	
27	1.36875V
28	1.36250V
29	1.35625V
2A	1.35000V
2B	1.34375V
2C	1.33750V
2D	1.33125V
2E	1.32500V
2F	1.31875V
30	1.31250V
31	1.30625V
32	1.30000V
33	1.29375V
34	1.28750V
35	1.28125V
36	1.27500V
37	1.26875V
38	1.26250V
39	1.25625V
3A	1.25000V
3B	1.24375V
3C	1.23750V
3D	1.23125V
3E	1.22500V
3F	1.21875V
40	1.21250V
41	1.20625V
42	1.20000V
43	1.19375V
44	1.18750V
45	1.18125V
46	1.17500V
47	1.16875V
48	1.16250V
49	1.15625V
4A	1.15000V
4B	1.14375V
4C	1.13750V
4D	1.13125V

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*To be continued*

Table 2. Output Voltage Program (VRD11)

Pin Name	Nominal Output Voltage DACOUT
HEX	
4E	1.12500V
4F	1.11875V
50	1.11250V
51	1.10625V
52	1.10000V
53	1.09375V
54	1.08750V
55	1.08125V
56	1.07500V
57	1.06875V
58	1.06250V
59	1.05625V
5A	1.05000V
5B	1.04375V
5C	1.03750V
5D	1.03125V
5E	1.02500V
5F	1.01875V
60	1.01250V
61	1.00625V
62	1.00000V
63	0.99375V
64	0.98750V
65	0.98125V
66	0.97500V
67	0.96875V
68	0.96250V
69	0.95625V
6A	0.95000V
6B	0.94375V
6C	0.93750V
6D	0.93125V
6E	0.92500V
6F	0.91875V
70	0.91250V
71	0.90625V
72	0.90000V
73	0.89375V
74	0.88750V

Pin Name	Nominal Output Voltage DACOUT
HEX	
75	0.88125V
76	0.87500V
77	0.86875V
78	0.86250V
79	0.85625V
7A	0.85000V
7B	0.84375V
7C	0.83750V
7D	0.83125V
7E	0.82500V
7F	0.81875V
80	0.81250V
81	0.80625V
82	0.80000V
83	0.79375V
84	0.78750V
85	0.78125V
86	0.77500V
87	0.76875V
88	0.76250V
89	0.75625V
8A	0.75000V
8B	0.74375V
8C	0.73750V
8D	0.73125V
8E	0.72500V
8F	0.71875V
90	0.71250V
91	0.70625V
92	0.70000V
93	0.69375V
94	0.68750V
95	0.68125V
96	0.67500V
97	0.66875V
98	0.66250V
99	0.65625V
9A	0.65000V
9B	0.64375V

To be continued



**Table 2. Output Voltage Program (VRD11)**

Pin Name	Nominal Output Voltage DACOUT
HEX	
9C	0.63750V
9D	0.63125V
9E	0.62500V
9F	0.61875V
A0	0.61250V
A1	0.60625V
A2	0.60000V
A3	0.59375V
A4	0.58750V
A5	0.58125V
A6	0.57500V
A7	0.56875V
A8	0.56250V
A9	0.55625V
AA	0.55000V
AB	0.54375V
AC	0.53750V
AD	0.53125V
AE	0.52500V
AF	0.51875V
B0	0.51250V
B1	0.50625V
B2	0.50000V
B3	X
B4	X
B5	X
B6	X
B7	X
B8	X
B9	X
BA	X
BB	X
BC	X
BD	X
BE	X
BF	X
C0	X
C1	X
C2	X

Pin Name	Nominal Output Voltage DACOUT
HEX	
C3	X
C4	X
C5	X
C6	X
C7	X
C8	X
C9	X
CA	X
CB	X
CC	X
CD	X
CE	X
CF	X
D0	X
D1	X
D2	X
D3	X
D4	X
D5	X
D6	X
D7	X
D8	X
D9	X
DA	X
DB	X
DC	X
DD	X
DE	X
DF	X
E0	X
E1	X
E2	X
E3	X
E4	X
E5	X
E6	X
E7	X
E8	X
E9	X

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*To be continued*

Table 2. Output Voltage Program (VRD11)

Pin Name	Nominal Output Voltage DACOUT
HEX	
EA	X
EB	X
EC	X
ED	X
EE	X
EF	X
F0	X
F1	X
F2	X
F3	X
F4	X
F5	X
F6	X
F7	X
F8	X
F9	X
FA	X
FB	X
FC	X
FD	X
FE	OFF
FF	OFF

Note: (1) 0 : Connected to GND

(2) 1 : Open

(3) X : Don't Care

**Table 3. Output Voltage Program (K8)**

VID4	VID3	VID2	VID1	VID0	Nominal Output Voltage DACOUT
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.200
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

Note: (1) 0 : Connected to GND  
(2) 1 : Open

Table 4. Output Voltage Program (K8\_M2)

Pin Name						Nominal Output Voltage DACOUT
VID5	VID4	VID3	VID2	VID1	VID0	
0	0	0	0	0	0	1.5500
0	0	0	0	0	1	1.5250
0	0	0	0	1	0	1.5000
0	0	0	0	1	1	1.4750
0	0	0	1	0	0	1.4500
0	0	0	1	0	1	1.4250
0	0	0	1	1	0	1.4000
0	0	0	1	1	1	1.3750
0	0	1	0	0	0	1.3500
0	0	1	0	0	1	1.3250
0	0	1	0	1	0	1.3000
0	0	1	0	1	1	1.2750
0	0	1	1	0	0	1.2500
0	0	1	1	0	1	1.2250
0	0	1	1	1	0	1.2000
0	0	1	1	1	1	1.1750
0	1	0	0	0	0	1.1500
0	1	0	0	0	1	1.1250
0	1	0	0	1	0	1.1000
0	1	0	0	1	1	1.0750
0	1	0	1	0	0	1.0500
0	1	0	1	0	1	1.0250
0	1	0	1	1	0	1.0000
0	1	0	1	1	1	0.9750
0	1	1	0	0	0	0.9500
0	1	1	0	0	1	0.9250
0	1	1	0	1	0	0.9000
0	1	1	0	1	1	0.8750
0	1	1	1	0	0	0.8500
0	1	1	1	0	1	0.8250
0	1	1	1	1	0	0.8000
0	1	1	1	1	1	0.7750
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.7500

To be continued

**Table 4. Output Voltage Program (K8\_M2)**

Pin Name						Nominal Output Voltage DACOUT
VID5	VID4	VID3	VID2	VID1	VID0	
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.7250
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7000
1	0	0	1	1	0	0.6875
1	0	0	1	1	1	0.6750
1	0	1	0	0	0	0.6625
1	0	1	0	0	1	0.6500
1	0	1	0	1	0	0.6375
1	0	1	0	1	1	0.6250
1	0	1	1	0	0	0.6125
1	0	1	1	0	1	0.6000
1	0	1	1	1	0	0.5875
1	0	1	1	1	1	0.5750
1	1	0	0	0	0	0.5625
1	1	0	0	0	1	0.5500
1	1	0	0	1	0	0.5375
1	1	0	0	1	1	0.5250
1	1	0	1	0	0	0.5125
1	1	0	1	0	1	0.5000
1	1	0	1	1	0	0.4875
1	1	0	1	1	1	0.4750
1	1	1	0	0	0	0.4625
1	1	1	0	0	1	0.4500
1	1	1	0	1	0	0.4375
1	1	1	0	1	1	0.4250
1	1	1	1	0	0	0.4125
1	1	1	1	0	1	0.4000
1	1	1	1	1	0	0.3875
1	1	1	1	1	1	0.3750

Note: (1) 0 : Connected to GND

(2) 1 : Open

(3) The voltage above are load independent for desktop and server platforms. For mobile platforms the voltage above correspond to zero load current.

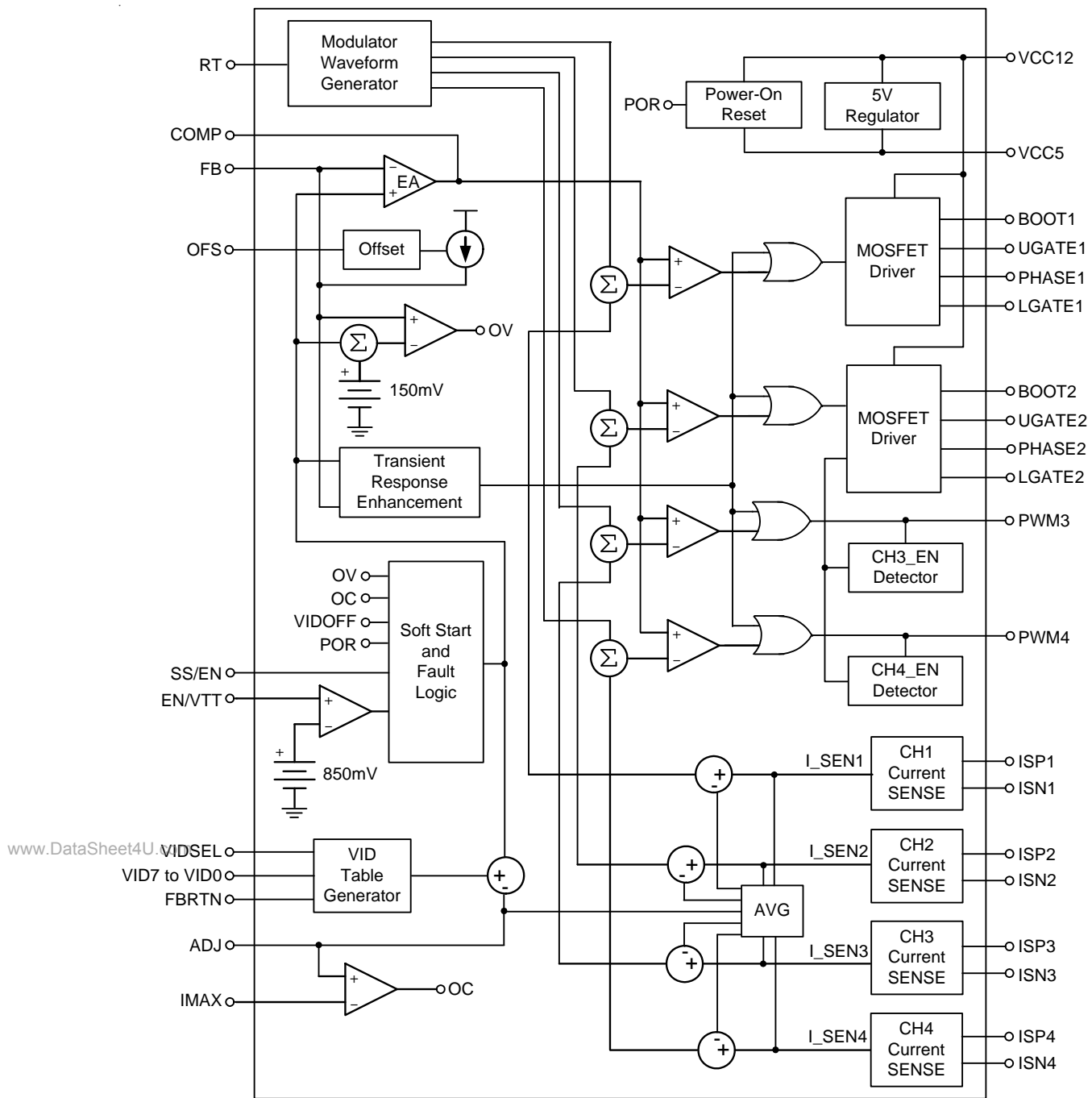
## Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VIDSEL	VID DAC Selection Pin.
2	FBRN	Negative remote sense pin of output voltage.
3	SS/EN	Connect this pin to GND by a capacitor to adjust soft start time. Pull this pin to GND to disable controller.
4	ADJ	Connect this pin to GND by a resistor to set loadline.
5	COMP	Output of error-amp and input of PWM comparator.
6	FB	Inverting input of error-amp.
7	OFS	Connect this pin to GND by a resistor to set no-load offset voltage.
8	RT	Connect this pin to GND by a resistor to adjust frequency.
9	IMAX	Negative input of OCP comparator. (Positive input of OCP comparator is ADJ).
10	GND	Ground Pin
11,14,15,18	ISP4, ISP3, ISP2, ISP1	Positive current sense pin of channel 1, 2, 3 and 4.
12,13,16,17	ISN4, ISN3, ISN2, ISN1	Negative current sense pin of channel 1, 2, 3 and 4.
19	VCC5	Connect this pin to GND by a ceramic cap larger than 1 uF.
20,21	PWM4, PWM3	PWM output for channel 4 and channel 3.
22,30	BOOT2, BOOT1	Bootstrap supply for channel 2 and channel 1.
23,29	UGATE2, UGATE1	Upper gate driver for channel 2 and channel 1.
24,28	PHASE2, PHASE1	Switching node of channel 2 and channel 1.
25,27	LGATE2, LGATE1	Lower gate driver for channel 2 and channel 1.
26	VCC12	IC power supply. Connect to 12V.
31	PWRGD	Power good indicator.
32	EN/VTT	VTT voltage detector input.
33 to 40	VID7 to VID0	Voltage identification input for DAC.
Exposed pad(41)	GND	Exposed pad should be soldered to PCB board and connected to GND.

### VID Table Selection

VIDSEL	VID [7]	Table
VTT	X	VR11
GND	X	VR10.x
VCC5	VTT	K8
VCC5	GND	K8_M2

Function Block Diagram



**Absolute Maximum Ratings** (Note 1)

- Supply Input Voltage ----- -0.3V to 15V
- BOOTx to PHASEx ----- -0.3V to 15V
- BOOTx to GND ----- -0.3V to 30V
- PHASEx to GND ----- -2V to 15V
- Input/Output Voltage ----- -0.3V to 7V
- Power Dissipation, P<sub>D</sub> @ T<sub>A</sub> = 25°C
- WQFN-40L 6x6 ----- 2.778W
- Package Thermal Resistance (Note 4)
- WQFN-40L 6x6, θ<sub>JA</sub> ----- 36°C/W
- Junction Temperature ----- 150°C
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- ESD Susceptibility (Note 2)
- HBM (Human Body Mode) ----- 2kV
- MM (Machine Mode) ----- 200V

**Recommended Operating Conditions** (Note 3)

- Supply Voltage, VCC12 ----- 12V ± 10%
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- 0°C to 70°C

**Electrical Characteristics**

(VCC12 = 12V, V<sub>GND</sub> = 0V, T<sub>A</sub> = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>VCC12 Supply Input</b>						
VCC12 Supply Voltage	V <sub>VCC12</sub>		10.8	12	13.2	V
VCC12 Supply Current	I <sub>CC</sub>		--	6	--	mA
<b>VCC5 power</b>						
VCC5 Supply Voltage	V <sub>VCC5</sub>	I <sub>LOAD</sub> = 10mA	4.75	5.0	5.25	V
VCC5 Output Sourcing	I <sub>VCC5</sub>		20	--	--	mA
<b>Power-On Reset</b>						
VCC12 Rising Threshold	V <sub>VCC12TH</sub>	VCC12 Rising	9.2	9.6	10.0	V
VCC12 Hysteresis	V <sub>VCC12HY</sub>	VCC12 Falling	--	0.9	--	V
VCC5 Rising Threshold	V <sub>VCC5TH</sub>	VCC5 Rising	4.4	4.6	4.8	V
VCC5 Hysteresis	V <sub>VCC5HY</sub>	VCC5 Falling	--	0.4	--	V
<b>Power Monitor</b>						
Power Monitor Maximum Output Voltage			--	1.15	--	V
<b>EN/VTT</b>						
EN/VTT Rising Threshold	V <sub>ENVTT</sub>	EN/VTT Rising	0.80	0.85	0.90	V
Enable Hysteresis	V <sub>ENVTTHY</sub>	EN/VTT Falling	--	100	--	mV
<b>Reference Voltage accuracy</b>						
DAC Accuracy		0.8V to 1.6V	-5	--	+5	mV
		0.5V to 0.8V	-8	--	+8	mV

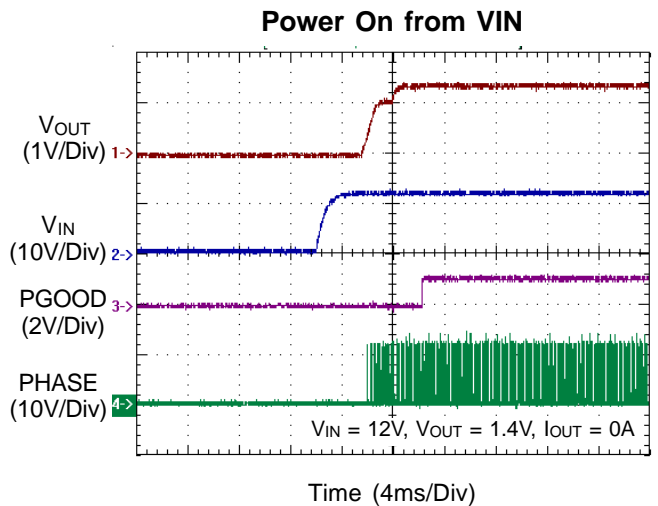
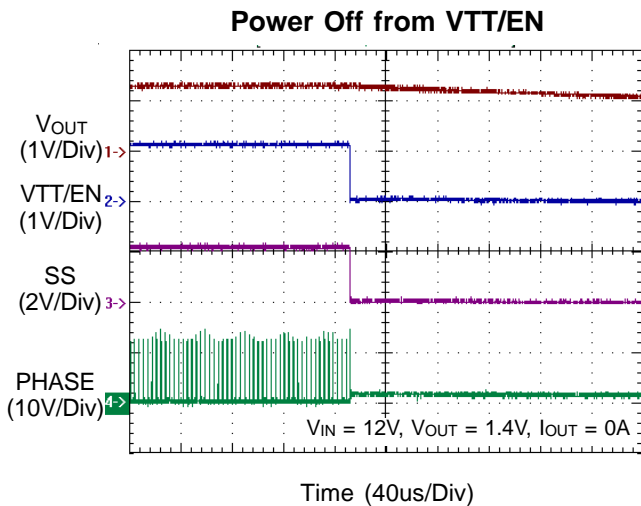
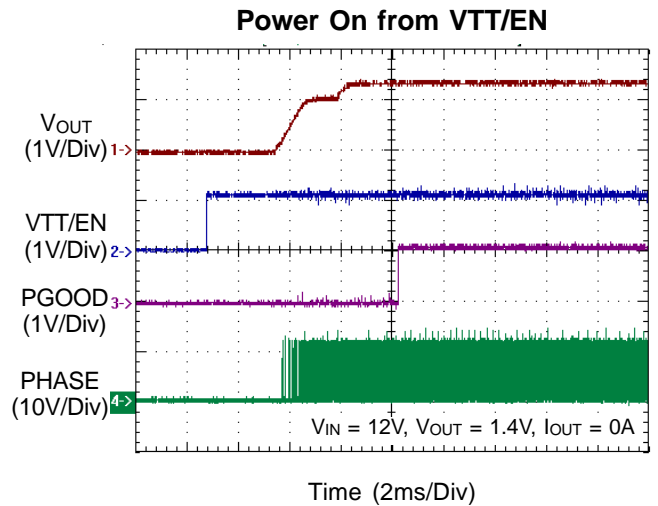
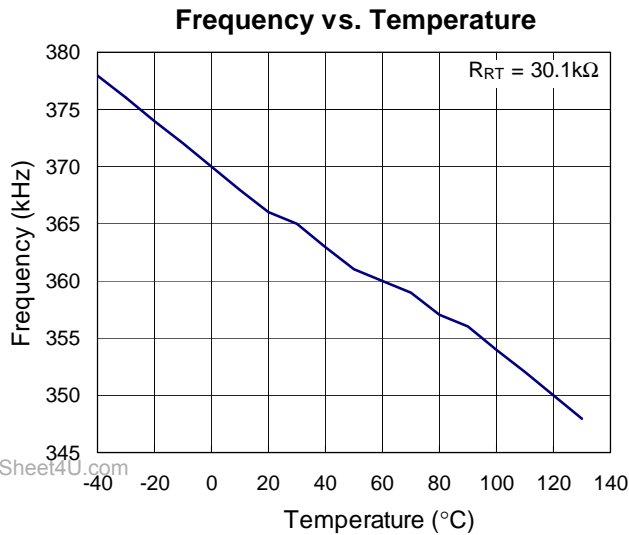
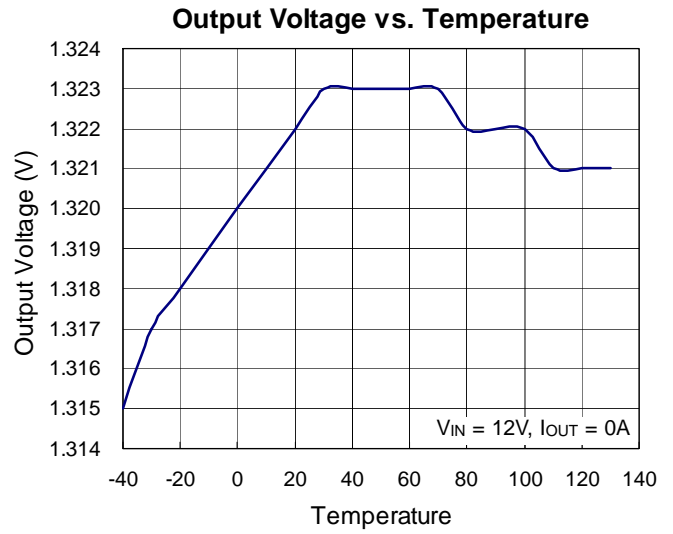
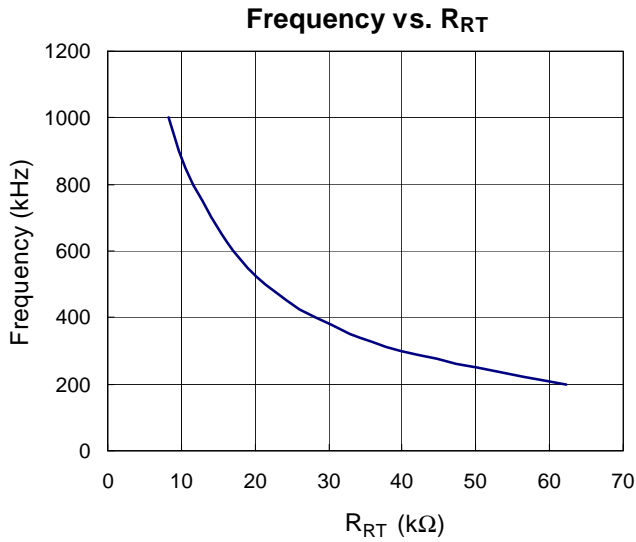
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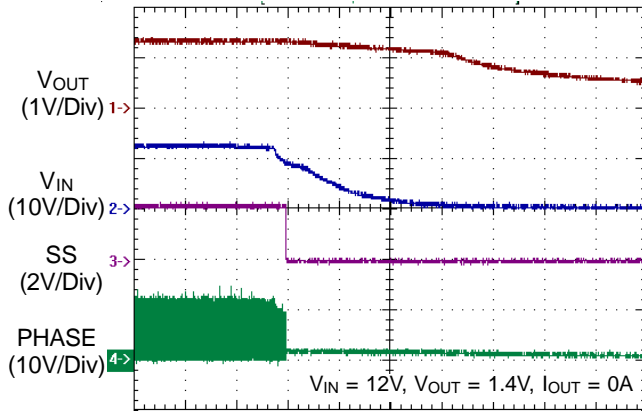
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Error Amplifier</b>						
DC Gain	A <sub>DC</sub>	No Load	--	80	--	dB
Gain-Bandwidth	GBW	C <sub>LOAD</sub> = 10pF	--	10	--	MHz
Slew Rate	SR	C <sub>LOAD</sub> = 10pF	10	--	--	V/μs
Output voltage range	V <sub>COMP</sub>		0.5		3.6	V
Max Current	I <sub>EA_SLEW</sub>	Slew	300	--	--	μA
<b>Power Sequence</b>						
PWRGD Low Voltage	V <sub>PGOOD</sub>	I <sub>PWRGD</sub> = 4mA	--	--	0.4	V
Soft-Start Delay	T <sub>D1</sub>		--	2	--	ms
V <sub>BOOT</sub> Duration	T <sub>D3</sub>		--	0.8	--	ms
PWRGD Delay	T <sub>D5</sub>	Measured the time form V <sub>BOOT</sub> change to PWRGD = 1	--	1.6	--	ms
<b>Current Sense Amplifier</b>						
Max Current	I <sub>GMMAX</sub>	V <sub>CSP</sub> = 1.3V Sink Current from CSN	100	--	--	μA
Input Offset Voltage	V <sub>OCS</sub>		-1	0	1	mV
Running Frequency	f <sub>OSC</sub>	R <sub>RT</sub> = 40kΩ	280	300	320	kHz
RT Pin Voltage	V <sub>RT</sub>	R <sub>RT</sub> = 40kΩ	1.52	1.60	1.68	V
Ramp Amplitude	V <sub>RAMP</sub>	R <sub>RT</sub> = 40kΩ	--	1.60	--	V
<b>Soft Start</b>						
Soft Start Current	I <sub>SS1</sub>	Slew	6	8	10	μA
VID change Current	I <sub>SS2</sub>	Slew	60	80	100	μA
<b>Gate Driver</b>						
UGATE Drive Source	R <sub>UGATEsr</sub>	BOOT – PHASE = 8V 250mA Source Current	--	1	--	Ω
UGATE Drive Sink	R <sub>UGATEsk</sub>	BOOT – PHASE = 8V 250mA Sink Current	--	1	--	Ω
LGATE Drive Source	R <sub>LGATEsr</sub>	V <sub>LGATE</sub> = 8V	--	1	--	Ω
LGATE Drive Sink	R <sub>LGATEsk</sub>	250mA Sink Current	--	0.8	--	Ω
<b>Protection</b>						
Over-Voltage Threshold	V <sub>OVP</sub>	Sweep FB Voltage, V <sub>FB,EAP</sub>	125	150	175	mV
Over-Current Threshold	V <sub>OCP</sub>	Sweep I <sub>MAX</sub> Voltage, V <sub>I<sub>MAX</sub>,ADJ</sub>	-10	0	+10	mV
<b>Dynamic Characteristic</b>						
UGATE Rise Time	t <sub>rUGATE</sub>	C <sub>iss</sub> = 3000p	--	15	--	ns
UGATE Fall Time	t <sub>fUGATE</sub>		--	10	--	ns
LGATE Rise Time	t <sub>rLGATE</sub>		--	15	--	ns
LGATE Fall Time	t <sub>fLGATE</sub>		--	10	--	ns

- Note 1.** Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.
- Note 2.** Devices are ESD sensitive. Handling precaution recommended.
- Note 3.** The device is not guaranteed to function outside its operating conditions.
- Note 4.**  $\theta_{JA}$  is measured in the natural convection at  $T_A = 25^\circ\text{C}$  on a effective single layer thermal conductivity test board of JEDEC thermal measurement standard.

Typical Operating Characteristics

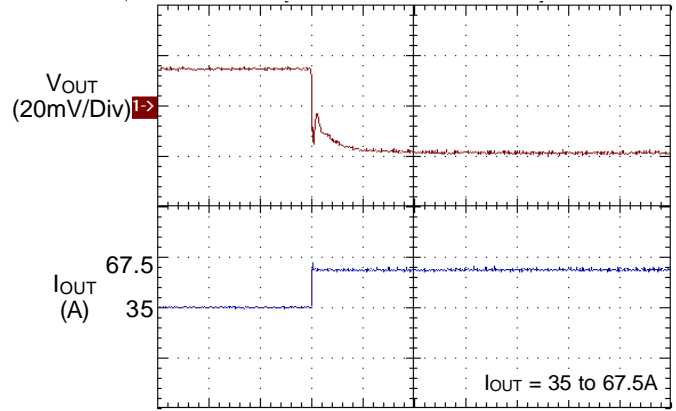


Power Off from VIN



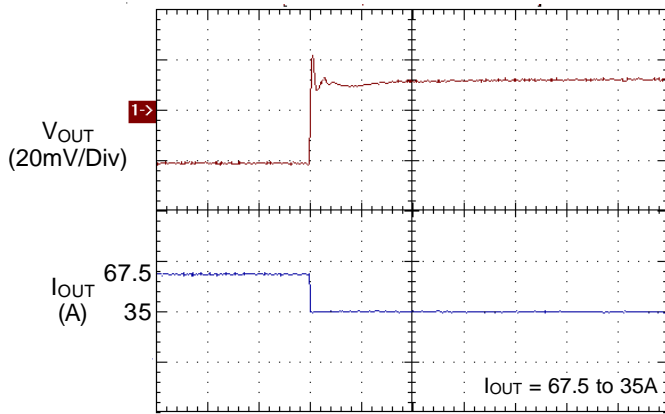
Time (4ms/Div)

ACLL Drop



Time (20us/Div)

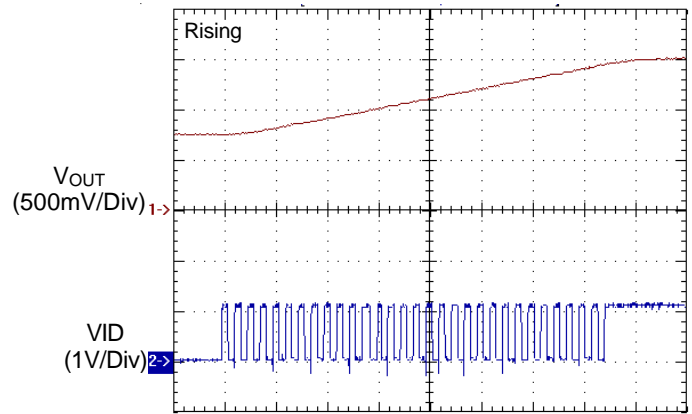
ACLL Overshoot



Time (20us/Div)

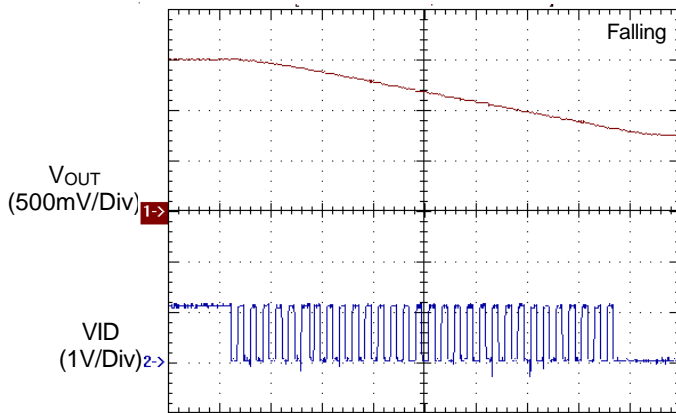
www.DataSheet4U.com

Dynamic VID



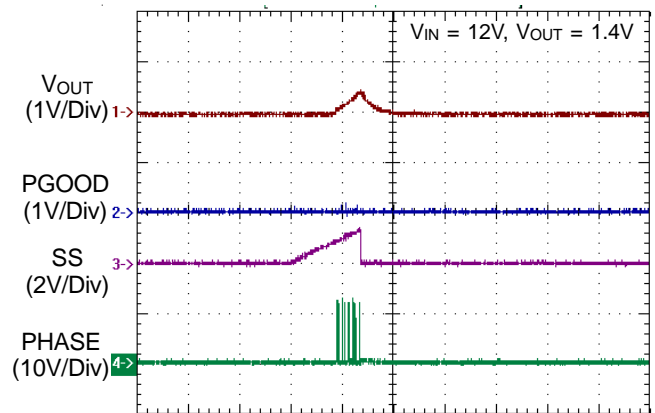
Time (40us/Div)

Dynamic VID



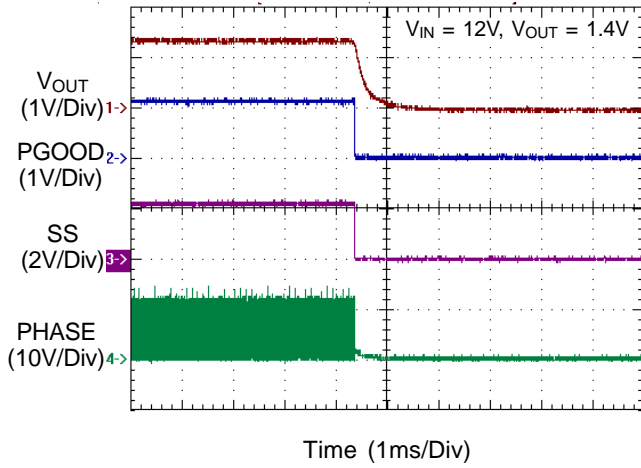
Time (40us/Div)

Output Short then Power On

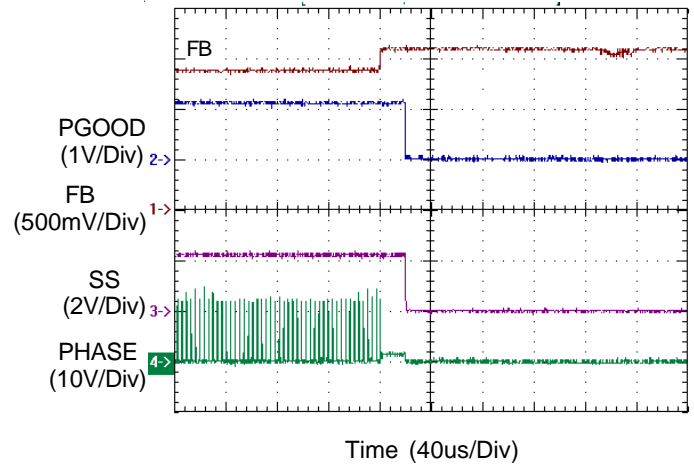


Time (1ms/Div)

Power On then Output Short



OVP



## Application Information

RT8841 is a 4/3/2/1-phase synchronous buck DC/DC converter with 2 embedded MOSFET drivers. The internal VIDDAC is designed to interface with the Intel 8-bit VR11 compatible CPUs.

### Power Ready Detection

During start-up, RT8841 will detect  $V_{CC12}$ ,  $V_{CC5}$  and  $V_{TT}$ . When  $V_{CC12} > 9.6V$ ,  $V_{CC5} > 4.6V$  and  $V_{TT} > 0.85V$  POR will go high. POR (Power On Reset) is the internal signal to indicate all voltage powers are ready to let RT8841 and the companioned MOSFET drivers to work properly. When  $POR = L$ , RT8841 will try to turn off both high side and low side MOSFETs.

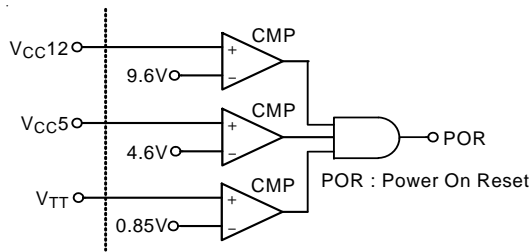


Figure 1. Circuit for Power Ready Detection

### Phase Detection

The number of operational phases is determined by the internal circuitry that monitors the ISN<sub>x</sub> voltages during start up. Normally, the RT8841 operates as a 4-phase PWM controller. Pull ISN<sub>4</sub> and ISP<sub>4</sub> to  $V_{CC5}$  programs 3-phase operation, pull ISN<sub>3</sub> and ISP<sub>3</sub> to  $V_{CC5}$  programs 2-phase operation, and pull ISN<sub>2</sub> and ISP<sub>2</sub> to  $V_{CC5}$  programs 1-phase operation. RT8841 detects the voltage of ISN<sub>4</sub>, ISN<sub>3</sub> and ISN<sub>2</sub> at POR rising edge. At the rising edge, RT8841 detects whether the voltage of ISN<sub>4</sub>, ISN<sub>3</sub> and ISN<sub>2</sub> are higher than " $V_{CC5} - 1V$ " respectively to decide how many phases should be active. Phase detection is only active during start up. When  $POR = H$ , the number of operational phases is determined and latched.

### Phase Switching Frequency

The phase switching frequency of the RT8841 is set by an external resistor connected from the RT pin to GND. The frequency follows the graph in Figure 2.

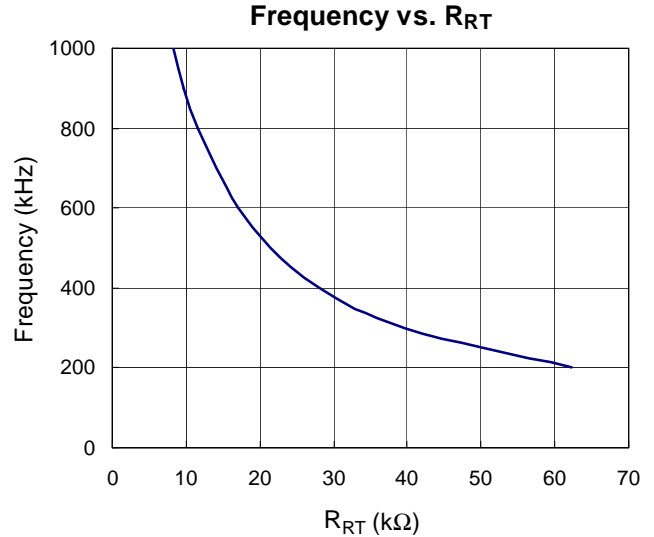


Figure 2.  $R_{RT}$  vs Phase Switching Frequency

### V<sub>DAC</sub> Generator

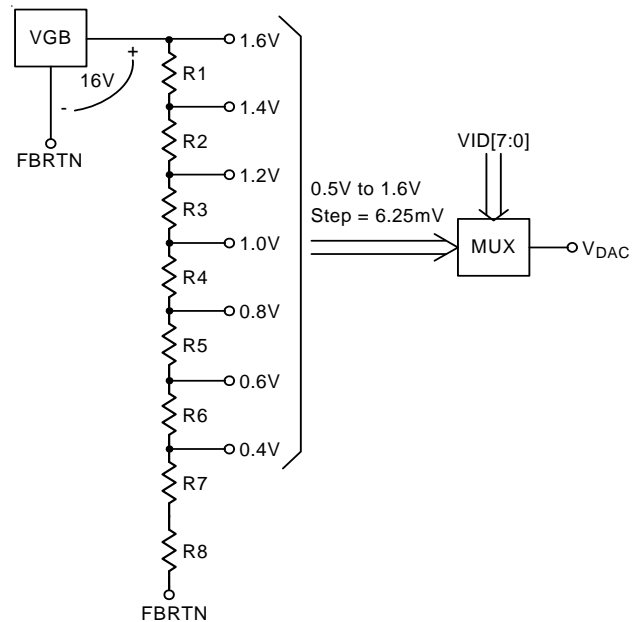


Figure 3.  $V_{DAC}$  Generator Circuit

RT8841 builds a precise bandgap reference circuit inside. The output voltage of bandgap reference is 1.6V referred to FBRTN. In Figure 3, RT8841 uses plural resistors to generate precise reference voltages ranging from 0.5V to 1.6V. All the voltages connect to a multiplexer (MUX). According to the VID inputs, multiplexer outputs the selected voltage,  $V_{DAC}$ . Please be careful that all the voltage values in Figure 3 are referred to FBRTN.

**Soft Start**

Output current of OPSS ( $I_{SS}$ ) is limited and variant

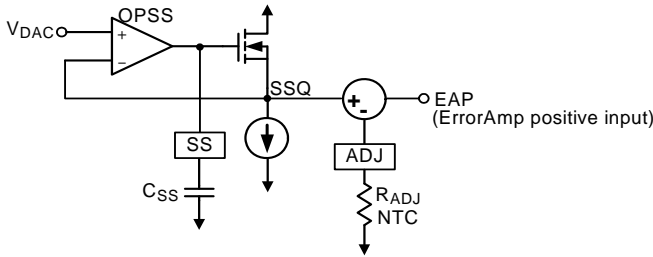


Figure 4. Circuit for Soft Start and Dynamic VID

The  $V_{OUT}$  start-up time is set by a capacitor from the SS pin to GND. In power\_on\_reset state ( $POR = L$ ), the SS pin is held at GND. After power\_on\_reset stae ( $POR = H$ ) and an extra delay 1600 $\mu$ s,  $V_{SS}$  and  $V_{SSQ}$  begin to rise till  $V_{SSQ} = V_{BOOT}$ . When  $V_{SSQ} = V_{BOOT}$ , RT8841 stays in this state for 800 $\mu$ s waiting for valid VID code sent by CPU. After receiving valid VID code,  $V_{OUT}$  continues ramping up or down to the voltage specified by VID code. Before  $PWRGD = H$ , output current of OPSS ( $I_{SS}$ ) is limited to 8 $\mu$ A ( $I_{SS1}$ ). When  $PWRGD = H$ ,  $I_{SS}$  is limited to 80 $\mu$ A ( $I_{SS2}$ ). The soft start waveform is shown in Figure 5.

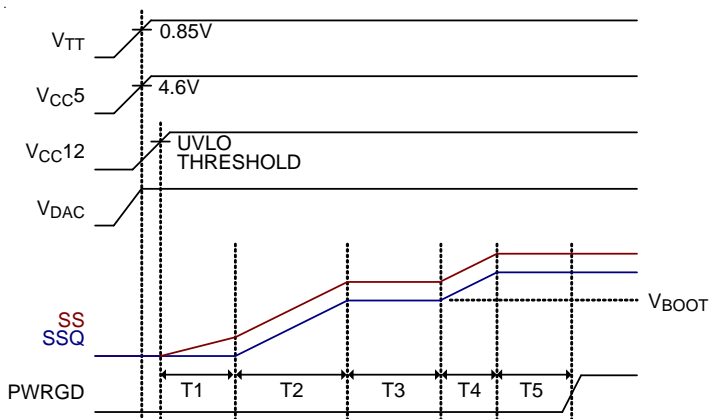


Figure 5. Soft Start Waveforms

$V_{OUT}$  will trace  $V_{EAP}$  which is equal to " $V_{SSQ} - V_{ADJ}$ ".  $V_{ADJ}$  is a small voltage signal which is proportional to  $I_{OUT}$ . This voltage is used to generate loadline and will be described later.  $T1$  is the delay time from power\_on\_reset state to the beginning of  $V_{OUT}$  rising.

$$T1 = 1600\mu s + 0.6V \times C_{SS}/I_{SS1} \tag{1}$$

$T2$  is the soft start time from  $V_{OUT} = 0$  to  $V_{OUT} = V_{BOOT}$ .

$$T2 = V_{BOOT} \times C_{SS}/I_{SS1} \tag{2}$$

$T3$  is the dwelling time for  $V_{OUT} = V_{BOOT}$ .  $T3 = 800\mu s$ .

$T4$  is the soft start time from  $V_{OUT} = V_{BOOT}$  to  $V_{OUT} = V_{DAC}$ .

$$T4 \sim |V_{DAC} - V_{BOOT}| \times C_{SS}/I_{SS1} \tag{3}$$

$T5$  is the power good delay time,  $T5 \sim 1600\mu s$ .

**Dynamic VID**

The RT8841 can accept VID input changing while the controller is running. This allows the output voltage ( $V_{OUT}$ ) to change while the DC/DC converter is running and supplying current to the load. This is commonly referred to as VID on-the-fly (OTF). A VID OTF can occur under either light or heavy load conditions. The CPU changes the VID inputs in multiple steps from the start code to the finish code. This change can be positive or negative. Theoretically,  $V_{OUT}$  should follow  $V_{DAC}$  which is a staircase waveform. In RT8841, as mentioned in soft start session,  $V_{DAC}$  slew rate is limited by  $I_{SS2}/C_{SS}$  when  $PWRGD = H$ . This slew rate limiter works as a low pass filter of  $V_{DAC}$  and makes the bandwidth of  $V_{DAC}$  waveform finite. By smoothing  $V_{DAC}$  staircase waveform,  $V_{OUT}$  will no longer overshoot or undershoot. On the other hand,  $C_{SS}$  will increase the settling time of  $V_{OUT}$  during VID OTF. In most cases, 1nF to 30nF ceramic capacitor is suitable for  $C_{SS}$ .

Output Voltage Differential Sensing

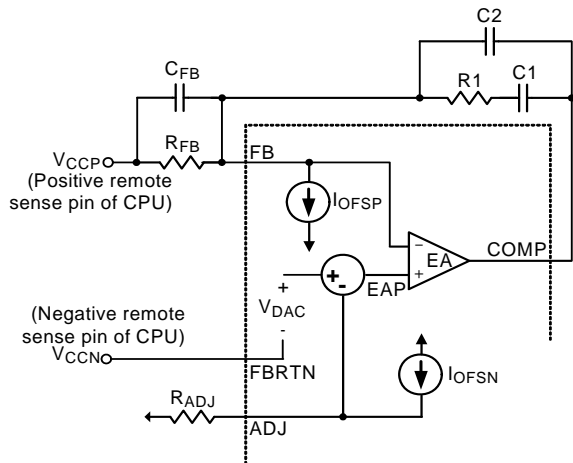


Figure 6. Circuit for V<sub>OUT</sub> Differential Sensing and No Load Offset

The RT8841 uses differential sensing by a high gain low offset ErrorAmp. The CPU voltage is sensed between the FB and FBRTN pins. A resistor (R<sub>FB</sub>) connects FB pin and the positive remote sense pin of the CPU (V<sub>CCP</sub>). FBRTN pin connects to the negative remote sense pin of CPU (V<sub>CCN</sub>) directly. The ErrorAmp compares EAP (= V<sub>DAC</sub> – V<sub>ADJ</sub>) with the V<sub>FB</sub> to regulate the output voltage.

No-Load Offset

In Figure 6, I<sub>OFSN</sub> and I<sub>OFSP</sub> are used to generate no-load offset. Either I<sub>OFSN</sub> or I<sub>OFSP</sub> is active during normal operation. Connect a resistor from OFS pin to GND to activate I<sub>OFSN</sub>. I<sub>OFSN</sub> flows through R<sub>ADJ</sub> from ADJ pin to GND. In this case, negative no-load offset voltage (V<sub>OFSN</sub>) is generated.

$$V_{OFSN} = I_{OFSN} \times R_{ADJ} = 0.8 \times R_{ADJ} / R_{OFS} \quad (4)$$

Connect a resistor from OFS pin to V<sub>CC5</sub> to activate I<sub>OFSP</sub>. I<sub>OFSP</sub> flows through R<sub>FB</sub> from the V<sub>CCP</sub> to FB pin. In this case, positive no-load offset voltage (V<sub>OFSP</sub>) is generated.

$$V_{OFSP} = I_{OFSP} \times R_{FB} = 6.4 \times R_{FB} / R_{OFS} \quad (5)$$

Load Transient Quick Response

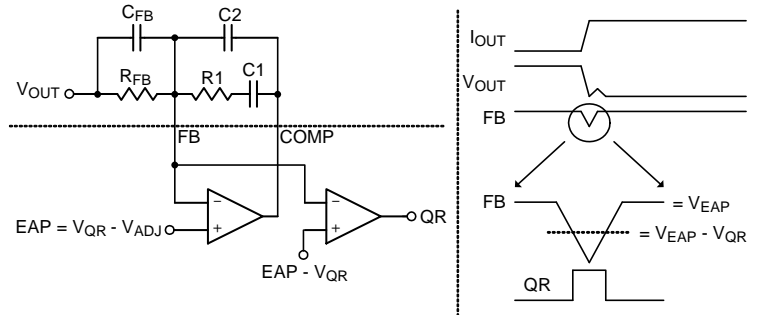


Figure 7. Load Transient Quick Response

In steady state, the voltage of V<sub>FB</sub> is controlled to be very close to V<sub>EAP</sub>. While a load step transient from light load to heavy load could cause V<sub>FB</sub> lower than V<sub>EAP</sub> by several tens of mV. In prior design, owing to limited control bandwidth, controller is hard to prevent V<sub>OUT</sub> undershoot during quick load transient from light load to heavy load. RT8841 detects load transient by comparing V<sub>FB</sub> and V<sub>EAP</sub>. If V<sub>FB</sub> suddenly drops below “V<sub>EAP</sub> – V<sub>QR</sub>”, V<sub>QR</sub> is a predetermined voltage. The quick response indicator QR rises up. When QR = H, RT8841 turns on all high side MOSFETs and turn off all low side MOSFETs. The sensitivity of quick response can be adjusted by the values of C<sub>FB</sub> and R<sub>FB</sub>. Smaller R<sub>FB</sub> and/or larger C<sub>FB</sub> will make QR easier to be triggered. Figure 7 is the circuit and typical waveforms.

Output Current Sensing

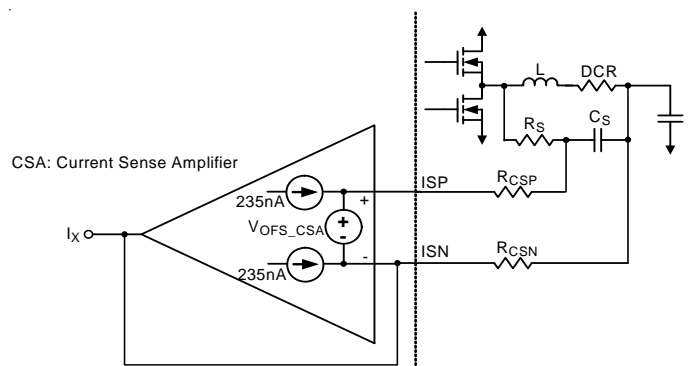


Figure 8. Circuit for Channel Current Sensing



The RT8841 provides low input offset current-sense amplifier (CSA) to monitor the output current of every channel. Output current of CSA ( $I_{X[n]}$ ) is used for channel current balance and active voltage position. In this inductor current sensing topology,  $R_S$  and  $C_S$  must be set according to the equation below :

$$L/DCR = R_S \times C_S \tag{6}$$

Then the output current of CSA will follow the equation below :

$$I_X = [I_L \times DCR - V_{OFS-CSA} + 235n \times (R_{CSP} - R_{CSN})]/R_{CSN} \tag{7}$$

235nA is typical value of CSA input offset current.  $V_{OFS-CSA}$  is the input offset voltage of CSA.  $V_{OFS-CSA}$  of RT8841 is smaller than +/- 1mV. Usually, " $V_{OFS-CSA} + 235n \times (R_{CSP} - R_{CSN})$ " is negligible except at very light load and the equation can be simplified as the equation below :

$$I_X = I_L \times DCR/R_{CSN} \tag{8}$$

**Loadline**

Output current of CSA is summed and averaged in RT8841. Then  $0.5 \sum(I_{X[n]})$  is sent to ADJ pin. Because  $\sum I_{X[n]}$  is a PTC (Positive Temperature Coefficient) current, an NTC (Negative Temperature Coefficient) resistor is needed to connect ADJ pin to GND. If the NTC resistor is properly selected to compensate the temperature coefficient of  $I_{X[n]}$ , the voltage on ADJ pin will be proportional to  $I_{OUT}$  without temperature effect. In RT8841, the positive input of ErrorAmp is " $V_{DAC} - V_{ADJ}$ ".  $V_{OUT}$  will follow " $V_{DAC} - V_{ADJ}$ ", too. Thus, the output voltage decreasing linearly with  $I_{OUT}$  is obtained. The loadline is defined as

$$\begin{aligned} LL(\text{loadline}) &= \Delta V_{OUT}/\Delta I_{OUT} = \Delta V_{ADJ}/\Delta I_{OUT} \\ &= 0.5 \times DCR \times R_{ADJ}/R_{CSN} \end{aligned} \tag{9}$$

Briefly, the resistance of  $R_{ADJ}$  sets the resistance of loadline. The temperature coefficient of  $R_{ADJ}$  compensates the temperature effect of loadline.

**Current Balance**

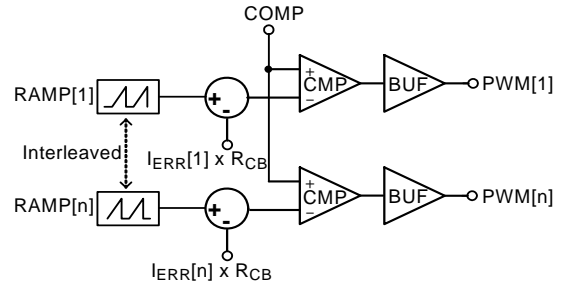


Figure 9. Circuit for Channel Current Balance

In Figure 8,  $I_{X[n]}$  is the current signal which is proportional to current flowing through channel n. In Figure 9, the current error signals  $I_{ERR}[n] (= I_{X[n]} - \text{AVG}(I_{X[n]}))$  are used to raise or lower the internal sawtooth waveforms (RAMP[1] to RAMP[n]) which are compared with ErrorAmp output (COMP) to generate PWM signal. The raised sawtooth waveform will decrease the PWM duty of the corresponding channel while the lowered will increase. Eventually, current flowing through each channel will be balanced.

**Channel Current Adjust**

If channel current is not balanced due to asymmetric PCB layout of power stage, external resistors can be adjusted to correct current imbalance. Figure 10 shows two types of current imbalance, constant ratio type and constant difference type.

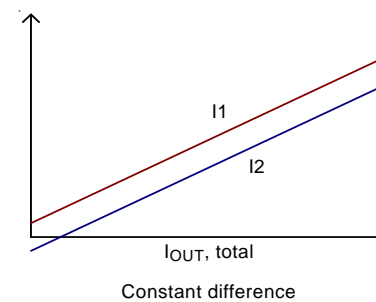
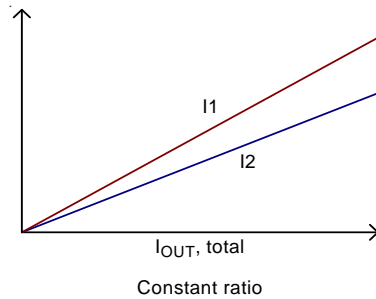


Figure 10. Channel Current vs. Total Current

If the initial current distribution is constant ratio type, according to Equation(8), reduce  $R_{CSN}[1]$  can reduce  $I_L[1]$  and improve current balance. If the initial current distribution is constant difference type, according to Equation(7), increase  $R_{CSP}[1]$  can reduce  $I_L[1]$  and improve current balance.

### Over Current Protection (OCP)

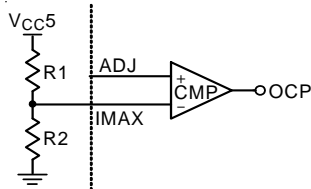


Figure 11. Over Current Protection

In Figure 11,  $V_{IMAX}$  is equal to  $5V \times R2 / (R1 + R2)$ . In RT8841,  $V_{ADJ}$  is proportional to  $I_{OUT}$  and is thermally compensated. Once  $V_{ADJ}$  is larger than  $V_{IMAX}$ , OCP is triggered and latched. RT8841 will turn off both high side MOSFET and low side MOSFET of all channels. A 20 $\mu$ s delay is used in OCP detection circuit to prevent false trigger.

### Over Voltage Protection (OVP)

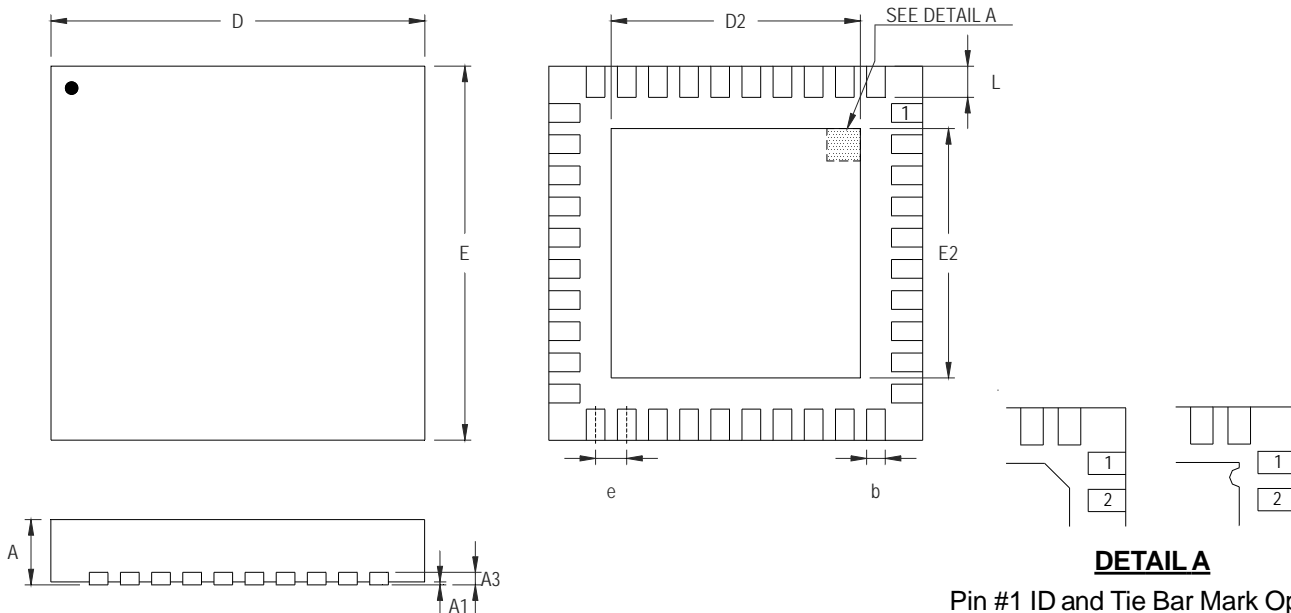
The over voltage protection monitors the output voltage via the FB pin. Once  $V_{FB}$  exceeds " $V_{EAP} + 150mV$ ", OVP is triggered and latched. RT8841 will try to turn on low side MOSFET and turn off high side MOSFET to protect CPU. A 20 $\mu$ s delay is used in OVP detection circuit to prevent false trigger.

**Datasheet Revision History**

Version	Date	Page No.	Item	Description
00C	2007/5/25			First Edition
01C	2007/7/30		Pin Configurations Typical Operating Characteristics Application Information	Modify Add Curve
02C	2007/9/14		Pin Configurations Function Block	Modify pin10.

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Outline Dimension



**DETAIL A**  
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	5.950	6.050	0.234	0.238
D2	4.000	4.750	0.157	0.187
E	5.950	6.050	0.234	0.238
E2	4.000	4.750	0.157	0.187
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

**W-Type 40L QFN 6x6 Package**

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