

NLX2G06

Dual Inverter, Open Drain

The NLX2G06 MiniGate™ is an advanced high-speed CMOS dual inverter with open drain output in ultra-small footprint.

The NLX2G06 input and output structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

Features

- High Speed: $t_{PD} = 2.4 \text{ ns}$ (Typ) @ $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation: $I_{CC} = 1 \mu\text{A}$ (Max) at $T_A = 25^\circ\text{C}$
- Power Down Protection Provided on inputs
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input and Output Pins
- Ultra-Small Packages
- These are Pb-Free Devices

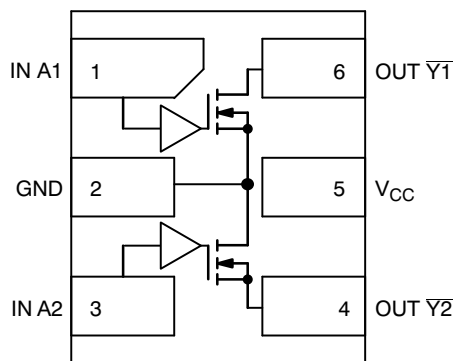


Figure 1. Pinout (Top View)

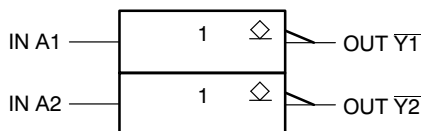


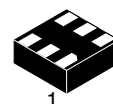
Figure 2. Logic Symbol



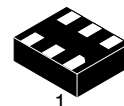
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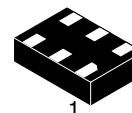
MARKING DIAGRAMS



ULLGA6
1.0 x 1.0
CASE 613AD



ULLGA6
1.2 x 1.0
CASE 613AE



ULLGA6
1.45 x 1.0
CASE 613AF



P = Device Marking
M = Date Code

PIN ASSIGNMENT

1	IN A1
2	GND
3	IN A2
4	OUT $\bar{Y}2$
5	V_{CC}
6	OUT $\bar{Y}1$

FUNCTION TABLE

A	\bar{Y}
L	Z
H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NLX2G06

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage	-0.5 to +7.0	V
I _{IK}	DC Input Diode Current V _{IN} < GND	-50	mA
I _{OK}	DC Output Diode Current V _{OUT} < GND	-50	mA
I _O	DC Output Source/Sink Current	±50	mA
I _{CC}	DC Supply Current Per Supply Pin	±100	mA
I _{GND}	DC Ground Current per Ground Pin	±100	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature Under Bias	150	°C
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
I _{LATCHUP}	Latchup Performance Above V _{CC} and Below GND at 125 °C (Note 5)	±500	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage	1.65	5.5	V
V _{IN}	Digital Input Voltage	0	5.5	V
V _{OUT}	Output Voltage	0	5.5	V
T _A	Operating Free-Air Temperature	-55	+125	°C
Δt/ΔV	Input Transition Rise or Fall Rate V _{CC} = 2.5 V ± 0.2 V V _{CC} = 3.3 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0 0 0	20 10 5	ns/V

NLX2G06

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25 °C			T _A = +85°C		T _A = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Low-Level Input Voltage		1.65-1.95	0.75 x V _{CC}			0.75 x V _{CC}		0.75 x V _{CC}		V
			2.3 to 5.5	0.70 x V _{CC}			0.70 x V _{CC}		0.70 x V _{CC}		
V _{IL}	Low-Level Input Voltage		1.65-1.95			0.25 x V _{CC}		0.25 x V _{CC}		0.25 x V _{CC}	V
			2.3 - 5.5			0.30 x V _{CC}		0.30 x V _{CC}		0.30 x V _{CC}	
V _{OL}	Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OL} = 100 μA	1.65 - 5.5			0.1		0.1		0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = 4 mA	1.65	0.08	0.24		0.24		0.24		
		I _{OH} = 8 mA	2.3	0.2	0.3		0.3		0.3		
		I _{OH} = 12 mA	2.7	0.22	0.4		0.4		0.4		
		I _{OH} = 16 mA	3.0	0.28	0.4		0.4		0.4		
		I _{OH} = 24 mA I _{OH} = 32 mA	3.0 4.5	0.38 0.42	0.55 0.55		0.55 0.55		0.55 0.55		
I _{LKG}	Z-State Output Leakage Current	V _{IN} = V _{IL} , V _{OUT} = V _{CC} or GND	5.5			±5.0		±10		±10	μA
I _{IN}	Input Leakage Current	0 ≤ V _{IN} ≤ 5.5 V	0 to 5.5			±0.1		±1.0		±1.0	μA
I _{OFF}	Power-Off Output Leakage Current	V _{IN} or V _{OUT} = 5.5 V	0			1.0		10		10	μA
I _{CC}	Quiescent Supply Current	0 ≤ V _{IN} ≤ V _{CC}	5.5			1.0		10		10	μA

NLX2G06

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ nS)

Symbol	Parameter	V_{CC} (V)	Test Condition	$T_A = 25^\circ\text{C}$			$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
t_{pZL}	Propagation Delay (Figures 3 and 4)	1.65-1.95	$R_L = R_1 = 5000\ \Omega$, $C_L = 15\ \text{pF}$	2.0	5.7	10.5	2.0	11	ns
		2.3-2.7	$R_L = R_1 = 500\ \Omega$, $C_L = 50\ \text{pF}$	0.8	3.0	3.6	0.8	4.1	
		3.0-3.6	$R_L = R_1 = 500\ \Omega$, $C_L = 50\ \text{pF}$	0.8	2.4	3.2	0.8	3.7	
		4.5-5.5	$R_L = R_1 = 500\ \Omega$, $C_L = 50\ \text{pF}$	0.5	2.4	3.0	0.5	3.5	
t_{pLZ}	Propagation Delay (Figures 3 and 4)	1.65-1.95	$R_L = R_1 = 5000\ \Omega$, $C_L = 15\ \text{pF}$	2.0	5.7	10.5	2.0	11	ns
		2.3-2.7	$R_L = R_1 = 500\ \Omega$, $C_L = 50\ \text{pF}$	0.8	3.8	3.6	0.8	4.1	
		3.0-3.6	$R_L = R_1 = 500\ \Omega$, $C_L = 50\ \text{pF}$	0.8	2.9	3.2	0.8	3.7	
		4.5-5.5	$R_L = R_1 = 500\ \Omega$, $C_L = 50\ \text{pF}$	0.5	1.2	3.0	0.5	3.5	
C_{IN}	Input Capacitance	5.5	$V_{IN} = 0\ \text{V}$ or V_{CC}		2.5				pF
C_{OUT}	Output Capacitance	5.5	$V_{IN} = 0\ \text{V}$ or V_{CC}		4				pF
C_{PD}	Power Dissipation Capacitance (Note 6)	3.3	10 MHz		4				pF
		5.5	$V_{IN} = 0\ \text{V}$ or V_{CC}						

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

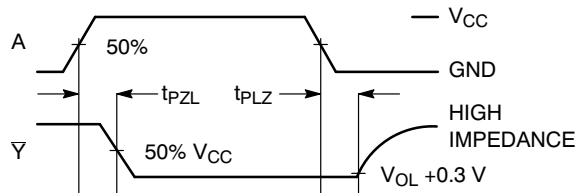


Figure 3. Switching Waveforms

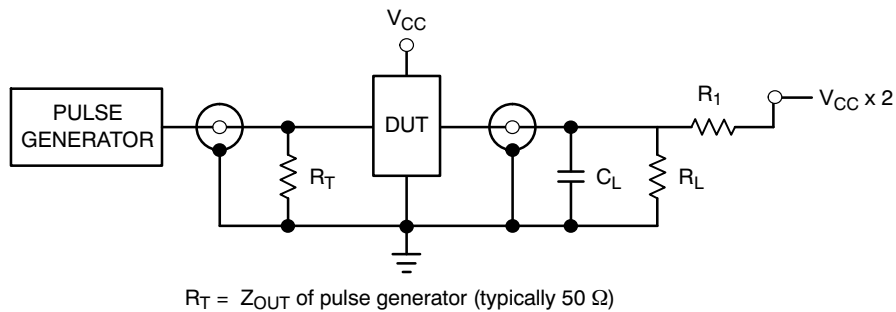


Figure 4. Test Circuit

NLX2G06

ORDERING INFORMATION

Device	Package	Shipping†
NLX2G06AMX1TCG	ULLGA6, 1.45 x 1.0, 0.5P (Pb-Free)	3000 / Tape & Reel
NLX2G06BMX1TCG	ULLGA6, 1.2 x 1.0, 0.4P (Pb-Free)	3000 / Tape & Reel
NLX2G06CMX1TCG	ULLGA6, 1.0 x 1.0, 0.35P (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NLX2G06

PACKAGE DIMENSIONS

ULLGA6 1.0x1.0, 0.35P
CASE 613AD-01
ISSUE A

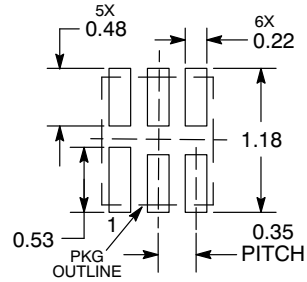


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.12	0.22
D	1.00 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

**MOUNTING FOOTPRINT
SOLDERMASK DEFINED***



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NLX2G06

PACKAGE DIMENSIONS

ULLGA6 1.2x1.0, 0.4P
CASE 613AE-01
ISSUE A

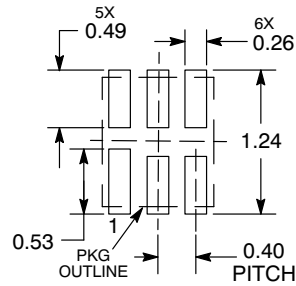


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3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.20 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.25	0.35
L1	0.35	0.45

**MOUNTING FOOTPRINT
SOLDERMASK DEFINED***



DIMENSIONS: MILLIMETERS

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PACKAGE DIMENSIONS

ULLGA6 1.45x1.0, 0.5P
CASE 613AF-01
ISSUE A

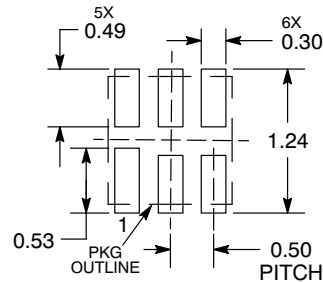


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4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

DIM	MILLIMETERS	
	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT SOLDERMASK DEFINED*



DIMENSIONS: MILLIMETERS

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