

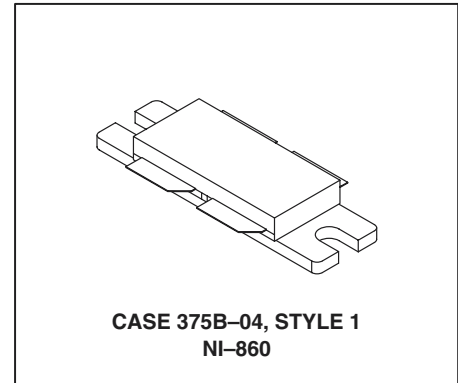
The RF MOSFET Line
RF Power Field-Effect Transistor
N-Channel Enhancement-Mode Lateral MOSFET

MRF186

**1.0 GHz, 120 W, 28 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFET**

Designed for broadband commercial and industrial applications with frequencies from 800 MHz to 1.0 GHz. The high gain and broadband performance of this device make it ideal for large-signal, common source amplifier applications in 28 volt base station equipment.

- Guaranteed Performance @ 960 MHz, 28 Volts
Output Power — 120 Watts PEP
Power Gain — 11 dB
Efficiency — 30%
Intermodulation Distortion — -28 dBc
- Excellent Thermal Stability
- 100% Tested for Load Mismatch Stress at all Phase Angles with 5:1 VSWR @ 28 Vdc, 960 MHz, 120 Watts CW



MAXIMUM RATINGS (2)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	65	Vdc
Drain-Gate Voltage (R _{GS} = 1 MΩ)	V _{DGR}	65	Vdc
Gate-Source Voltage	V _{GS}	±20	Vdc
Drain Current — Continuous	I _D	14	Adc
Total Device Dissipation @ T _C = 70°C Derate above 70°C	P _D	162.5 1.25	Watts W/°C
Storage Temperature Range	T _{stg}	- 65 to +150	°C
Operating Junction Temperature	T _J	200	°C

THERMAL CHARACTERISTICS (2)

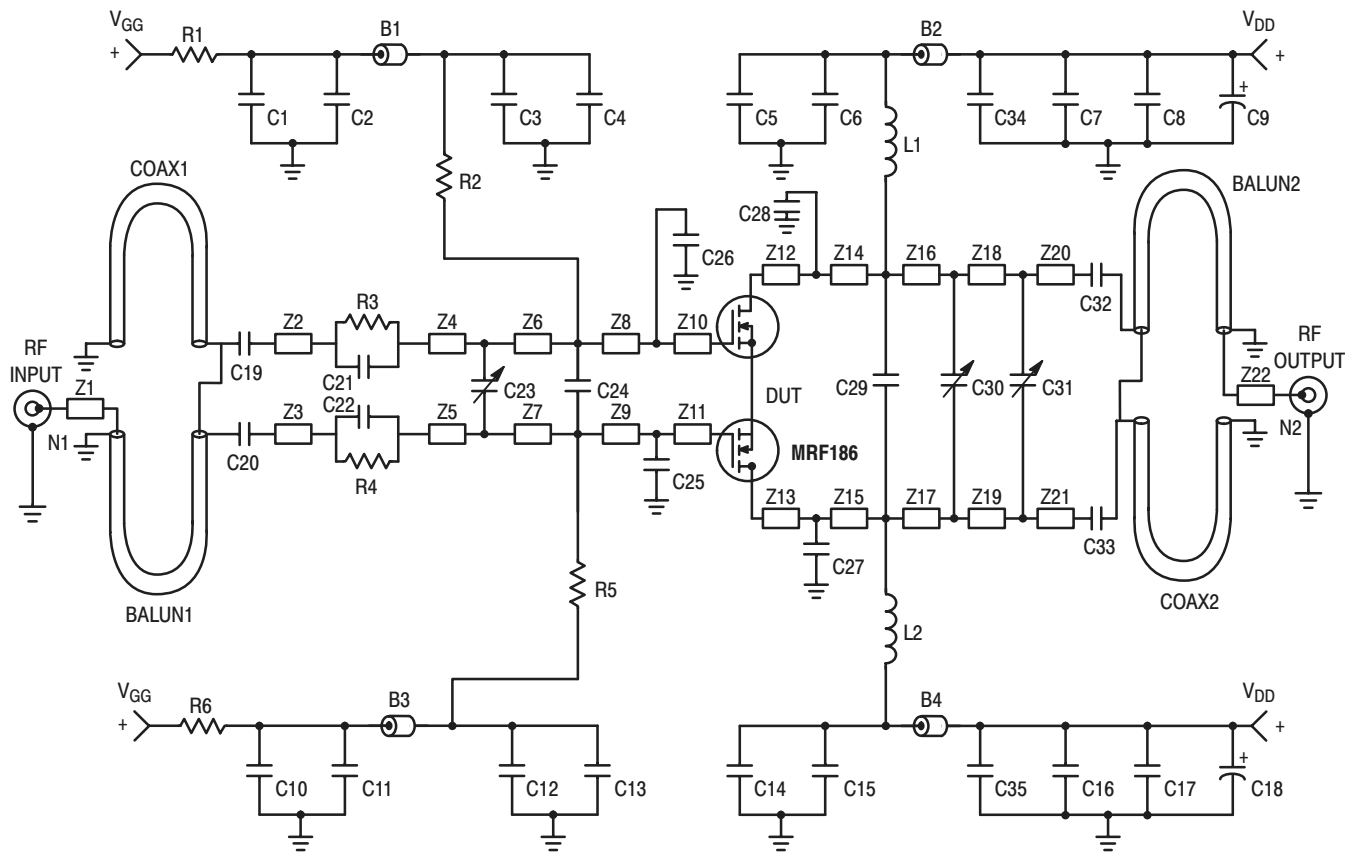
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	0.8	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 50\ \mu\text{Adc}$)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current ($V_{GS} = 20\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS (1)					
Gate Quiescent Voltage ($V_{DS} = 26\text{ Vdc}$, $I_D = 300\ \mu\text{Adc}$ Per Side)	$V_{GS(th)}$	2.5	3	4	Vdc
Gate Quiescent Voltage ($V_{DS} = 26\text{ Vdc}$, $I_D = 300\ \text{mAdc}$ Per Side)	$V_{GS(Q)}$	3.3	4.2	5	Vdc
Delta Gate Threshold Voltage (Side to Side) ($V_{DS} = 28\text{ V}$, $I_D = 300\ \text{mA}$ Per Side)	$\Delta V_{GS(Q)}$	—	—	0.3	Vdc
Drain–Source On–Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 3\ \text{Adc}$ Per Side)	$V_{DS(on)}$	—	0.58	0.7	Vdc
Forward Transconductance ($V_{DS} = 10\text{ Vdc}$, $I_D = 3\ \text{Adc}$ Per Side)	g_{fs}	2.4	2.8	—	S
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (Per Side) ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0$, $f = 1\ \text{MHz}$)	C_{iss}	—	177	—	pF
Output Capacitance (Per Side) ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0$, $f = 1\ \text{MHz}$)	C_{oss}	—	45	—	pF
Reverse Transfer Capacitance (Per Side) ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0$, $f = 1\ \text{MHz}$)	C_{rss}	—	3.4	—	pF
FUNCTIONAL CHARACTERISTICS (In Motorola Test Fixture, 50 ohm system) (2)					
Two–Tone Common Source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 120\ \text{W PEP}$, $I_{DQ} = 2 \times 400\ \text{mA}$, $f_1 = 960.0\ \text{MHz}$, $f_2 = 960.1\ \text{MHz}$)	G_{ps}	11	12.2	—	dB
Two–Tone Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 120\ \text{W PEP}$, $I_{DQ} = 2 \times 400\ \text{mA}$, $f_1 = 960.0\ \text{MHz}$, $f_2 = 960.1\ \text{MHz}$)	η	30	35	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 120\ \text{W PEP}$, $I_{DQ} = 2 \times 400\ \text{mA}$, $f_1 = 960.0\ \text{MHz}$, $f_2 = 960.1\ \text{MHz}$)	IMD	—	–32	–28	dBc
Input Return Loss ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 120\ \text{W PEP}$, $I_{DQ} = 2 \times 400\ \text{mA}$, $f_1 = 960.0\ \text{MHz}$, $f_2 = 960.1\ \text{MHz}$)	IRL	9	16	—	dB
Two–Tone Common Source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 120\ \text{W PEP}$, $I_{DQ} = 2 \times 400\ \text{mA}$, $f_1 = 945.0\ \text{MHz}$, $f_2 = 945.1\ \text{MHz}$)	G_{ps}	—	12	—	dB
Two–Tone Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 120\ \text{W PEP}$, $I_{DQ} = 2 \times 400\ \text{mA}$, $f_1 = 945.0\ \text{MHz}$, $f_2 = 945.1\ \text{MHz}$)	η	—	33	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 120\ \text{W PEP}$, $I_{DQ} = 2 \times 400\ \text{mA}$, $f_1 = 945.0\ \text{MHz}$, $f_2 = 945.1\ \text{MHz}$)	IMD	—	–32	—	dBc
Input Return Loss ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 120\ \text{W PEP}$, $I_{DQ} = 2 \times 400\ \text{mA}$, $f_1 = 945.0\ \text{MHz}$, $f_2 = 945.1\ \text{MHz}$)	IRL	—	16	—	dB
Output Mismatch Stress ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 120\ \text{W CW}$, $I_{DQ} = 2 \times 400\ \text{mA}$, $f = 960\ \text{MHz}$, $V_{SWR} = 5:1$, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

- (1) Each side of device measured separately.
- (2) Device measured in push–pull configuration.



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|---------------------------|---|-----------------|---|
| B1 – B4 | Fair Rite Products Short Ferrite Bead, 2743021446 | C31 | 0.8 – 8.0 pF, Variable Capacitor, Johanson Gigatrim |
| C1, C7, C8, C10, C16, C17 | 10 μ F, 50 V, Tantalum | L1, L2 | 3 Turns, #20 AWG, IDIA 0.126", 24.7 nH |
| C2, C11, C34, C35 | 0.1 μ F, Chip Capacitor | N1, N2 | Type N Connectors |
| C3, C6, C12, C15 | 330 pF, Chip Capacitor | R1, R6 | 1 k Ω , 1/4 W, Carbon Resistor |
| C4, C5, C13, C14, | | R2, R5 | 1.2 k Ω , 0.1 W, Chip Resistor |
| C19, C20, C32, C33 | 47 pF, Chip Capacitor | R3, R4 | 75 Ω , 0.1 W, Chip Resistor |
| C9, C18 | 250 μ F, 50 V, Electrolytic Capacitor | Z1 – Z22 | Microstrip (See Component Placement) |
| C21, C22 | 12 pF, Chip Capacitor | Balun1, Balun2, | |
| C23, C30 | 0.6 – 4.5 pF, Variable Capacitor, Johanson Gigatrim | Coax1, Coax2 | 2.20" 50 Ω , 0.086" OD Semi-Rigid Coax |
| C24, C25, C26 | 5.1 pF, Chip Capacitor | Board | 1/32" Glass Teflon [®] , $\epsilon_r = 2.55$ |
| C27, C28 | 3.9 pF, Chip Capacitor | | |

Figure 1. 930 – 960 MHz Test Circuit Schematic

TYPICAL CHARACTERISTICS

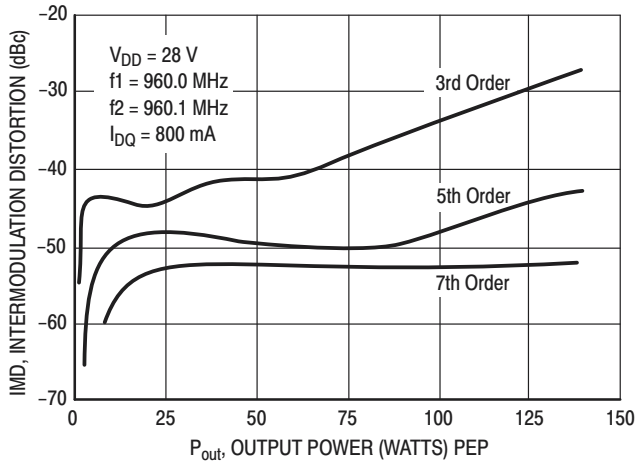


Figure 2. Intermodulation Distortion Products versus Output Power

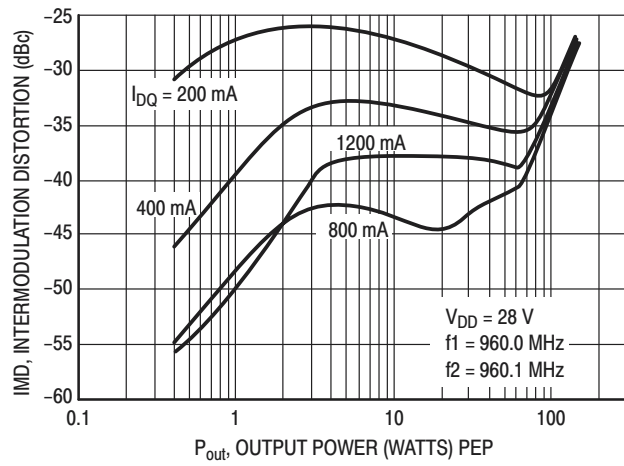


Figure 3. Intermodulation Distortion versus Output Power

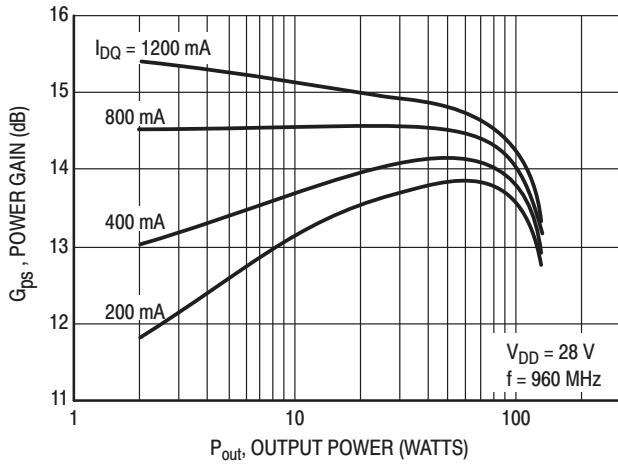


Figure 4. Power Gain versus Output Power

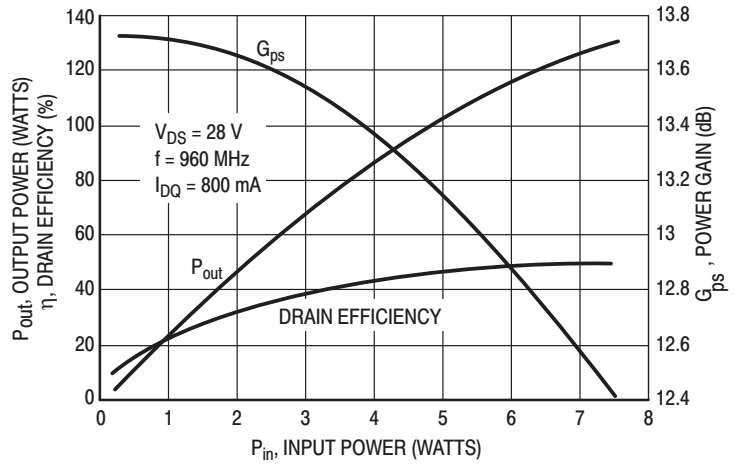


Figure 5. Output Power versus Input Power

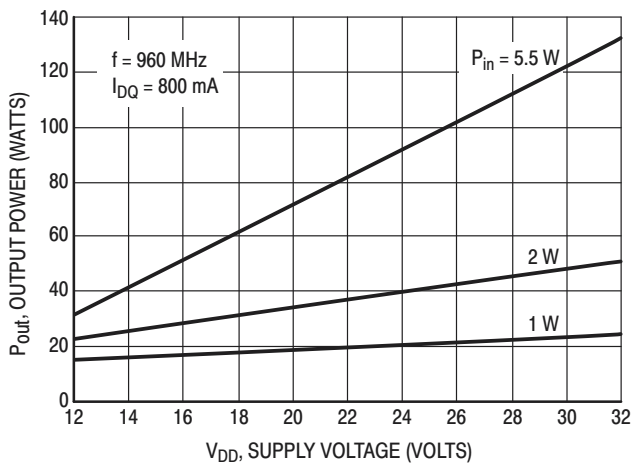


Figure 6. Output Power versus Supply Voltage

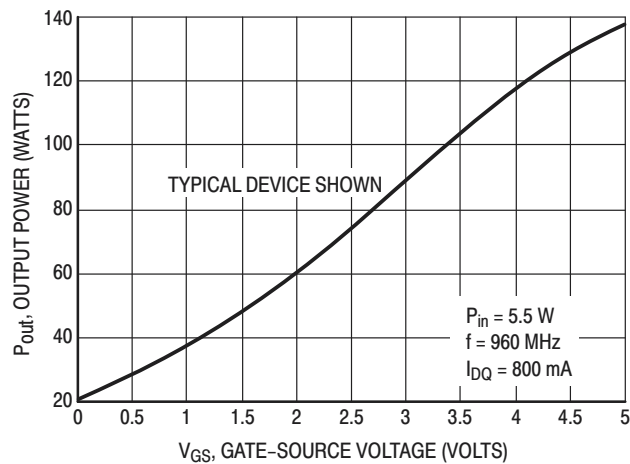


Figure 7. Output Power versus Gate Voltage

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TYPICAL CHARACTERISTICS

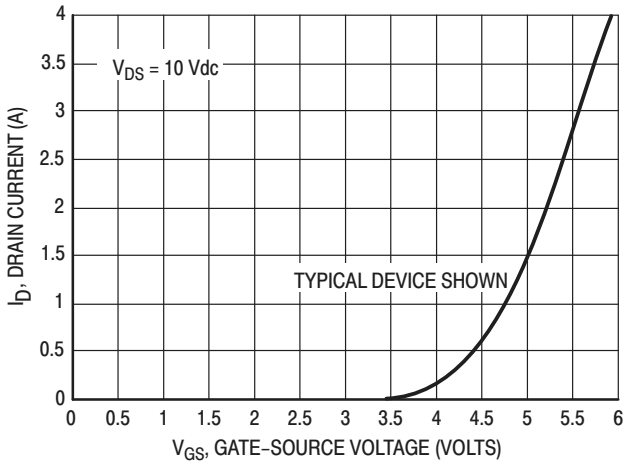


Figure 8. Drain Current versus Gate Voltage

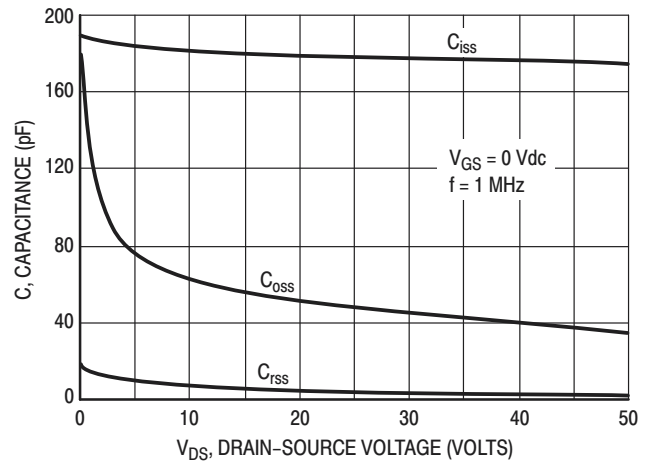


Figure 9. Capacitance versus Voltage

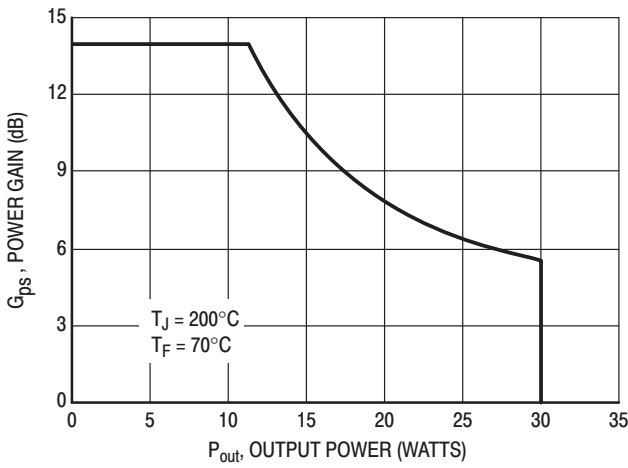


Figure 10. DC Safe Operating Area

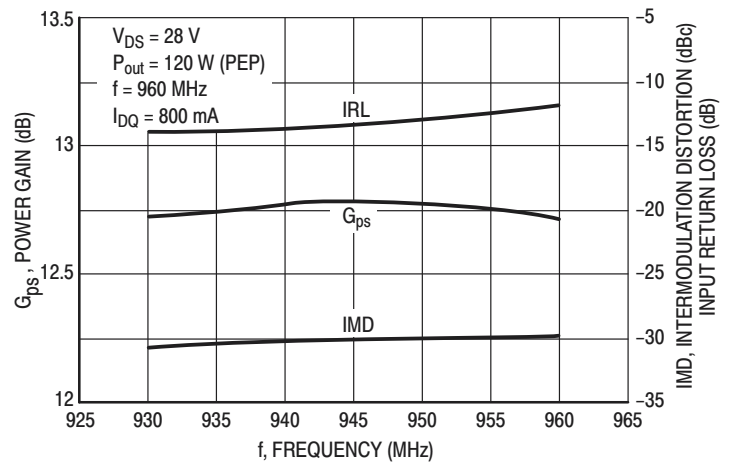
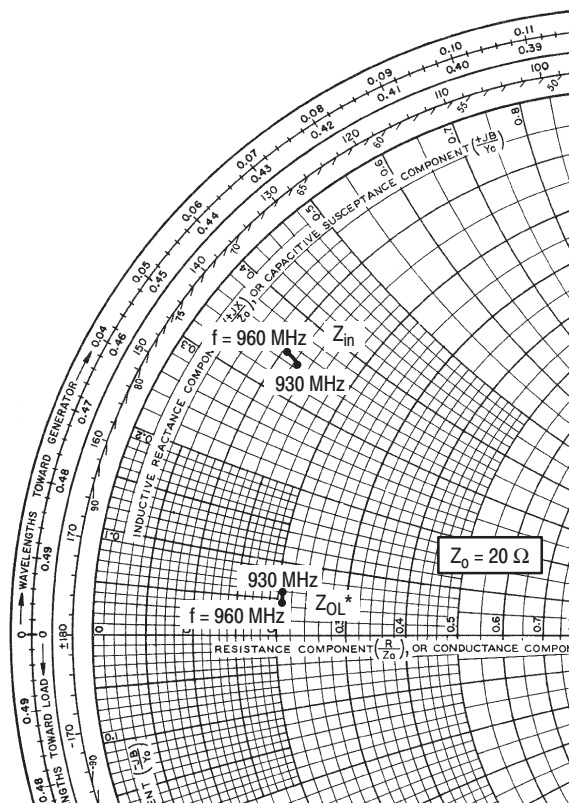


Figure 11. Broadband Circuit Performance

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$V_{CC} = 28\text{ V}$, $I_{DQ} = 2 \times 400\text{ mA}$, $P_{out} = 120\text{ W PEP}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
930	$2.5 + j6.9$	$4.3 + j1.2$
945	$2.5 + j7.0$	$4.3 + j1.0$
960	$2.2 + j7.1$	$4.3 + j0.9$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current, efficiency and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation performance. Impedances shown represent a single channel (1/2 of MRF186) impedance measurement.

Figure 12. Series Equivalent Input and Output Impedance

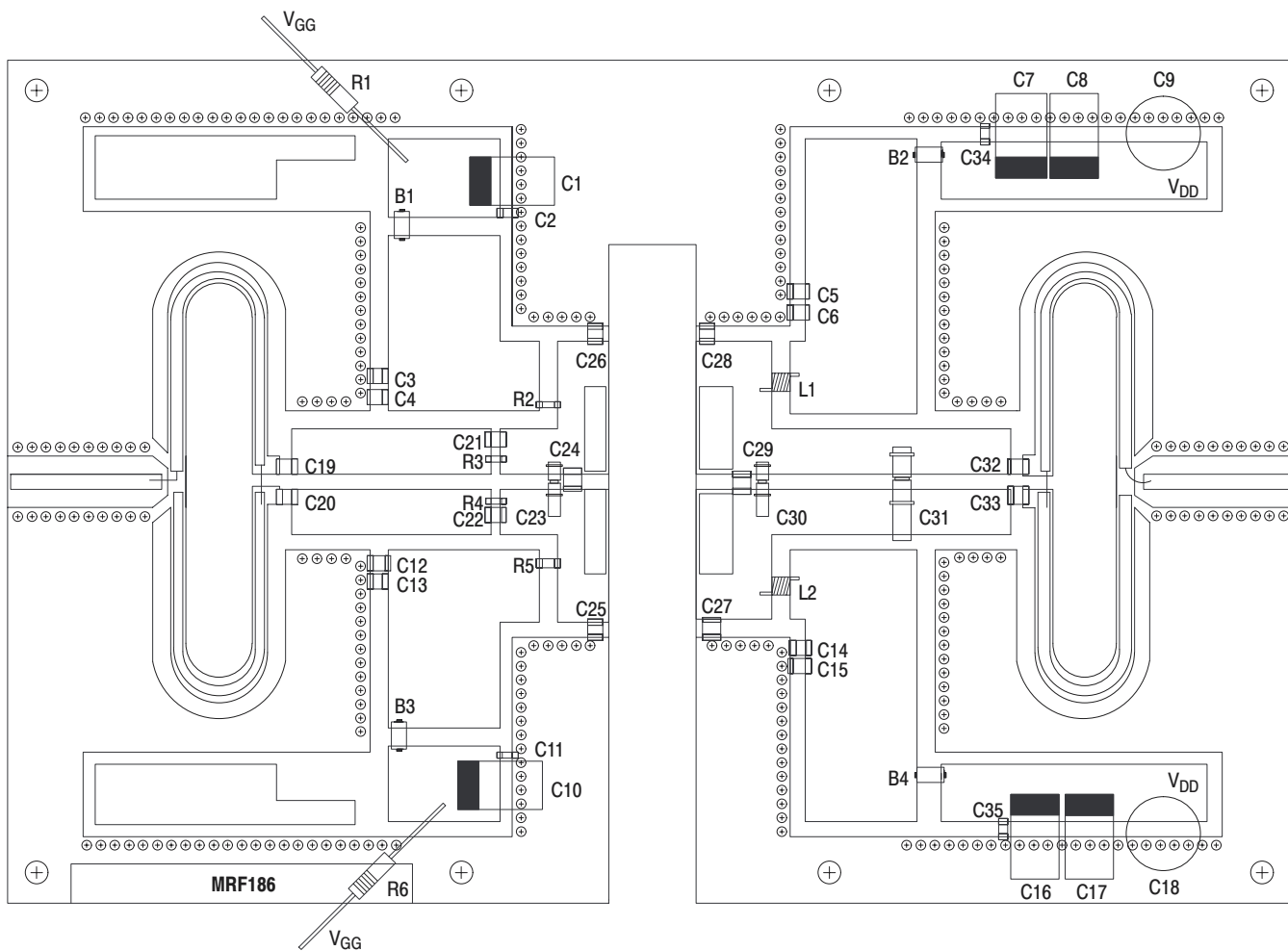
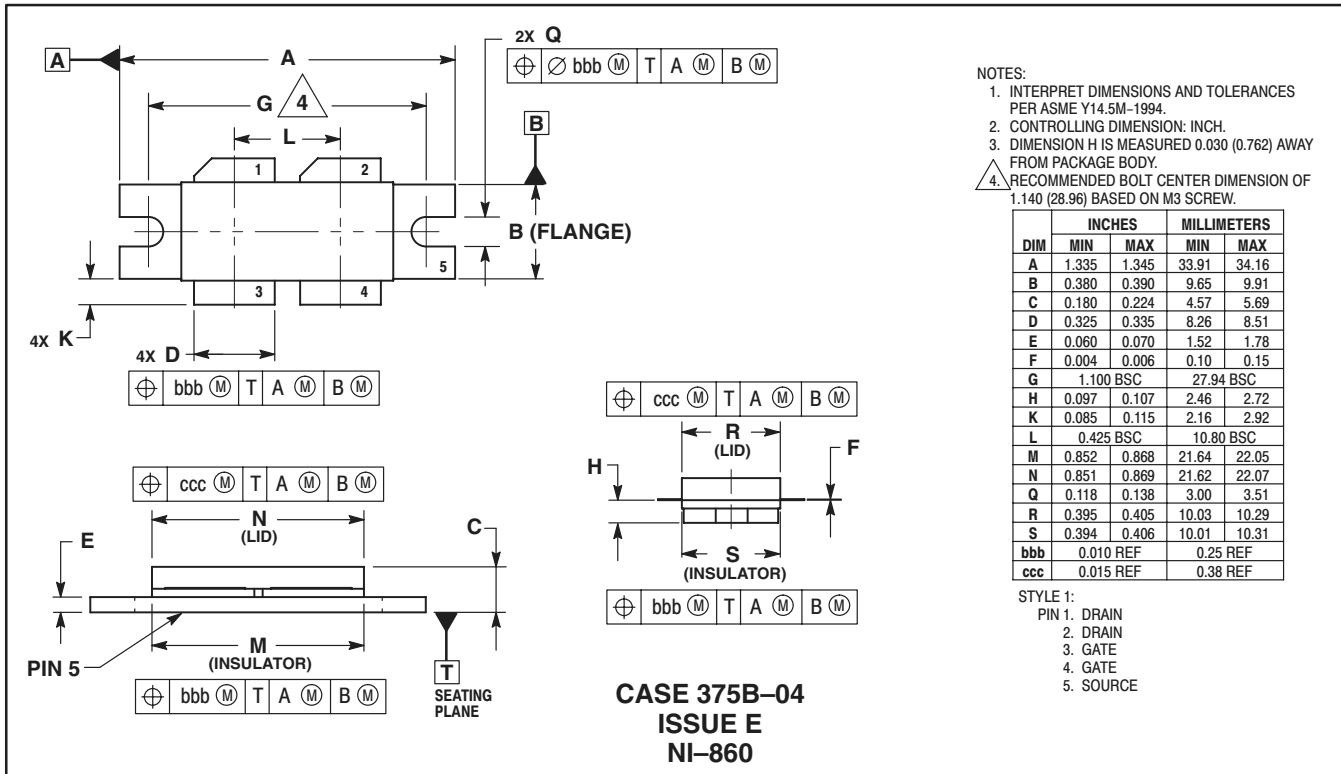


Figure 13. Component Placement Diagram of 930 - 960 MHz Broadband Test Fixture

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PACKAGE DIMENSIONS



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