MH64D64AKQH-75,-10

4,294,967,296-BIT (67,108,864-WORD BY 64-BIT) Double Data Rate Synchronous DRAM Module

DESCRIPTION

The MH64D64AKQH is 67108864 - word x 64-bit Double Data Rate(DDR) Synchronous DRAM mounted module.

This consists of 16 industry standard 32M x 8 DDR Synchronous DRAMs in Small TSOP with SSTL_2 interface which achieves very high speed data rate up to 133MHz.

This socket-type memory module is suitable for main memory in computer systems and easy to interchange or add modules.

FEATURES

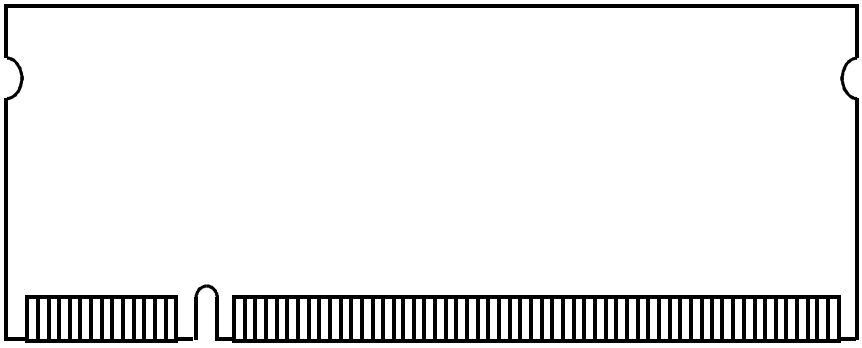
Type name	Max. Frequency	CLK Access Time [component level]
MH64D64AKQH-75	133MHz	± 0.75ns
MH64D64AKQH-10	100MHz	± 0.8ns

- Utilizes industry standard 32M X 8 DDR Synchronous DRAMs in Smal TSOP package , industry standard EEPROM(SPD) in TSSOP package
- 200pin SO-DIMM
- Vdd=Vddq=2.5v ±0.2V
- Double data rate architecture; two data transfers per clock cycle
- Bidirectional, data strobe (DQS) is transmitted/received with data
- Differential clock inputs (CLK and /CLK)
- DLL aligns DQ and DQS transitions with CLK transition edges of DQS
- Commands entered on each positive CLK edge
- Data and data mask referenced to both edges of DQS
- 4bank operation concontrolled by BA0,BA1(Bank Address ,discrete)
- /CAS latency - 2.0/2.5 (programmable)
- Burst length- 2/4/8 (programmable)
- Burst Type - sequential/interleave(programmable)
- Auto precharge / All bank precharge controlled by A10
- 8192 refresh cycles /64ms
- Auto refresh and Self refresh
- Row address A0-12 / Column address A0-9
- SSTL_2 Interface
- Module 2bank Configration

APPLICATION

Main memoryunit for Note PC, Mobile etc.

PCB Outline



(Front) 1 199
(Back) 2 200

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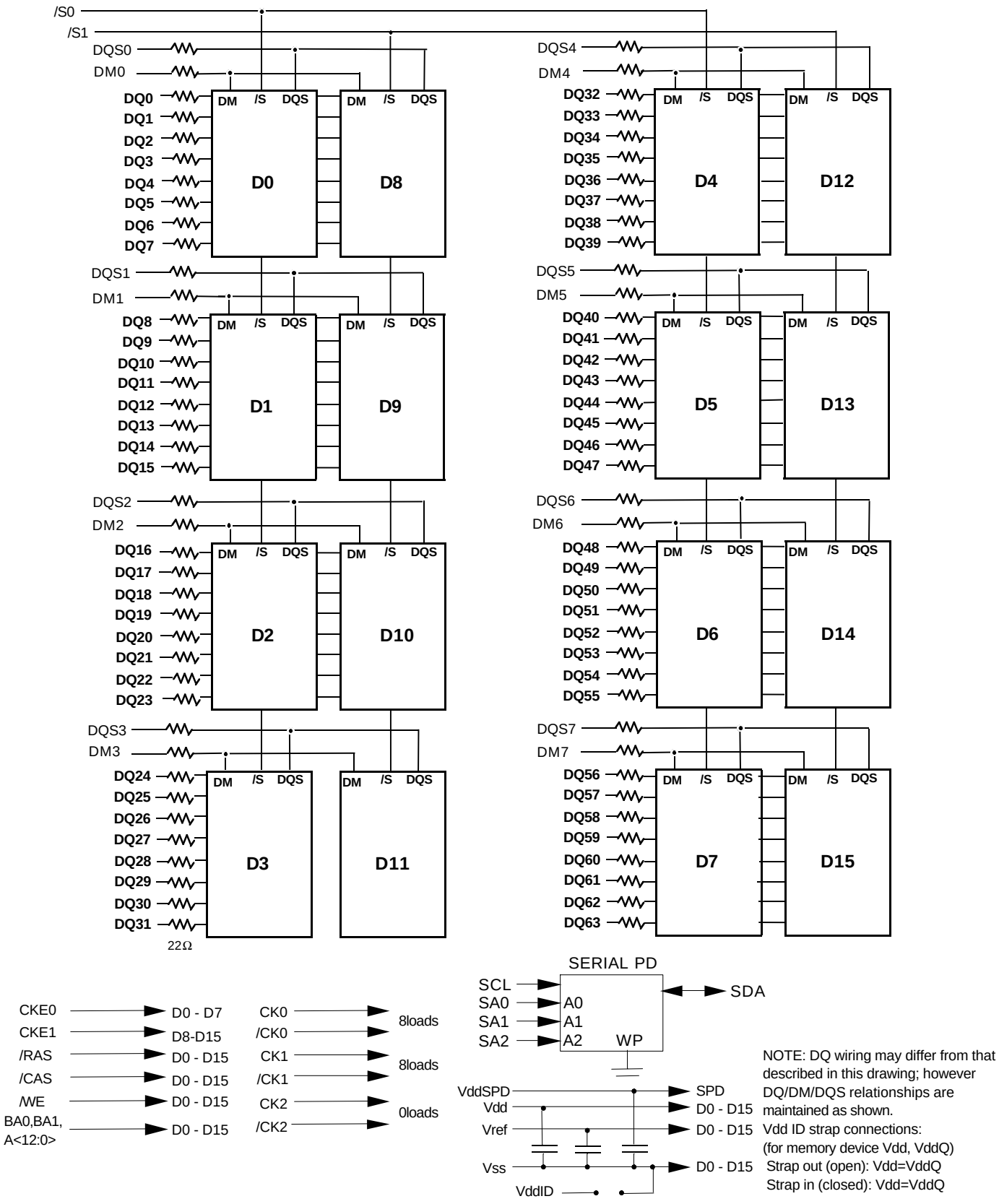
PIN CONFIGURATION

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	Vref	2	Vref	85	NC	86	NC	169	DQS6	170	DM6
3	Vss	4	Vss	87	Vss	88	Vss	171	DQ50	172	DQ54
5	DQ0	6	DQ4	89	CK2	90	Vss	173	Vss	174	Vss
7	DQ1	8	DQ5	91	/CK2	92	Vdd	175	DQ51	176	DQ55
9	Vdd	10	Vdd	93	Vdd	94	Vdd	177	DQ56	178	DQ60
11	DQS0	12	DM0	95	CKE1	96	CKE0	179	Vdd	180	Vdd
13	DQ2	14	DQ6	97	NC	98	NC	181	DQ57	182	DQ61
15	Vss	16	Vss	99	A12	100	A11	183	DQS7	184	DM7
17	DQ3	18	DQ7	101	A9	102	A8	185	Vss	186	Vss
19	DQ8	20	DQ12	103	Vss	104	Vss	187	DQ58	188	DQ62
21	Vdd	22	Vdd	105	A7	106	A6	189	DQ59	190	DQ63
23	DQ9	24	DQ13	107	A5	108	A4	191	Vdd	192	Vdd
25	DQS1	26	DM1	109	A3	110	A2	193	SDA	194	SA0
27	Vss	28	Vss	111	A1	112	A0	195	SCL	196	SA1
29	DQ10	30	DQ14	113	Vdd	114	Vdd	197	VddSPD	198	SA2
31	DQ11	32	DQ15	115	A10/AP	116	BA1	199	VddID	200	NC
33	Vdd	34	Vdd	117	BA0	118	/RAS				
35	CK0	36	Vdd	119	/WE	120	/CAS				
37	/CK0	38	Vss	121	/S0	122	/S1				
39	Vss	40	Vss	123	NC	124	NC				
41	DQ16	42	DQ20	125	Vss	126	Vss				
43	DQ17	44	DQ21	127	DQ32	128	DQ36				
45	Vdd	46	Vdd	129	DQ33	130	DQ37				
47	DQS2	48	DM2	131	Vdd	132	Vdd				
49	DQ18	50	DQ22	133	DQS4	134	DM4				
51	Vss	52	Vss	135	DQ34	136	DQ38				
53	DQ19	54	DQ23	137	Vss	138	Vss				
55	DQ24	56	DQ28	139	DQ35	140	DQ39				
57	Vdd	58	Vdd	141	DQ40	142	DQ44				
59	DQ25	60	DQ29	143	Vdd	144	Vdd				
61	DQS3	62	DM3	145	DQ41	146	DQ45				
63	Vss	64	Vss	147	DQS5	148	DM5				
65	DQ26	66	DQ30	149	Vss	150	Vss				
67	DQ27	68	DQ31	151	DQ42	152	DQ46				
69	Vdd	70	Vdd	153	DQ43	154	DQ47				
71	NC	72	NC	155	Vdd	156	Vdd				
73	NC	74	NC	157	Vdd	158	/CK1				
75	Vss	76	Vss	159	Vss	160	CK1				
77	NC	78	NC	161	Vss	162	Vss				
79	NC	80	NC	163	DQ48	164	DQ52				
81	Vdd	82	Vdd	165	DQ49	166	DQ53				
83	NC	84	NC	167	Vdd	168	Vdd				

NC: No Connect

Block Diagram



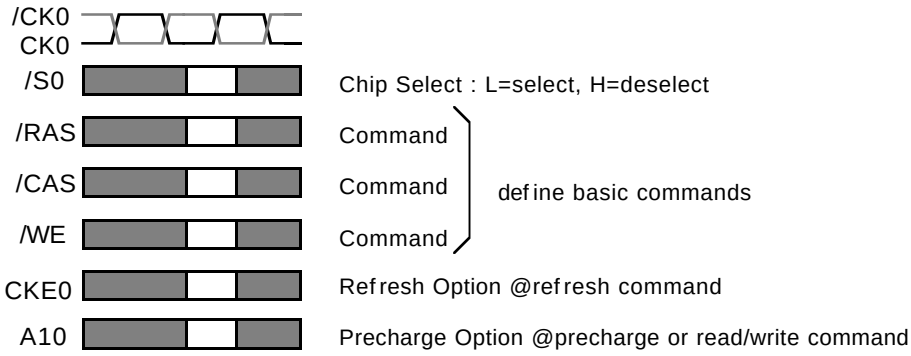
NOTE: DQ wiring may differ from that described in this drawing; however DQ/DM/DQS relationships are maintained as shown.
Vdd ID strap connections:
(for memory device Vdd, VddQ)
Strap out (open): Vdd=VddQ
Strap in (closed): Vdd=VddQ

PIN FUNCTION

SYMBOL	TYPE	DESCRIPTION
CK0-2,/CK0-2	Input	Clock: CK0-2 and /CK0-2 are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK0-2 and negative edge of /CK0-2. Output (read) data is referenced to the crossings of CK0-2 and /CK0-2 (both directions of crossing).
CKE0-1	Input	Clock Enable: CKE0-1 controls internal clock. When CKE0-1 is low, internal clock for the following cycle is ceased. CKE0-1 is also used to select auto / self refresh. After self refresh mode is started, CKE0-1 becomes asynchronous input. Self refresh is maintained as long as CKE is low.
/S0-1	Input	Chip Select: When /S0-1 is high, any command means No Operation.
/RAS, /CAS, /WE	Input	Combination of /RAS, /CAS, /WE defines basic commands.
A0-12	Input	A0-12 specify the Row / Column Address in conjunction with BA0,1. The Row Address is specified by A0-12. The Column Address is specified by A0-9. A10 is also used to indicate precharge option. When A10 is high at a read / write command, an auto precharge is performed. When A10 is high at a precharge command, all banks are precharged.
BA0-1	Input	Bank Address: BA0-1 specifies one of four banks in SDRAM to which a command is applied. BA0-1 must be set with ACT, PRE, READ, WRITE commands.
DQ 0-63	Input / Output	Data Input/Output: Data bus
DQS0-7	Input / Output	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data.
DM0-7	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM0-7 is sampled HIGH along with that input data during a WRITE access. DM0-7 is sampled on both edges of DQS0-7. Although DM pins are input only, the DM0-7 loading matches the DQ0-63 and DQS0-7 loading.
Vdd, Vss	Power Supply	Power Supply for the memory array and peripheral circuitry.
Vddspd	Power Supply	Power Supply for SPD
Vref	Input	SSTL_2 reference voltage.
SDA	Input / Output	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected to Vdd to act as a pullup.
SCL	Input / Output	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL to Vdd to act as a pullup.
SA0-2	Input	Address pins used to select the Serial Presence Detect.
VddID	Output	Vdd identification flag

BASIC FUNCTIONS

The MH64D64AKQH provides basic functions, bank (row) activate, burst read / write, bank (row) precharge, and auto / self refresh. Each command is defined by control signals of /RAS, /CAS and /WE at CLK rising edge. In addition to 3 signals, /CS ,CKE and A10 are used as chip select, refresh option, and precharge option, respectively. To know the detailed definition of commands, please see the command truth table.



Activate (ACT) [/RAS =L, /CAS =/WE =H]

ACT command activates a row in an idle bank indicated by BA.

Read (READ) [/RAS =H, /CAS =L, /WE =H]

READ command starts burst read from the active bank indicated by BA. First output data appears after /CAS latency. When A10 =H at this command, the bank is deactivated after the burst read (auto-precharge,**READA**)

Write (WRITE) [/RAS =H, /CAS =/WE =L]

WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is set by burst length. When A10 =H at this command, the bank is deactivated after the burst write (auto-precharge, **WRITEA**).

Precharge (PRE) [/RAS =L, /CAS =H, /WE =L]

PRE command deactivates the active bank indicated by BA. This command also terminates burst read /write operation. When A10 =H at this command, all banks are deactivated (precharge all, **PREA**).

Auto-Refresh (REFA) [/RAS =/CAS =L, /WE =CKE0 =H]

REFA command starts auto-refresh cycle. Refresh address including bank address are generated internally. After this command, the banks are precharged automatically.

COMMAND TRUTH TABLE

COMMAND	MNEMONIC	CKE n-1	CKE n	/S	/RAS	/CAS	/WE	BA0,1	A10 /AP	A0-9, 11-12	note
Deselect	DESEL	H	X	H	X	X	X	X	X	X	
No Operation	NOP	H	X	L	H	H	H	X	X	X	
Row Address Entry & Bank Activate	ACT	H	H	L	L	H	H	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	V	L	X	
Precharge All Banks	PREA	H	H	L	L	H	L	X	H	X	
Column Address Entry & Write	WRITE	H	H	L	H	L	L	V	L	V	
Column Address Entry & Write with Auto-Precharge	WRITEA	H	H	L	H	L	L	V	H	V	
Column Address Entry & Read	READ	H	H	L	H	L	H	V	L	V	
Column Address Entry & Read with Auto-Precharge	READA	H	H	L	H	L	H	V	H	V	
Auto-Refresh	REFA	H	H	L	L	L	H	X	X	X	
Self-Refresh Entry	REFS	H	L	L	L	L	H	X	X	X	
Self-Refresh Exit	REFSX	L	H	H	X	X	X	X	X	X	
		L	H	L	H	H	H	X	X	X	
Burst Terminate	TERM	H	H	L	H	H	L	X	X	X	1
Mode Register Set	MRS	H	H	L	L	L	L	L	L	V	2

H=High Level, L=Low Level, V=Valid, X=Don't Care, n=CLK cycle number

NOTE:

1. Applies only to read bursts with autoprecharge disabled; this command is undefined (and should not be used) for read bursts with autoprecharge enabled, and for write bursts.
2. BA0-BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0-BA1 are reserved; A0-A12 provide the op-code to be written to the selected Mode Register.

FUNCTION TRUTH TABLE

Current State	/S	/RAS	/CAS	/WE	Address	Command	Action	Notes
IDLE	H	X	X	X	X	DESEL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	BA	TERM	ILLEGAL	2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	Bank Active, Latch RA	
	L	L	H	L	BA, A10	PRE / PREA	NOP	4
	L	L	L	H	X	REFA	Auto-Refresh	5
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set	5
ROW ACTIVE	H	X	X	X	X	DESEL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	BA	TERM	NOP	
	L	H	L	H	BA, CA, A10	READ / READA	Begin Read, Latch CA, Determine Auto-Precharge	
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Begin Write, Latch CA, Determine Auto-Precharge	
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	Precharge / Precharge All	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
READ (Auto-Precharge Disabled)	H	X	X	X	X	DESEL	NOP (Continue Burst to END)	
	L	H	H	H	X	NOP	NOP (Continue Burst to END)	
	L	H	H	L	BA	TERM	Terminate Burst	
	L	H	L	H	BA, CA, A10	READ / READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge	3
	L	H	L	L	BA, CA, A10	WRITE WRITEA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	Terminate Burst, Precharge	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

FUNCTION TRUTH TABLE (continued)

Current State	/S	/RAS	/CAS	/WE	Address	Command	Action	Notes
WRITE (Auto-Precharge Disabled)	H	X	X	X	X	DESEL	NOP (Continue Burst to END)	
	L	H	H	H	X	NOP	NOP (Continue Burst to END)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ / READA	Terminate Burst, Latch CA, Begin Read, Determine Auto-Precharge	3
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto-Precharge	3
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	Terminate Burst, Precharge	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
READ with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)	
	L	H	H	H	X	NOP	NOP (Continue Burst to END)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ / READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	PRECHARGE/ILLEGAL	2
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
WRITE with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)	
	L	H	H	H	X	NOP	NOP (Continue Burst to END)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ / READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	PRECHARGE/ILLEGAL	2
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

FUNCTION TRUTH TABLE (continued)

Current State	/S	/RAS	/CAS	/WE	Address	Command	Action	Notes
PRE - CHARGING	H	X	X	X	X	DESEL	NOP (Idle after tRP)	
	L	H	H	H	X	NOP	NOP (Idle after tRP)	
	L	H	H	L	BA	TERM	ILLEGAL	2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	NOP (Idle after tRP)	4
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
ROW ACTIVATING	H	X	X	X	X	DESEL	NOP (Row Active after tRCD)	
	L	H	H	H	X	NOP	NOP (Row Active after tRCD)	
	L	H	H	L	BA	TERM	ILLEGAL	2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL	2
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
WRITE RE-COVERING	H	X	X	X	X	DESEL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	BA	TERM	ILLEGAL	2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL	2
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

FUNCTION TRUTH TABLE (continued)

Current State	/S	/RAS	/CAS	/WE	Address	Command	Action	Notes
RE-FRESHING	H	X	X	X	X	DESEL	NOP (Idle after tRC)	
	L	H	H	H	X	NOP	NOP (Idle after tRC)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
MODE REGISTER SETTING	H	X	X	X	X	DESEL	NOP (Idle after tRSC)	
	L	H	H	H	X	NOP	NOP (Idle after tRSC)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

ABBREVIATIONS:
H=High Level, L=Low Level, X=Don't Care
BA=Bank Address, RA=Row Address, CA=Column Address, NOP=No Operation

NOTES:
1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.

ILLEGAL = Device operation and/or data-integrity are not guaranteed.

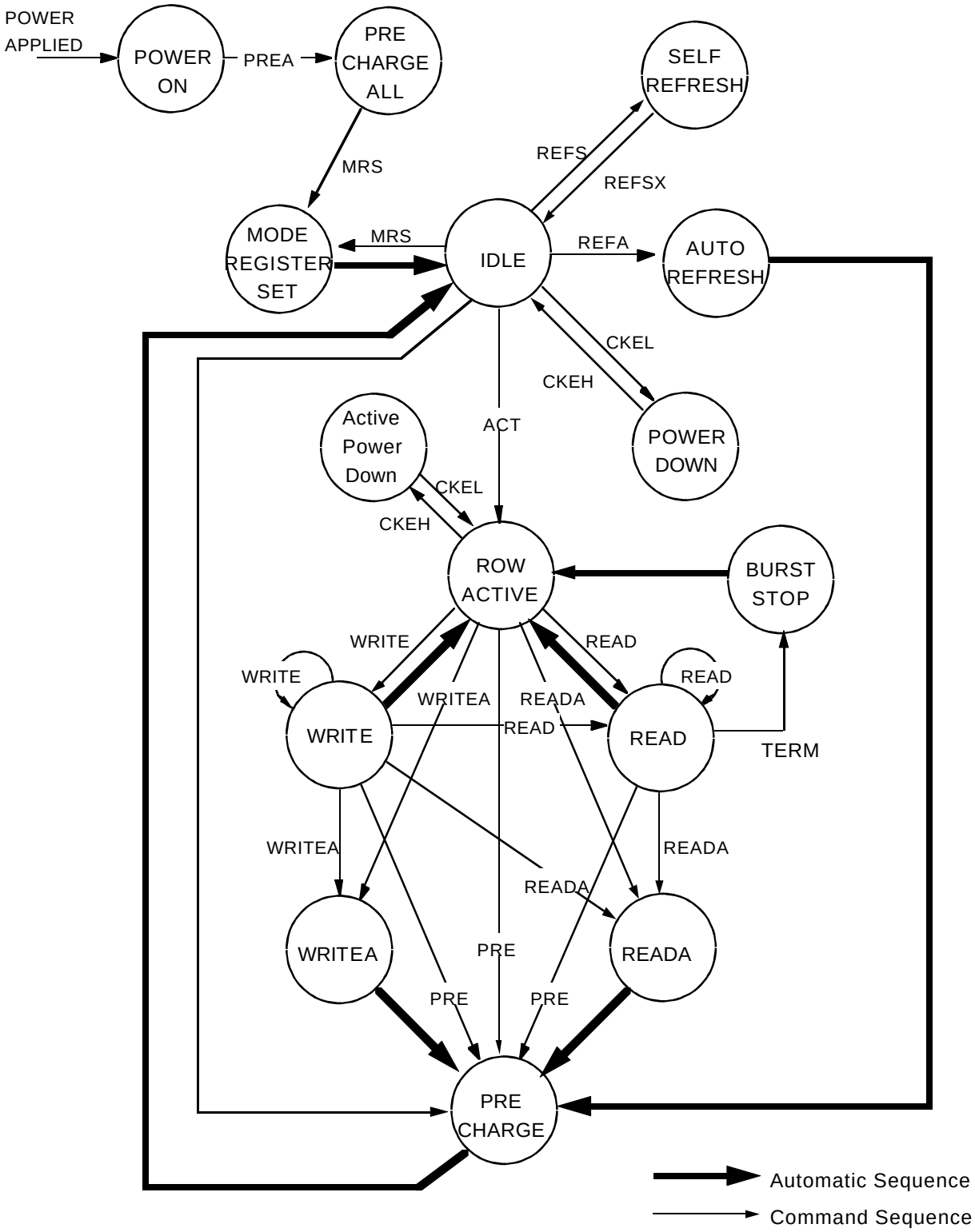
FUNCTION TRUTH TABLE for CKE

Current State	CKE0 n-1	CKE0 n	/S0	/RAS	/CAS	/WE	Add	Action	Notes
SELF-REFRESH	H	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	Exit Self-Refresh (Idle after tRC)	1
	L	H	L	H	H	H	X	Exit Self-Refresh (Idle after tRC)	1
	L	H	L	H	H	L	X	ILLEGAL	1
	L	H	L	H	L	X	X	ILLEGAL	1
	L	H	L	L	X	X	X	ILLEGAL	1
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)	1
POWER DOWN	H	X	X	X	X	X	X	INVALID	
	L	H	X	X	X	X	X	Exit Power Down to Idle	
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)	
ALL BANKS IDLE	H	H	X	X	X	X	X	Refer to Function Truth Table	2
	H	L	L	L	L	H	X	Enter Self-Refresh	2
	H	L	H	X	X	X	X	Enter Power Down	2
	H	L	L	H	H	H	X	Enter Power Down	2
	H	L	L	H	H	L	X	ILLEGAL	2
	H	L	L	H	L	X	X	ILLEGAL	2
	H	L	L	L	X	X	X	ILLEGAL	2
	L	X	X	X	X	X	X	Refer to Current State =Power Down	2
ANY STATE other than listed above	H	H	X	X	X	X	X	Refer to Function Truth Table	
	H	L	X	X	X	X	X	Begin CLK Suspend at Next Cycle	3
	L	H	X	X	X	X	X	Exit CLK Suspend at Next Cycle	3
	L	L	X	X	X	X	X	Maintain CLK Suspend	

ABBREVIATIONS:
H=High Level, L=Low Level, X=Don't Care

NOTES:
1. CKE Low to High transition will re-enable CK0 and other inputs **asynchronously**
. A minimum setup time must be satisfied before any command other than EXIT.
2. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
3. Must be legal command.

SIMPLIFIED STATE DIAGRAM



POWER ON SEQUENCE

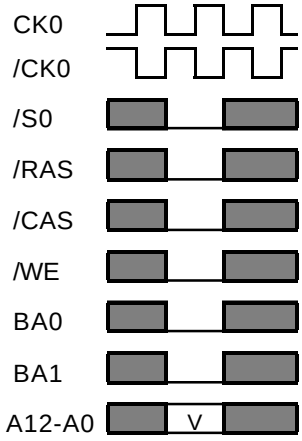
Before starting normal operation, the following power on sequence is necessary to prevent a SDRAM from damaged or multifunctioning.

1. Apply VDD before or the same time as VDDQ
2. Apply VDDQ before or at the same time as VTT & Vref
3. Maintain stable condition for 200us after stable power and CLK, apply NOP or DSEL
4. Issue precharge command for all banks of the device
5. Issue EMRS
6. Issue MRS for the Mode Register and to reset the DLL
7. Issue 2 or more Auto Refresh commands
8. Maintain stable condition for 200 cycle

After these sequence, the SDRAM is idle state and ready for normal operation.

MODE REGISTER

Burst Length, Burst Type and /CAS Latency can be programmed by setting the mode register (MRS). The mode register stores these data until the next MRS command, which may be issued when all banks in discrete are in idle state. After tMRD from a MRS command, the DDR DIMM is ready for new command.



BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	DR	0	LTMODE			BT	BL		

	CL	/CAS Latency
Latency Mode	0 0 0	R
	0 0 1	R
	0 1 0	2
	0 1 1	R
	1 0 0	R
	1 0 1	R
	1 1 0	2.5
	1 1 1	R

	BL	BT= 0	BT= 1
Burst Length	0 0 0	R	R
	0 0 1	2	2
	0 1 0	4	4
	0 1 1	8	8
	1 0 0	R	R
	1 0 1	R	R
	1 1 0	R	R
	1 1 1	R	R

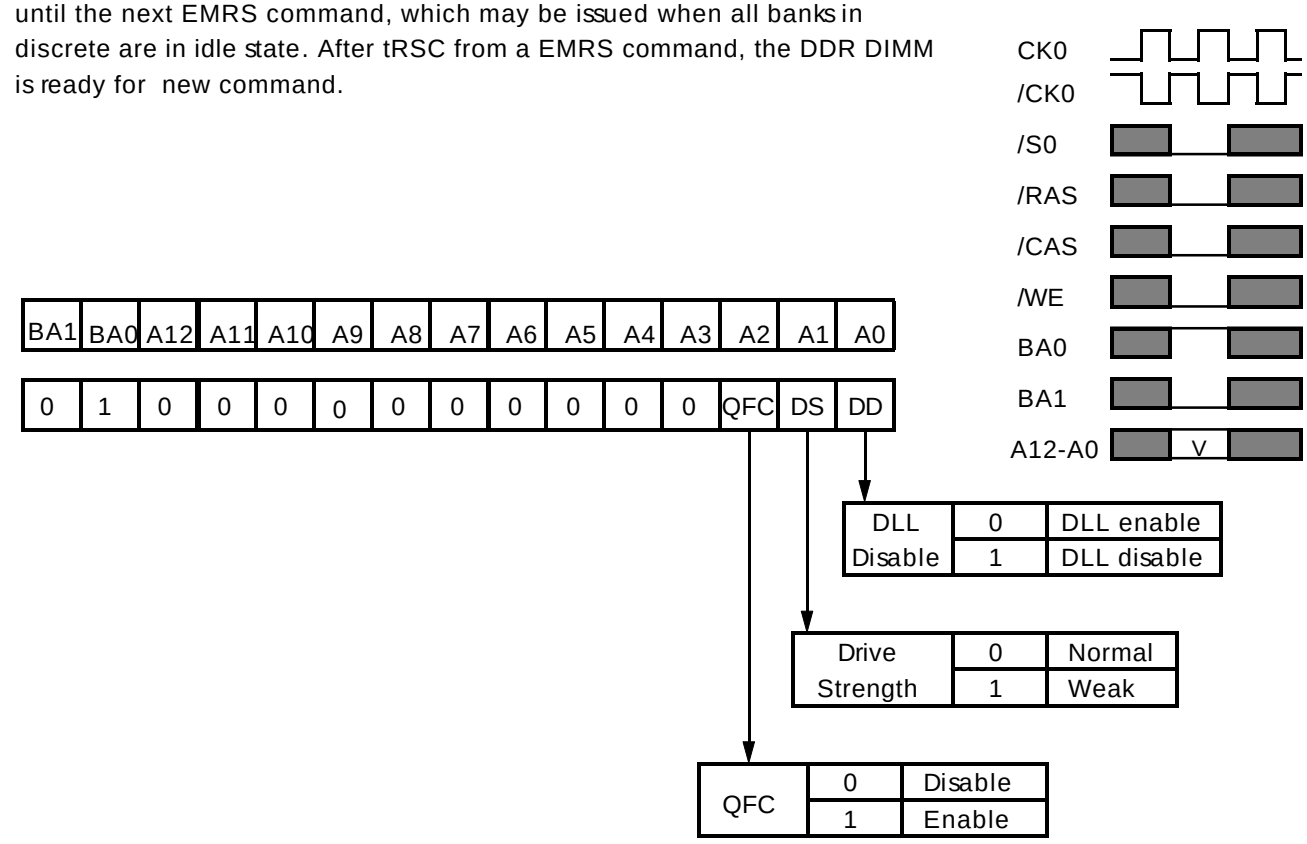
Burst Type	0	Sequential
	1	Interleaved

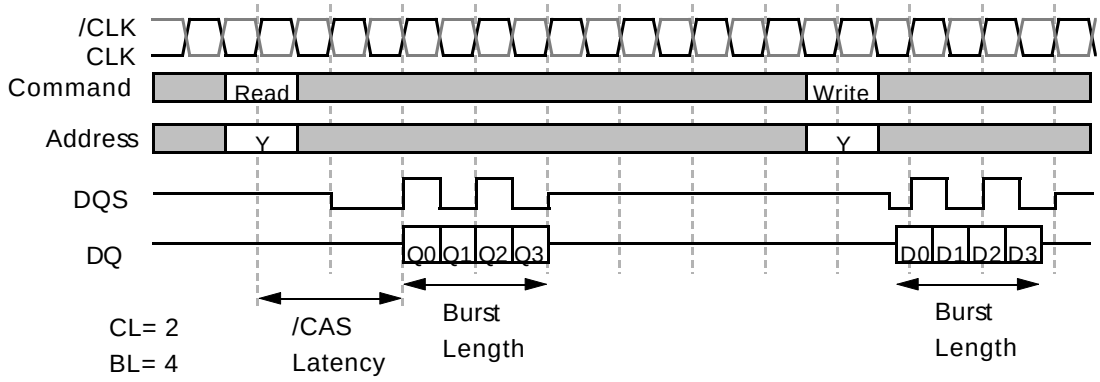
DLL Reset	0	NO
	1	YES

R: Reserved for Future Use

EXTENDED MODE REGISTER

DLL disable / enable mode can be programmed by setting the extended mode register (EMRS). The extended mode register stores these data until the next EMRS command, which may be issued when all banks in discrete are in idle state. After tRSC from a EMRS command, the DDR DIMM is ready for new command.





Initial Address			BL	Column Addressing															
A2	A1	A0		Sequential								Interleaved							
0	0	0	8	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1		1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0		2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1		3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0		4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1		5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0		6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1		7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0
-	0	0	4	0	1	2	3					0	1	2	3				
-	0	1		1	2	3	0					1	0	3	2				
-	1	0		2	3	0	1					2	3	0	1				
-	1	1		3	0	1	2					3	2	1	0				
-	-	0	2	0	1							0	1						
-	-	1		1	0							1	0						

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vdd	Supply Voltage	with respect to Vss	-0.5 ~ 3.7	V
VI	Input Voltage	with respect to Vss	-0.5 ~ Vdd+0.5	V
VO	Output Voltage	with respect to Vss	-0.5 ~ Vdd+0.5	V
IO	Output Current		50	mA
Pd	Power Dissipation	Ta = 25°C	16	W
Topr	Operating Temperature		0 ~ 70	°C
Tstg	Storage Temperature		-45 ~ 100	°C

DC OPERATING CONDITIONS

(Ta=0 ~ 70°C , unless otherwise noted)

Symbol	Parameter	Limits			Unit	Notes
		Min.	Typ.	Max.		
Vdd	Supply Voltage	2.3	2.5	2.7	V	
Vref	Input Reference Voltage	0.49*Vdd	0.5*Vdd	0.51*Vdd	V	5
VIH(DC)	High-Level Input Voltage	Vref + 0.18		Vdd+0.3	V	
VIL(DC)	Low-Level Input Voltage	-0.3		Vref - 0.18	V	
VIN(DC)	Input Voltage Level, CK0 and /CK0	-0.3		Vdd + 0.3	V	
VID(DC)	Input Differential Voltage, CK0 and /CK0	0.36		Vdd + 0.6	V	7
VTT	I/O Termination Voltage	Vref - 0.04		Vref + 0.04	V	6

CAPACITANCE

(Ta=0 ~ 70°C , Vdd = VddQ = 2.5 ± 0.2V, Vss = VssQ = 0V, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits(max.)	Unit	Notes
CI(A)	Input Capacitance, address pin	VI - 1.25V f=100MHz VI = 25mVrm	80	pF	11
CI(C)	Input Capacitance, control pin		80	pF	11
CI(K)	Input Capacitance, CK0 pin		45	pF	11
CI/O	Input Capacitance, I/O pin		20	pF	11

AVERAGE SUPPLY CURRENT from Vdd

(Ta=0 ~ 70°C , Vdd = VddQ = 2.5 ± 0.2V, Vss = VssQ = 0V, Output Open, unless otherwise noted)

Symbol	Parameter/Test Conditions	Limits(max)		Unit	Notes
		-75	-10		
IDD0	OPERATING CURRENT: One Bank(Discrete); Active-Precharge; t RC = t RC MIN; t CK = t CK MIN; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1480	1400	mA	
IDD1	OPERATING CURRENT: One Bank(Discrete); Active-Read-Precharge; Burst = 2; t RC = t RC MIN; CL = 2.5; t CK = t CK MIN; IOUT= 0 mA;Address and control inputs changing once per clock cycle	1520	1440	mA	
IDD2P	PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; power-down mode; CKE≦VIL (MAX); t CK = t CK MIN	320	320	mA	
IDD2N	IDLE STANDBY CURRENT: /CS > VIH (MIN); All banks idle; CKE > VIH (MIN); t CK = t CK MIN; Address and other control inputs changing once per clock cycle	640	640	mA	
IDD3P	ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; power-down mode; CKE≦VIL (MAX); t CK = t CK MIN	480	480	mA	
IDD3N	ACTIVE STANDBY CURRENT: /CS > VIH (MIN); CKE > VIH (MIN); One bank; Active-Precharge; t RC = t RAS MAX; t CK = t CK MIN; DQ,DM and DQS inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	1040	960	mA	
IDD4R	OPERATING CURRENT: Burst = 2; Reads; Continuous burst;One bank active(Discrete); Address and control inputs changing once per clock cycle; CL = 2.5; t CK = t CK MIN; IOUT = 0 mA	1960	1840	mA	
IDD4W	OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active(Discrete); Address and control inputs changing once per clock cycle; CL = 2.5; t CK = t CK MIN; DQ, DM and DQS inputs changing twice per clock cycle	1920	1800	mA	
IDD5	AUTO REFRESH CURRENT: t RC = t RFC (MIN)	2960	2800	mA	
IDD6	SELF REFRESH CURRENT: CKE≦0.2V	48	48	mA	9

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Ta=0 ~ 70°C , Vdd = VddQ = 2.5 ± 0.2V, Vss =VssQ= 0V, unless otherwise noted)

Symbol	Parameter/Test Conditions	Limits		Unit	Notes
		Min.	Max.		
VIH(AC)	High-Level Input Voltage (AC)	Vref + 0.35		V	
VIL(AC)	Low-Level Input Voltage (AC)		Vref - 0.35	V	
VID(AC)	Input Differential Voltage, CLK and /CLK	0.7	Vdd + 0.6	V	7
VIX(AC)	Input Crossing Point Voltage, CLK and /CLK	0.5*Vdd-0.2	0.5*Vdd+0.2	V	8
IOZ	Off-state Output Current /Q floating Vo=0~V_{DD}Q	-10	10	µA	
Ii	Input Current / VIN=0 ~ VddQ	-32	32	µA	

AC TIMING REQUIREMENTS (Component Level)

(Ta=0 ~ 70°C , Vdd = VddQ = 2.5 ± 0.2V, Vss = VssQ = 0V, unless otherwise noted)

	AC Characteristics		-75		-10			
Symbol	Parameter		Min.	Max.	Min.	Max.	Unit	Notes
tAC	DQ Output Valid data delay time from CLK//CLK		-0.75	+0.75	-0.8	+0.8	ns	
tDQSCK	DQ Output Valid data delay time from CLK//CLK		-0.75	+0.75	-0.8	+0.8	ns	
tCH	CLK High level width		0.45	0.55	0.45	0.55	tCK	
tCL	CLK Low level width		0.45	0.55	0.45	0.55	tCK	
tCK	CLK cycle time	CL=2.5	7.5	15	8	15	ns	
		CL=2	10	15	10	15	ns	
tDS	Input Setup time (DQ,DM)		0.5		0.6		ns	
tDH	Input Hold time(DQ,DM)		0.5		0.6		ns	
tDIPW	DQ and DM input pulse width (for each input)		1.75		2		ns	
tHZ	Data-out-high impedance time from CLK//CLK		-0.75	+0.75	-0.8	+0.8	ns	14
tLZ	Data-out-low impedance time from CLK//CLK		-0.75	+0.75	-0.8	+0.8	ns	14
tDQSQ	DQ Valid data delay time from DQS			+0.5		+0.6	ns	
tHP	Clock half period		tCLmin or tCHmin		tCLmin or tCHmin		ns	
tQH	Output DQS valid window		tHP-0.75		tHP-1.0		ns	
tDQSS	Write command to first DQS latching transition		0.75	1.25	0.75	1.25	tCK	
tDQSH	DQS input High level width		0.35		0.35		tCK	
tDQSL	DQS input Low level width		0.35		0.35		tCK	
tDSS	DQS falling edge to CLK setup time		0.2		0.2		tCK	
tDSH	DQS falling edge hold time from CLK		0.2		0.2		tCK	
tMRD	Mode Register Set command cycle time		15		15		ns	
tWPRES	Write preamble setup time		0		0		ns	16
tWPST	Write postamble		0.4	0.6	0.4	0.6	tCK	15
tWPRE	Write preamble		0.25		0.25		tCK	
tIS	Input Setup time (address and control)		0.9		1.1		ns	19
tIH	Input Hold time (address and control)		0.9		1.1		ns	19
tRPST	Read postamble		0.4	0.6	0.4	0.6	tCK	
tRPRE	Read preamble		0.9	1.1	0.9	1.1	tCK	

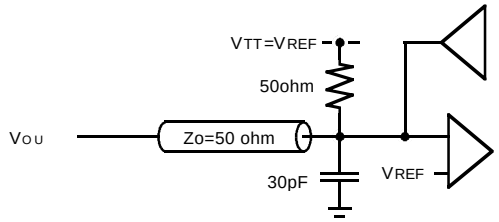
AC TIMING REQUIREMENTS(Continues)

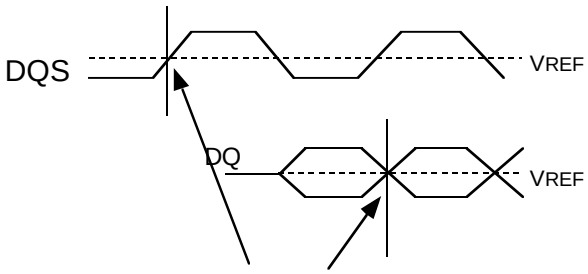
(Ta=0 ~ 70°C , Vdd = VddQ = 2.5 ± 0.2V, Vss = VssQ = 0V, unless otherwise noted)

	AC Characteristics	-75		-10			
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit	Notes
tRAS	Row Active time	45	120,000	50	120,000	ns	
tRC	Row Cycle time(operation)	65		70		ns	
tRFC	Auto Ref. to Active/Auto Ref. command period	75		80		ns	
tRCD	Row to Column Delay	20		20		ns	
tRP	Row Precharge time	20		20		ns	
tRRD	Act to Act Delay time	15		15		ns	
tWR	Write Recovery time	15		15		ns	
tDAL	Auto Precharge write recovery + precharge time	35		35		ns	
tWTR	Internal Write to Read Command Delay	1		1		tCK	
tXSNR	Exit Self Ref. to non-Read command	75		80		ns	
tXSRD	Exit Self Ref. to -Read command	200		200		tCK	
tXPNR	Exit Power down to command	1		1		tCK	
tXPRD	Exit Power down to -Read command	1		1		tCK	18
tREFI	Average Periodic Refresh interval	7.8		7.8		us	17

Output Load Condition

(for component measurement)





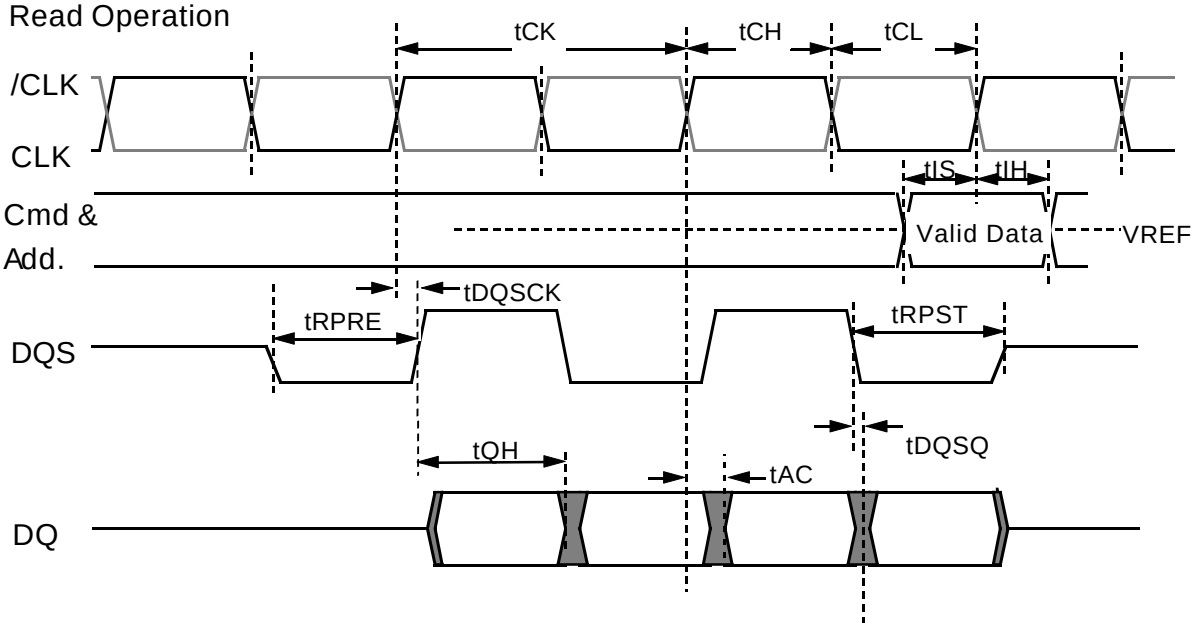
Output Timing Measurement Reference Point

Notes

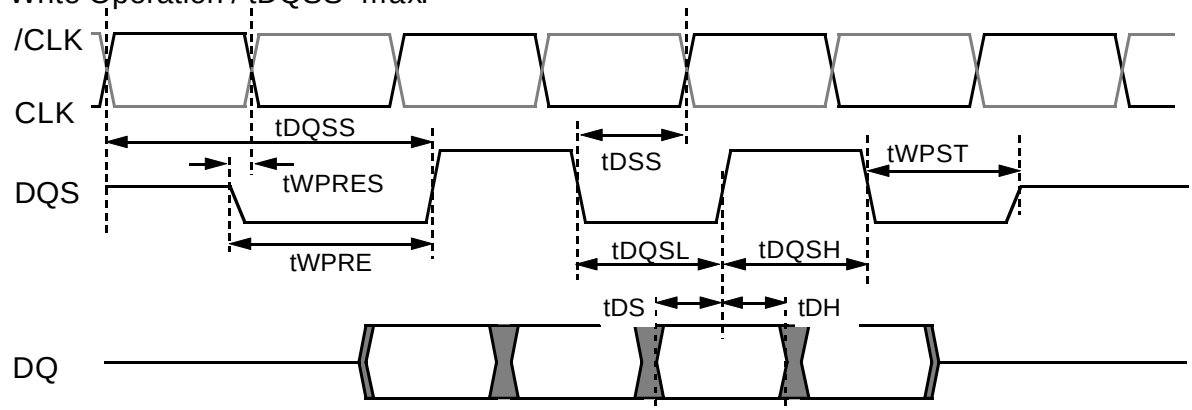
1. All voltages referenced to Vss.
2. Tests for AC timing, IDD, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. AC timing and IDD tests may use a VIL to VIH swing of up to 1.5V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK//CK), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between VIL(AC) and VIH(AC).
4. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.
5. VREF is expected to be equal to 0.5*VddQ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed +/-2% of the DC value.
6. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF.
7. VID is the magnitude of the difference between the input level on CLK and the input level on /CLK.
8. The value of VIX is expected to equal 0.5*VddQ of the transmitting device and must track variations in the DC level of the same.
9. Enables on-chip refresh and address counters.
10. IDD specification are tested after the device is properly initialized.
11. This parameter is sampled. VddQ = +2.5V+/-0.2V, Vdd = +2.5V+/-0.2V, f =100MHz, Ta = 25°C , VOUT(DC)= VddQ/2, VOUT(PEAK TO PEAK) = 25mV, DM inputs are grouped with I/O pins - reflecting the fact that they are matched in laoding (to faciliate trace matching at the board level).
12. The CLK//CLK input reference level (for timing referenced to CLK//CLK) is the point at which CLK and /CLK cross; the input reference level for signals other than CLK//CLK, is VREF.
13. Inputs are not recognized as valid until VREF stabilized. Exception: during the period before VREF stabilizes, CKE=< 0.3VddQ is recognized as LOW.
14. t HZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ), or begins driving (LZ).
15. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
16. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CLK edge. A valid transition is defined as monotonic, and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
17. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
18. tXPRD should be 200 tCLK in the condition of the unstable CLK operation during the power down mode.
19. For command/address and CLK & /CLK slew rate ≥1.0V/ns.

(Component Level)

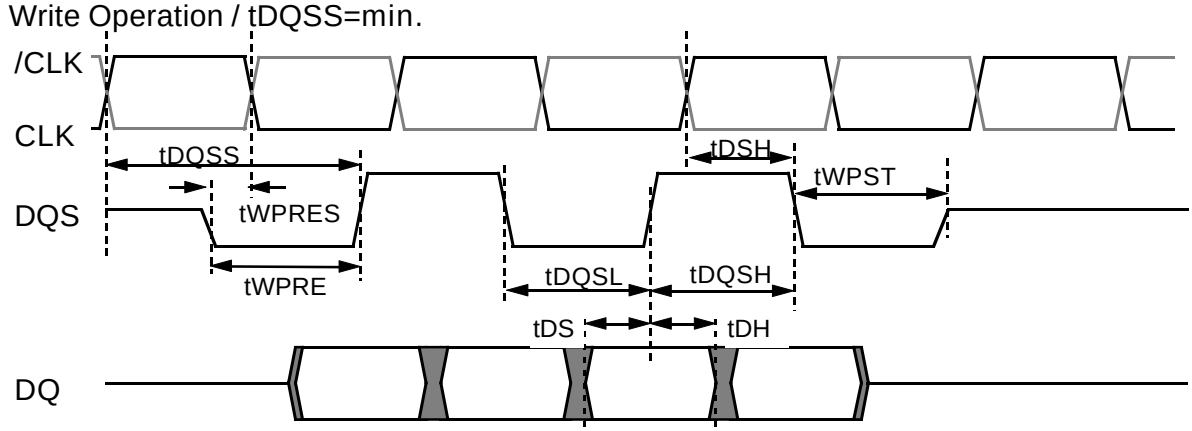
Read Operation



Write Operation / tDQSS=max.



Write Operation / tDQSS=min.



OPERATIONAL DESCRIPTION (Component Level)

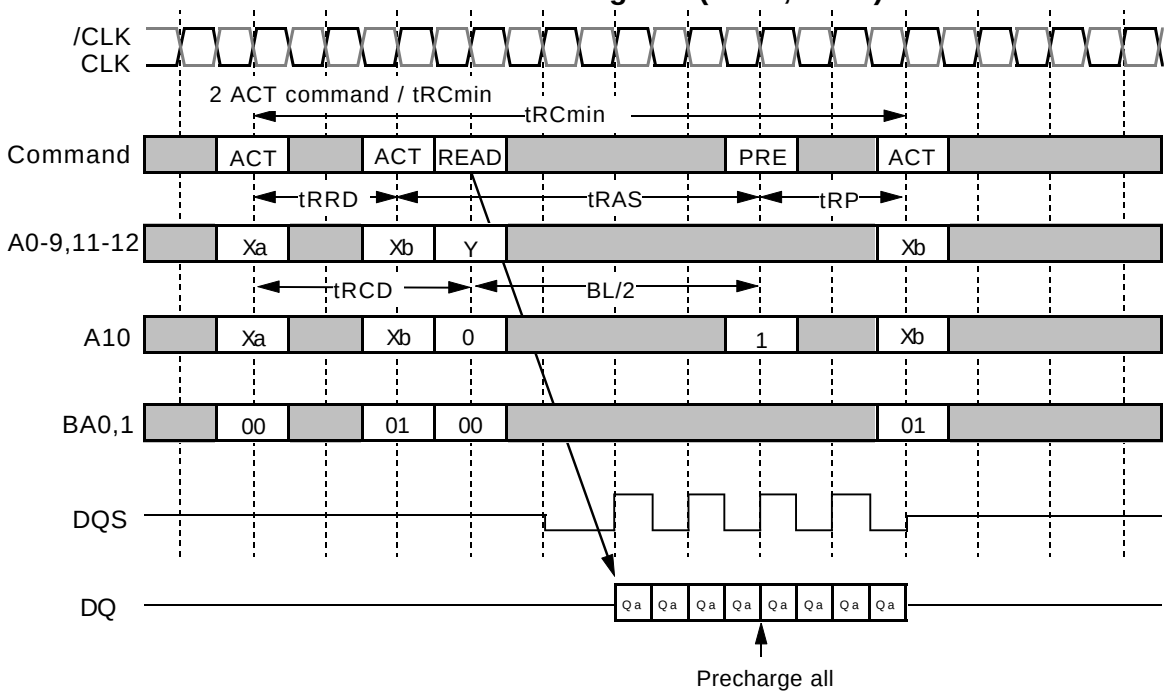
BANK ACTIVATE

The DDR SDRAM has four independent banks. Each bank is activated by the ACT command with the bank addresses (BA0,1). A row is indicated by the row address A12-0. The minimum activation interval between one bank and the other bank is tRRD.

PRECHARGE

The PRE command deactivates the bank indicated by BA0,1. When multiple banks are active, the precharge all command (PREA,PRE+A10=H) is available to deactivate them at the same time. After tRP from the precharge, an ACT command to the same bank can be issued.

Bank Activation and Precharge All (BL=8, CL=2)

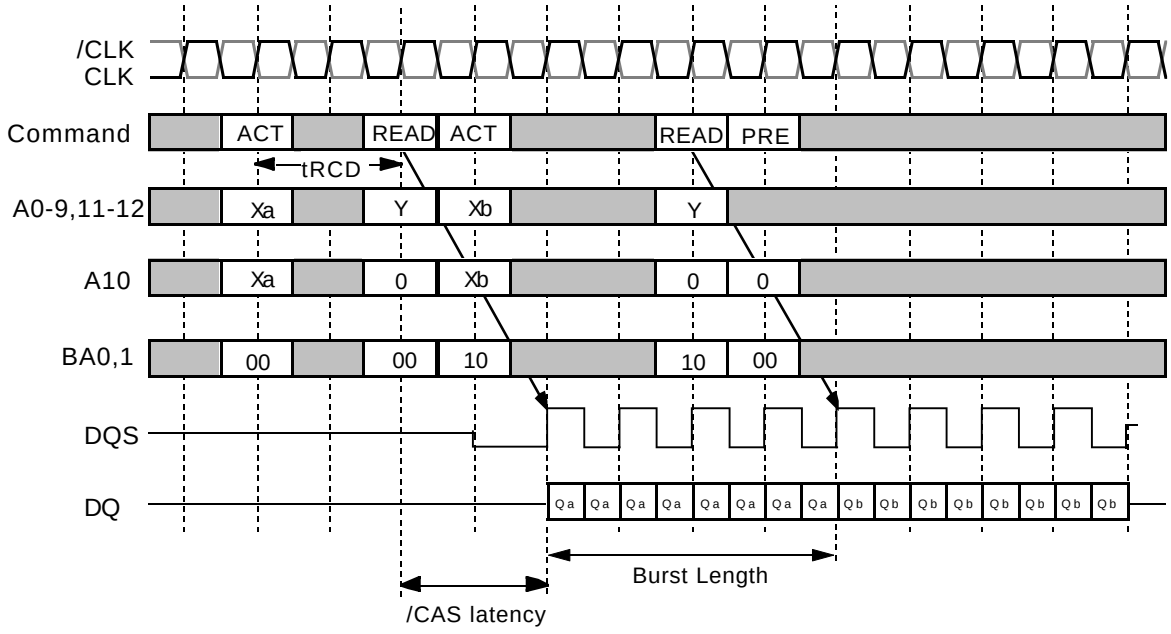


A precharge command can be issued at BL/2 from a read command without data loss.

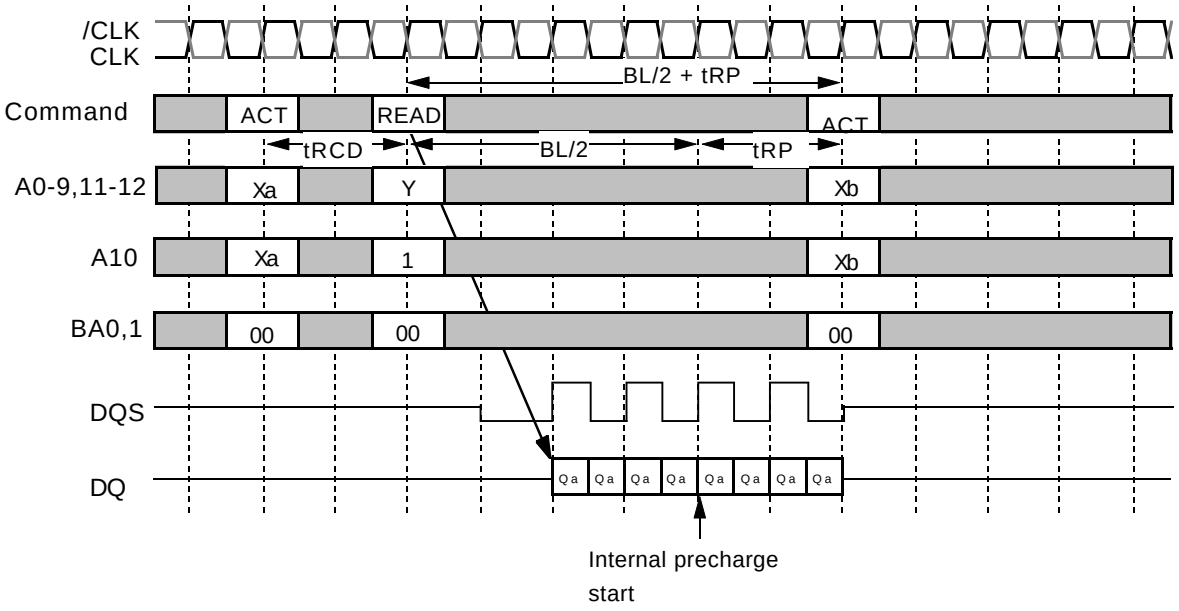
READ

After tRCD from the bank activation, a READ command can be issued. 1st Output data is available after the /CAS Latency from the READ, followed by (BL-1) consecutive data when the Burst Length is BL. The start address is specified by A9-A0, and the address sequence of burst data is defined by the Burst Type. A READ command may be applied to any active bank, so the row precharge time (tRP) can be hidden behind continuous output data by interleaving the multiple banks. When A10 is high at a READ command, the auto-precharge(READA) is performed. Any command(READ,WRITE,PRE,ACT) to the same bank is inhibited till the internal precharge is complete. The internal precharge starts at BL/2 after READA. The next ACT command can be issued after (BL/2+tRP) from the previous READA.

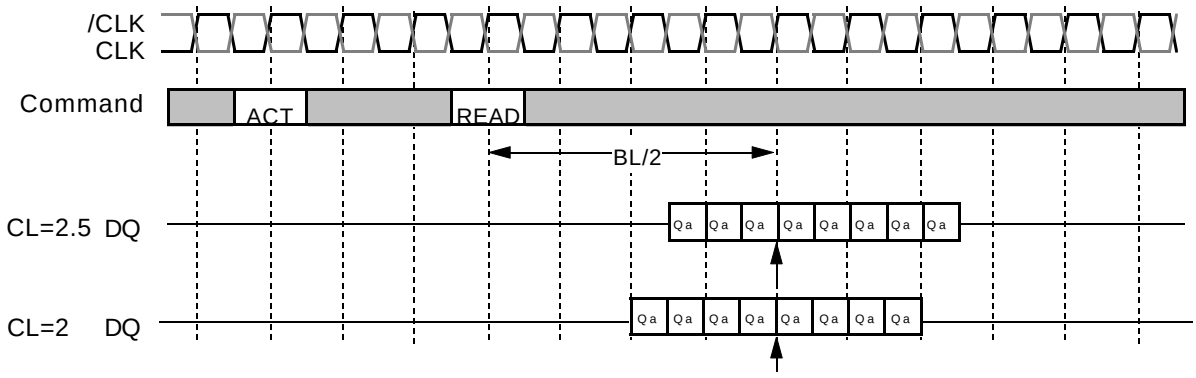
Multi Bank Interleaving READ (BL=8, CL=2)



READ with Auto-Precharge (BL=8, CL=2)



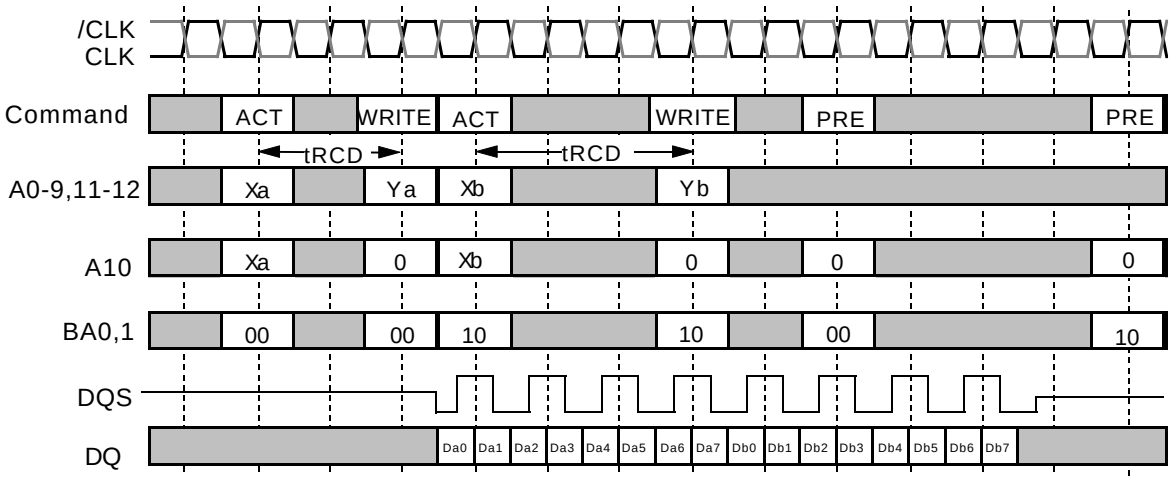
READ Auto-Precharge Timing (BL=8)



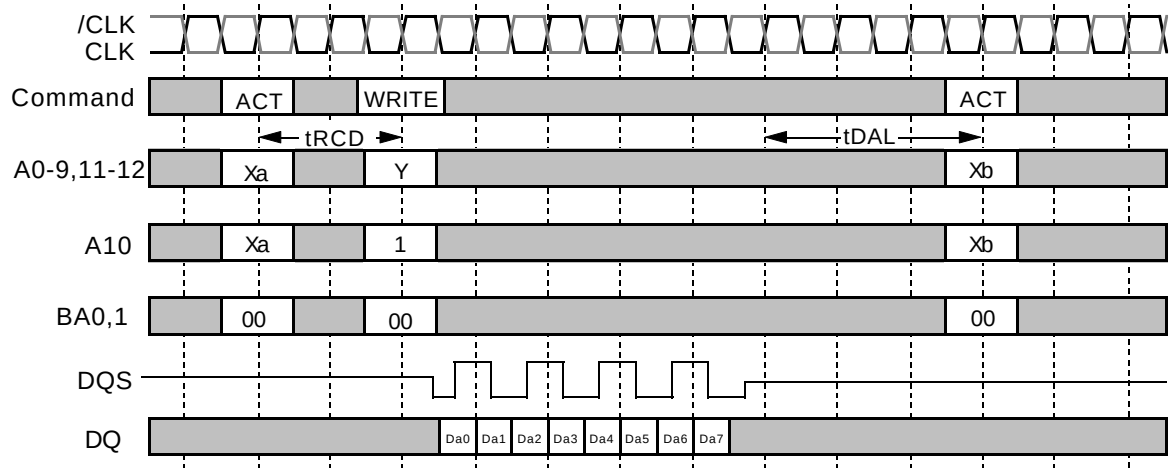
WRITE

After tRCD from the bank activation, a WRITE command can be issued. 1st input data is set from the WRITE command with data strobe input, following (BL-1) data are written into RAM, when the Burst Length is BL. The start address is specified by A9-A0, and the address sequence of burst data is defined by the Burst Type. A WRITE command may be applied to any active bank, so the row precharge time (tRP) can be hidden behind continuous input data by interleaving the multiple banks. From the last data to the PRE command, the write recovery time (tWRP) is required. When A10 is high at a WRITE command, the auto-precharge(WRITEA) is performed. Any command(READ,WRITE,PRE,ACT) to the same bank is inhibited till the internal precharge is complete. The next ACT command can be issued after tDAL from the last input data cycle.

Multi Bank Interleaving WRITE (BL=8)



WRITE with Auto-Precharge (BL=8)

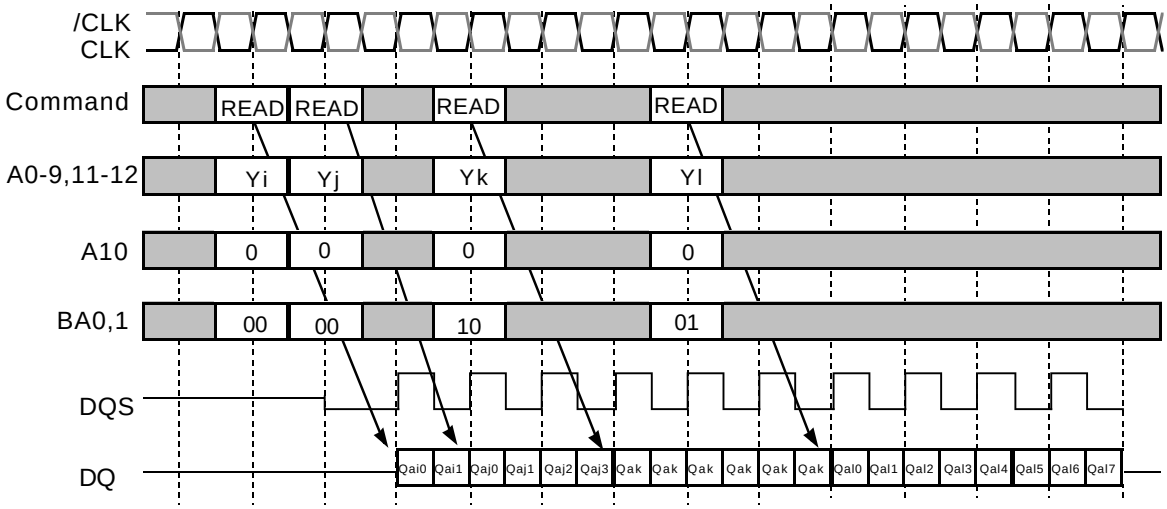


BURST INTERRUPTION

[Read Interrupted by Read]

Burst read operation can be interrupted by new read of any bank. Random column access is allowed. READ to READ interval is minimum 1CLK.

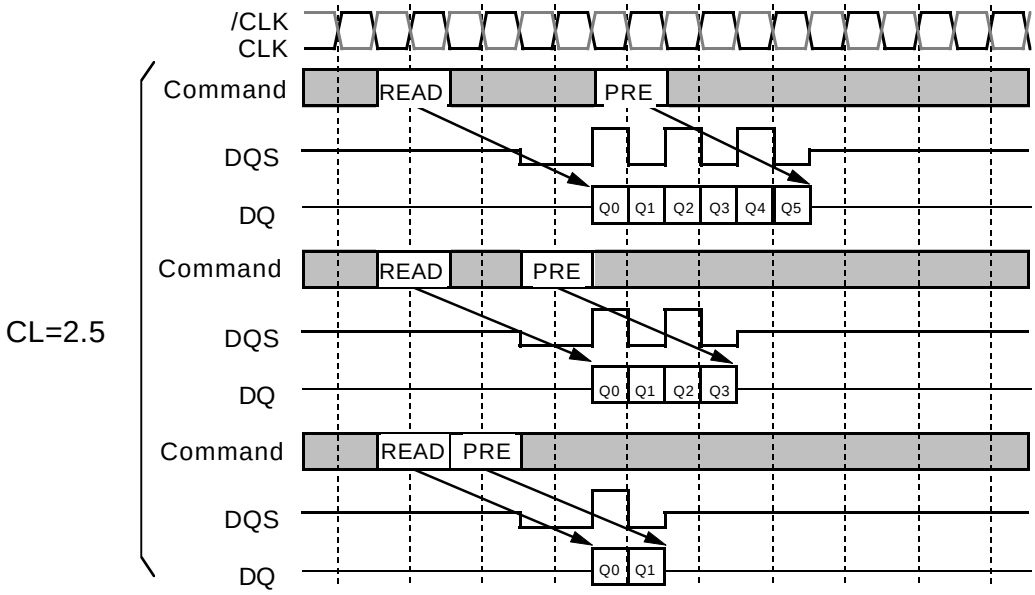
Read Interrupted by Read (BL=8, CL=2)



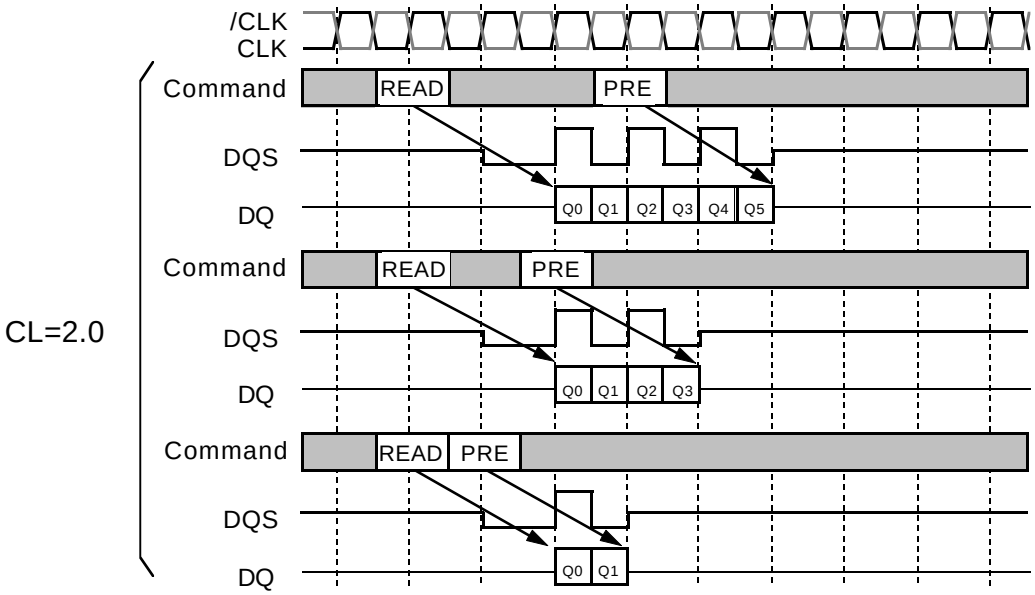
[Read Interrupted by precharge]

Burst read operation can be interrupted by precharge of the same bank. READ to PRE interval is minimum 1 CLK. A PRE command to output disable latency is equivalent to the /CAS Latency. As a result, READ to PRE interval determines valid data length to be output. The figure below shows examples of BL=8.

Read Interrupted by Precharge (BL=8)



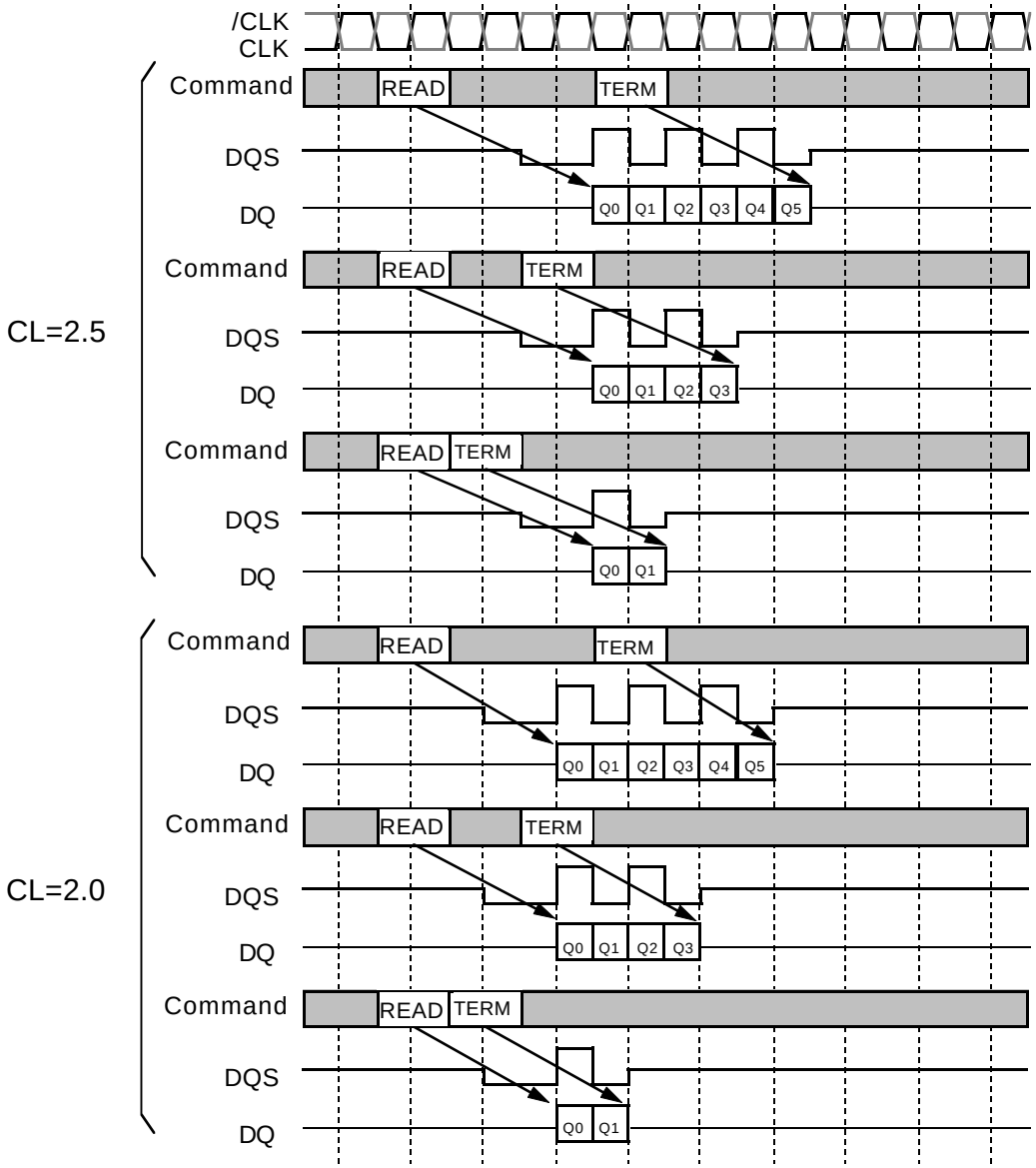
Read Interrupted by Precharge (BL=8)



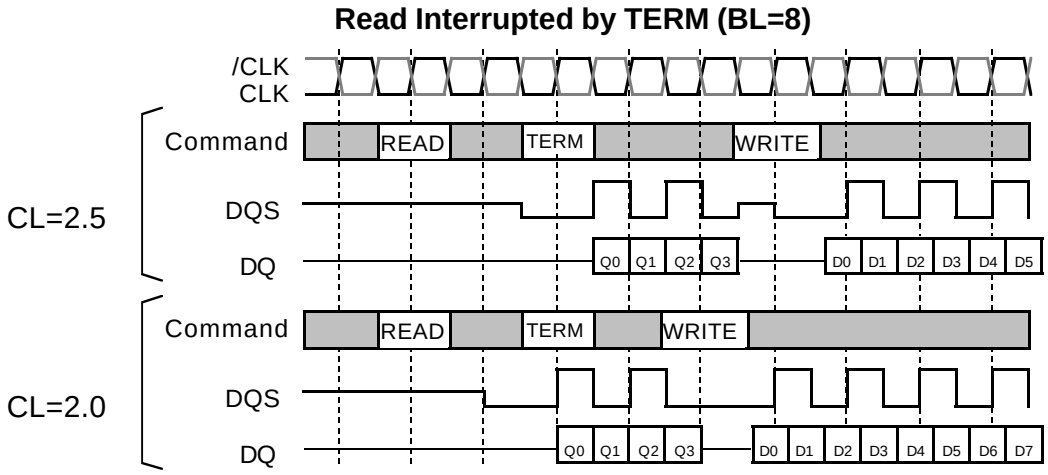
[Read Interrupted by Burst Stop]

Burst read operation can be interrupted by a burst stop command(TERM). READ to TERM interval is minimum 1 CLK. A TERM command to output disable latency is equivalent to the /CAS Latency. As a result, READ to TERM interval determines valid data length to be output. The figure below shows examples of BL=8.

Read Interrupted by TERM (BL=8)



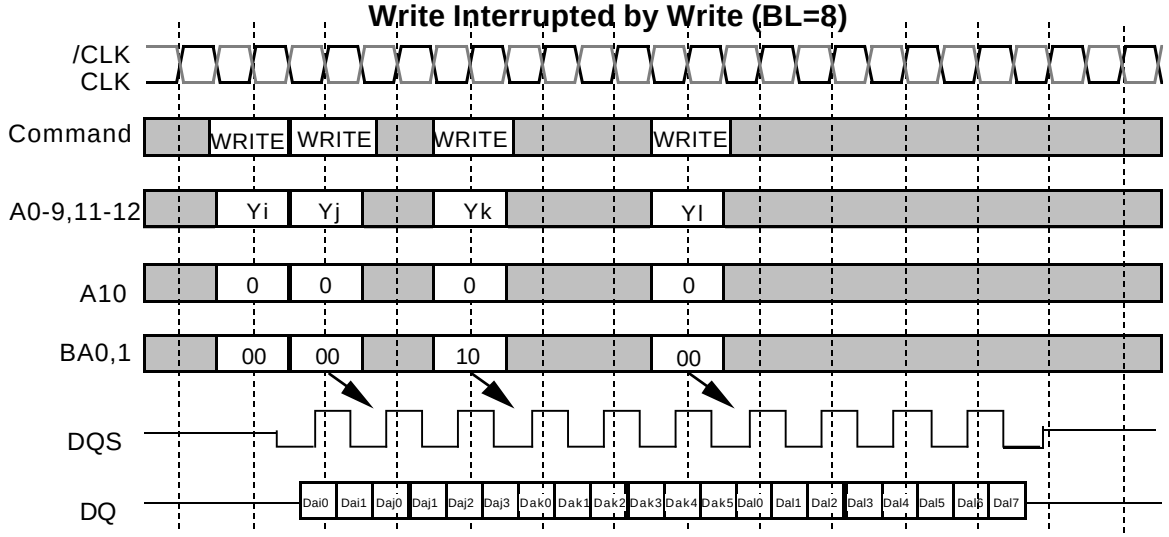
[Read Interrupted by Write with TERM]



[Write interrupted by Write]

Burst write operation can be interrupted by write of any bank. Random column access is allowed. WRITE to WRITE interval is minimum 1 CLK.

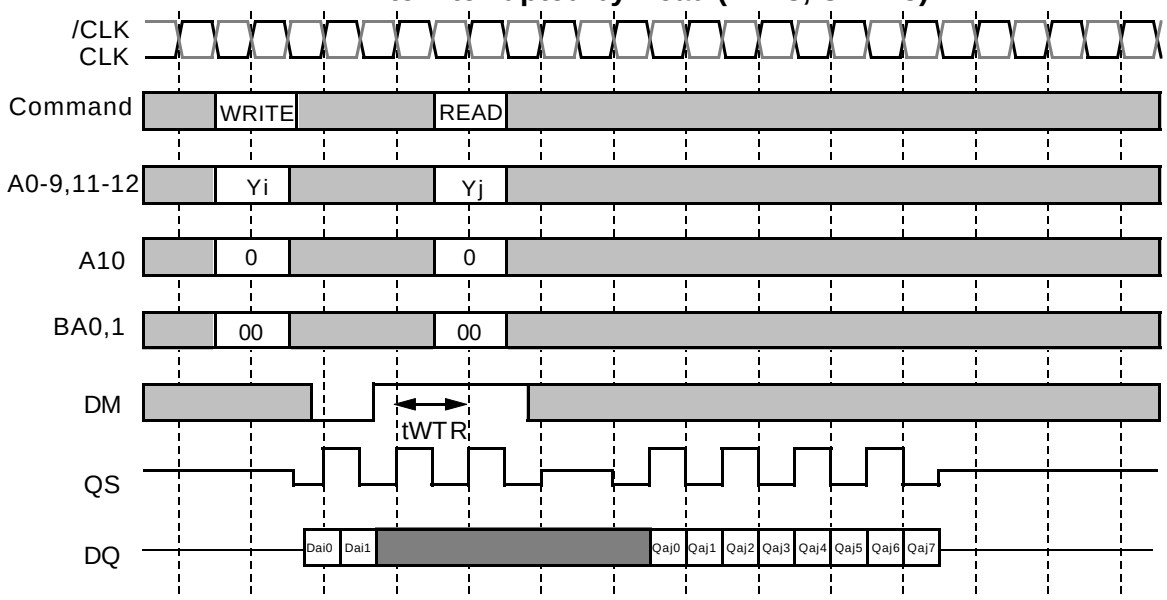
Write Interrupted by Write (BL=8)



[Write interrupted by Read]

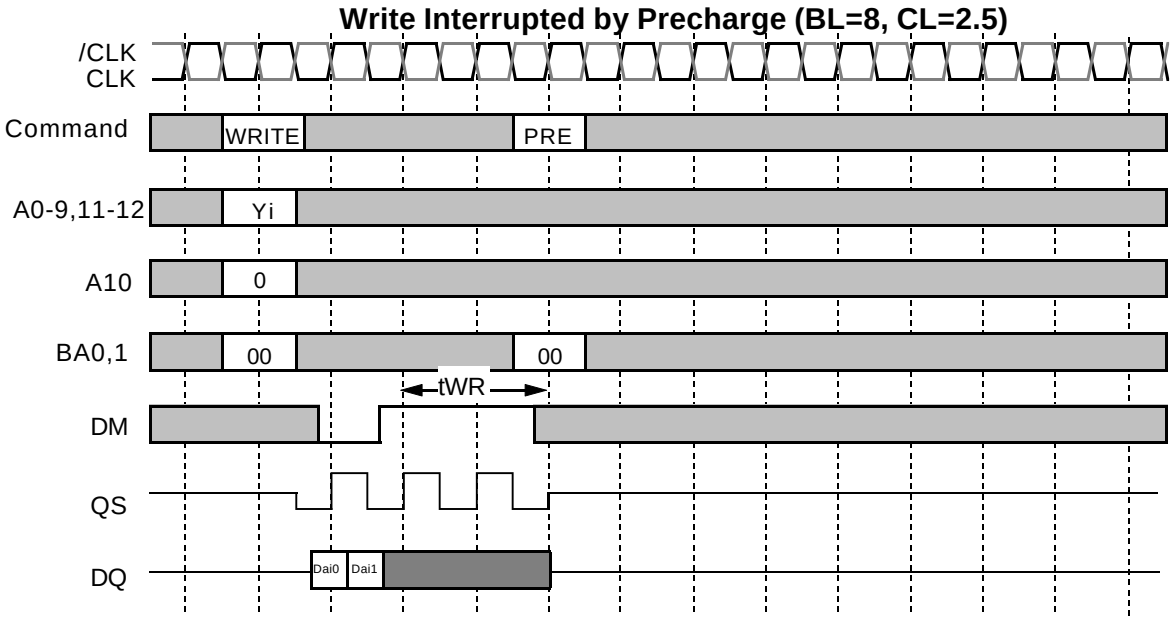
Burst write operation can be interrupted by read of the same or the other bank. Random column access is allowed. Internal WRITE to READ command interval(tWTR) is minimum 1 CLK. The input data on DQ at the interrupting READ cycle is "don't care". tWTR is referenced from the first positive edge after the last data input.

Write Interrupted by Read (BL=8, CL=2.5)

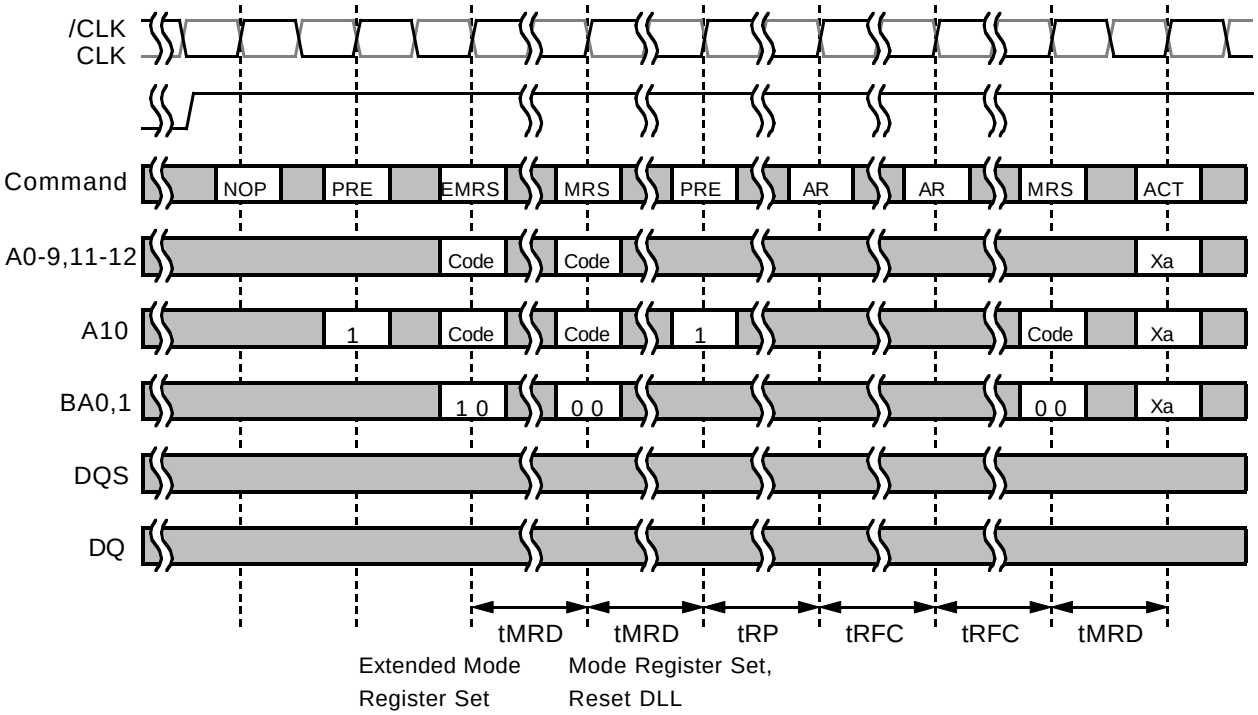


[Write interrupted by Precharge]

Burst write operation can be interrupted by precharge of the same or all bank. Random column access is allowed. tWR is referenced from the first positive CLK edge after the last data input.

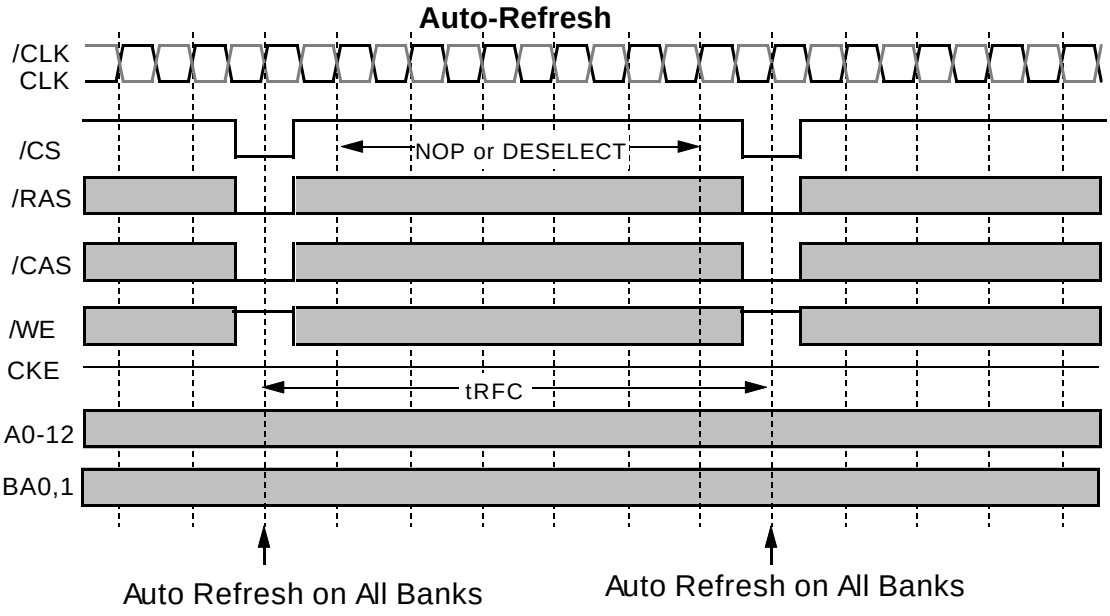


[Initialize and Mode Register sets]



[AUTO REFRESH]

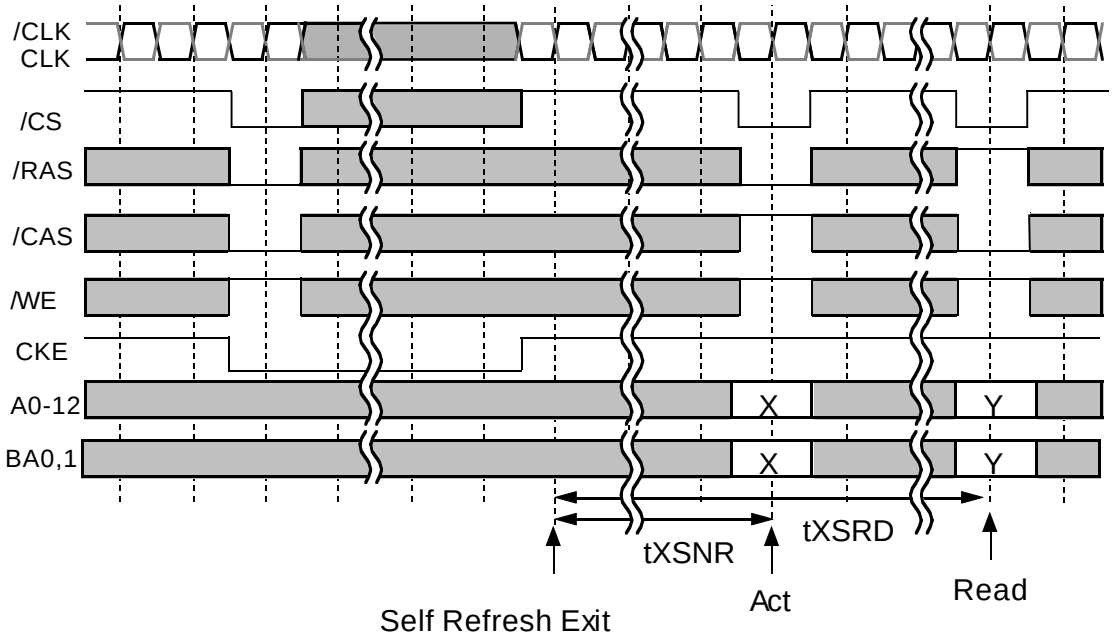
Single cycle of auto-refresh is initiated with a REFA(/CS=/RAS=/CAS=L,/WE=CKE=H) command. The refresh address is generated internally. 8192 REFA cycles within 64ms refresh 256Mbits memory cells. The auto-refresh is performed on 4 banks concurrently. Before performing an auto refresh, all banks must be in the idle state. Auto-refresh to auto-refresh interval is minimum tRFC . Any command must not be supplied to the device before tRFC from the REFA command.



[SELF REFRESH]

Self -refresh mode is entered by issuing a REFS command (/CS=/RAS=/CAS=L,/WE=H,CKE=L). Once the self-refresh is initiated, it is maintained as long as CKE is kept low. During the self-refresh mode, CKE is asynchronous and the only enable input, all other inputs including CLK are disabled and ignored, so that power consumption due to synchronous inputs is saved. To exit the self-refresh, supplying stable CLK inputs, asserting DESEL or NOP command and then asserting CKE for longer than tXSNR/tXSRD.

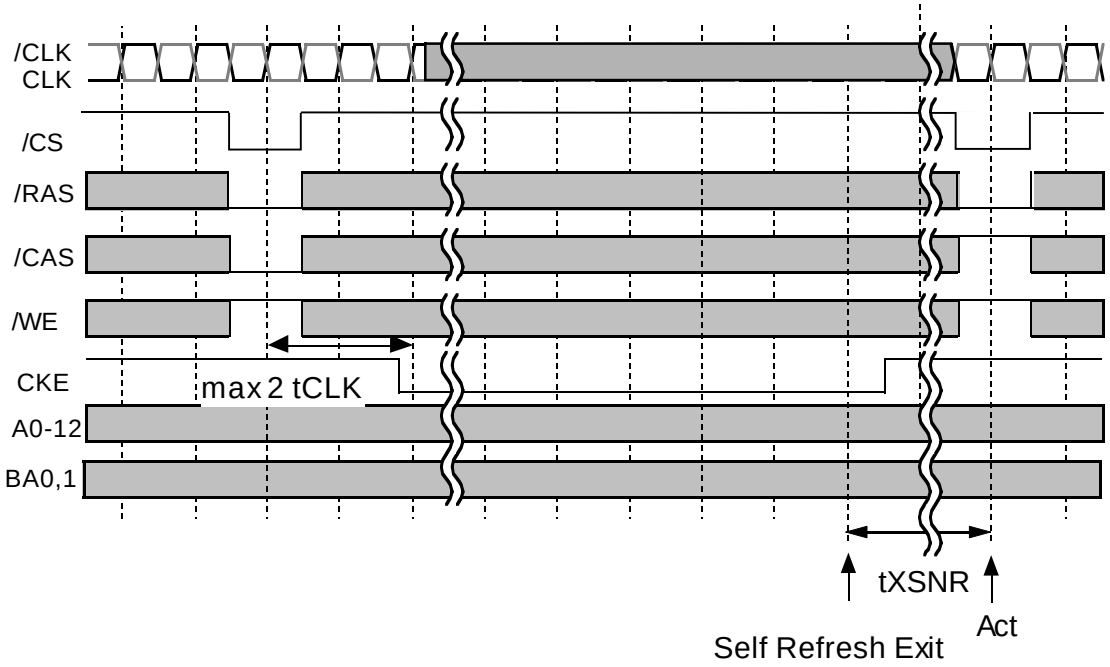
Self-Refresh



[Asynchronous SELF REFRESH]

Asynchronous Self -refresh mode is entered by CKE=L within 2 tCLK after issuing a REFA command (/CS=/RAS=/CAS=L,/WE=H). Once the self-refresh is initiated, it is maintained as long as CKE is kept low. During the self-refresh mode, CKE is asynchronous and the only enable input, all other inputs including CLK are disabled and ignored, so that power consumption due to synchronous inputs is saved. To exit the self-refresh, supplying stable CLK inputs, asserting DESEL or NOP command and then asserting CKE for longer than tXSNR/tXSRD.

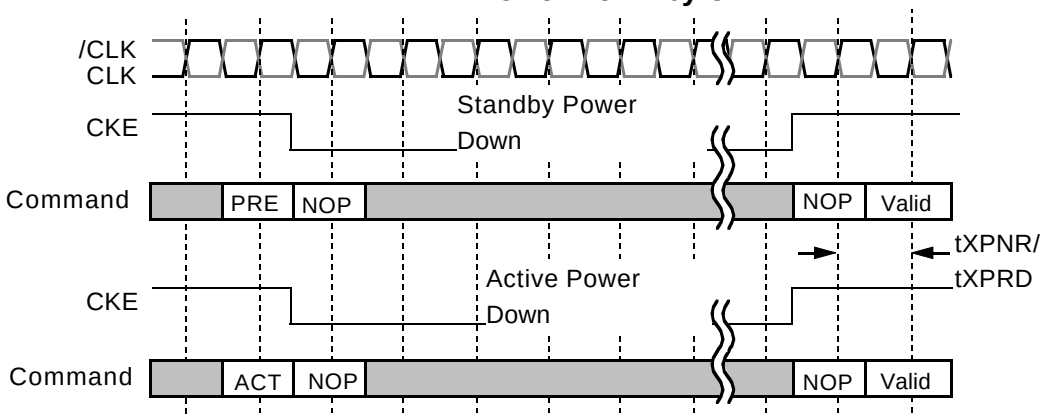
Asynchronous Self-Refresh



[Power DOWN]

The purpose of CLK suspend is power down. CKE is synchronous input except during the self-refresh mode. A command at cycle is ignored. From CKE=H to normal function, DLL recovery time is NOT required in the condition of the stable CLK operation during the power down mode.

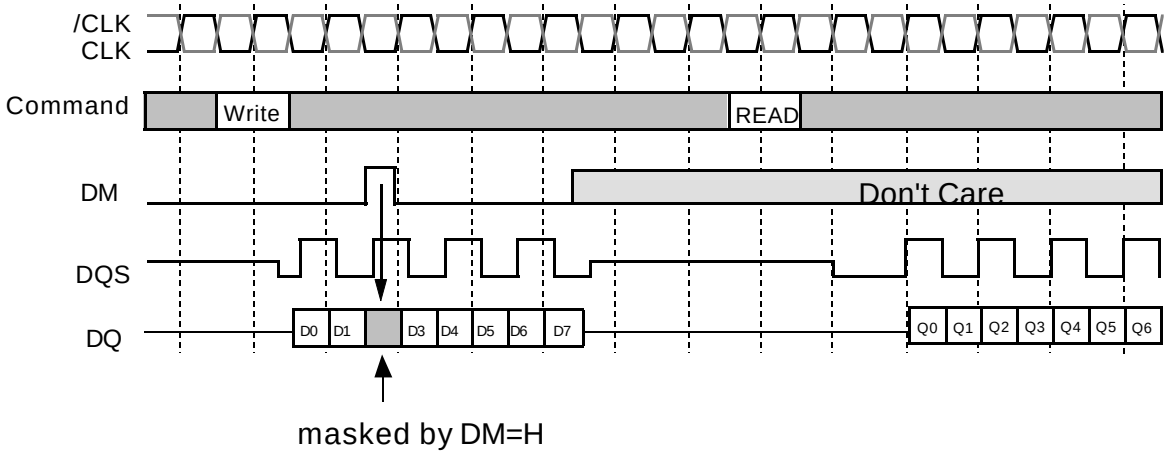
Power Down by CKE



[DM CONTROL]

DM is defined as the data mask for writes. During writes,DM masks input data word by word. DM to write mask latency is 0.

DM Function(BL=8,CL=2)



Serial Presence Detect Table I

Byte	Function described		SPD enrty data	SPD DATA(hex)
0	Number of Serial PD Bytes Written during Production		128	80
1	Total # bytes of SPD memory device		256 Bytes	08
2	Fundamental memory type		SDRAM DDR	07
3	# Row Addresses on this assembly		13	0D
4	# Column Addresses on this assembly		10	0A
5	# Module Banks on this assembly		2BANK	02
6	Data Width of this assembly...		x64	40
7	... Data Width continuation		0	00
8	Voltage interface standard of this assembly		SSTL2.5V	04
9	SDRAM Cycletime at Max. Supported CAS Latency (CL).	-75	7.5ns	75
	Cycle time for CL=2.5	-10	8.0ns	80
10	SDRAM Access from Clock	-75	±0.75ns	75
	tAC for CL=2.5	-10	±0.8 ns	80
11	DIMM Configuration type (Non-parity,Parity,ECC)		None-parity,Non-ECC	00
12	Refresh Rate/Type		7.8uS/SR	82
13	SDRAM width,Primary DRAM		x8	08
14	Error Checking SDRAM data width		N/A	00
15	MIimum Clock Delay, Random Column Access		1 clock	01
16	Burst Lengths Supported		2, 4, 8	0E
17	Number of Device Banks		4bank	04
18	CAS# Latency		2.0, 2.5	0C
19	CS# Latency		0	01
20	WE Latency		1	02
21	SDRAM Module Attributes		Differential Clock	20
22	SDRAM Device Attributes:General		VDD± 0.2V	00
23	SDRAM Cycle time(2nd highest CAS latency)	-75	10ns	A0
	Cycle time for CL=2	-10	10ns	A0
24	SDRAM Access form Clock(2nd highest CAS latency)	-75	±0.75ns	75
	tAC for CL=2	-10	±0.8ns	80
25	SDRAM Cycle time(3rd highest CAS latency)	-75	Undefined	00
		-10	Undefined	00
26	SDRAM Access form Clock(3rd highest CAS latency)	-75	Undefined	00
		-10	Undefined	00
27	Minimum Row Precharge Time (tRP)		20ns	50
28	Minimum Row Active to Row Active Delay (tRRD)		15ns	3C
29	RAS to CAS Delay Minv (tRCD)		20ns	50
30	Active to Precharge Min (tRAS)	-75	45ns	2D
		-10	50ns	32

Serial Presence Detect Table II

31	Density of each bank on module		256MByte	40
32	Command and Address signal input setup time	-75	0.9nS	90
		-10	1.1nS	B0
33	Command and Address signal input hold time	-75	0.9nS	90
		-10	1.1nS	B0
34	Data signal input setup time	-75	0.5nS	50
		-10	0.6nS	60
35	Data signal input hold time	-75	0.5nS	50
		-10	0.6nS	60
36-61	Superset Information (may be used in future)		option	00
62	SPD Revision		0	00
63	Checksum for bytes 0-62		Check sum for -75	C0
			Check sum for -10	46
64-71	Manufactures Jedec ID code per JEP-108E		MITSUBISHI	1CFFFFFFFFFFFFFF
72	Manufacturing location		Manufacturing Location	XX
73-90	Manufactures Part Number		MH64D64AKQH-75	4D483634443634414B51482D373520202020
			MH64D64AKQH-10	4D483634443634414B51482D313020202020
91-92	Revision Code		PCB revision	rrrr
93-94	Manufacturing date		year/week code	yyww
95-98	Assembly Serial Number		serial number	ssssssss
99-127	Reserved		Undefined	00
128-255	Open for Customer Use		Undefined	00

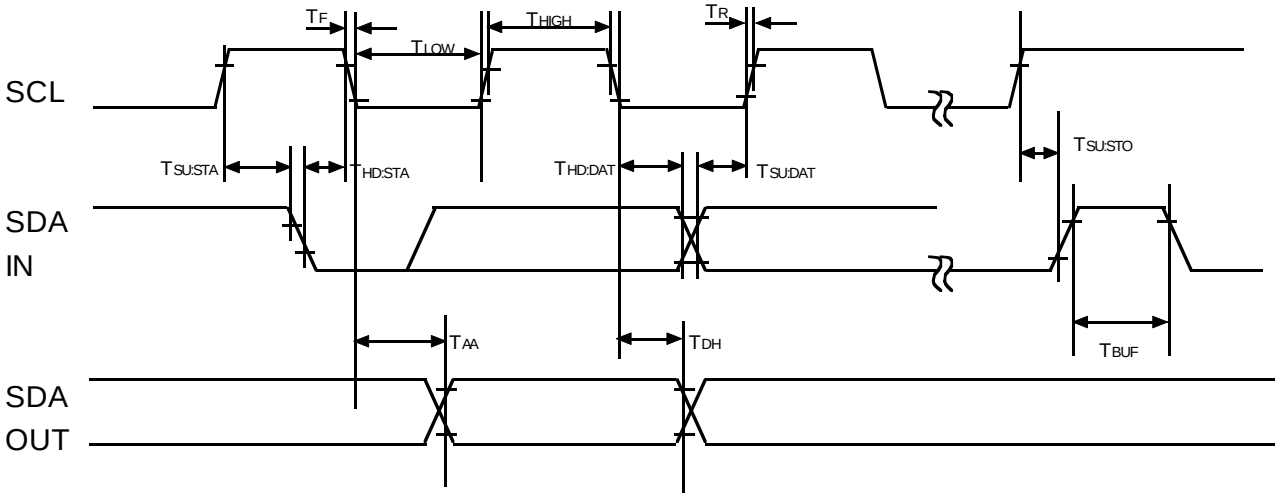
EEPROM Components A.C. and D.C. Characteristics

Symbol	Parameter	Limits			Units
		Min.	Typ.	Max.	
V_{CC}	Supply Voltage	2.2		5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	Vccx0.7		Vcc+0.5	V
V_{IL}	Input Low Voltage	-1		Vccx0.3	V
V_{OL}	Output Low Voltage			0.4	V

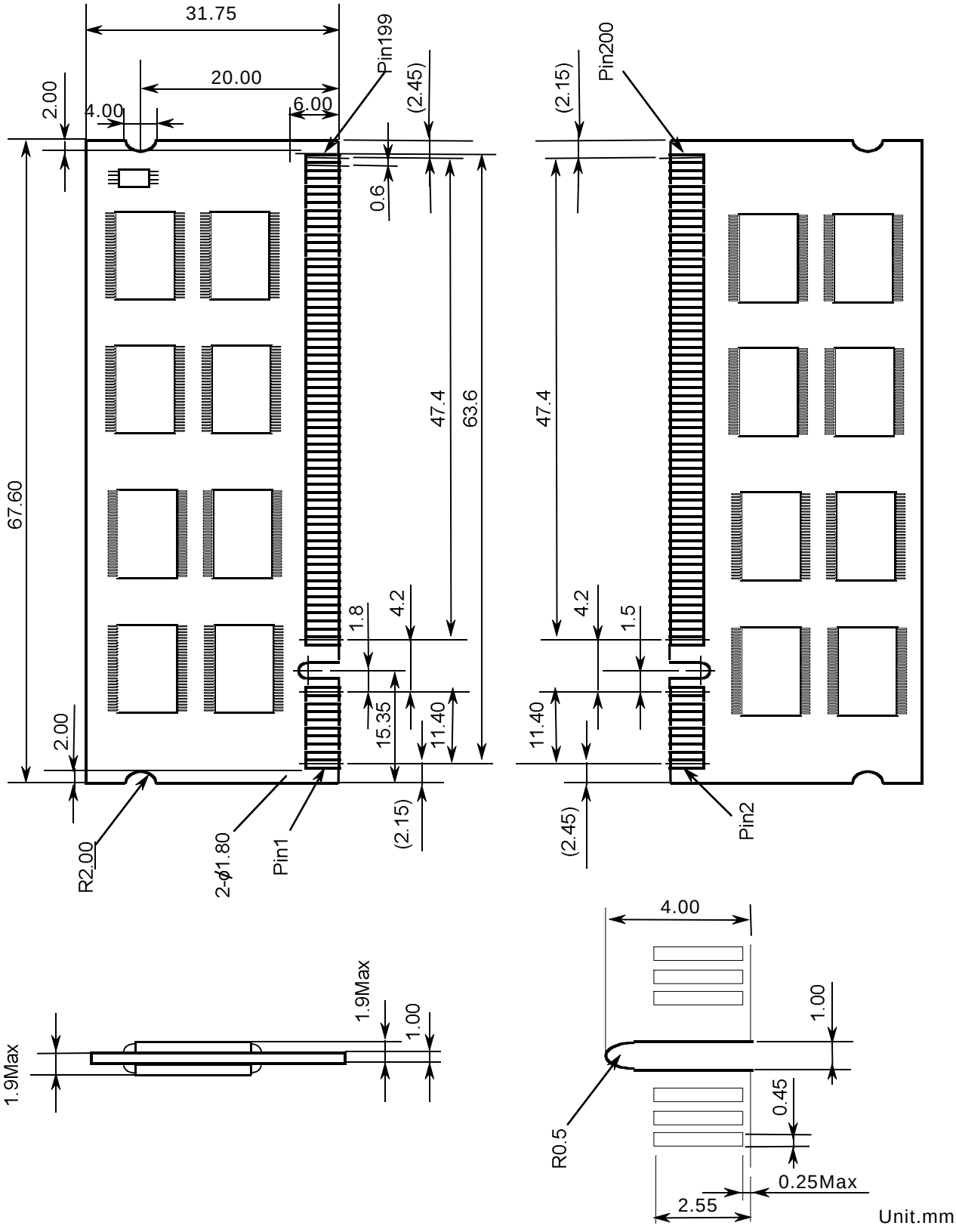
EEPROM A.C.Timing Parameters (Ta=0 to 70°C)

Symbol	Parameter	Limits		Units
		Min.	Max.	
fSCL	SCL Clock Frequency		100	KHz
TI	Noise Supression Time Constant at SCL, SDA inputs		200	ns
TAA	SCL Low to SDA Data Out Valid		3.5	us
TBUF	Time the Bus Must Be Free before a New Transmission Can Start	4.7		us
THD:STA	Start Condition Hold Time	4.0		us
TLOW	Clock Low Time	4.7		us
THIGH	Clock High Time	4.0		us
TSU:STA	Start Condition Setup Time	4.7		us
THD:DAT	Data In Hold Time	0		us
TSU:DAT	Data In Setup Time	250		ns
TR	SDA and SCL Rise Time		1	us
TF	SDA and SCL Fall Time		300	ns
TSU:STO	Stop Condition Setup Time	4.0		us
TDH	Data Out Hold Time	100		ns
TWR	Write Cycle Time		10	ms

tWR is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle.



OUTLINE


31.75
20.00
2.00
4.00
6.00
Pin199
(2.45)
0.6
47.4
63.6
67.60
1.8
4.2
15.35
11.40
2.00
(2.15)
R2.00
2-φ1.80
Pin1
(2.15)
Pin200
47.4
4.2
1.5
11.40
(2.45)
Pin2
1.9Max
1.00
1.9Max
4.00
1.00
0.45
R0.5
0.25Max
2.55
Unit.mm

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