DRAM

4M x 4 DRAM

EDO PAGE MODE

FEATURES

- X4 organization
- EDO (Extended Data-Out) access mode
- Single power supply :
  5V ± 10% Vcc for 5V product
  3.3V ± 10% Vcc for 3.3V product
- Interface for inputs and outputs
  TTL-compatible for 5V products
  LVTTL-compatible for 3.3V products
- 2048-cycle refresh in 32ms
- Refresh modes : $\overline{RAS}$ only, $\overline{CAS}$ BEFORE $\overline{RAS}$ (CBR) and HIDDEN capabilities,
- Optional self-Refresh capabilities(S-ver. Only)
- JEDEC standard pinout
- Key AC Parameter

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-45	45	11	77	16
-50	50	13	84	20
-60	60	15	104	25

ORDERING INFORMATION - PACKAGE

24 / 26-pin 300mil SOJ
24 / 26-pin 300mil TSOP (TypeII)

PRODUCT NO.	Refresh	Vcc	PACKING TYPE
M11B1644A-45J/50J/60J	Normal	5V	SOJ
M11B1644SA-45J/50J/60J	*Self-Refresh		
M11L1644A-45J/50J/60J	Normal	3.3V	
M11L1644SA-45J/50J/60J	Self-Refresh		
M11B1644A-45T/50T/60T	Normal	5V	TSOPII
M11B1644SA-45T/50T/60T	*Self-Refresh		
M11L1644A-45T/50T/60T	Normal	3.3V	
M11L1644SA-45T/50T/60T	Self-Refresh		

*** Ordered by special request**

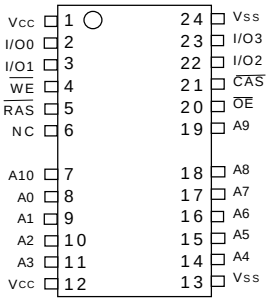
GENERAL DESCRIPTION

The M11B1644/M11L1644 series is a randomly accessed solid state memory, organized as 4,194,304 x 4 bits device. It offers Extended Data-Output access mode. Single power supply (5V ± 10%, 3.3V ± 10%), access time (-45,-50,-60), self-refresh function and package type (SOJ, TSOP II) are optional features of this family. All these family have $\overline{CAS}$ - before - $\overline{RAS}$, $\overline{RAS}$ -only refresh and Hidden refresh.

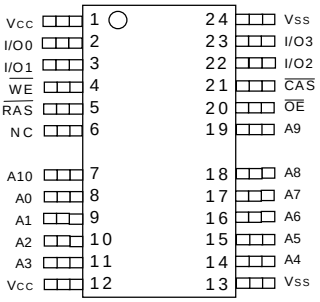
The primary advantage of EDO is the availability of data-out even after $\overline{CAS}$ returns high. EDO allows $\overline{CAS}$ precharge time (t_{PC}) to occur without the output data going invalid. This elimination of $\overline{CAS}$ output control allows pipeline Read.

PIN ASSIGNMENT

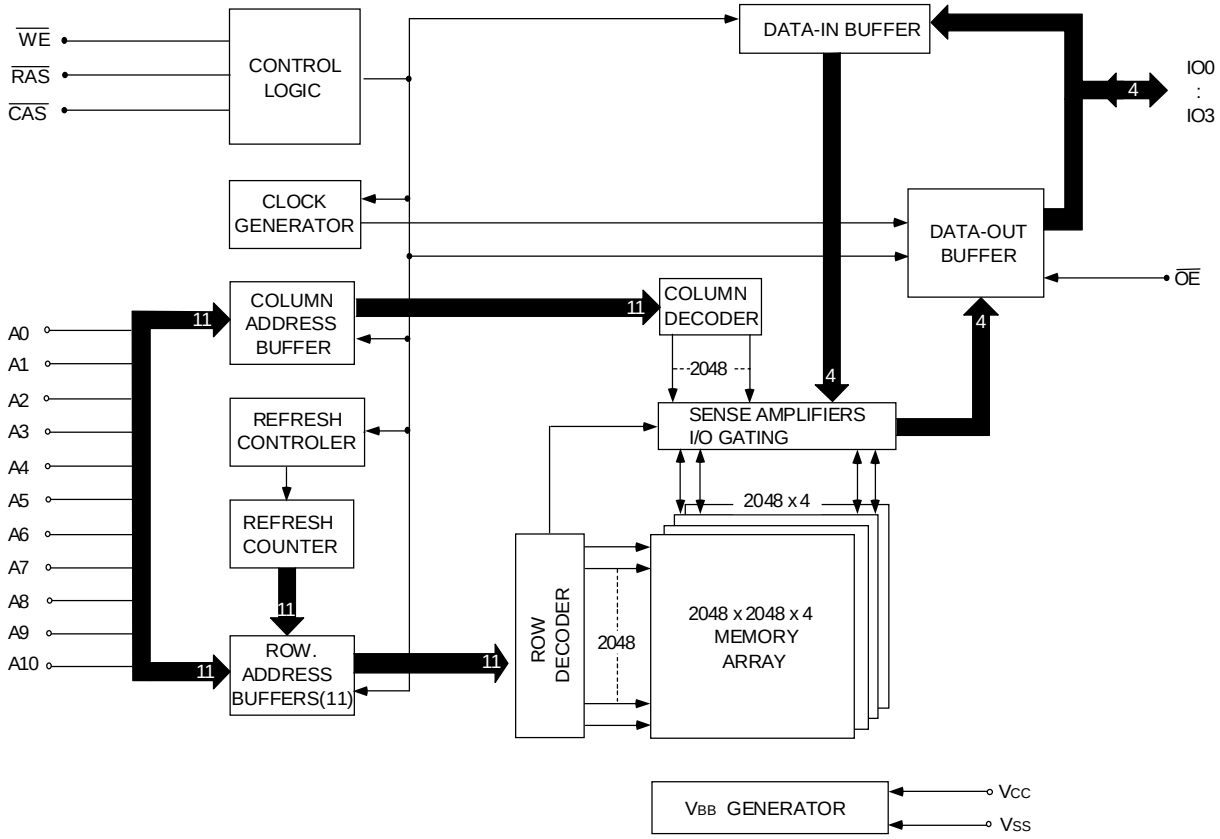
SOJ Top View



TSOP (TypeII) Top View



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NO.	PIN NAME	TYPE	DESCRIPTION
8~11,14~19,7	A0~A10	Input	Address Input Row Address : A0~A10 Column Address : A0~A10
5	$\overline{RAS}$	Input	Row Address Strobe
21	$\overline{CAS}$	Input	Column Address Strobe
4	$\overline{WE}$	Input	Write Enable
20	$\overline{OE}$	Input	Output Enable
2,3,22,23	I/O0 ~ I/O3	Input / Output	Data Input / Output
1,12	V_{CC}	Supply	Power, (5V or 3.3V)
13,24	V_{SS}	Ground	Ground
6	NC	-	No Connect

ABSOLUTE MAXIMUM RATINGS

Voltage on Any pin Relative to Vss
5V Product ... .-1V to +7V
3.3V Product ... .-0.5V to +4.6V

Operating Temperature, T_A (ambient) ....0 °C to +70 °C

Storage Temperature (plastic) .....-55 °C to +150 °C

Power Dissipation 1.0W

Short Circuit Output Current 50mA

Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only, and functional operation of the device above those conditions indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS ($0\,°C \le T_A \le 70\,°C$)

PARAMETER	CONDITIONS		SYMBOL	3.3V		5V		UNITS	NOTES
				MIN	MAX	MIN	MAX		
Supply Voltage			V_{CC}	3.0	3.6	4.5	5.5	V	1
Supply Voltage			V_{SS}	0	0	0	0	V	
Input High Voltage			V_{IH}	2.0	V_{CC} +0.3	2.4	V_{CC} +0.3	V	1
Input Low Voltage			V_{IL}	-0.3	0.8	-0.3	0.8	V	1
Input Leakage Current	$0V \le V_{IN} \le V_{IH(max)}$		I_{LI}	-10	10	-10	10	μA	
Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ Output(s) disable		I_{LO}	-10	10	-10	10	μA	
Output High Voltage	5V	I_{OH} = -5 mA	V_{OH}	2.4	-	2.4	-	V	
	3.3V	I_{OH} = -2 mA							
Output Low Voltage	5V	I_{OL} = 4.2 mA	V_{OL}	-	0.4	-	0.4	V	
	3.3V	I_{OL} = 2 mA							

Note : 1.All Voltages referenced to V_{SS}

PARAMETER	CONDITIONS	SYMBOL	MAX			UNITS	NOTES
			-45	-50	-60		
Operating Current	$\overline{RAS}$, $\overline{CAS}$ cycling , t_{RC} =min	I_{CC1}	150	140	130	mA	1,2
Standby Current	TTL interface , $\overline{RAS}$, $\overline{CAS}$ = V_{IH} , D_{OUT} =High-Z	I_{CC2}	4	4	4	mA	
	CMOS interface, $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC}-0.2V		2	2	2	mA	
$\overline{RAS}$ only refresh Current	t_{RC} = min	I_{CC3}	150	140	130	mA	2
EDO Page Mode Current	t_{PC} = min	I_{CC4}	150	140	130	mA	1,3
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	t_{RC} = min	I_{CC6}	150	140	130	mA	
Battery Backup Current (S-ver. Only)	Standby with CBR refresh, t_{RC} =31.2us $t_{RAS} \le$ 300ns, D_{OUT} =Hi-Z, CMOS interface	I_{CC7}	2	2	2	mA	
Self Refresh Current	$\overline{RAS}$, $\overline{CAS}$ ≤ 0.2V, D_{OUT} =Hi-Z, CMOS interface	I_{CC8}	2	2	2	mA	

Note : 1. I_{CC} max is specified at the output open condition.
2. Address can be changed twice or less while $\overline{RAS}$ =V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ =V_{IH} .

CAPACITANCE (Ta = 25 °C , V_{CC} = 5V ± 10% or 3.3V ± 10%)

PARAMETER	SYMBOL	TYP	MAX	UNIT
Input Capacitance (address)	C_{I1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	-	7	pF
Output capacitance (I/O0~I/O3)	$C_{I/O}$	-	10	pF

AC ELECTRICAL CHARACTERISTICS (Ta = 0 to 70 °C , V_{CC} =5V ± 10% or 3.3V ± 10%, V_{SS} = 0V) (note 14)

Test Conditions

Input timing reference levels : 0.8V, 2.4V (for 5V power supply), 0.8V, 2.0V (for 3.3V power supply)
Output reference level : V_{OL}= 0.8V, V_{OH}=2.0V
Output Load : 2TTL gate + CL (50pF)
Assumed t_T = 2ns

PARAMETER	SYMBOL	-45		-50		-60		UNIT	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Read or Write Cycle Time	t_{RC}	77		84		104		ns	
Read Write Cycle Time	t_{RWC}	97		110		135		ns	
EDO-Page-Mode Read or Write Cycle Time	t_{PC}	16		20		25		ns	
EDO-Page-Mode Read-Write Cycle Time	t_{PCM}	53		58		68		ns	
Access Time From $\overline{RAS}$	t_{RAC}		45		50		60	ns	4
Access Time From $\overline{CAS}$	t_{CAC}		11		13		15	ns	5
Access Time From $\overline{OE}$	t_{OAC}		11		13		15	ns	13
Access Time From Column Address	t_{AA}		22		25		30	ns	
Access Time From $\overline{CAS}$ Precharge	t_{ACP}		25		28		33	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	45	10,000	50	10,000	60	10,000	ns	
$\overline{RAS}$ Pulse Width (EDO Page Mode)	t_{RASC}	45	100,000	50	100,000	60	100,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	6		7		10		ns	
$\overline{RAS}$ Precharge Time	t_{RP}	28		30		40		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	6	10,000	7	10,000	10	10,000	ns	18
$\overline{CAS}$ Hold Time	t_{CSH}	35		37		40		ns	
$\overline{CAS}$ Precharge Time	t_{CP}	6		7		10		ns	6
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	10	34	11	37	14	45	ns	7
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	6		7		10		ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	8	23	9	25	12	30	ns	8
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	6		7		10		ns	
Column Address Hold Time (Reference to $\overline{RAS}$)	t_{AR}	40		44		55		ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	23		25		30		ns	
Column Address setup to $\overline{CAS}$ precharge	t_{ACH}	10		11		13		ns	

(Continued)

PARAMETER	SYMBOL	-45		-50		-60		UNIT	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Command Setup Time	t_{RCS}	0		0		0		ns	15
Read Command Hold Time Reference to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9,15
Read Command Hold Time Reference to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
$\overline{CAS}$ to Output in Low-Z	t_{CLZ}	0		0		0		ns	
Output Buffer Turn-off Delay From $\overline{CAS}$ or $\overline{RAS}$	t_{OFF1}	0	11	0	13	0	15	ns	10,17
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	0	11	0	13	0	15	ns	17,19
Write Command Setup Time	t_{WCS}	0		0		0		ns	11,15
Write Command Hold Time	t_{WCH}	6		7		10		ns	15
Write Command Hold Time(Reference to $\overline{RAS}$)	t_{WCR}	40		44		55		ns	15
Write Command Pulse Width	t_{WP}	6		7		10		ns	15
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	11		13		15		ns	15
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	6		7		10		ns	15
Data-in Setup Time	t_{DS}	0		0		0		ns	12
Data-in Hold Time	t_{DH}	6		7		10		ns	12
Data-in Hold Time (Reference to $\overline{RAS}$)	t_{DHR}	40		44		55		ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	57		67		79		ns	11
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	34		42		49		ns	11
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	23		30		34		ns	11
Transition Time (rise or fall)	t_T	1	50	1	50	1	50	ns	2,3
Refresh Period (2048 cycles)	t_{REF}		32		32		32	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ Setup Time(CBR REFRESH)	t_{CSR}	5		5		5		ns	1
$\overline{CAS}$ Hold Time(CBR REFRESH)	t_{CHR}	10		10		10		ns	1
$\overline{OE}$ Hold Time From $\overline{WE}$ During Read-Mode-Write Cycle	t_{OEH}	6		7		10		ns	16
$\overline{OE}$ Low to $\overline{CAS}$ High Setup Time	t_{OES}	5		5		5		ns	
$\overline{OE}$ High Hold Time From $\overline{CAS}$ High	t_{OEHC}	2		2		2		ns	
$\overline{OE}$ precharge time	t_{OEP}	2		2		2		ns	
$\overline{OE}$ Setup Prior to $\overline{RAS}$ During Hidden Refresh Cycle	t_{ORD}	0		0		0		ns	
Data Output Hold After $\overline{CAS}$ Returning Low	t_{COH}	3		3		3		ns	
Output Disable Delay From $\overline{WE}$	t_{WHZ}	0	11	0	13	0	15	ns	
Self Refresh $\overline{RAS}$ Low Pulse width	t_{RASS}	100		100		100		us	20,21
Self Refresh $\overline{RAS}$ High Precharge Time	t_{RPS}	77		84		104		ns	20,21
Self Refresh $\overline{CAS}$ Hold Time	t_{CHS}	-50		-50		-50		ns	20,21
$\overline{WE}$ Setup Time Reference to $\overline{RAS}$ in CBR/SR	t_{RSR}	0		0		0		ns	20,21
$\overline{WE}$ Hold Time Reference to $\overline{RAS}$ in CBR/SR	t_{RHR}	6		7		10		ns	20,21

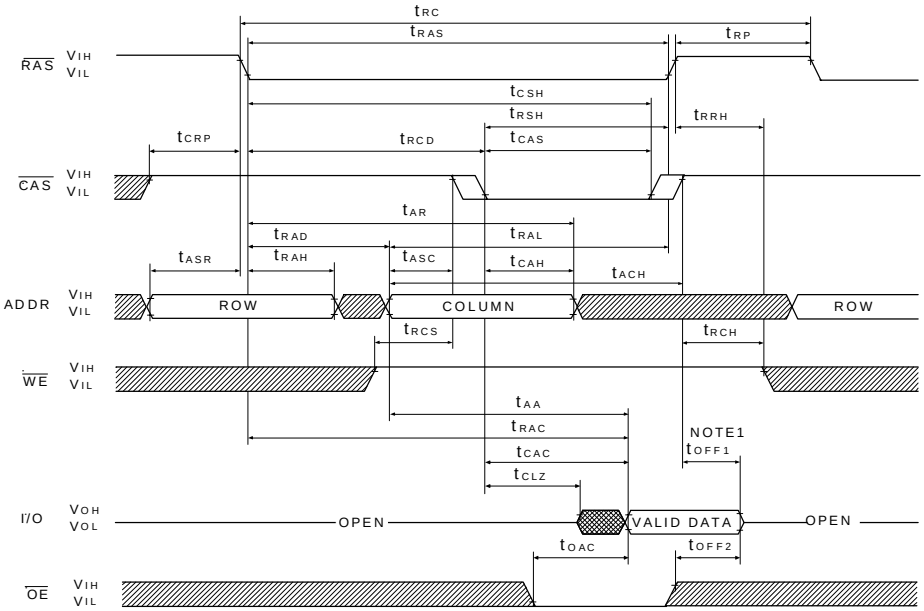
Notes :

1. Enables on-chip refresh and address counters.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
3. In addition to meet the transition rate specification, all input signals must transit between V_{IH} and V_{IL} in a monotonic manner.
4. Assume that $t_{RCD} < t_{RCD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assume that $t_{RCD} \geq t_{RCD}$ (max)
6. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, data-out will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ and $\overline{RAS}$ must be pulsed high.
7. Operation within the t_{RCD} limit ensures that t_{RCD} (max) can be met, t_{RCD} (max) is specified as a reference point only ; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled by t_{CAC}.
8. Operation within the t_{RAD} limit ensures that t_{RAD}(max) can be met. t_{RAD}(max) is specified as a reference point only ; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled by t_{AA}.
9. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
10. t_{OFF1}(max) defines the time at which the output achieves the open circuit condition ; it is not a reference to V_{OH} or V_{OL}.
11. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If $t_{WCS} \geq t_{WCS(min)}$, the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CWD} \geq t_{CWD(min)}$, the cycle is READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until $\overline{CAS}$ and $\overline{RAS}$ or $\overline{OE}$ go back to V_{IH}) is indeterminate. $\overline{OE}$ held high and $\overline{WE}$ taken low after $\overline{CAS}$ goes low result in a LATE WRITE ($\overline{OE}$-controlled) cycle.
12. Those parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY- WRITE cycles.
13. During a READ cycle, if $\overline{OE}$ is low then taken HIGH before $\overline{CAS}$ goes high, I/O goes open, if $\overline{OE}$ is tied permanently low, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
14. An initial pause of 200 μs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ only or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
15. WRITE command is defined as $\overline{WE}$ going low.
16. LATE WRITE and READ-MODIFY-WRITE cycles must have both tOFF2 and t_{OEH} met ($\overline{OE}$ high during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycles.
17. The I/Os open during READ cycles once tOFF1 or tOFF2 occur.
18. Each $\overline{CAS}$ must meet minimum pulse width.
19. All IOs controlled by $\overline{OE}$, regardless $\overline{CAS}$.
20. Self refresh mode is initiated by performing a CBR refresh cycle and holding $\overline{RAS}$ low for the specified tRASS. Self refresh mode is terminated by rising $\overline{RAS}$ high for a minimum time of tRPS.
21. For all of the refresh mode except the distributed CBR refresh mode, all rows must be refreshed within the refresh rate before and after self refresh.

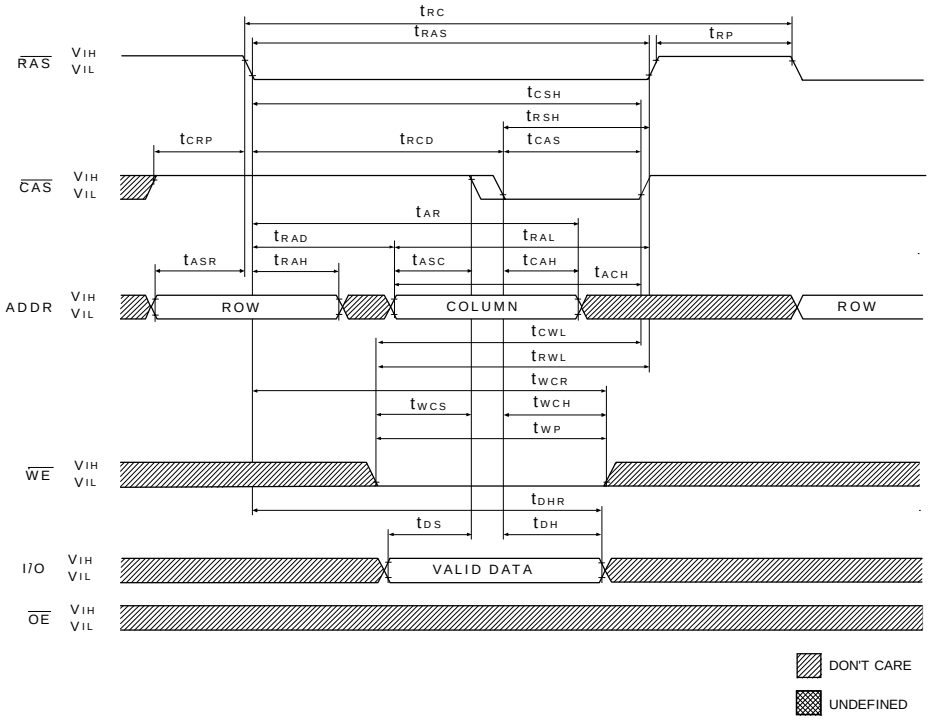
TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES		DQs
						ROW	COL	
Standby		H	H→X	X	X	X	X	High-Z
Read		L	L	H	L	ROW	COL	Data-Out
Write (Early Write)		L	L	L	X	ROW	COL	Data-In
Read-Write		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
EDO-Page-Mode Read	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	X	COL	Data-Out
	Any Cycle	L	L→H	H	L	X	X	Data-Out
EDO-Page-Mode Write (Early)	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	X	COL	Data-In
EDO-Page-Mode Read-Write	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	X	COL	Data-Out, Data-In
Hidden Refresh		L→H→L	L	H	L	ROW	COL	Data-Out
$\overline{RAS}$ -Only Refresh		L	H	X	X	ROW	X	High-Z
CBR Refresh		H→L	L	H	X	X	X	High-Z
Self Refresh		H→L	L	H	X	X	X	High-Z

READ CYCLE

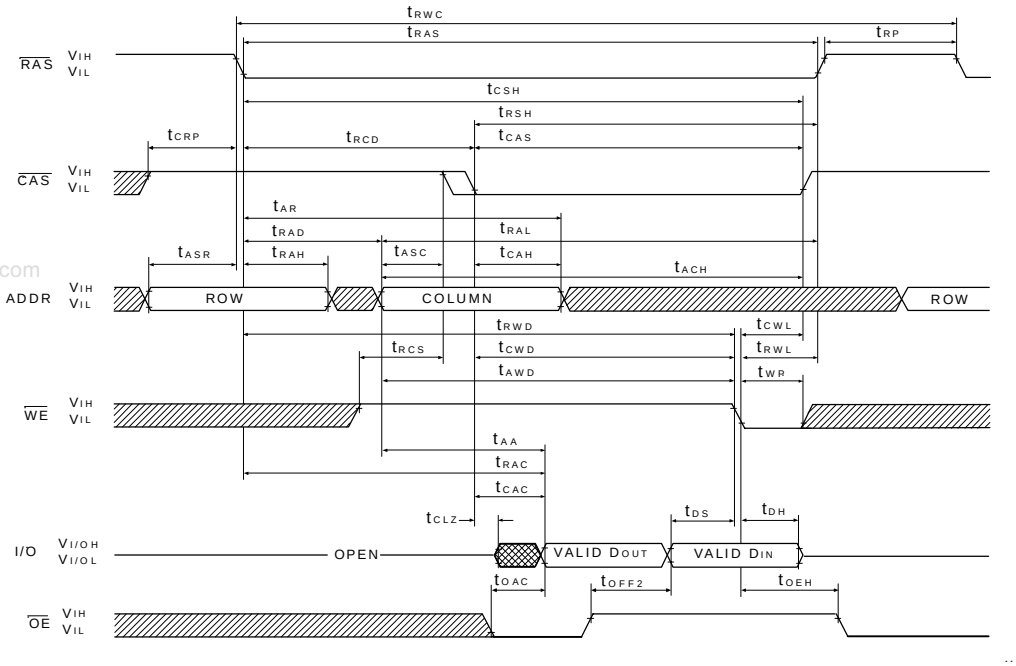


EARLY WRITE CYCLE

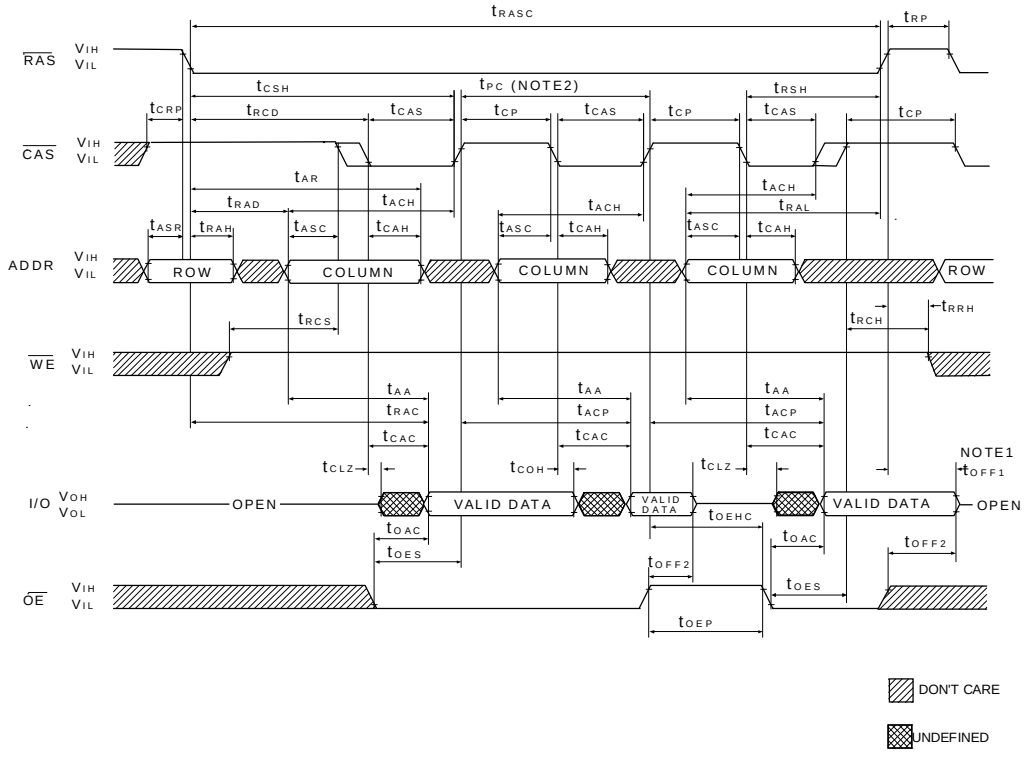


Note: 1. t_{OFF1} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



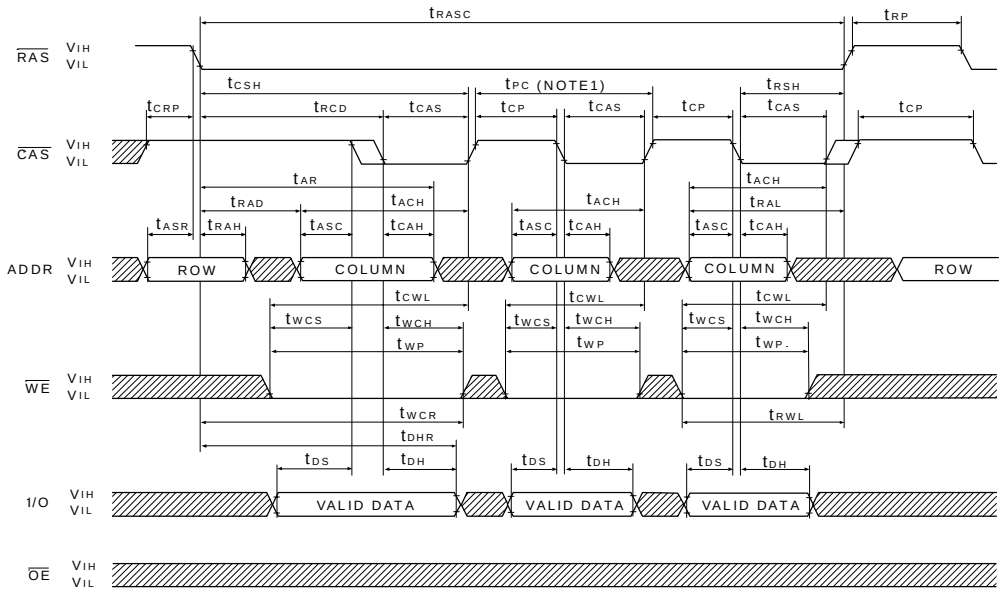
EDO-PAGE-MODE READ CYCLE



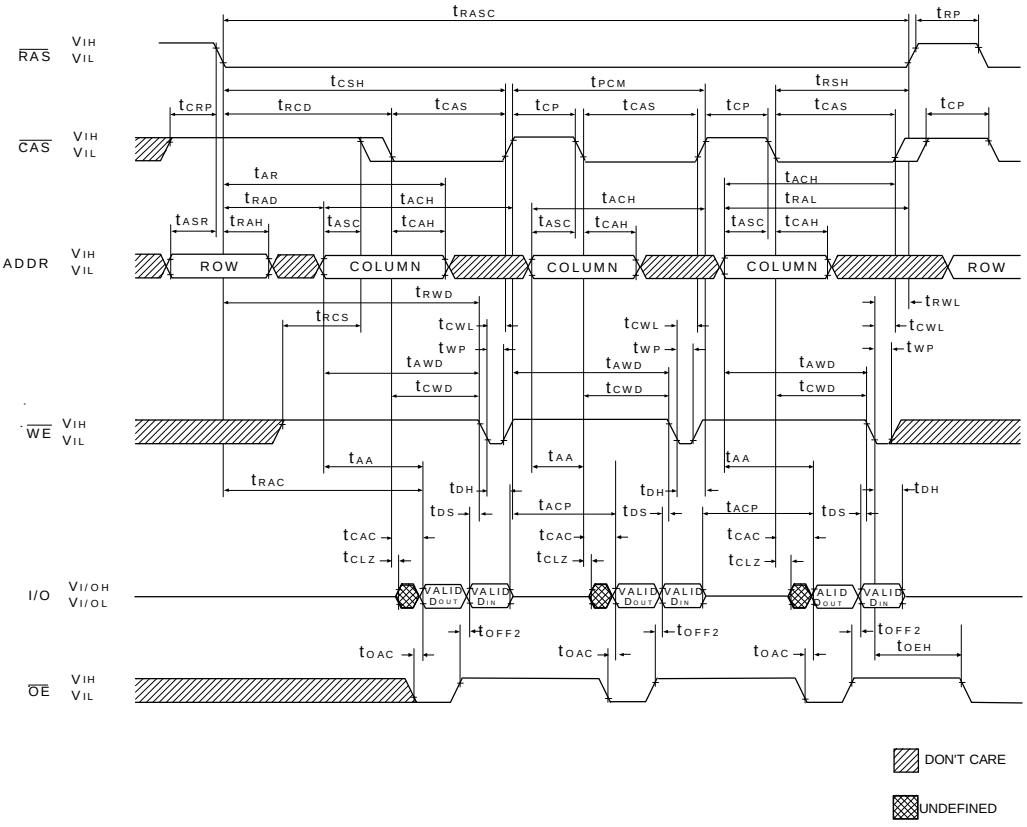
*NOTE : 1. t_{OFF1} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

2. t_{PC} can be measured from falling edge of $\overline{CAS}$ to falling edge of $\overline{CAS}$, or from rising edge of $\overline{CAS}$ to rising edge of $\overline{CAS}$. Both measurements must meet the t_{PC} specification.

EDO-PAGE-MODE EARLY-WRITE CYCLE

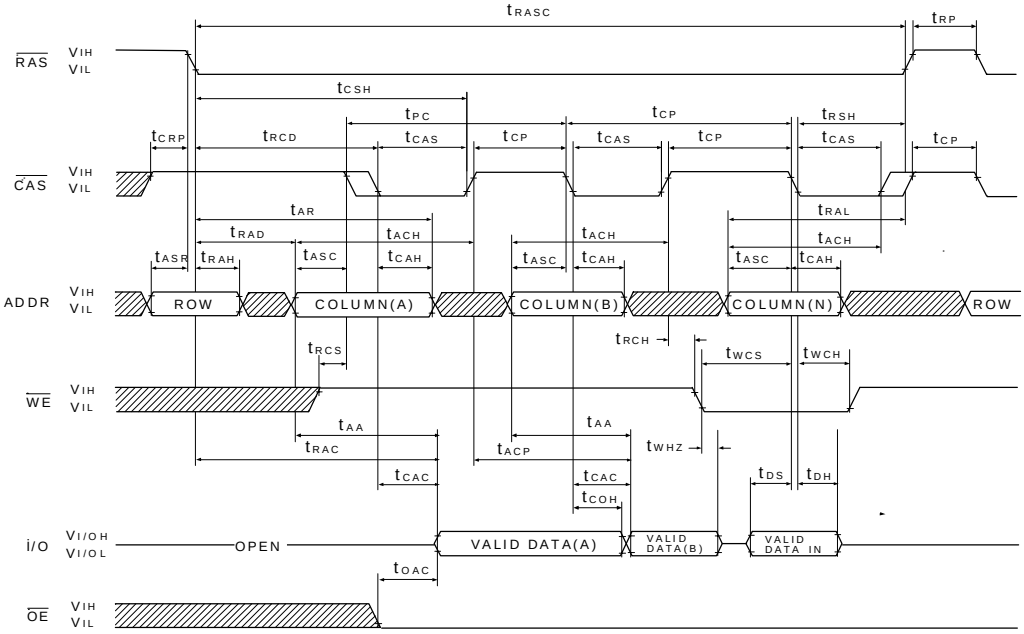


EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)

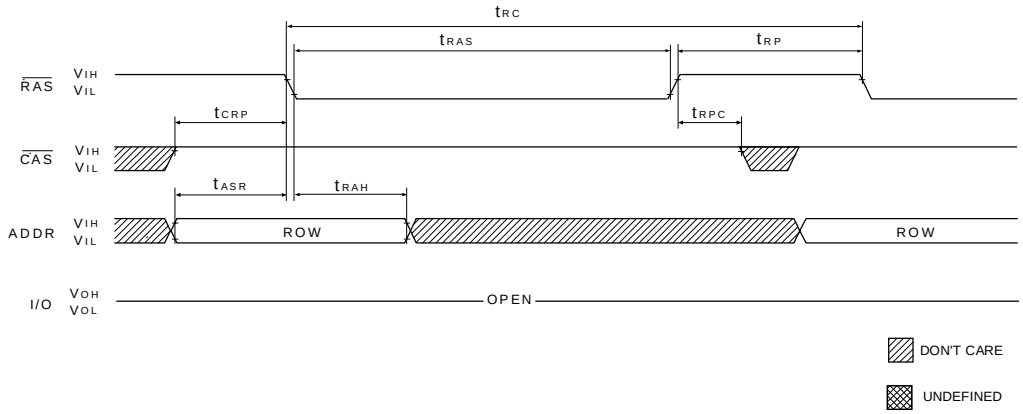


Note : 1. t_{PC} can be measured from falling edge to falling edge of $\overline{CAS}$, or from rising edge to rising edge of $\overline{CAS}$. Both measurements must meet the t_{PC} specification.

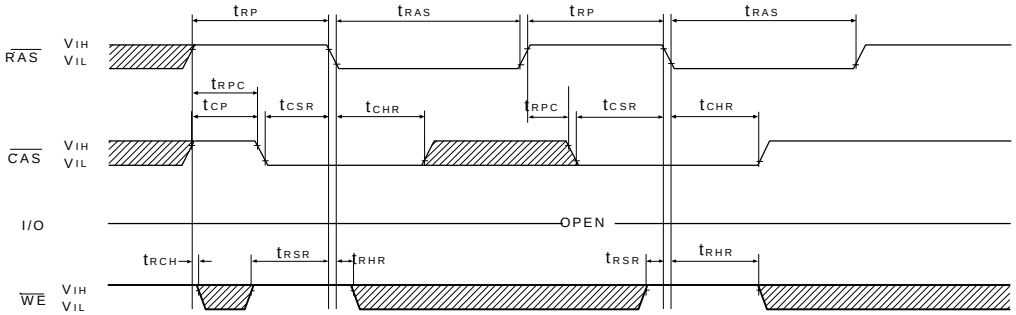
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Psuedo READ-MODIFY-WRITE)



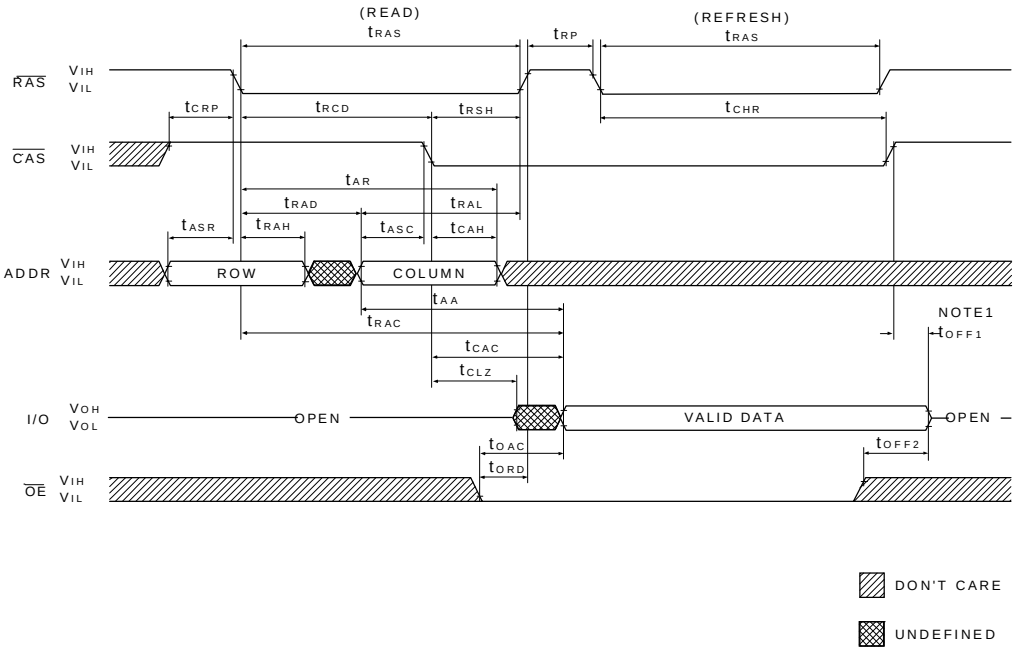
RAS ONLY REFRESH CYCLE
(ADDR = A0~A10 ; OE , WE = DON'T CARE)



CBR REFRESH CYCLE
(A0~A10 ; $\overline{OE}$ = DON'T CARE)

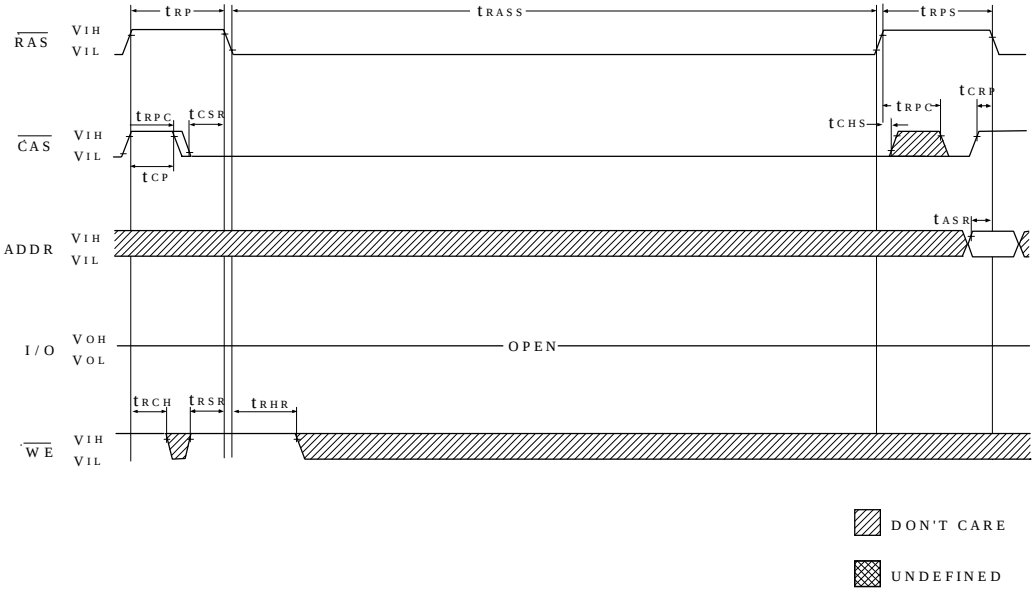


HIDDEN REFRESH CYCLE
($\overline{WE}$ = HIGH ; $\overline{OE}$ = LOW)



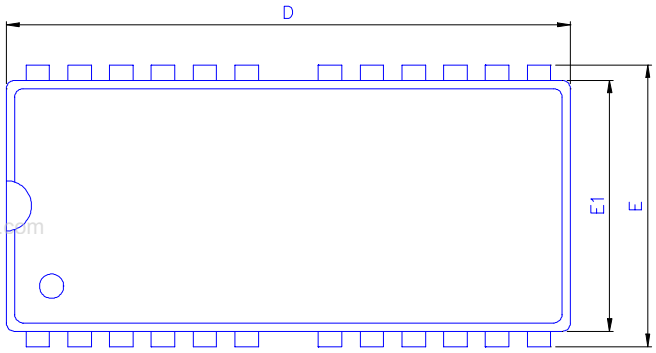
Note : 1. t_{OFF1} is reference from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

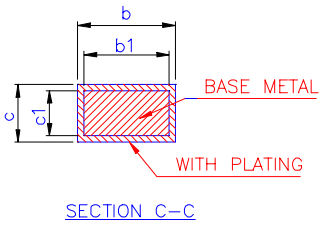
SELF REFRESH CYCLE
($\overline{OE}$ = DON'T CARE)

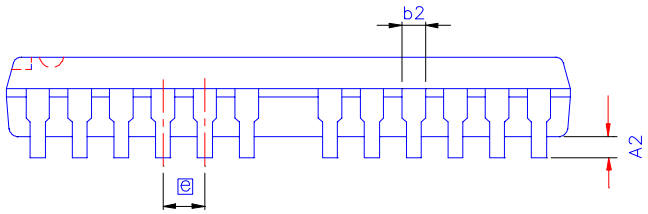


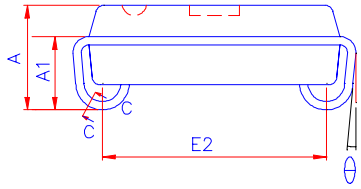
PACKING DIMENSIONS

24 / 26-LEAD SOJ(300mil)





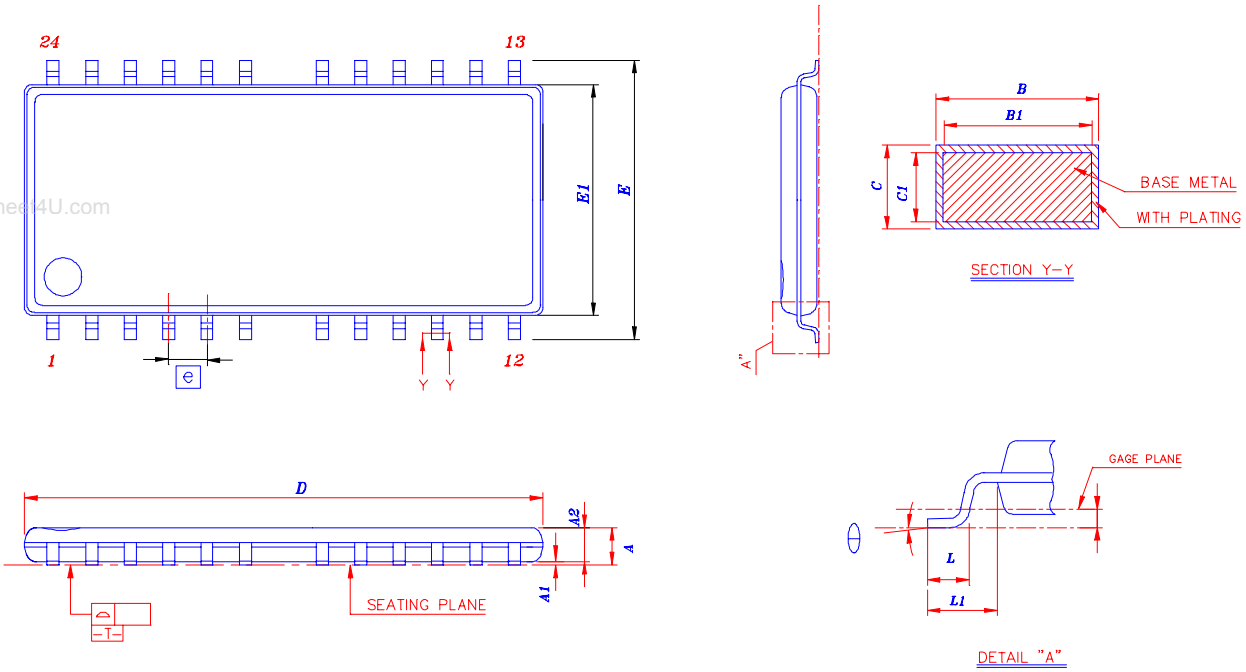




Symbol	Dimension mm			Dimension inch		
	Min	Nom	Max	Min	Nom	Max
A	3.25	3.51	3.76	0.128	0.138	0.148
A1	2.08	-	-	0.082	-	-
A2	0.635	-	-	0.025	-	-
B	0.41		0.51	0.016		0.020
B1	0.41	0.46	0.48	0.016	0.018	0.019
B2	0.66	0.71	0.81	0.026	0.028	0.032
C	0.18	0.20	0.28	0.007	0.008	0.012
C1	0.18		0.28	0.007		0.011
D	17.02	17.15	17.27	0.670	0.675	0.680
E		8.51			0.335	
E1	7.49	7.62	7.75	0.295	0.300	0.305
θ	0°		10°	0°		10°
e	1.27 BASIC			0.050 BASIC		

PACKING **DIMENSIONS**

24 / 26-LEAD **TSOP(II)** **DRAM(300mil)**



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
B	0.30	-	0.52	0.012	-	0.02
B1	0.30	0.40	0.45	0.012	0.016	0.018
C	0.12	-	0.21	0.005	-	0.008
C1	0.12	0.15	0.16	0.005	0.006	0.0063
D	17.01	17.14	17.27	0.67	0.675	0.68
ZD		0.95 REF			0.374 REF	
E	9.02	9.22	9.42	0.355	0.363	0.371
E1	7.49	7.62	7.75	0.295	0.3	0.305
L	0.40	0.50	0.60	0.016	0.020	0.024
L1		0.031 REF			0.080 REF	
e		1.27 BSC			0.05 BSC	
R	0.12	-	0.25	0.005	-	0.01
R1	0.12	-	-	0.005	-	-
θ	0°	-	5°	0°	-	5°
y	-	-	0.10	-	-	0.004

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