PRELIMINARY

Integrated Circuit Systems, Inc.

ICS840001-31

FEMTOCLOCKS™ CRYSTAL-TO-LVCMOS/LVTTL FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The ICS840001-31 is a two output LVCMOS/LVTTL Synthesizer and a member of the HiPerClocks™ family of high performance devices from ICS. One output is the LVCMOS/LVTTL main synthesized clock output (Q) and one output is a three-state LVCMOS/LVTTL reference clock (REF_CLK) output at the frequency of the crystal oscillator. The device can accept 26.5625MHz and 40MHz crystals and can synthesize 106.25MHz or 100MHz outputs. The ICS840001-31 has excellent <1ps phase jitter performance over the 637kHz – 10MHz integration range. The ICS840001-31 is packaged in a 3mm x 3mm 16-pin VFQFN, making it ideal for use on space constrained boards.

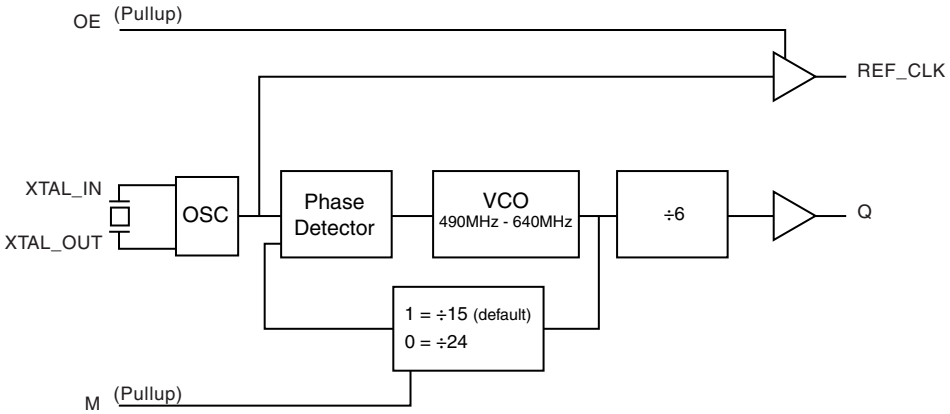
FEATURES

- (2) LVCMOS/LVTTL outputs, 20Ω typical output impedence
  (1) Main clock output (Q)
  (1) Three-state reference clock output (REF_CLK)
- Crystal oscillator interface can accept 26.5625MHz or 40MHz 18pF parallel resonant crystals
- Output frequency range: 106.25MHz or 100MHz
- VCO range: 490MHz to 640MHz
- RMS phase jitter @ 106.25MHz, using a 26.5625MHz crystal (637kHz - 10MHz): 0.38ps (typical)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature

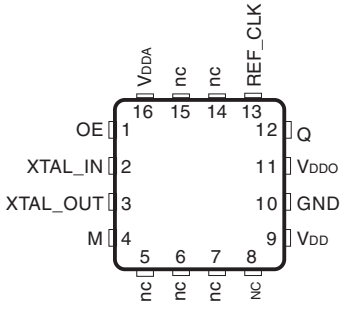
FUNCTION TABLE

Inputs				Outputs		Application
Crystal	M	OE	VCO (MHz)	Q Frequency (MHz)	REF_CLK Frequency (MHz)	
26.5625	0	0	637.5	106.25	High-Z	Fibre Channel
40	1 (or Floating)	1 (or Floating)	600	100	40	Serial Attached (SCSI)

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS840001-31
16-Lead VFQFN
3mm x 3mm x 0.95 package body
K Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	OE	Input	Pullup	Output enable pin. When HIGH, REF_CLK output is enabled. When LOW, forces REF_CLK to HiZ state. LVCMOS/LVTTL interface levels.
2,3	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
4	M	Input	Pullup	M divider input. 0 = ÷24, 1 = ÷15 (default). LVCMOS/LVTTL interface levels.
5, 6, 7, 8, 14, 15	nc	Unused		No connect.
9	V_{DD}	Power		Core supply pin.
10	GND	Power		Power supply ground.
11	V_{DDO}	Power		Output supply pin.
12	Q	Output		Single-ended clock output. LVCMOS/LVTTL interface levels. 20Ω typical output impedance.
13	REF_CLK	Output		Single-ended three-state reference clock output. LVCMOS/LVTTL interface levels. 20Ω typical output impedance.
16	V_{DDA}	Power		Analog supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance	V_{DD}, $V_{DDA,}$ V_{DDO} = 3.465V		8		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
R_{OUT}	Output Impedance			20		Ω

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	51.5°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			70		mA
I_{DDA}	Analog Supply Current			6		mA
I_{DDO}	Output Supply Current			27		mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	OE, M	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	OE, M	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage; NOTE 1			2.6			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DD}/2$. See Parameter Measurement Information Section, "3.3V Output Load Test Circuit".

TABLE 5. CRYSTAL CHARACTERISTICS

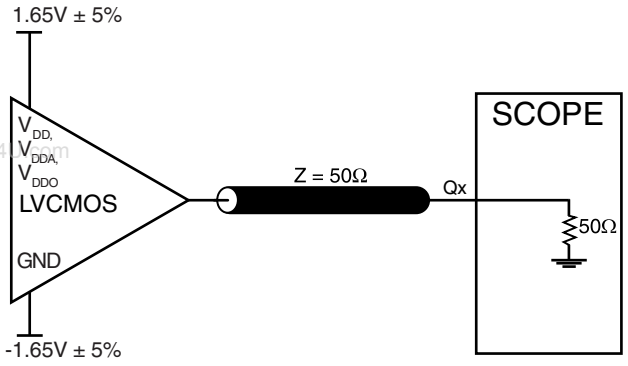
Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		26.5625		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

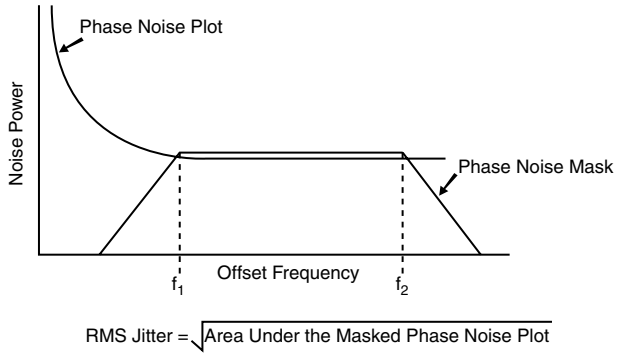
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			100		MHz
				106.25		MHz
$t_{jit}(Ø)$	RMS Phase Jitter (Random); NOTE 1	100MHz, Integration Range: 637kHz to 10MHz		0.54		ps
		106.25MHz, Integration Range: 637kHz to 10MHz		0.38		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		470		ps
odc	Output Duty Cycle			50		%

All parameters are characterized @ 100MHz and 106.25MHz.
NOTE 1: Please refer to the Phase Noise Plot.

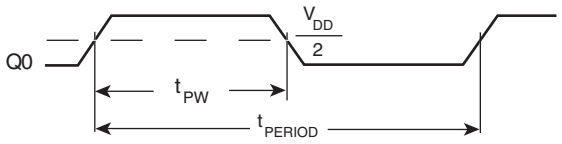
PARAMETER MEASUREMENT INFORMATION



3.3V OUTPUT LOAD AC TEST CIRCUIT

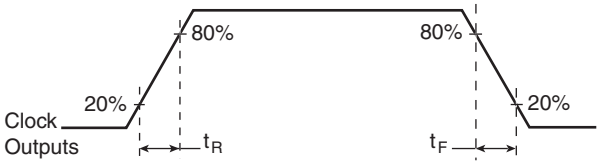


RMS PHASE JITTER



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS840001-31 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

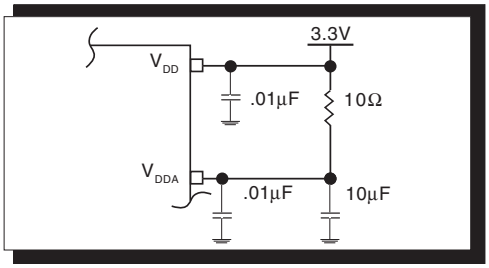


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS840001-31 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 26.5625MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

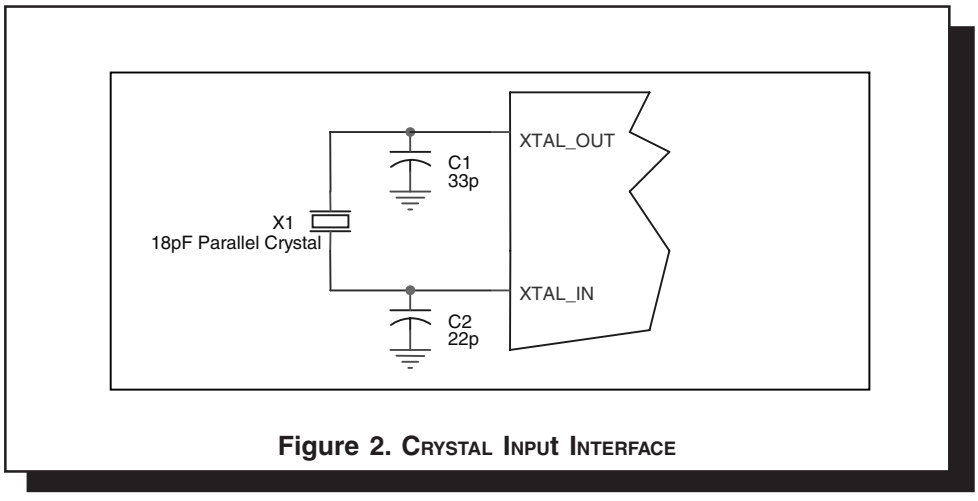


Figure 2. CRYSTAL INPUT INTERFACE

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD VFQFN

θ_{JA} at 0 Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

TRANSISTOR COUNT

The transistor count for ICS840001-31 is: 2805

PACKAGE OUTLINE - K SUFFIX FOR 16 LEAD VFQFN

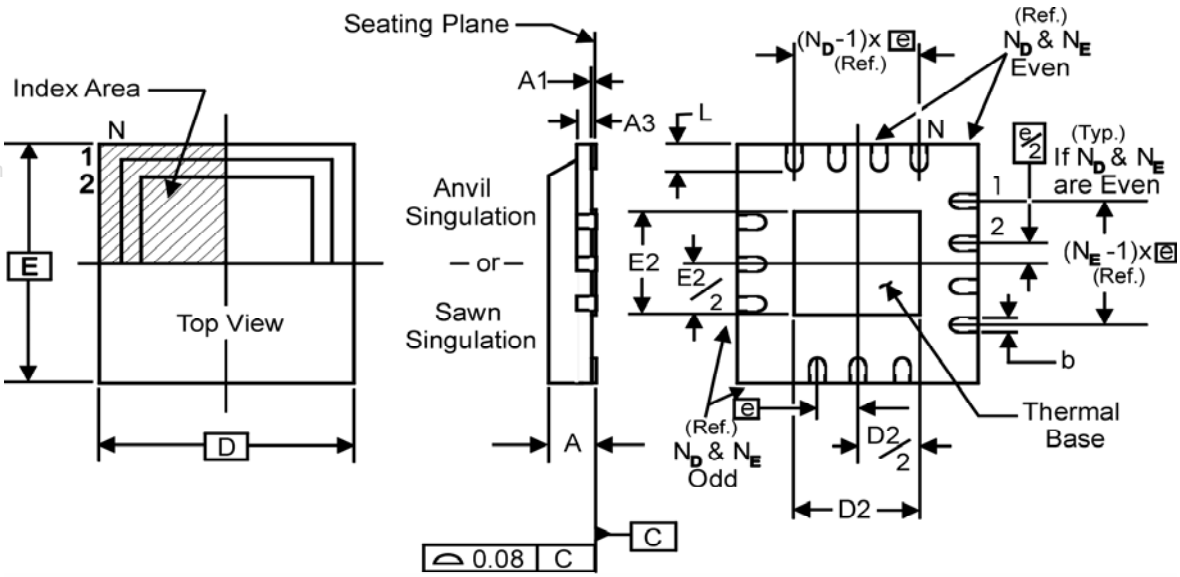


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	16	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	4	
N_E	4	
D	3.0	
D2	0.25	1.25
E	3.0	
E2	0.25	1.25
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS840001AK-31	1A31	16 Lead VFQFN	tray	0°C to 70°C
ICS840001AK-31	1A31	16 Lead VFQFN	2500 tape & reel	0°C to 70°C