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PART NO : <u>GG1206N8SKN1T</u> FOR MESSRS :

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Accepted by : _____

Proposed by :

Date : 10,25,2002

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RECORD OF REVISION

	DATE	PAGE	SUMMARY	
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DIOMON GOLDENTEK DISPLAY CORP. GG1206N8SKN1T REV:1	OLOMON GOLDI	ENTEK DISPLAY COR	P. GG1206NIQCVNIT	REV : 1
EL: 886-7-788-6800 FAX: 886-7-788-6806~8 OG12001085K1N11 PAGE: 2	`EL : 886-7-788-6800	FAX : 886-7-788-6806~	8 001200105K1111	PAGE : 2

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3. GENERAL SPECIFICATIONS AND MECHANICAL DATA 3.1 GENERAL SPECIFICATIONS PLEASE REFER TO: "CUSTOMER ACCEPTANCE STANDARD SPECIFICATIONS (SP-10-000)".

3.2 THIS INDIVIDUAL SPECIFICATION IS PRIOR TO GENERAL SPECIFICATIONS.

3.3 MECHANICAL DATA

- (1) NUMBER OF DOTS ------ 128Wx 64H DOTS
- (2) MODULE SIZE ------ 71.0Wx 59.3Hx 2.0D (MAX.) mm
- (3) VEWING AREA ----- 67.0W× 37.0H mm
- (4)DISPLAY AREA ----- 64.41Wx 30.69Hmm
- (5) DOT SIZE ----- 0.45W× 0.45H mm
- (6) DOT PITCH ----- 0.48W× 0.48H mm
- (7) VIEWING DIRECTION ----- 6 O'CLOCK
- (8) LCD COLOR ------ STN, GRAY, TRANSFLECTIVE

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4. ABSOLUTE MAXIMUM RATINGS4.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN.	MAX.	UNIT	COMMENT
POWER SUPPLY FOR LOGIC	VDD-VSS	2.4	6.0	V	
INPUT VOLTAGE	VI	VSS	VDD	V	
STATIC ELECTRICITY			100	V	NOTE (1)

NOTE (1) : TEST METHOD AND CONDITIONS AFTER CHARGING UP 200PF CAPACITOR BY STATED VOLTAGE, THE CAPACITOR IS CONNECTED WITH INTERFACE PINS OF THE MODULE.

4.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RAINGS

ITEM	OPER	ATING	STO	RAGE	COMMENT
	MIN.	MAX.	MIN.	MAX.	COMMULINI
AMBIENT TEMPERATURE	0°C	50°C	-20°C	60°C	NOTE (2)
HUMIDITY	NOTE (3)		NOTE (3)		WITHOUT CONDENSATION
		4.9 m/s^2		19.6 m/s^2	10~300HZ XYZ
VIBRATION		(0.5G)		(2G)	DIRECTIONS 1 Hr. EACH
SHOCK		29.4 m/s ²		49.0 m/s^2	10 ms XYZ
SHOCK		(3G)		(5G)	DIRECTIONS 1 TIME EACH
CORROSIVE GAS	NOT ACCEPTABLE		NOT ACCEPTABLE		

NOTE (2) : Ta AT -20°C : 48HR MAX. Ta AT 60°C : 168HR MAX.

NOTE (3) : Ta $\leq 40^{\circ}$ C : 90% RH MAX.

Ta > 40°C : ABSOLUTE HUMIDITY MUST BE LOWER THAN THE HUMIDITY OF 90%RH AT 40°C . (50% RH AT 50°C)

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5. ELECTRICAL AND OPTICAL CHARACTERISTICS

5.1 ELECRICAL CHARACTERISTICS

$Ta = 25^{\circ}C$	VDD = 2.4V	~6.0V				
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
LOGIC CIRCUIT POWER SUPPLY VOLTAGE	VDD-VSS		2.4		6.0	V
INPUT VOLTAGE	VOH	NOTE (1)	0.7*VDD		VDD	V
INPUT VOLTAGE	VOL	NOTE (1)	GND		0.3*VDD	V
LOGIC CIRCUIT POWER SUPPLY CURRENT	IDD	VDD-VSS =5.0V		1.0	3.0	mA
RECOMMENDED	VDD - VO	Ta = 0°C				V
LCD DRIVING	DUTY = 1/64	$Ta = 25^{\circ}C$		(8.8)		V
VOLTAGE (NOTE 1)	§ =10°	$Ta = 50^{\circ}C$				V

NOTE (1): CS1, CS2, R/W, D/I, DB0~DB7, E, RST

NOTE (2): RECOMMENDED LCD DRIVING VOLTAGE MAY FLUCTUATE ABOUT \pm 0.5V BY EACH MODULE.

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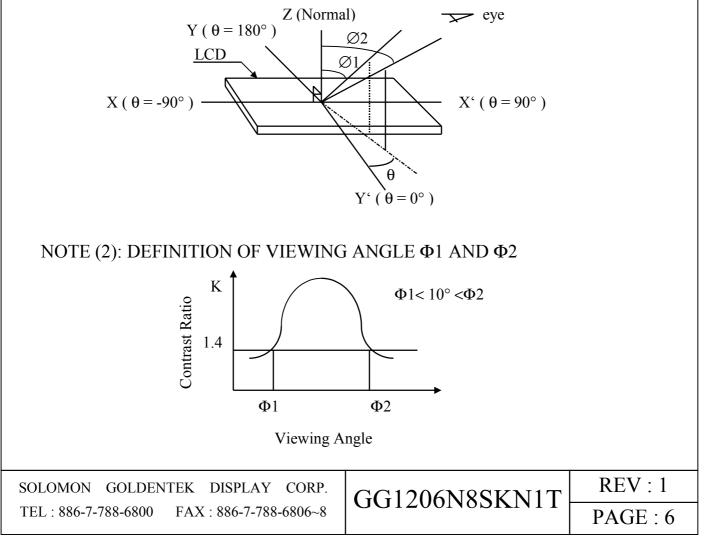
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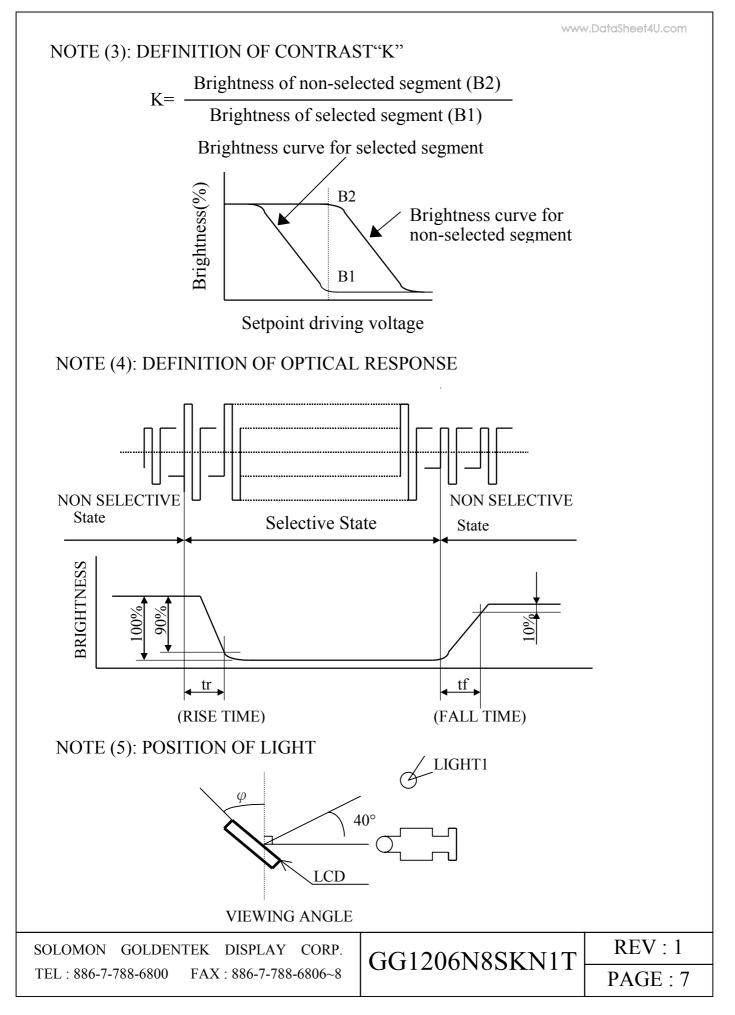
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5.2 OPTICAL CHARACTERISTICS

$Ta = 25^{\circ}C$	VDD = 2	.4V~6.0V				
I T E M	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
VIEWING AREA	Ф2-Ф1	$K \ge 1.4$	20			deg.
CONTRAST RATIO	К	$\Phi = 10^{\circ}$ $\Theta = 0^{\circ}$		4		
DESDONSE TIME	tr(rise)	$\Phi = 10^{\circ}$ $\Theta = 0^{\circ}$		250	350	ms
RESPONSE TIME	tf(fall)	$\Phi = 10^{\circ}$ $\Theta = 0^{\circ}$		300	400	ms

NOTE (1): DEFINITION OF θ AND Φ





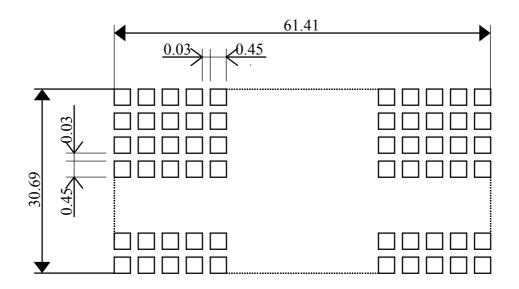
6. OUTLINE DIMENSION

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r - 1	ر ب ب		ЭМАХ <u>.</u> 4.8			67	71.0 2.0MIN.4 61.41 ±	(V,A,)					0.7 ±0.0		0MAX. 7 ±0.07	
59.3±0.5 43.5	40.5	30.69±0.1				0.48 0.45		0.45						Ç		
		7.35		. 17.5 . 14.5 . 9.2		P1.0	36.(36.(#42=4 w=0.5: 52.6	<u>2.0 ±0.</u> ±0.05)MAX.	
PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
SYMBOL	N.C	FR	CL	DOF	CS1	CS2	RES	A0	R/W	Е	D0	D1	D2	D3	D4	D5
PIN	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
SYMBOL	D6	D7	VDD	VSS	VSS2	VOUT	CAP3-	CAP1+	CAP1-	CAP2-	CAP2+	VRS	VDD	V1	V2	V3
PIN	33	34	35	36	37	38	39	40	41	42	43					
SYMBOL	V4	V5	VR	VDD	M/S	CLS	C86	P/S	NUI	SPEC T : mr LE : Ì		TOL	ERAN	ICE: <u>-</u>	=0.3	
SOLOMO	N G	OLDE	INTER	C DIS	SPLAY	CC	ORP.			061	18 5	K VI	<u>1</u> Т	I	REV	:1
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NOTE (1): DETAIL DRAWING OF MATRIX PATTERN



INTERFACE CONNECTOR PIN

Pin Name	I/O		Function									
COM0	О	These are te liquid crys	stal common driv	ve output.								
to		Part No.	COM		Part NO.							
COM31		SED1565*	COM0~CO	M63	SED1565*	64						
		SED1566*	COM0~CO	M47	SED1566*	48						
		SED1567*	COM0~CO	M31	SED1567*	32						
		Through a combination VDD,V1,V4,and V5	n of the contents	of the scan data and with th	e FR signal, a single level	is selected from						
		Scan Da	ta	FR	Ou	tput Voltage						
		Н		Н		V5						
		Н		L		VDD						
		L		Н		V1						
		L		L		V4						
		Power Sa	ve			VDD						
COMS	0	These ae the COM out	put terminals for	ls output the same signal.								
		Leave these open if the	Leave these open if they are not used.									
		When in master/slave	mode, the same	signal is output by both mas	ter and slave.							

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VSS POWER SUPPLY This is no V terminal connected to the system (SD.) VSS POWER SUPPLY This is no certainly input VREG power supply for the 1CD power supply voltage regulator. VSS POWER SUPPLY This is no certainly input VREG power supply for the 1CD power supply or longer regulator. V122 POWER SUPPLY This is a multi-velop power supply for the low voltage drivide or through changing the impedance to an on power supply criticalis produce the V1 to V4 voltage shown below. V/D/C V152 POWER SUPPLY Master operation. When the power supply the the voltage activation and the carbon set of the state of the voltage activation and the carbon set of the voltage activation and the CAP-terminal. CAP1+ O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1-terminal. CAP2- O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2-terminal. CAP2- O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1-terminal. CAP2- O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1-terminal. CAP2- O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1-terminal. CAP2- O DC/DC voltage converter. Connect a capacitor between this terminal a	PIN NAME VDD	I/O POWER SUPPLY	Shared with the N	IPU nower	supply t	FOUNCTION erminal Vcc	\AAAA	DataSheet4U.con		
VYSE POWER SUPPLY This is the reference power supply for the step-up voltage crount for the luquid crystal drive. VRS POWER SUPPLY This is the reference power supply for the ICD power supply voltage regulator V1.02 POWER SUPPLY This is a multi-level power supply for the liquid crystal drive. The voltage applied is determined by the liquid crystal drive. The voltage applied is determined by the liquid crystal drive. The voltage applied is determined by the input drive. V1.9 POWER SUPPLY This is a multi-level power supply for the liquid crystal drive. The voltage applied is determined by the input drive. V1.9 POWER SUPPLY This is a multi-level power supply for the liquid crystal drive. The voltage applied is determined by the input drive. V1.9 POWER SUPPLY This is a multi-level power supply for the liquid crystal drive. The voltage criteria crystal drive. V3.4 V3 are applied in the power supply turns ON, the internal applied increating internal internal. V3.4 O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal. CAP1- O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal. CAP2- O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal. CAP3- O DC/DC voltage conv				*						
VRS POWER SUPPLY This is the estemally-input VEEG power supply for the LCD power supply voltage regulator : These are only enabled for the models with the VEEG external input option. V1.V2 POWER SUPPLY This is a multi-hevel power supply for the liquid crystal dirts. The voltage applied is determined by the liquid crystal ecl, and a changed through the use of a resistive voltage direded or through changing the impedance us and on pum. Voltage levels are determined based on VDD, and must maintain the relative magnitudes shown below. VDD VDV/VDV2/V2/V2/V32/V42V5 Master operation :When the power supply times ON, the internal power supply circuits produce the V1 to V4 voltage shown below. The voltage scattering are selected using the LCD bias set command. CAP1+ O DC/DC voltage converter Connect a capacitor between this terminal and the CAP1 terminal. CAP2- O DC/DC voltage converter Connect a capacitor between this terminal and the CAP1 terminal. CAP2- O DC/DC voltage converter Connect a capacitor between this terminal and the CAP1 terminal. VR 1 Output voltage converter Connect a capacitor between this terminal and the CAP1 terminal. VR 1 Output voltage converter Connect a capacitor between the streaminal and the CAP1 terminal. VR 1 Output voltage converter Connect a capacitor between the streaminal and the CAP1 terminal. VR 1 Output vol							the liquid crystal driv	20		
VI.V2 VI.V2 <th< td=""><td></td><td></td><td>-</td><td></td><td>-</td><td></td><td></td><td></td></th<>			-		-					
V1.V2 POWER SUPPLY This is a multi-level power supply for the liquid cystal drive. The voltage inpide is determined by the liquid cystal eql, and is changed through the use of a resistive voltage divided or through changing the impedance as an op amp. Voltage levels are determined based on VDD, and must maintain the relative magnitudes shown below. VD VDD-(V10)EV122EV32V42V5 Master operation. When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltage shown below. VDD/PO/DEV122V32V32V42V5 CAP1+ O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal. CAP2+ O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal. CAP2- O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal. CAP3- O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal. CAP3- O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal. V0IT O DD/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal. V0IT O DD/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal. V0IT O DD/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal. VR I <td>VIC</td> <td>TOWER SOTTET</td> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td>	VIC	TOWER SOTTET	-							
V3.V4 crystal cell, and is changed through the use of a resistive voltage divided or theogh changing the impedance us an op amp. Voltage levels are determined based on VDD, and must maintain the relative magnitudes shown below. V10L	V1 V2	POWER SUPPLY						ermined by the liquid		
V5 an op amp. Voltage levels are determined based on VDD, and must maintain the relative magnitudes shown below:		TOWERBOITET	-		-					
below: VDD(-V0)2V12V22V32V42V5 Master operation: "When the power supply turns ON, the internal power supply circuits produce the V1 to V4 Voltage shown below. The voltage settings are selected using the 1CD bias set command. CAP1+ O O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal. CAP2+ O O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal. CAP2- O O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal. CAP2- O O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal. VR 1 Output voltage regulator internal resistors are used (RS="17). these cannot be used when the 'S voltage regulator internal resistors are used (RS="17). these cannot be used when the 'S voltage regulator internal resistors are used (RS="17). D7 to D0 100 This is an 8-bit bi-directional dua to that connects to an 8-bit of 16 bit standard MPU dua bas. (St) and D6 serves as the serial clock input terminal. (SCL). At this time, D0 to D7 are set to high impedance. When the chap select is inactive, D0 to D7 are display data. A0="1".idicates that D0 to D7 are control data. /RES 1 When (RES is set to "1'he settings			-			-				
VDQ-V0j2V12V22V32V42V5 Master operation : When the power supply turns ON , the internal power supply circuits produce the V1 to V4 voltage shown below. The voltage settings are selected using the LCD bias set command. CAPI- O DC/DC voltage converter Connect a capacitor between this terminal and the CAPI - terminal. CAP2- O DC/DC voltage converter Connect a capacitor between this terminal and the CAPI - terminal. CAP2- O DC/DC voltage converter Connect a capacitor between this terminal and the CAPI - terminal. CAP3- O DC/DC voltage converter Connect a capacitor between this terminal and the CAPI - terminal. VWR 1 Output voltage regulator terminal. Provides the voltage between VDI and V5 through a resistive voltage drive These are only enabled when the V5 voltage regulator interminal resistors are not used(RS="1"). D7 to D0 I/O This is an 8-bit bi-directional data bus that connects to an 8-bit of 16 bit standard MPU data bus. (Si) When the serial interface is selected (PS="1", then D7 serves as the serial data in input terminal (SI) and D6 serves as the serial data view. D0 to D7 are voltage between VD1 to D7 are control data. A0 1 This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data tare data or a command. (SI) and D6 serves as the serial data to C21. At this tititin, D0 to D7 are control data.										
Master operation: When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltage advants below. The voltage settings are selected using the LCD bias set command. CAP1+ O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal. CAP2+ O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal. CAP2- O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal. CAP3- O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal. CAP3- O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal. VR I Output voltage regulator terminal. Provides the voltage between VDD and V5 through a resistive voltage divide. VR I Output voltage regulator internal resistors are not sed(RS=1'). O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal. (S) I Output voltage regulator internal resistors are not sed(RS=1'). O DD/D IO Dis is a S=bit b-directional data bus that connects to an 8-bit of 16 bit standard MPU data bus. (S) II Other the set signal theor. Dit D7 are set to high impedance.			VDD(=V0)≥V1≥V2≥	V3≥V4≥V5						
CAPI+ O DC/DC voltage converter Connect a capacitor between this terminal and the CAPI+ terminal. CAPI+ O DC/DC voltage converter Connect a capacitor between this terminal and the CAPI+ terminal. CAP2+ O DC/DC voltage converter Connect a capacitor between this terminal and the CAP2+ terminal. CAP3- O DC/DC voltage converter Connect a capacitor between this terminal and the CAP2+ terminal. CAP3- O DC/DC voltage converter Connect a capacitor between this terminal and the CAP2+ terminal. VR I Output voltage regulator terminal. Provides the voltage between VDD and V5 through a resistive voltage divid These are only enabled when the V5 outlage regulator internal resistors are not used(R85-TL7). these cannot be used when the V5 outlage regulator internal resistors are not used(R85-TL7). these cannot be used when the V5 outlage regulator internal resistors are not used(R85-TL7). these are only enabled when the V5 outlage regulator internal resistors are not used(R85-TL7). these are only enabled when the V5 outlage regulator internal resistors are not used(R85-TL7). these are only enabled when the V5 outlage regulator internal resistors are used (R85-TL7). these are not used(R85-TL7). The the chip select is inactive, D0 to D7 are set to high impedance. This is connect to the least significant bit of the normal MPU data bus. are eat a or a command. A0 The indicates that D0 to D7 are set to high impedance. A0 I This is connect to the "The settings are initialized. The reset operation is performed by the 'RES signal level.					supply turi	ns ON, the internal p	ower supply circuits j	produce the V1 to V4		
CAPI O DC/DC voltage converter Connect a capacitor between this terminal and the CAPI+ terminal. CAP2+ O DC/DC voltage converter Connect a capacitor between this terminal and the CAPI+ terminal. CAP3- O DC/DC voltage converter Connect a capacitor between this terminal and the CAPI+ terminal. CAP3- O DC/DC voltage converter Connect a capacitor between this terminal and the CAPI+ terminal. VR I Output voltage converter Connect a capacitor between this terminal and VS through a resistive voltage divided to the set of the set of voltage regulator internal resistors are not used(IRS="1"). D7 to D0 UO This is an 8-bit bit-directional data bus that connects to an 8-bit ot 16 bit standard MPU data bus. (S1) and Do serves as the serial obte finant terminal (S1). and Do serves as the serial obter function terminal (S1). A0 I This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bare can output statis when the visit obter more data. A0="1".'Idicates that D0 to D7 are control data. //RES I When Res is set of when the RS signal level. //CS1.CS2 I This is the financiant by the /RES signal level. //CS1.CS2 I This is the financiant of the RS signal of the 8080 MPU and the SED 1565 series data bus is in an output statasit when th			voltage shown below.	The voltage s	ettings are	selected using the LO	CD bias set command	l.		
CAP2- O DC/DC voltage converter Connect a capacitor between this terminal and the CAP2- terminal. CAP2- O DC/DC voltage converter Connect a capacitor between this terminal and the CAP1+ terminal. CAP3- O DC/DC voltage converter Connect a capacitor between this terminal and the CAP1+ terminal. VW 1 Output voltage regulator terminal. Provides the voltage between VDD and V5 through a resistive voltage drive these are only cambled when the V5 voltage regulator internal resistors are not usder(RS="L"). These are only cambled when the V5 voltage regulator internal resistors are not usder(RS="L"). These are only cambled when the V5 voltage regulator internal resistors are not usder(RS="L"). These are only cambled when the V5 voltage regulator internal resistors are not usder(RS="L"). The times are only cambled when the V5 voltage regulator internal resistors are not usder(RS="L"). The times are only cambled when the V5 voltage regulator internal resistors are not usder(RS="L"). The times are only cambled when the V5 voltage regulator internal resistors are not usder(RS="L"). The times are only cambled when the V5 voltage regulator internal resistors are not usder(RS="L"). The time the chip select is and D0 to D3 are set to high impedance. Whe the chip select is in active, D0 to D7 are set to high impedance. A0 1 This is a connect to the least significant bit of the normal MPU address bus, and it determines whether the data tare data or a command. A0 1 This is to connect to the RSS tignal of the S00 MPU. A1 The resist operation is performed by the rRES signal level. <	CAP1+	0	DC/DC voltage conve	erter.Connect	a capacitor	between this termina	I and the CAP1- term	ninal.		
CAP2- O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal. CAP3- O DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal. VW 1 Output voltage regulator terminal. Provides the voltage between VDD and V5 through a resistive voltage divid. These are only enabled when the V5 voltage regulator internal resistors are not used (RES="1"). DT to D0 I/O This is an 8-bit bi-directional data bus that connects to an 8-bit of 16 bit standard MPU data bus. (S1) When the serial interface is selected (P/S="1"), then D7 serves as the serial data input terminal (S0) (SCL) and D6 serves as the serial data input terminal. (SCL) and D6 serves as the serial data input terminal CL). At this time, D0 to D5 are set to high impedance. Whe the chip select is inactive, D0 to D7 are display data. A0="1":licitates that D0 to D7 are control data. A0 1 This is connect to the last significant bit of the normal MPU address bus, and it determines whether the data bit are tare accound by the /RES signal level. //RES 1 When the CS1="1" and CS2="1" idicates that D0 to D7 are control data. //REVE 1 When connected to an 8080 MPU, this is active LOW. //REVE 1 When connected to a 8080 MPU, this is active LOW. This is the 6800 Series MPU interminal. <td>CAP1-</td> <td>0</td> <td>DC/DC voltage conve</td> <td>erter.Connect</td> <td>a capacitor</td> <td>between this termina</td> <td>and the CAP1+ terr</td> <td>ninal.</td>	CAP1-	0	DC/DC voltage conve	erter.Connect	a capacitor	between this termina	and the CAP1+ terr	ninal.		
CAP3 O DC/DC voltage converter Connect a capacitor between this terminal and the CAP1+ terminal. VOUT O DC/DC voltage converter Connect a capacitor between this terminal and Vss VR I Output voltage converter Connect a capacitor between this terminal and Vss VR I Output voltage regulator timinal provides the voltage between VDD and V5 through a resistive voltage dvic These are only enabled when the V5 voltage regulator internal resistors are not usdet(RS="1"). D7 to D0 I/O This is an 8-bit to bit standard MPU data bus. (S1) When the serial interface is selected (P/S="1", then D7 serves as the serial data input terminal (S1) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance. Whether the chip select is significant bit of the normal MPU address bus, and it determines whether the data bare data or a command. A0 I This is connect to the last significant bit of the normal MPU address bus, and it determines whether the data bare data or a command. /RES I When (RES is set or "L" he settings are initialized. /RES I When (RES is set or "L" he settings are initialized. /RES I When (RCS is set or "L" and CS2="H", then the chip select becomes active, and data" output status when this signal of the 8080 MPU, and the SED 1565 series data bus is in an output status when this signal of the 8080 MPU, and the SED 1565 series data bus is in an output status when this	CAP2+	0	DC/DC voltage conve	erter.Connect	a capacitor	between this termina	I and the CAP2- term	ninal.		
VOUT O DC/DC volage converter.Connect a capacitor between this terminal and Vss VR 1 Output voltage regulator terminal. Provides the voltage between VDD and VS through a resistive voltage divid These are only enabled when the VS voltage regulator internal resistors are used (IRS="1"). D7 to D0 I/O This is an 8-bit bi-directional data bus that connects to an 8-bit of 16 bit standard MPU data bus. (S1) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance. Whe the chip select is inactive, D0 to D7 are set to high impedance. A0 1 This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data b are data or a command. A0="1":Indicates that D0 to D7 are display data. A0="1":Idicates that D0 to D7 are control data. //RES 1 When R/EE is set to "1",the settings are initialized. The reset operation is performed by the /RES signal level. //CS1,CS2 1 This is the chip select to an 8080 MPU, this is active LOW. This pin is connected to an 8080 MPU, this is active LOW. This pin is connected to the R/D signal of the 8080 MPU and the SED 1565 series data bus is in an output straus when this signal is "1". When connected to a 8080 Series MPU this is active HIGH. This is the 6800 Series MPU this is active HIGH. This is the 6800 Series MPU this is active HIGH. This is the 6800 Series MPU this is active HIGH. This is the Red/write control signal input terminal. When R/W="11".Red. When R/W="1".Write Wren connected to a 80808 MPU this as active HIGH. This is the Red/Write memost to the	CAP2-	0	DC/DC voltage conve	erter.Connect	a capacitor	between this termina	and the CAP2+ terr	ninal.		
VR I Output voltage regulator terminal. Provides the voltage togulator internal resistors are used (RS="1").	CAP3-	0	DC/DC voltage conve	erter.Connect	a capacitor	between this termina	I and the CAP1+ terr	ninal.		
These are only enabled when the V5 voltage regulator internal resistors are used (RS="1"). these cannot be used when the V5 voltage regulator internal resistors are used (RS="1"). D7 to D0 I/O This is an 8-bit bid directional data bus that connects to an 8-bit of 16 bit standard MPU data bus. (S1) When the serial interface is selected (P/S="1"), then D7 serves as the serial data input terminal (S1) and D5 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance. A0 1 This is a concent to the least significant bit of the normal MPU datess bus, and it determines whether the data bare data or a command. A0="H1".indicates that D0 to D7 are estro bigh impedance. /RES 1 When /RES is set to "L" be settings are initialized. The reset operation is performed by the /RES signal level. ////////////////////////////////////	VOUT	0	DC/DC voltage conve	erter.Connect	a capacitor	between this termina	ll and Vss			
these cannot be used when the v5 voltage regulator internal resistors are used (IRS="H'). D7 to D0 1/O This is an 8-bit bi-directional data bus that connects to an 8-bit or 16 bit standard MPU data bus. (S1) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance. Whe the chip select is inactive, D0 to D7 are set to high impedance. A0 A0 I This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data b are data or a command. A0="H':Indicates that D0 to D7 are set to high impedance. /RES I When /RES is set to "L' the settings are initialized. The reset operation is performed by the /RES signal level. //CS1,CS2 I This is the chip select signal. When /CS1="L"and CS2="H",then the chip select becomes active, and data/command UO is cnable. /RD(E) I When connected to a 8080 MPU, this is active LOW. This is the 6800 Series MPU anable clock input termined. When connected to a 6800 Series MPU. /WR,(R/W) I When connected to a 8080 MPU, this is active LOW. This is the cad/write control signal of the S080 MPU and the data bus are latched at the rising edge of the /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. /WR,(R/W) I When connected to a 6800 Series MPU interface.	VR	Ι	Output voltage regula	tor terminal. I	Provides th	e voltage between VI	DD and V5 through a	resistive voltage divid		
D7 to D0 I/O This is an 8-bit bi-directional data bus that connects to an 8-bit of 16 bit standard MPU data bus. (S1) When the serial interface is selected (PS="1"), then D7 serves as the serial data input terminal (S1) and D6 serves as the serial chock input terminal (SCL). At this time, D0 to D5 are set to high impedance. Whe the chip select is inactive, D0 to D7 are set to high impedance. A0 I This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data be are data or a command. A0="H":Indicates that D0 to D7 are display data. A0="L":Idicates that D0 to D7 are control data. /RES I When /RES is set to "L" the settings are initialized. The reset operation is performed by the /RES signal level. /RCS1,CS2 I This is the chip select signal. When /CS1 ="L"and CS2="I", then the chip select becomes active, and data/command I/O is enable. /RD(E) I When connected to a 8080 MPU, this is active LOW. This is in a orupt status when this signal is "L". When connected to a 6800 Series MPU enable clock input termined. /WR,(R/W) I When connected to a 8080 MPU with is active LOW. This is the read/write control signal is "L". When connected to a 6800 Series MPU is signal. The signals on the data bus are latched at the rising edge of the /WR signal. /WR,(R/W) I When connected to a 6800 Series MPU is is active LOW. This is the read/write control signal input terminal. /WR, (R/W) I When conneceted to a 6800 Series MPU interface.			•		-	•		,		
(SI) When the serial interface is selected (P/S="L"), then D7 serves as the serial data input terminal (SI) (SCL) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance . Whe the chip select is inactive, D0 to D7 are set to high impedance. A0 1 This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bar data or a command. A0="H":Indicates that D0 to D7 are display data. A0="L":Idicates that D0 to D7 are control data. /RES 1 When /RES is set to "L":the settings are initialized. /RES 1 This is connected to an 8080 MPU, this is active LOW. /RD(E) 1 When connected to an 8080 MPU, this is active LOW. /This pin is connected to the R/D signal of the 8080 MPU, and the SED 1565 series data bus is in an output status when this signal is "L". . When connected to an 8080 MPU, this is active HGH . This is the 6800 Series MPU enable clock input termined. /WR,(R/W) 1 When connected to a 8080 MPU with is active HGH . This is the ead/write control signal input terminal. When R/W= #T*:Read/WHO WR signal. /Wen R/W="H":Read/Write Control signal input terminal. When R/W=#T*:Read/When R/W=+T*:Write. C86 1 This is the P0/Dimetrace switch terminal. When R/W=#T*:Read/When R/W=+T*:Senia										
(SCL) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance. Whe the chip select is inactive, D0 to D7 are set to high impedance. A0 I This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data b are data or a command. A0="11":Indicates that D0 to D7 are display data. A0="11":Indicates that D0 to D7 are control data. //RES I When /RES is set to "1."the settings are initialized. The reset operation is performed by the /RES signal level. //CSI_CS2 I This is the chip select signal. When /CS1 ="1."and CS2="11";then the chip select becomes active, and data/command I/O is enable. //RD,(E) I . When connected to a 8080 MPU, this is active LOW. This pin is connected to the (RD signal of the 8080 MPU, and the SED 1565 series data bus is in an output status when this signal is "1.". When connected to a 6800 Series MPU inbit is active LOW. This is in is connected to a 6800 Series MPU inbit is active LOW. This is the read/write control signal input terminal. When R/N="11";Read. When R/N="11";Write. //WR,(R/W) I . When connected to a 6800 MPU inbit is active LOW. This is the read/write control signal input terminal. When R/N="11";Read. When R/N="11";Write. //WR, R/W) I . When connected to a 6800 Series MPU is active LOW. This is is the read/write control signal input terminal. When R/N="11";Read. When R/N="11";Read. When R/N="11";Write. //WR, R/W) I . When connected to a 6800 Series MPU is active LOW. This is is the tread/write control sig		I/O								
A0 I This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data b are data or a command. A0-"H'.Indicates that D0 to D7 are display data. A0-"L":Idicates that D0 to D7 are control data. /RES I When /RES is set to "L"the settings are initialized. The reset operation is performed by the /RES signal level. //RD(E) I This is the chip select signal. When /CS1 ="L"and CS2="H", then the chip select becomes active, and data/command I/O is enable. //RD(E) I . When connected to an 8080 MPU, this is active LOW. This pin is connected to the /RD signal of the 8080 MPU, and the SED 1565 series data bus is in an output status when this signal is "L". . When connected to a 6800 Series MPU, this is active HGH . This is the 6800 Series MPU enable clock input termined. /WR,(R/W) I When connected to an 8080 MPU, this is active LOW. This is the factor on 8080 MPU (Mis is active LOW . This is the 6800 Series MPU in terminal. . When connected to a 6800 Series MPU : This is the read/write control signal input terminal. . When connected to a 6800 Series MPU : This is the read/write control signal input terminal. . When R/W="H":Read, When R/W="L":Write. C86 I This is the MPU interface switch terminal. . Read/Write C86="H":6800 MPU /WR signal at input. The following applies depending on the P/S status: . P/S I This is the paralled data input/serial data input. . The following applies depending on the P/S status: . P/S I This is the paralled data input/serial data input. . The following a							-			
A0 I This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data b are data or a command. A0 — H":Indicates that D0 to D7 are display data. A0="L":Idicates that D0 to D7 are control data. /RES I When /RES is set to "L"the settings are initialized. /RES I This is the chip select signal. When /CS1 ="L"and CS2="H",then the chip select becomes active, and data/command I/O is enable. /RD,(E) I . When connected to a 8080 MPU, this is active LOW. This is the chip select signal. When /CS1 ="L"and CS2="H",then the chip select becomes active, and data/command I/O is enable. /RD,(E) I . When connected to a 8080 MPU, this is active LOW. This is the 6800 Series MPU enable clock input termined. . When connected to a 8080 MPU /WR signal . The signals on the data bus are latched at the rising edge of the /WR signal. /WR,(R/W) I . When connected to a 6800 Series MPU : This is the read/write control signal input terminal. /When R/W="H":Read. When R/W="L":Write. This is the Parallel data input serial data input switch terminal. /WR, (R/W) I . When CMC="L":Write. /WR I This is the MPU interface. C86="L":%300 MPU interface /WR I This is the parallel data input switch terminal. When R/W=":L":Main data input sw	(SCL)			-	-		, D0 to D5 are set to	high impedance. Whe		
are data or a command. A0="H":Indicates that D0 to D7 are display data. A0="L":Idicates that D0 to D7 are control data. /RES 1 When /RES is set to "L" the settings are initialized. The reset operation is performed by the /RES signal level.		-								
A0="H":Indicates that D0 to D7 are display data. A0="L":Idicates that D0 to D7 are control data. /RES I When /RES is set to "L"the settings are initialized. /RES I The reset operation is performed by the /RES signal level. //CS1,CS2 I This is the chip select signal. When /CS1 ="L":Idicates that D0 to D7 are control data. /RD,(E) I . When connected to an 8080 MPU ,this is active LOW. This pin is connected to the <i>k</i> PD signal of the 8080 MPU, and the SED 1565 series data bus is in an output status when this signal is "L". . When connected to a 6800 Series MPU this is active HIGH. This is the 6800 Series MPU enable clock input termined. /WR,(R/W) I . When connected to a 8080 MPU /this is active LOW. This is the foot of the /WR signal. . When connected to a 6800 Series MPU intermined. /WR,(R/W) I . When connected to a 6800 Series MPU intermined. /WR,(R/W) I . When connected to a 6800 Series MPU interminal. . When connected to a 6800 Series MPU interminal. . When R/W="H":Read. When R/W="L":Write. C86 I This is the Paralle data input. P/S="L":Sorial data input. P/S I This is the paralle data input. P/S="L":Sorial data input. P/S Data/Command Data R	A0	I		-	ant bit of th	ne normal MPU addre	ess bus, and it determine	nes whether the data b		
/RES 1 When /RES is set to "L"the settings are initialized. The reset operation is performed by the /RES signal level. /CS1,CS2 1 This is the chip select signal. When /CS1 ="L"and CS2="H",then the chip select becomes active, and data/command I/O is enable. /RD,(E) 1 . When connected to an 8080 MPU, this is active LOW. This pin is connected to the /RD signal of the 8080 MPU, and the SED 1565 series data bus is in an output status when this signal is "L". . When connected to a 6800 Series MPU, this is active HIGH. This is it the 6800 Series MPU enable clock input termined. /WR,(R/W) 1 . When connected to a 8080 MPU, this is active LOW . This terminal connects to the 8080 MPU /WR signal .The signals on the data bus are latched at the rising edge of the /WR signal input terminal. . When connected to a 6800 Series MPU : This is the read/write control signal input terminal. . When connected to a 6800 Series MPU : This is the read/write control signal input terminal. . When R/W="H":Read. When R/W="L":Write. C86 1 This is the paralle data input serial data input switch terminal. . C86="H":6800 Series MPU interface C86="L":8080 MPU interface. P/S 1 This is the parallel data input. P/S="L":Serial data input. . The following applies depending on the P/S status: 						AO	h - + D0 + - D7	41		
The reset operation is performed by the /RES signal level. /CS1,CS2 I This is the chip select signal. When /CS1="L"and CS2="H", then the chip select becomes active, and data/command I/O is enable. /RD,(E) I When connected to an 8080 MPU, this is active LOW. This pin is connected to the /RD signal of the 8080 MPU, and the SED 1565 series data bus is in an output status when this signal is "L". When connected to a 6800 Series MPU enable clock input termined. (WR,(R/W) I When connected to a 8080 MPU, this is active LOW. This is the 6800 Series MPU enable clock input termined. (WR,(R/W) I When connected to a 8080 MPU is active LOW. This terminal connects to the 8080 MPU is active LOW. (WR,(R/W) I When connected to a 6800 Series MPU : This is active LOW. This is the read/write control signal. (WR,(R/W) I When connected to a 6800 Series MPU : This is the read/write control signal input terminal. When connected to a 6800 Series MPU : This is the pradimeter set is the maint. (WR, (R/W) I This is the praville data input terminal. When R/W="1"; Write. (WR, (R/W) I This is the praville data input serial data input serial data input. The following applies depending on the P/S status: (P/S) I This is the paralle data input. P/S Data Read/Write	DES	т					that D0 to D7 are con			
/CS1,CS2 I This is the chip select signal. When /CS1 ="L"and CS2="H", then the chip select becomes active, and data/command I/O is enable. /RD,(E) I . When connected to an 8080 MPU, this is active LOW. This pin is connected to the /RD signal of the 8080 MPU, and the SED 1565 series data bus is in an output status when this signal is "L"	/KES	1		-						
data/command I/O is enable. /RD,(E) I . When connected to a 8080 MPU, this is active LOW. This pin is connected to the /RD signal of the 8080 MPU, and the SED 1565 series data bus is in an output status when this signal is "L". . When connected to a 6800 Series MPU this is active HIGH . This is the 6800 Series MPU enable clock input termined. (WR,(R/W) I . When connected to a 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. . When connected to a 6800 Series MPU : This terminal connects to the 8080 MPU /WR signal . The signals on the data bus are latched at the rising edge of the /WR signal. . When connected to a 6800 Series MPU : This is the read/write control signal input terminal. . When R/W="H":Read. When R/W="L": Write. C86 I This is the maPUinterface switch terminal. C86="H":6800 Series MPU interface. C86="L":8080 MPU interface P/S I This is the paralle data input/serial data input. P/S="H":Parallel data input. P/S="L":Serial data input. The following applies depending on the P/S status: P/S Data Read/Write Serial Clock "H" P/S Data/Command Data Read/Write Serial Clock "H" A0 SI(D7) Write only SCL(D6) When P/S="L",D0 to D5 are HZ. D0 to D5 may be "H","L" or Open ./RD(E)and /WR(R/W)are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported. REV : 1	/CS1 CS2	I					he chin select becom	es active and		
/RD,(E) I . When connected to a 8080 MPU ,this is active LOW. This pin is connected to the /RD signal of the 8080 MPU, and the SED 1565 series data bus is in an output status when this signal is "L". . When connected to a 6800 Series MPU this is active HIGH . This is the 6800 Series MPU enable clock input termined. /WR,(R/W) I . When connected to a 8080 MPU ,this is active LOW . This terminal connects to the 8080 MPU /WR signal .The signals on the data bus are latched at the rising edge of the /WR signal. . When connected to a 6800 Series MPU : This is the read/write control signal input terminal. . When connected to a 6800 Series MPU : This is the read/write control signal input terminal. . When connected to a 6800 Series MPU : This is the read/write control signal input terminal. . When R/W="1":Read. When R/W="L":Write. C86 I This is the MPUinterface switch terminal. C86="H":6800 Series MPU interface. C86="L":8080 MPU interface P/S I This is the parallel data input. P/S="T":Parallel data input. P/S="L":Serial data input. The following applies depending on the P/S status: P/S Data/Command Data Read/Write Serial Clock "H" "H" A0 D0 to D7 /RD/WR "L" SCL(D6) When P/S="L",'D0 to D5 are HZ. D0 to D5 may be "H", "L" or Open ./RD(E)and /WR(R/W)are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported.	/051,052	1	-	-	COI L	and C52 11 ,then t	ne emp select becom	es active, and		
This pin is connected to the /RD signal of the 8080 MPU ,and the SED 1565 series data bus is in an output status when this signal is "L". When connected to a 6800 Series MPU ,this is active HIGH . This is the 6800 Series MPU enable clock input termined. /WR,(R/W) I When connected to a 8000 MPU ,this is active LOW . This terminal connects to the 8080 MPU /WR signal . The signals on the data bus are latched at the rising edge of the /WR signal. When connected to a 6800 Series MPU : This is the read/write control signal input terminal. When R/W="H":Read. When R/W="L": Write. C86 I This is the PUInterface switch terminal. WS="H":8800 Series MPU interface. C86="L":8080 MPU interface P/S I P/S I P/S I P/S I P/S Data Read/Write Serial Clock "H" A0 D0 to D7 /RD/WR YL" A0 SI(D7) Write only SCL(D6) When P/S="L",D0 to D5 are HZ. D0 to D5 may be "H","L" or Open ./RD(E)and /WR(R/W)are fixed to either "H" A0 SI(D7) Write only SCL(D6) When P/S="L",D0 to D5 are HZ. D0 to D5 may be "H","L" or Open ./RD(/RD.(E)	I			this is act	ive LOW.				
an output status when this signal is "L". When connected to a 6800 Series MPU this is active HIGH . This is the 6800 Series MPU enable clock input termined. (WR,(R/W) I When connected to an 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. When connected to a 6800 Series MPU : This terminal connects to the 8080 MPU /WR signal. When connected to a 6800 Series MPU : This is the read/write control signal input terminal. When R/W="H":Read. When R/W="L":Write. C86 I This is the read/write control signal input terminal. When R/W="H":Read. When R/W="L":Write. C86 I This is the paralle data input/serial data input switch terminal. P/S I This is the paralle data input/serial data input. The following applies depending on the P/S status: P/S Data/Command P/S Data/Comm										
. When connected to a 6800 Series MPU this is active HIGH . This is the 6800 Series MPU enable clock input termined. /WR,(R/W) I . When connected to an 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. . When connected to a 6800 Series MPU : This terminal connects to the 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. . When connected to a 6800 Series MPU : This is the read/write control signal input terminal. . When R/W="H":Read. When R/W="L":Write. When R/W="H":Read. When R/W="L":Write. C86 I This is the MPU interface switch terminal. C86 I This is the paralle data input. P/S I This is the paralle data input. P/S="H":Parallel data input. P/S="T.":Serial data input. The following applies depending on the P/S status: P/S P/S Data/Command Data Read/Write Serial Clock "H" A0 D0 to D7 "H" or "L". With serial data input, RAM display data reading is not supported. SCL(D6)										
WR,(R/W) I . When connected to an 8080 MPU ,this is active LOW . This terminal connects to the 8080 MPU /WR signal . The signals on the data bus are latched at the rising edge of the /WR signal. . When connected to a 6800 Series MPU : This is the read/write control signal input terminal. When R/W="H":Read. When R/W="L":Write. C86 I This is the MPUInterface switch terminal. C86="H":6800 Series MPU interface. C86="L":8080 MPU interface P/S I This is the paralle data input/serial data input switch terminal. P/S="H":Parallel data input. P/S="L":Serial data input. The following applies depending on the P/S status: P/S I This is the Zarallel data input. P/S="L":Serial data input. The following applies depending on the P/S status: P/S Data/Command Data Read/Write Serial Clock "H" A0 D0 to D7 /RD,/WR SCL(D6) When P/S="L",D0 to D5 are HZ. D0 to D5 may be "H", "L" or Open ./RD(E)and /WR(R/W)are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported. REV : 1										
A This terminal connects to the 8080 MPU /WR signal .The signals on the data bus are latched at the rising edge of the /WR signal. . When connected to a 6800 Series MPU : This is the read/write control signal input terminal. When R/W="H":Read. When R/W="L":Write. When R/W="H":Read. When R/W="L":Write. C86 I This is the MPUInterface switch terminal. C86 I This is the paralle data input/serial data input switch terminal. P/S I This is the paralle data input. P/S="L":Serial data input. P/S="H":Parallel data input. P/S erial Clock "H" A0 D0 to D7 "K" A0 SI(D7) Write only SCL(D6) When P/S=""L",D0 to D5 are HZ. D0 to D5 may be "H", "L" or Open ./RD(E)and /WR(R/W)are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported.			This is the 6800 Series MPU enable clock input termined.							
the rising edge of the /WR signal. . When connected to a 6800 Series MPU : This is the read/write control signal input terminal. When R/W="H":Read. When R/W="L":Write. C86 I This is the MPUinterface switch terminal. C86="H":6800 Series MPU interface. C86="L":8080 MPU interface P/S I This is the parallel data input/serial data input switch terminal. P/S="H":Parallel data input. The following applies depending on the P/S status: P/S Data/Command P/S Data/Command P/S Data/Command P/S Data/Command P/S Utal/Command P/S Data/Command P/S Data/Command P/S Data/Command When P/S="L",D0 to D5 are HZ. D0 to D5 may be "H","L" or Open ./RD(E)and /WR(R/W)are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported. LOMON GOLDENTEK DISPLAY CORP. GG1206N8SKN1T	/WR,(R/W)	Ι	. When connected to a	an 8080 MPU	,this is act	tive LOW .				
. When connected to a 6800 Series MPU : This is the read/write control signal input terminal. When R/W="H":Read. When R/W="L":Write. C86 I This is the MPU interface switch terminal. C86="H":6800 Series MPU interface. C86="L":8080 MPU interface P/S I This is the paralle data input/serial data input switch terminal. P/S="H":Parallel data input. P/S Data/Command Data Read/Write Serial Clock "H" A0 D0 to D7 /RD/WR "EL" A0 SI(D7) Write only SCL(D6) When P/S="L",D0 to D5 are HZ. D0 to D5 may be "H", "L" or Open ./RD(E)and /WR(R/W)are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported. LOMON GOLDENTEK DISPLAY CORP. GGG1206N8SKN11T			This terminal connect	ets to the 8080) MPU /W	R signal . The signals	on the data bus are la	itched at		
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When R/W="H":Read. When R/W="L":Write. C86 I This is the MPUinterface switch terminal. C86="H":6800 Series MPU interface. C86="L":8080 MPU interface P/S I This is the paralle data input/serial data input switch terminal. P/S="H":Parallel data input. P/S I The following applies depending on the P/S status: P/S Data/Command When P/S="L": Not to D5 are HZ. D0 to D7 When P/S="L": D0 to D5 are HZ. D0 to D5 may be "H"; "L" or Open ./RD(E)and /WR(R/W)are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported. LOMON GGC1206N8SKN1T REV: 1										
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C86="H":6800 Series MPU interface. C86="L":8080 MPU interface P/S I This is the paralle data input/serial data input switch terminal. P/S="H":Parallel data input. P/S="H":Parallel data input. P/S Data/Command Data Read/Write Serial Clock "H" A0 D0 to D7 "H" A0 SI(D7) Write only SCL(D6) When P/S="L",D0 to D5 are HZ. D0 to D5 may be "H", "L" or Open ./RD(E)and /WR(R/W)are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported.		_				te.				
P/S I This is the paralle data input/serial data input switch terminal. P/S="H":Parallel data input. P/S="L":Serial data input. The following applies depending on the P/S status: P/S Data/Command Data Read/Write Serial Clock "H" A0 D0 to D7 /RD,/WR "I" GG1206 N8SKN1T SCL(D6) When P/S="L",D0 to D5 are HZ. D0 to D5 may be "H","L" or Open ./RD(E)and /WR(R/W)are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported. REV : 1 LOMON GOLDENTEK DISPLAY CORP. GG1206N8SKN1T REV : 1	C86	I				2 2000 NOLL: 4 C				
P/S="H":Parallel data input. P/S="L":Serial data input. The following applies depending on the P/S status: P/S Data/Command Data Read/Write Serial Clock "H" A0 D0 to D7 /RD,/WR "L" A0 SI(D7) Write only SCL(D6) When P/S="L",D0 to D5 are HZ. D0 to D5 may be "H","L" or Open ./RD(E)and /WR(R/W)are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported. LOMON GOLDENTEK DISPLAY CORP. GG1206N8SKN1T REV : 1	D/S	т					UC			
The following applies depending on the P/S status: P/S Data/Command Data Read/Write Serial Clock "H" A0 D0 to D7 /RD,/WR "L" A0 SI(D7) Write only SCL(D6) When P/S="L",D0 to D5 are HZ. D0 to D5 may be "H", "L" or Open ./RD(E)and /WR(R/W)are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported. LOMON GOLDENTEK DISPLAY CORP. GG1206N8SKN1T REV : 1	P/S	1	-	-	-					
P/S Data/Command Data Read/Write Serial Clock "H" A0 D0 to D7 /RD,/WR "L" A0 SI(D7) Write only SCL(D6) When P/S="L",D0 to D5 are HZ. D0 to D5 may be "H", "L" or Open ./RD(E)and /WR(R/W)are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported. REV : 1 LOMON GOLDENTEK DISPLAY CORP. GG1206N8SKN1T REV : 1				-		-				
"H" A0 D0 to D7 /RD,/WR "L" A0 SI(D7) Write only SCL(D6) When P/S="L",D0 to D5 are HZ. D0 to D5 may be "H", "L" or Open ./RD(E)and /WR(R/W)are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported. SCL(D6) LOMON GOLDENTEK DISPLAY CORP. GG1206N8SKN1T REV : 1							Read/Write	Serial Clock		
"L" A0 SI(D7) Write only SCL(D6) When P/S="L",D0 to D5 are HZ. D0 to D5 may be "H","L" or Open ./RD(E)and /WR(R/W)are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported. REV : 1 LOMON GOLDENTEK DISPLAY CORP. GG1206N8SKN1T REV : 1								Serial Clock		
When P/S="L",D0 to D5 are HZ. D0 to D5 may be "H","L" or Open ./RD(E)and /WR(R/W)are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported. LOMON GOLDENTEK DISPLAY CORP. GG1206N8SKN1T							· · · · · · · · · · · · · · · · · · ·	SCL(D6)		
"H"or "L". With serial data input, RAM display data reading is not supported. LOMON GOLDENTEK DISPLAY CORP. GG1206N8SKN1T							5			
LOMON GOLDENTEK DISPLAY CORP. GG1206N8SKN1T REV:1						-		.,		
GG1206N8SKN11					1	<u> </u>				
L:886-7-788-6800 FAX:886-7-788-6806~8 UU12U0N85KN11 PAGE · 1	LOMON	GOLDENTER	K DISPLAY	CORP.		120(10)	CUNIT	REV : 1		
	L : 886-7-	788-6800 FA	AX : 886-7-788-6	5806~8	UU	1200N8	SKNII	PAGE : 1		

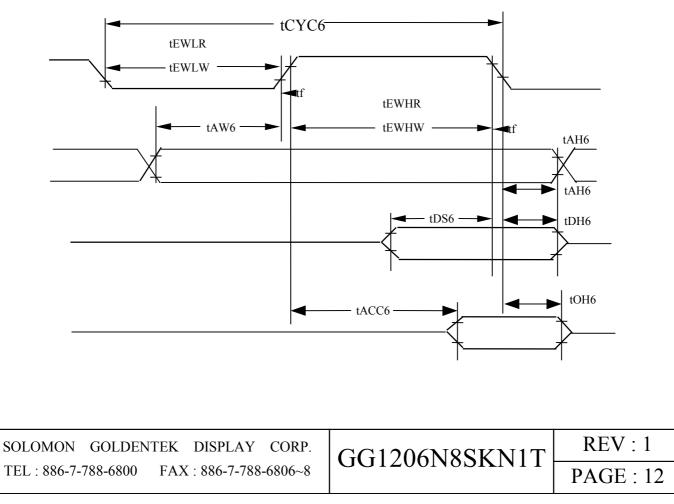
PAGE : 11

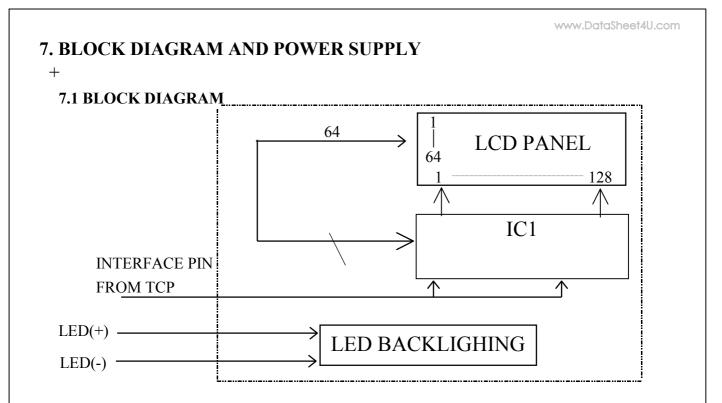
Pin Name	I/O				Fun	ction						
CLS	Ι				nable or disable the displa	a clock internal	oscillator circuit.					
		CLS="H":Internal oscillator circuit is enabled										
		CLS="	L":Inter	nal oscillator c	ircuit is disabled(requires	external input)						
		When CL	.S="L",ii	nput the displa	yclock through the CL ter	minal.						
M/S	Ι	This term	inalseled	ets the master/s	lave operation for the SEI	D1565 Series c	hips. Master oper	ation outputs	the timin			
		signals that are required for the LCD display, while slave operation inputs the timing signals required for the liquid										
		crystal dis	splay ,sy	nchronizing th	e liquid crystal display sy	stem.						
		M/S="	H":Mast	er operation	M/S="L":Slave operatio	n						
		The follow	wing is t	rue depending	on the M/S and CLS statu	15:						
		M/S C	LS OS	scillator Circui	t Power Supply Circuit	CL	FR	FRS	DOF			
		"H"	"H"	Enable	Enable	Output	Output	Output	Outpu			
			"L"	Disable	Enable	Iput	Output	Output	Outpu			
		"L"	"H"	Disable	Disable	Iput	Iput	Output	Iput			
			"L"	Disable	Disable	Iput	Iput	Output	Iput			
CL	I/O			clock input te		-F	-F	p	-1.01			
CE	10			-	on the M/S and CLS statu	15						
		The follow		M/S		LS		CL				
								Output				
			"Н" "Н" "L"									
			L									
		XX71 (1	GED 16	VC 0 · 1·				Input	1			
	*/0				s is used in master/slave n		is CL terminal mu	ist e connecte	d.			
FR	I/O				ing current signal I/O tern	nınal.						
		M/S ="H	-		-							
					is used in master/slave mo		FR terminals mu	st be connecte	ed.			
/DOF	I/O	This is the liquid crystal display blanking control terminal.										
		M/S="H":Output M/S="L":Input When the SED1565 SERies chip used in master/slave mode ,the various /DOF terminal must be connected.										
						de, the various	/DOF terminal m	ust be connec	ted.			
FRS	0		This is the output terminal for the static drive.									
		This is terminal is only enabled when the static indicator display is ON when in master operation mode, and is used in										
				the FR termina								
IRS	Ι				s for the V5 voltage level	adjustment.						
		IRS="H	":Use th	e internal resis	tors							
		IRS="L'	":Do not	use the interna	al resistors. The V5 voltag	e level is regula	ated by an externa	al resistive vo	ltage divi			
		attached t	to the VI	R terminal.								
		-		5	e master operation mode							
					hen the slave opertion mo							
/HPM	Ι		-		for the power supply circ	uit for liquid c	rystal drive.					
				mal mode								
		/HPM="	'L'':High	power mode								
		-		-	e master opertion mode is							
					hen the slave opertion mo							
SEG0	0	These ar	re the liq	uid crystal seg	ment drive outputs. Throu	igh a combinati	on of the content	s of the displa	ay RAM a			
to		with the F	FR signa	l , a singale lev	rel is selected from VDD,	V2,V3,and V5.						
SEG131		RAM I	DATA	FR		Output	Voltage					
					Normal Displa	iy	Re	verse Display	r			
		Н	[Н	VDD			V2				
		Н	[L	V5			V3				
		L	,	Н	V2			VDD				
		L	,	L	V3			V5				
		Power				V	DD					
I				. I								
									T 7 1			
LOMON	GOLDEN	TEK D	ISPLA	Y CORI	$\operatorname{GG120}^{2}$	GNIQO		RE	V:1			
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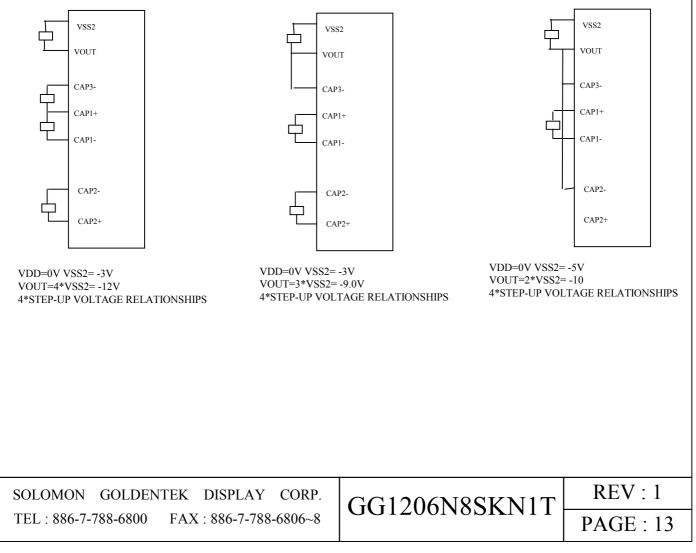
				▼33 5.6 ▼ ±	,	-	
Item		Sgnal	Symbol	Conditions	Min.	Max.	Unit
System cycle tii	ne		tCYC6		200		ns
Address setup t	ime	(A0)	tAW6		10		ns
address hold tin	ne	R/\overline{W}	tAH6		10		ns
Data setup time			tDS6		20		ns
Data hold time		D0 D7	tDH6		10		ns
Output disable	time	D0-D7	tOH6	CL=100Pf	10	50	ns
Access time			tACC5			70	ns
Enable H pulse	READ	ŗ	tEWHR		77		ns
width	WRITE	Ε	tEWHW		22		ns
Enable L pulse	READ	Ţ	tEWLR		117		ns
width	WRITE	Ε	tEWLW		172		ns
Input signal cha	inge		tr,tf			15	ns
time	-						

Vss=-5.0V± 10%,Ta=-30~85°C





7.2 POWER SUPPLY FOR LCM



8. FUNCTION OF EACH BLOCK

• Selecting the interfaec type

With the SED1565 Serieschips, data transfers are done through an 8-bit bidirectional data bus (D7 to D0)or through a serial data input(SI). Through selecting the P/S terminal polarity to the "H" or "L" it is possible to select either parallel data input or serial data input as shown in Table1.

P/S	CS1	CS2	A0	RD	WR	C86	D7	D6	D5-D0
H:Parallel Input	$\overline{\text{CS1}}$	CS2	A0	RD	$\overline{\mathrm{WR}}$	C86	D7	D6	D5-D0
L:Serial Input	CS1	$\overline{\text{CS2}}$	A0				SI	SCL	(Hz)

The Parallel interface

When the parallel interface has been selected (P/S="H"), then it is possible to connect directly to either an 8080-system MPU or a 6800 Series MPU (as shown in Table 2) by selecting the C86 terminal to either "H" or to "L".

C86	MPU type	$\overline{\text{CS1}}$	$\overline{\text{CS2}}$	A0	RD	WR	D7 TO D0
HIGH	6800-SERIES	$\overline{\text{CS1}}$	$\overline{\text{CS2}}$	A0	Е	R/W	D7 TO D0
LOW	8080-SERIES	$\overline{\text{CS1}}$	$\overline{\text{CS2}}$	A0	RD	WR	D7 TO D0

Moreover, data bus signals are recognized by a combination of A0,RD(E),WR(R/W) signals, as shown in table3.

Γ	· · · ·	6800 series	Ŭ Ź	Series	FUNTION					
-	Shareu				I'UNTION					
	A0	R/W	RD	WR						
	1	1	0	1	Reads the display data					
	1	0	1	0	Writes the display data					
	0	1	0	1	Status read					
	0	1	1	0	write control data (command)					

The Chip select

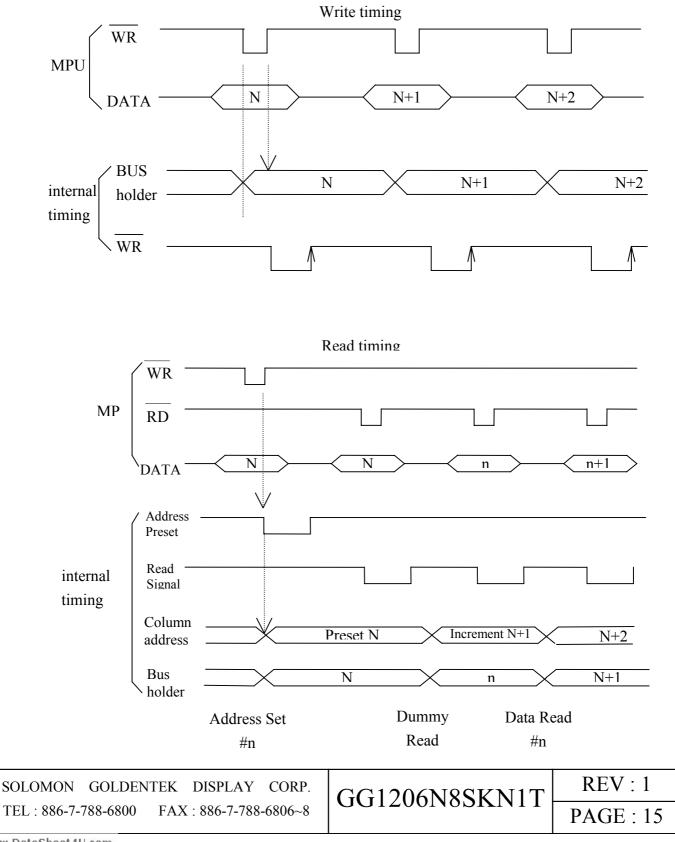
The SED1565 Series chips have two chip select terminals:CS1 and CS2. THE MPU interface is enabled only when CS1="L" and cs2="H" when the chip select is inactive,D0 to D7 enter a high impedance state, and the A0,RD,and WR inputs are inactive. When the serial interface is selected, the shift register and the counter are reset.

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GG1206N8SKN1T

The Busy Flag

When the busy flag is "I" it indicates that the SED1565 Series chip is running internal processes, and at this time no command aside from a status read will be received. If the cycle time (t_{cyc}) is maintained, it is not necessary to check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.



*There are constraints on the display data RAM read sequence. When an address set has been performed and is immediately follower by a read command,one must be cautious because the data that is output is not from the specified address; the data from the specified address is output the second time that the data is read.Consequently,one dummy read cycle is required after an has been set or after a write cycle.

Display Data RAM

Display Data RAM

The display data RAM is a RAM that stores the dot data for the display. It has a 65(8 page*8bit+1)*132 it structure. It is possible to access the desired bit by specifying the page address and the column address. Because, as is shown in Figure 3,the D7 to D0 display data from the MPU corresponds to the liguid crystal display common direction, there are few constraints at the time of display data transfer when multiple SED1565 series chips are used, thus and display structures can be created easily and with a high degree of freedom.

Moreover, reading form and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is assessed asynchronously during liquid crystal display, it will not cause adverse effects on the display(such as flickering).

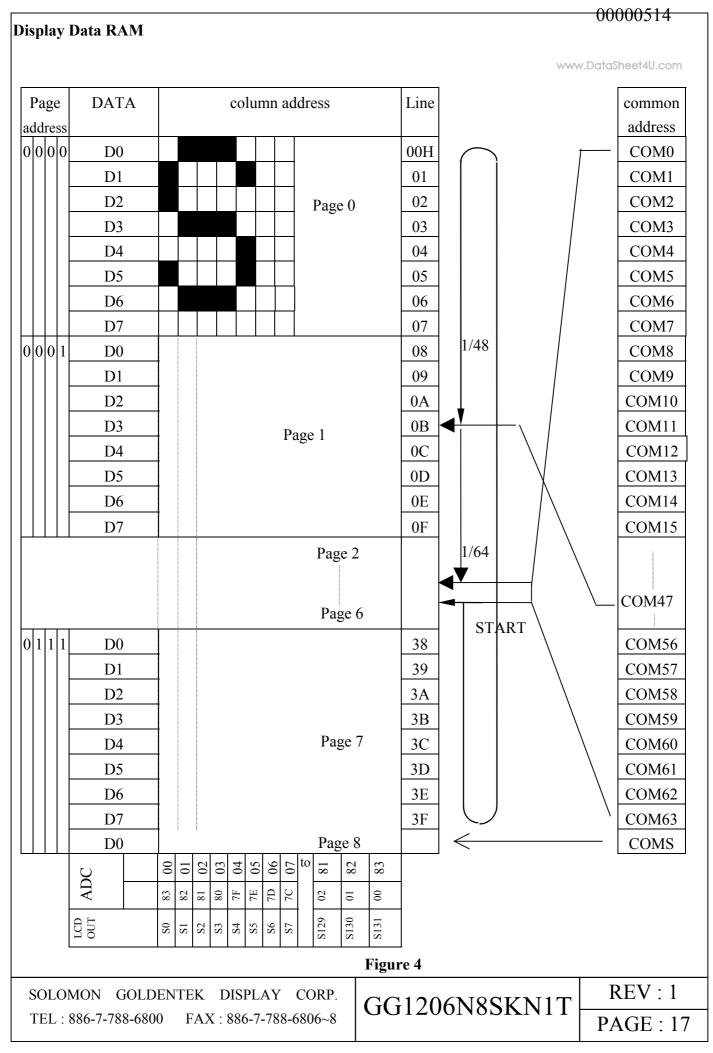
					 _
D0	0	1	1	1	
D1	1	0	0	0	
D2	0	0	0	0	
D3	0	1	1	1	
D4	1	0	0	0	

Display data RAM

COM0			
COM1			
COM2			
COM3			
COM4			

Liquid crystal Display





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COMMANDS

The SED1565 Series chips identify the data bus signals by a combination of

A0, $\overline{\text{RD}}(\text{E})$, $\overline{\text{WR}}(\text{R/W})$ signals. Command interpretation and execution does not depend on the external clock,but rather is performed through intermal timing only, and thus the processing is fast enough that normally a buy check is not required. In the 8080 MPU interface, commands are launched by inputting a low pulse to the $\overline{\text{RD}}$ terminal for reading, and inputting a low pulse to the $\overline{\text{WR}}$ terminal for writing. In the 6800 Series MPU interface, the interface is placed in a read mode when an "H" signal is input to the $\overline{\text{R/W}}$ terminal and placed in a write mode when a "L" signal is input to the $\overline{\text{R/W}}$ terminal and then the command is launched by inputting a high pulse to the $\overline{\text{E}}$ terminal.Consequently,the 6800 Series MPU interface is different than the 80x86 Series MPU interface in that in the explanations of commands and the display commands the status read and display data read $\overline{\text{RD}}(\text{E})$ becomes"1(H)".In the explanations below the commands are explained using the 8080 Series MPU interface as the example.

When the serial interface is selected, the data is input in sequence starting with D7.

<Explanation of Commands>

Display ON / OFF

This command turns the display ON and OFF

A0	$\overline{RD}(E)$	$\overline{WR}(R/\overline{W})$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	DISPLAY ON
										0	DISPLAY OFF

When the display OFF command is executed when in the display all points ON mode, power saver mode is entered. See the section on the power saver for details.

Display Start Line Set

This command is used to specify the display start line address of the display data RAM shown in Figure 4. for further details see the explanation of this function in "The Line Address Circuit".

A0	$\overline{RD}(E)$	$\overline{WR}(R/\overline{W)}$	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	0	0	1	0	2
							↓				\checkmark
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

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Page Address Set

This command specifies the page address of the display data RAM shown in Figure 4. See the explanation of this function in "The Page Address Circuit" for details.

A0	$\overline{RD}(E)$	$\overline{WR}(R/\overline{W})$	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
									7		\downarrow
							0	1	1	1	7
							1	0	0	0	8

Column Address Set

This command specifies the column address of the display data RAM shown in Figure 4. The column address is split into two sections (the higher 4 bits and the lower 4 bits)when it is set(fundamentally, set continuously).Each time the display data RAM is accessed, the column automatically increments (+1), making it possible for the MPU to continuously read from/write to the display data. See the function explanation in "The Column Address Circuit," for details.

	A0	$\overline{RD(E)}$	$\overline{WR}(R/\overline{W})$	D7	D6	D5	D4	D3	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0	Column
																				address
High bits	0	1	0	0	0	0	1	A7	A6	A5	A4	0	0	0	0	0	0	0	0	0
High bits							0	A3	A2	A1	A0	0	0	0	0	0	0	0	1	1
												0	0	0	0	0	0	1	0	2
																7				↓
												1	0	0	0	0	0	1	0	130
												1	0	0	0	0	0	1	1	131

Status Read

A0	RD(E)	$\overline{WR}(R/W)$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

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BUSY	When BUSY =1, it indicaltes that either processing is occurring internally or a reset
	condition is in process.While the chip does not accept commands until BUSY=0,if
	the cycle time can be satisfied, there is no need to check for BUSY conditions.
ADC	This showns the relationship between the column address and the segment driver.
	0:Reverse (column address 131-n↔SEG n)
	1:Normal (column address n↔SEG n)
	(The ADC command switches the polarity.)
ON/OFF	ON/OFF: indicates the display ON/OFF state.
	0:Display ON
	1:Display OFF
	(This display ON/OFF command switches the polarity.)
RESET	This indicates that the chip is in the process of initialization either because of a
	(RES)signal or because of a reset command.
	0:Operating state
	1:Reset in progress

Display Data Write

This command writes 8-bit data to the specified display data RAM address.

A0	$\overline{RD}(E)$	$\overline{WR}(R/\overline{W})$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0				Writ	e dat	a		

Display Data Read

This command reads 8-bit data from the specified display data RAM address. One dummy read required immediately after the column address has been set.SEE the function explanation in "Display Data RAM" for the explanation of accessing the internal registers.

A	$\overline{RD}(E)$	$\overline{WR}(R/\overline{W})$	D7	D6	D5	D4	D3	D2	D1	D0						
1	0	1				Read	l data	ı								
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ADC Select(Segment Driver Direction Select)

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This command can reverse the correspondence between the display RAM data column address and the segment driver output. See the explanation of the function in "Column Address Circuit" for details.

A0	RD(E)	$\overline{WR}(R/\overline{W})$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Rotate right(normal)
										1	Rotate left(reverse)

Display Normal/Reverse

This command can reverse the lit and unit display without overwriting the contents of the display data RAM. When this is done the display data RAM contents are maintained.

A0	$\overline{RD}(E)$	$\overline{WR}(R/\overline{W})$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM Data"H"
											LCDO Nvoltage(normal)
										1	RAM Data "L"
											LCD ON voltage (reverse)

Display All Point ON/OFF

This command makes it possible to force all display points ON regardless of the content of the display data RAM. The contents of the display data RAM are maintained when this is done. This command takes priority over the display normal/reverse command.

A0	$\overline{RD}(E)$	$\overline{WR}(R/\overline{W})$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display mode
										1	Display all points ON

When the display is in an OFF mode, excuting the display all points ON command will place the display in power save mode. For details, see the (20)Power Save section.

LCD Bias Set

This command selects the voltage bais ratio required for the liquid crystal display.

A0	$\overline{RD(E)}$	$\overline{WR}(R/\overline{W})$	D7	D6	D5	D4	D3	D2	D1	D0	select status
0	1	0	1	0	1	0	0	0	1	0	1/9 bias
										1	1/7 bias

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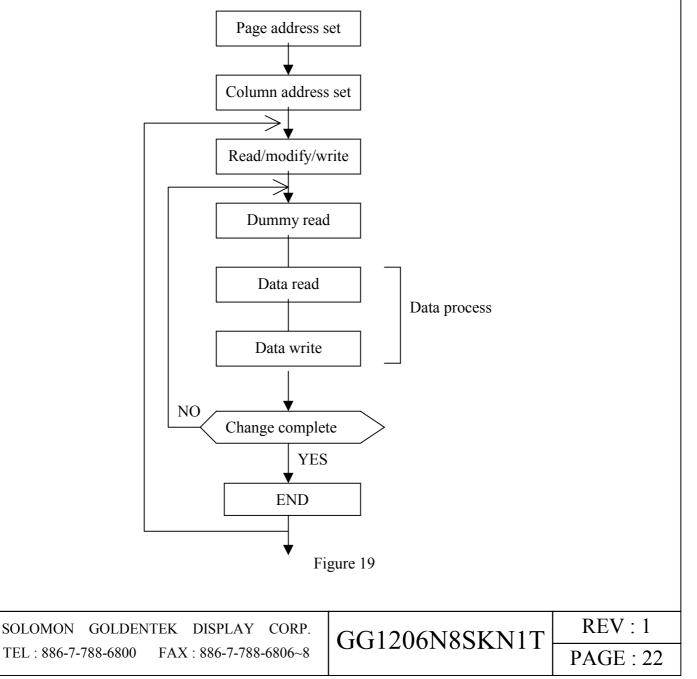
Read/Modify/Write

jamesThi@goddentekieom:Wpaired with the "END" command. Once this command has been input, the display data read command does not change the column address, but only the display data write command increments(+1)the column address. This mode is maintained unit the END command is input .When the END command is input, the column address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

A0	$\overline{RD}(E)$	$\overline{WR}(R/W)$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

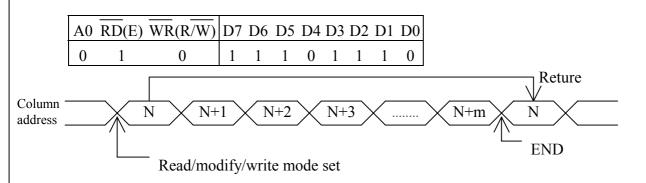
*Even in read/modify/write mode, other commands aside from display data read/write commands can also be used. However,the column address set command cannot be used.

*The sequence for cursor display



END

This command releases the read/modify/write mode, and returns the column addres to the address it was when the mode was entered.



Reset

This command initializes the display start line, the column address , the page address, the common output mode, the V5 voltgae regulator internal resistor ratio, the electronic volume, and the static indicator are reset, and the read/modify/write mode and test mode are released. There is no impact on the display data RAM. See the function explanation in "Reset" for details.

The initialization when the power supply is applied must be done through applying a reset signal to the RES terminal.

The reset operation is performed after the reset command is entered.

A0	$\overline{RD}(E)$	$\overline{WR}(R/\overline{W})$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

The initialization when the power supply is applied must be done through applying a reset signal to the $\overline{\text{RES}}$ terminal.

The reset command must not be used instead.

Command Output Mode Select

This command can select the scan direction of the COM output terminal. For details, see the function explanation "Command Output Mode Selet Circuit."

	A0	RD (E)	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
	0	1	0	1	1	0	0	0	*	*	*	Normal COM→COM63
\geq								1				Reverse COM63→COM
-												*Disabled bit

Power Controller Set

This command sets the power supply circuit functions. See the function explanation in "The Power Supply Circuit," for details

A0	$\overline{RD}(E)$	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	0	0	1	0	1	0			Set-up circuit:OFF
								1			Set-up circuit:ON
									0		Voltage regulator circuit:OFF
									1		Voltage regulator circuit:ON
										0	Voltage follower circuit:OFF
										1	Voltage follower circuit:ON

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[Translator's Note: the abbreviations explained within these parentheses for V and V/F have been written out in the English translation and are therefore no longer necessary.]

V5 Voltage Regulator Internal Resister Ratio Set

This command sets the V5 voltage regulator internal resistor ratio. For details, see the function explanation is "The Power Supply Circuits."

A0	$\overline{RD}(E)$	$\overline{WR}(R/\overline{W})$	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									\vee		
								1	1	0	\vee
								1	1	1	Large

The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal driver voltage V5 through the output from the voltage regulator circuits of the internal liquid crystal power supply. This command is a two byte command used as a pair with the electronic volume mode set command and electronic volume register set command, and both commands must be issued one after the other.

The Electronic Volume Mode Set

When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	$\overline{RD}(E)$	$\overline{WR}(R/\overline{W})$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal drive voltage V5 assumes one of the 64 voltage levels.

When this command is input, the electronic volume mode is released after the electronic volume register has been set.

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A0	RD(E)	$\overline{WR}(R/\overline{W})$	D7	D6	D5	D4	D3	D2	D1	D0	V5 www.DataShee	t4U.com
0	1	0	*	*	0	0	0	0	0	1	Small	
0	1	0	*	*	0	0	0	0	1	0		
0	1	0	*	*	0	0	0	0	1	1		
0	1	0					\bigvee					
0	1	0	*	*	1	1	1	1	1	0	\vee	
0	1	0	*	*	1	1	1	1	1	1	Large	
											*Inactive bit	

When the electronic volume function is not used this to (1,0,0,0,0,0)

* The Electronic Volume Register Set Sequence

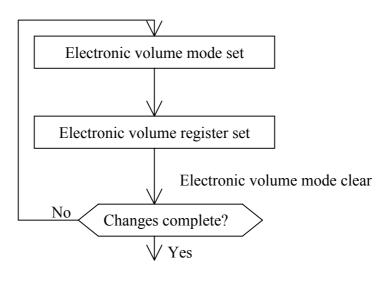


Figure 21

Static Indicator(Double Byte Command)

This command controls the static drive system indicator display. The staric indicator display is controlled by this command only, and is independent of other display control commands.

This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes.

The static indicator ON command is a double byte command paired with the static indicator register set command, and thus one must execute one after the other.(The static indicator OFF command is a single byte command.)

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*Static Indicator ON/OFF

When the static indicator ON command is entered, the static indicator register set command is enable. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

A0	E(RD)	R/W(WR)	D7	D6	D5	D4	D3	D2	D1	D0	Static indicator
0	1	0	1	0	1	0	1	1	0	0	OFF
										1	ON

*Static Indicator Register Set

This command sets two bits of data into the static indicator register, and is used to set the static indicator into blinking mode.

A0	E(RD)	R/W(WR)	D7	D6	D5	D4	D3	D2	D1	D0	Indicator Display Sets
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON(blinking at approximately one second intervals
									1	0	ON(blinking at approximately 0.5 second intervals
									1	1	ON (constantly on)

*Static Indicator Register Set Sequence

Static indicator mode set Static indicator register set No Changes complete? Figure 22 Yes

Power Save (Compound command)

When the display all points ON is performed while the display is in the OFF mode, the power saver mode is entered, thus greatly reducing power consumption.

The power saver mode has two different modes: the sleep mode and the standby mode. When the indicator is OFF, it is the sleep mode that is entered. When the static indicator is ON, it is the standby mode that is entered.

In the sleep mode and in the standby mode, the display data is saved as is the operating mode that was in effect before the power saver mode was initiated, and the MPU is still able to access the display data RAM.

The power saver mode is cleared by the display all points OFF command.

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*Disabled bit

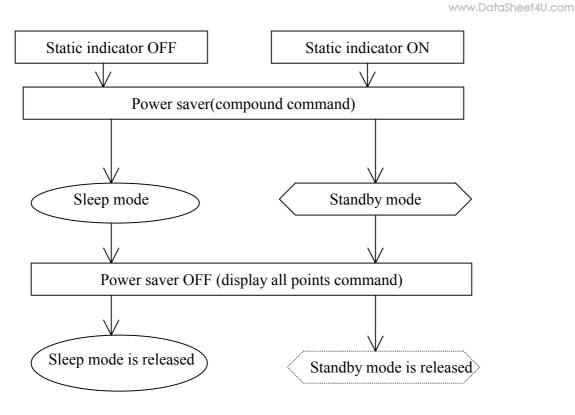


Figure 23

* Sleep Mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:

The oscillator circuit and the LCD power supply circuit are halted.

@All liquid crystal drive circuits are halted, and the segment in common drive outputs output a V_{DD} level.

*Standby mode

The duty LCD display system opertions are halted and only the static drive system for the indicator continues to operte, providing the minmun required consumption current for the static driver. The internal modes are in the following states during standby mode.

① The LCD power supply circuits are halted. The oscillator circuit continues to operate.

⁽²⁾ The duty drive system liquid crystal drive circuits are halted and the segment and common driver outputs output a VDD level. The static drive system does not operate.

When a reset command is performed while in standby mode, the system enters sleep mode.

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When an external power supply is used, it is recommended that the functions of the external power supply circuit be stopped when the power saver mode is started.For example, when the various levels of liquid crystal drive voltage are provided by external resistive voltage dividers, it is recommended that a citcuit be added in order to cut the electrical current floeing through the resistive voltage divider circuit when the power saver mode is in effect.The SED1565 series chips have a liquid crtstal display blanking control terminal DOF.This terminal enters an "L"state when the power saver mode is launched. Using the output of DOF, it is possible to stop the function of an external power supply circuit.

NOP

Non-OPeration Command

A0	$\overline{RD}(E)$	$\overline{WR}(R/\overline{W})$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

Test

This is a command for IC chip testing.Please do not use it.If the test command is used by accident, it can be cleared by applying a "L" signal to the $\overline{\text{RES}}$ input by the reset command or by using an NOP.

A0	RD(E)	$\overline{WR}(R/\overline{W})$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*
						*	Lea		. 1 .:+	

*Inactive bit

Note: The SED 1565 Series chips maintain their operating modes unit something happens to change them. Consequently, excessive external noise, etc., can change the internal modes of the SED 1565 Series chip. Thus in the packaging and system design it is necessary to suppress the noise or take measure to prevent the noise from influencing the chip. Moreover, it is recommended that the operating modes be refreshed periodically to prevent the effects of unanticipated noise.

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Table 16 Table of SED 1565 Series Commands

Command Code												
	L	n -							n •			
Command	A0								D2			Function
(1)Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0	LCD display ON/OFF
											1	0:OFF ,1:ON
(2)Display start line set	0	1	0	0	1	D	ispl	ay st				Sets the display RAM display start line address
(3)Page address set	0	1	0	1	0	1	1		ige a			Sets the display RAM page address
(4)Column address set	0	1	0	0	0	0	1					Sets the most significant 4 bits of the display
upper bit												RAM column address
Column address set	0	1	0	0	0	0	0			<u> </u>	ficant	6 1 5
lower bit											dress	
(5)status read	0	0	1		Sta	itus		0	0	0	0	Reads the status data
(6)Display data write	1	1	0			1	Writ	e da	ta			Write to the display RAM
(7)Display data read	1	0	1]	Read	d dat	ta			Reads from the display RAM
(8)ADC select	0	1	0	1	0	1	0	0	0	0	0	Sets the display RAM address SEG output
											1	correspondence 0:normal, 1:reverse
(9)Display normal/reverse	0	1	0	1	0	1	0	0	1	1	0	Sets the LCD display normal/reverse
											1	0:normal, 1:reverse
(10)Display all points	0	1	0	1	0	1	0	0	1	0	0	Display all points 0:normal display
ON/OFF											1	1:all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0	Sets the LCD drive voltage bias ratio
											1	SED 1565 0:1/9 , 1:1/7
(12)Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write:+1
												At read:0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15)Common output mode	0	1	0	1	1	0	0	0	*	*	*	Select COM output scan direction
select								1				0:normal direction 1:reverse direction
(16)Power control set	0	1	0	0	0	1	0	1	O	pera	ting	Select internal power supply operating mode
										moc	le	
(17)V5 voltage internal	0	1	0	0	0	1	0	0	R	lesis	ster	Select internal resister ratio (Rb/Ra)mode
resister ratio set										rati	0	
(18)Electronic volume	0	1	0	1	0	0	0	0	0	0	1	
mode set												
Electronic volume	0	1	0	*	*	Ele	ctro	nic v	olu	me	value	Set the v5 output voltage electronic volume
register set												register
(19)Static indicator	0	1	0	1	0	1	0	1	1	0	0	0:OFF , 1:ON
ON/OFF											1	
Static indicator	1	0	1	*	*	*	*	*	*	m	ode	Set the flashing mode
register set												
(20)Power saver												Display OFF and display all points ON
												compound command
(21) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(22)Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

(Note)*:disable data

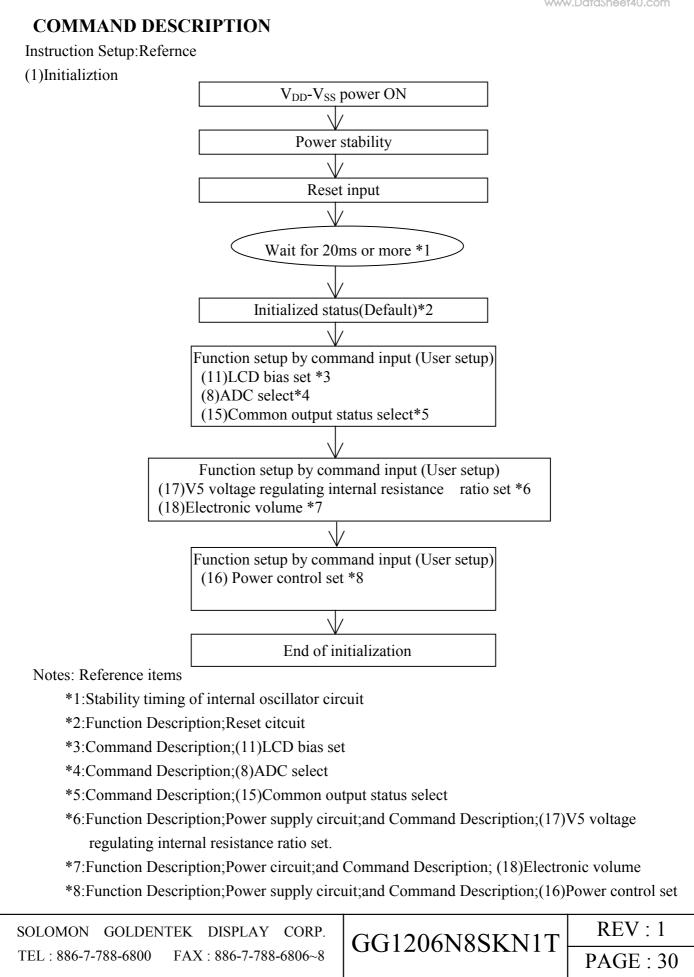
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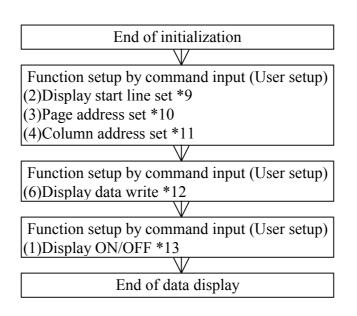


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(2)Data Display

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Notes:Reference items

*9:Command Description;(2)Display start line set

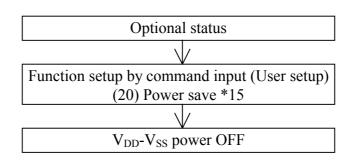
*10:Command Description;(3)Page address set

*11:Command Description;(4)Column address set

*12:Command Description;(6)Display data write

*13:Command Description;(1)Display ON/OFF

(3) Power OFF *14



Notes:Reference items

*14 After turning OFF the internal power supply, turn OFF the power supply of this IC.(Function Description - Power Supply Circuit)

When the power of this IC is turned OFF with the internal power suuply is held in the ON status, since the status where the voltage is supplies, even though an only little, to the internal LCD drive circuit is still continued, it is feared to ill affect the display quality of the LCD panel. To avoid this, be sure to observe the power OFF sequence strictly.

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*15 Command Description;(20)Power save

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