FT6116

2K X 8 CMOS SRAM

FORCE TECHNOLOGIES LTD

Features

- **High-speed access and chip select times**
  - *Military: 120/150ns (max.)*
- **Low-power consumption**
- **Battery backup operation**
  - *2V data retention voltage (Low power version only)*
- **Produced with advanced CMOS high-performance technology**
- **CMOS process virtually eliminates alpha particle soft-error rates**
- **Input and output directly TTL-compatible**
- **Static operation: no clocks or refresh required**
- **Available in ceramic and plastic 24-pin DIP, 24-pin Thin Dip,**

Description

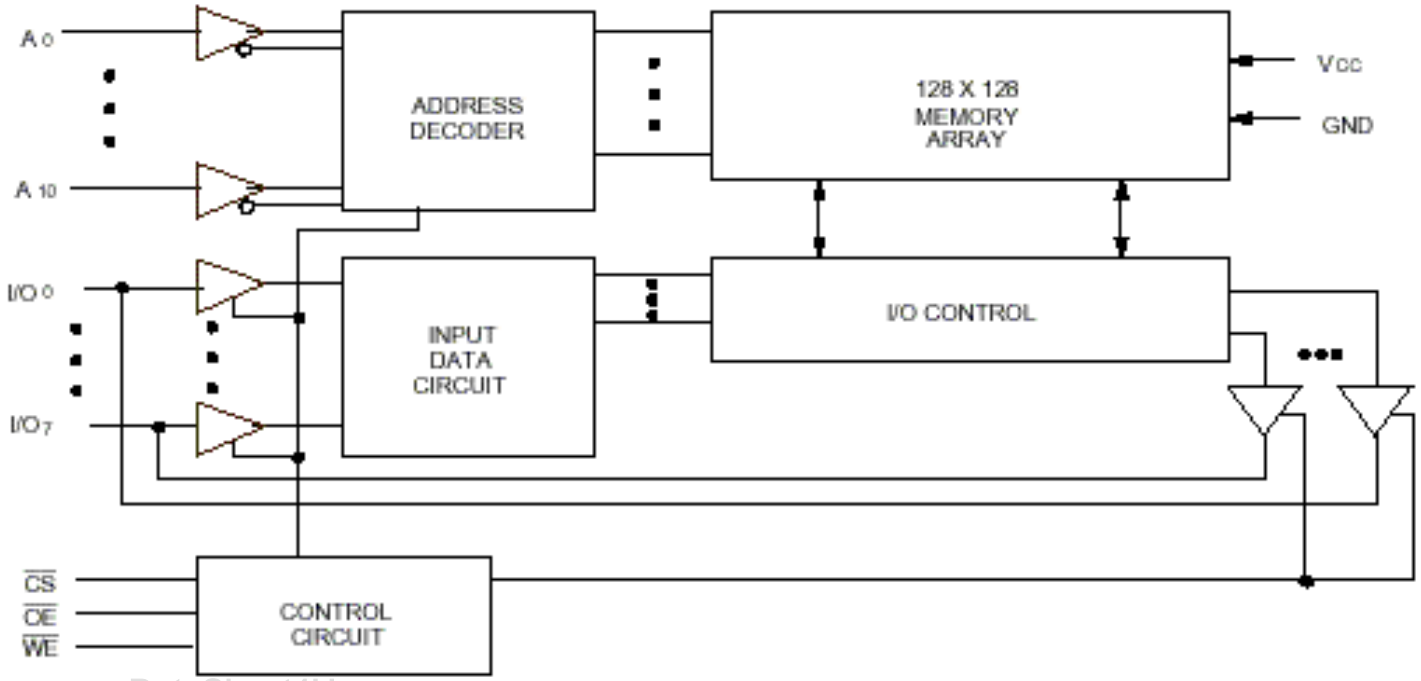
The FT6116 is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using FT's high-performance, high-reliability CMOS technology.

Access times as fast as 15ns are available. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to, and remain in, a standby power mode, as long as $\overline{CS}$ remains HIGH. This capability provides significant system level power and cooling savings. The low-power version also offers a battery backup data retention capability where the circuit typically consumes only 1µW to 4µW operating off a 2V battery.

All inputs and outputs of the FT6116 are TTL-compatible. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The FT6116 is packaged in 24-pin 600 and 300 mil plastic or ceramic DIP

Functional Block Diagram



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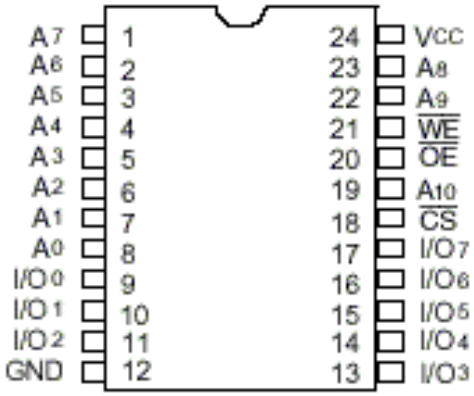
Pin Configurations



DIP
Top View

Pin Description

Name	Description
A_0 - A_{10}	Address Inputs
I/O_0 - I/O_7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground

Truth Table[1]

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O
Standby	H	X	X	High-Z
Read	L	L	H	$DATA_{OUT}$
Read	L	H	H	High-Z
Write	L	X	L	$DATA_{IN}$

NOTE:
1. H = V_{IH}, L = V_{IL}, X = Don't Care.

Capacitance (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

Absolute Maximum Ratings[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} +0.5V.

Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Industrial	-45°C to +85°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5[2]	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	V_{CC} +0.5	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTES:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns, once per cycle.
2. V_{IN} must not exceed V_{CC} +0.5V.

DC Electrical Characteristics
(Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Conditions				FT6116 Min.	FT6116 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.			— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.			— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.				—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.				4	—	V

DC Electrical Characteristics[1] (continued)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power						FT6116 120 Mil Only	FT6116 150 Mil Only	Unit
I_{CC1}	Operating Power Supply Current, $\overline{CS} \leq V_{IL}$, Outputs Open V_{CC} = Max., f = 0							90	90	mA
I_{CC2}	Dynamic Operating Current, $\overline{CS} \leq V_{IL}$, Outputs Open V_{CC} = Max., f = f_{MAX}[2]							100	90	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open V_{CC} = Max., f = f_{MAX}[2]							25	25	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level), $\overline{CS} \geq V_{HC}$, V_{CC} = Max., $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$, f = 0							10	10	mA

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC}, only address inputs are toggling at f_{MAX}, f = 0 means address inputs are not changing.

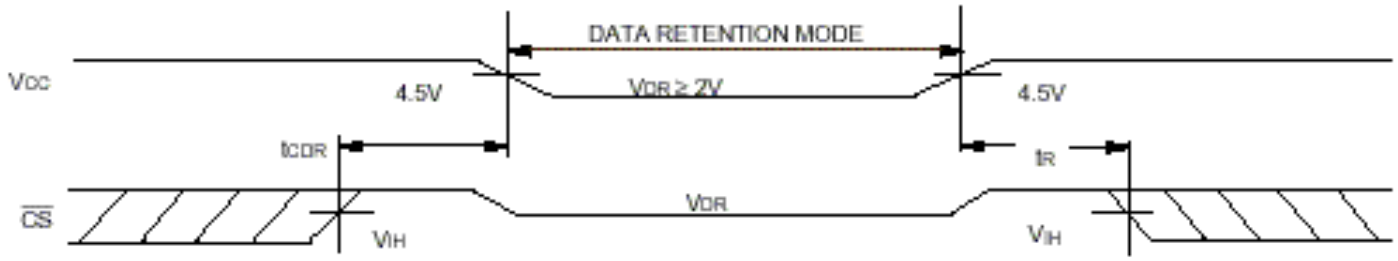
Data Retention Characteristics Over All Temperature Ranges

(LA Version Only) (V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	Test Condition		Min.	Typ.[1] V_{CC} @ 2.0V	Typ.[1] V_{CC} @ 3.0V	Max. V_{CC} @ 2.0V	Max. V_{CC} @ 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current		MIL.	—	0.5	1.5	200	300	µA
			COM'L.	—	0.5	1.5	20	30	
t_{CDR}[3]	Chip Deselect to Data Retention Time	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		—	0	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns
$\|I_{LI}\|$	Input Leakage Current			—	—	—	2	2	µA

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

Low Vcc Data Retention Waveform



AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

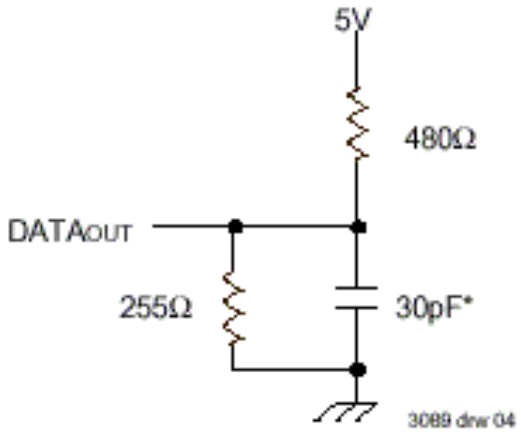


Figure 1. AC Test Load

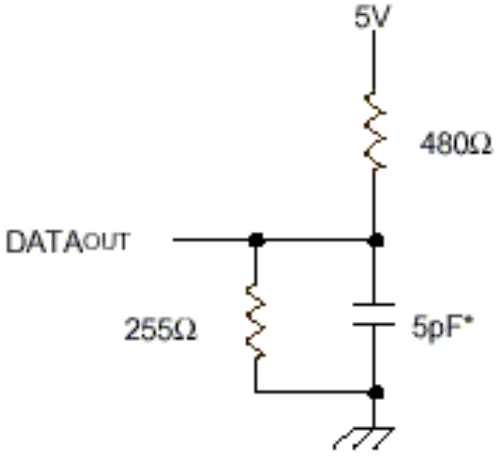


Figure 2. AC Test Load
(for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{BHZ}, t_{CHZ} & t_{OW})

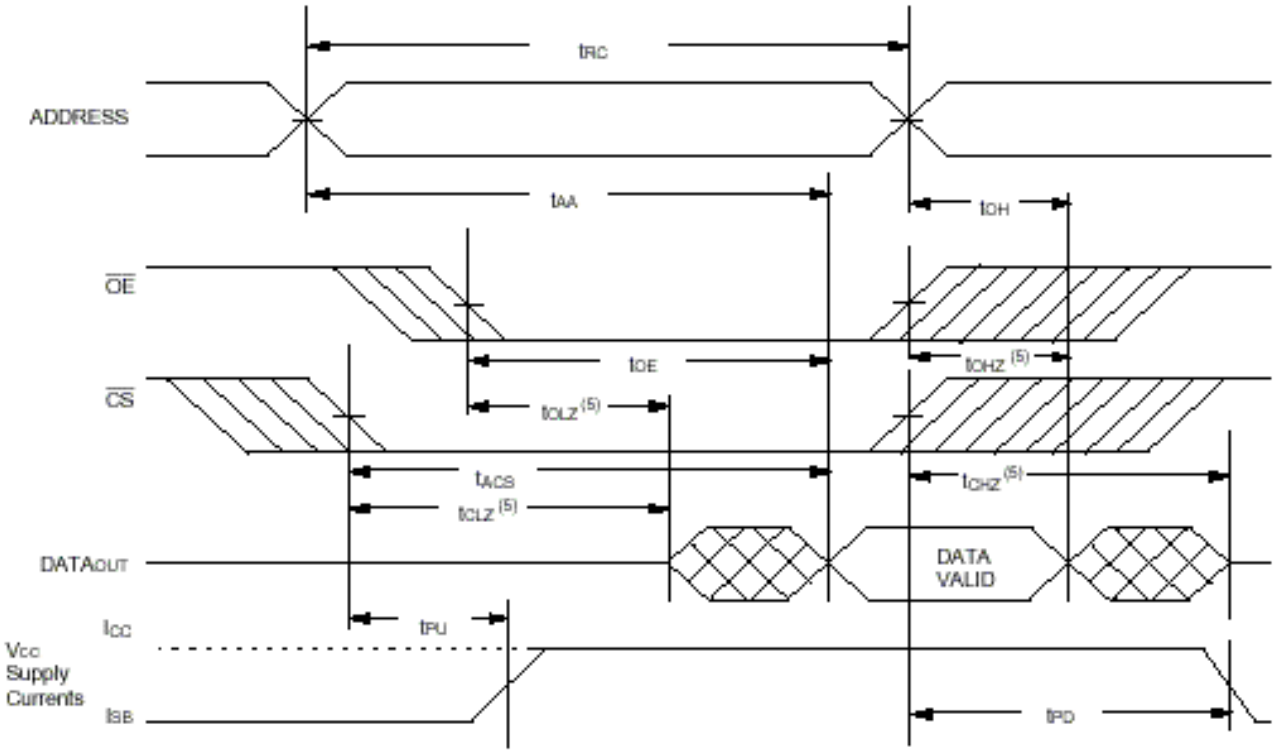
*Including scope and jig.

AC Electrical Characteristics (Vcc = 5V ± 10%, All Temperature Ranges) (continued)

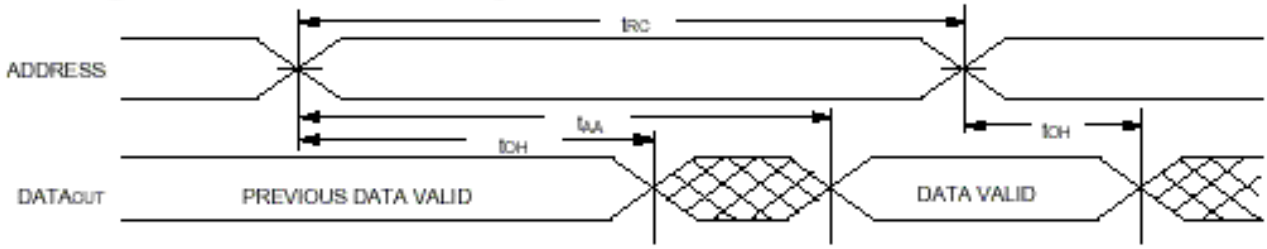
Symbol	Parameter									FT6116 120[2]		FT6116 150[2]		Unit
										Min.	Max.	Min.	Max.	
Read Cycle														
t_{RC}	Read Cycle Time									120	—	150	—	ns
t_{AA}	Address Access Time									—	120	—	150	ns
t_{ACS}	Chip Select Access Time									—	120	—	150	ns
t_{CLZ}[3]	Chip Select to Output in Low-Z									5	—	5	—	ns
t_{OE}	Output Enable to Output Valid									—	80	—	100	ns
t_{OLZ}[3]	Output Enable to Output in Low-Z									5	—	5	—	ns
t_{CHZ}[3]	Chip Deselect to Output in High-Z									—	40	—	40	ns
t_{OHZ}[3]	Output Disable to Output in High-Z									—	40	—	40	ns
t_{OH}	Output Hold from Address Change									5	—	5	—	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

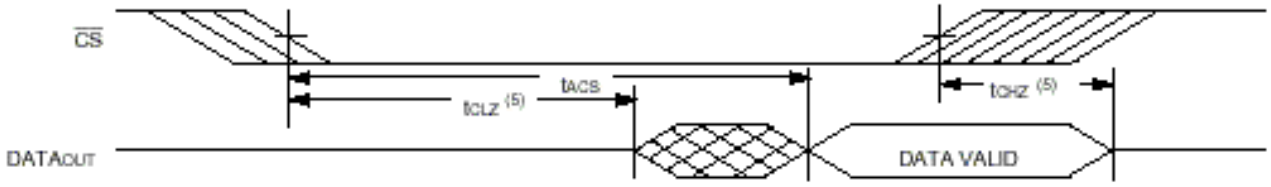
Timing Waveform of Read Cycle No. 1[1,3]



Timing Waveform of Read Cycle No. 2[1,2,4]



Timing Waveform of Read Cycle No. 3[1,3,4]



NOTES:
1. $\overline{WE}$ is HIGH for Read cycle.
2. Device is continously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±500mV from steady state.

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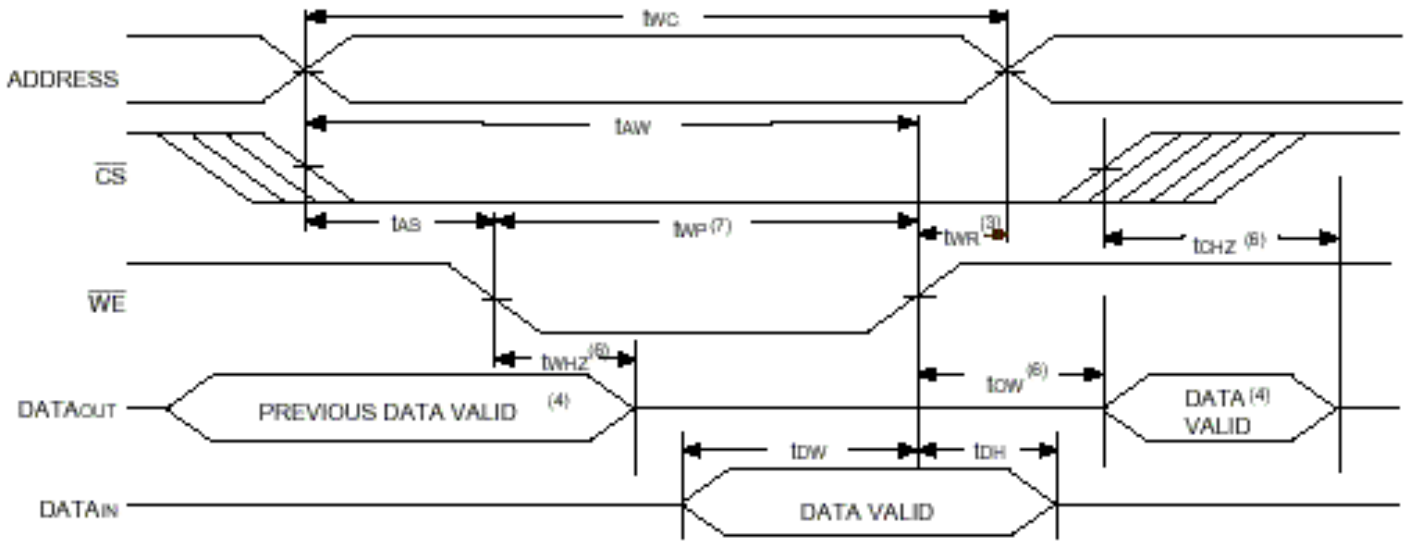
AC Electrical Characteristics (Vcc = 5V ± 10%, All Temperature Ranges)

Symbol	Parameter									FT6116 120[2]		FT6116 150[2]		Unit
										Min.	Max.	Min.	Max.	
Write Cycle														
t_{WC}	Write Cycle Time									120	—	150	—	ns
t_{CW}	Chip Select to End-of-Write									70	—	90	—	ns
t_{AW}	Address Valid to End-of-Write									105	—	120	—	ns
t_{AS}	Address Setup Time									20	—	20	—	ns
t_{WP}	Write Pulse Width									70	—	90	—	ns
t_{WR}	Write Recovery Time									5	—	10	—	ns
t_{WHZ}[3]	Write to Output in High-Z									—	40	—	40	ns
t_{DW}	Data to Write Time Overlap									35	—	40	—	ns
t_{DH}[3]	Data Hold from Write Time									5	—	10	—	ns
t_{OW}[3,4]	Output Active from End-of-Write									0	—	0	—	ns

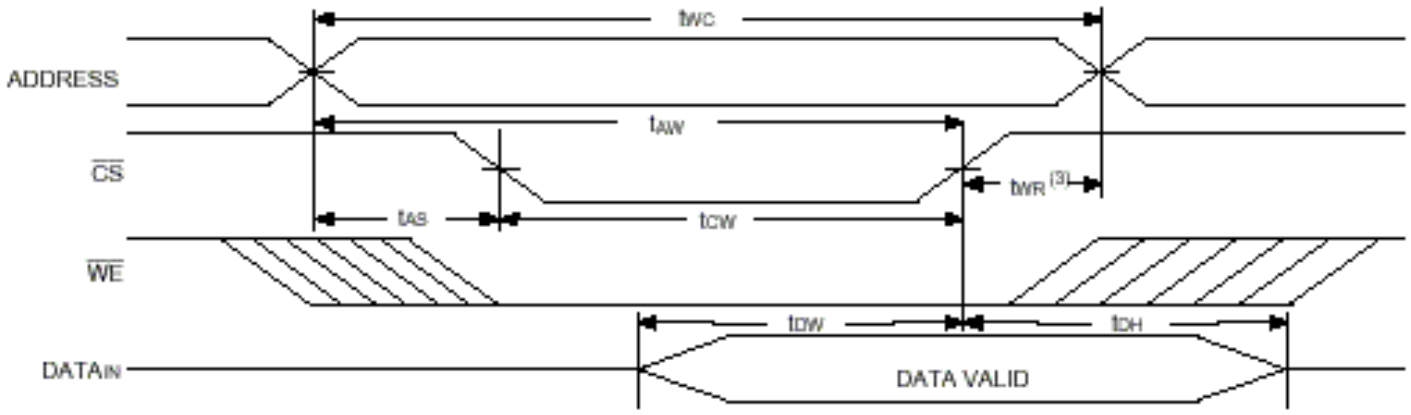
NOTES:

1. 0°C to +70°C temperature range only.
2. −55°C to +125°C temperature range only.
3. This parameter guaranteed with AC Load (Figure 2) by device characterization, but is not production tested.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operation conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)(1,2,5,7)



Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)(1,2,3,5,7)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and the input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in the high-impedance state.
6. Transition is measured ±500mV from steady state.
7. $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse is the specified t_{WP}. For a $\overline{CS}$ controlled write cycle, $\overline{OE}$ may be LOW with no degradation to t_{CW}.

FT6116

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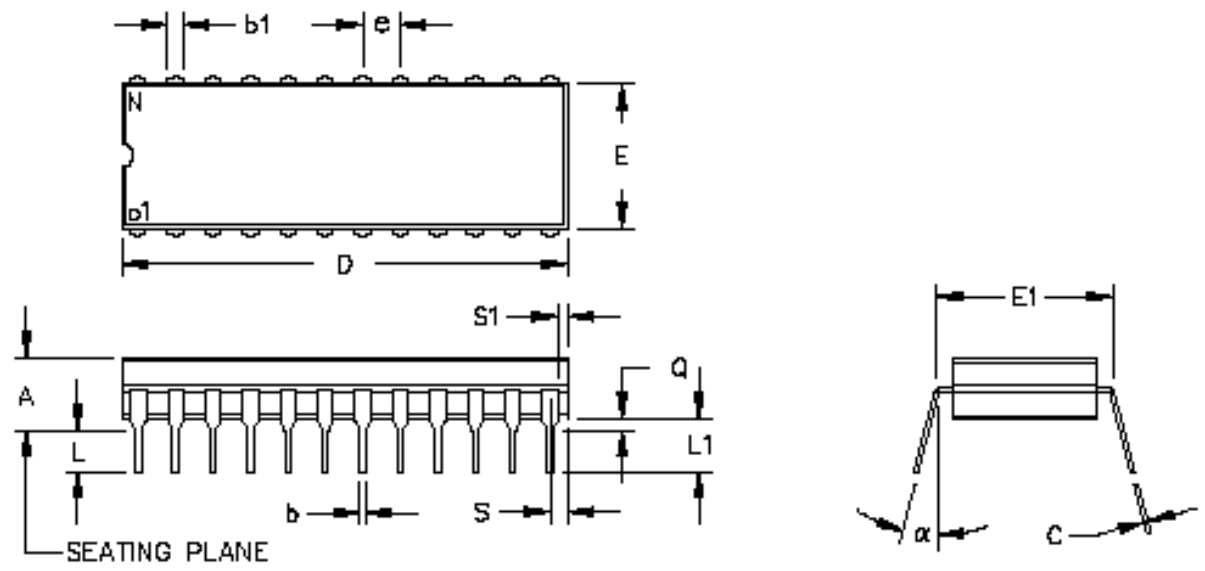
REV	DCN	DESCRIPTION	DATE	APPROVED
06	17517	UPDATED TO STANDARDIZE DWG		



NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "N" REPRESENTS THE NUMBER OF LEADS.

DWG #	D24-1	
SYMBOL	MIN	MAX
A	.140	.200
b	.015	.021
b1	.045	.065
C	.009	.014
D	1.240	1.280
E	.285	.310
E1	.300	.320
e	.100 BSC	
L	.125	.175
L1	.150	–
Q	.015	.060
S	.030	.080
S1	.005	–
α	0°	15°
N	24	

	CONFIGURATION	EXCEPTIONS
MIL-M-38510	D-9	NONE
JEDEC	MO-058-AA	NONE

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRAC ± – DEC ± – ANGLES ± –

APPROVALS	DATE
DRAWN	
CHECKED	

24 LD CERDIP MKT DWG
(300 MIL)

SCALE	SIZE	DRAWING NO.	REV
N/A	A		06

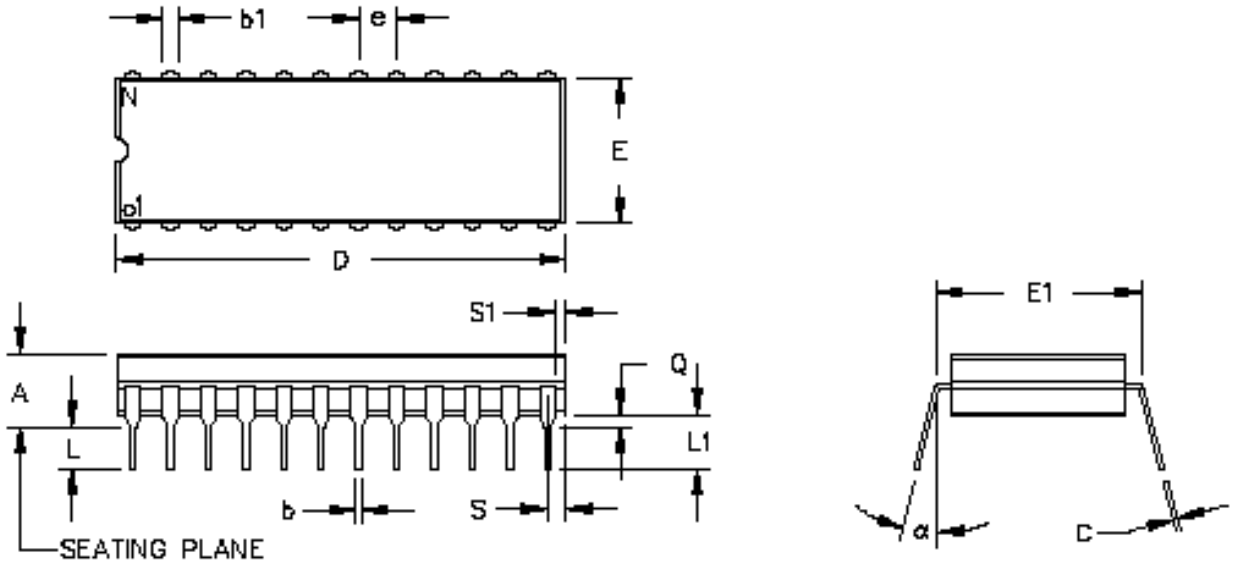
DO NOT SCALE DRAWING — SHEET 2 OF 2

FT6116

2K X 8 CMOS SRAM

FORCE TECHNOLOGIES LTD

REV	DCN	DESCRIPTION	DATE	APPROVED
06	17514	UPDATED TO STANDARDIZE DWG		
07	22234	CHANGED b1 MIN DIM		



NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "N" REPRESENTS THE NUMBER OF LEADS.

DWG #	D24-2	
SYMBOL	MIN	MAX
A	.090	.190
b	.014	.023
b1	.045	.060
C	.008	.012
D	1.230	1.290
E	.500	.610
E1	.590	.620
e	.100 BSC	
L	.125	.200
L1	.150	–
Q	.015	.060
S	.030	.080
S1	.005	–
α	0°	15°
N	24	

CONFIGURATION	EXCEPTIONS
MIL-M-38510	D-3	NONE
JEDEC	NOT REGISTERED	

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRAC ± – DEC ± – ANGLES ± –

APPROVALS	DATE
DRAWN	
CHECKED	

24 LD CERDIP MKT DWG
(600 MIL)

SCALE	SIZE	DRAWING NO.	REV
N/A	A		07

DO NOT SCALE DRAWING | SHEET 2 OF 2