REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 03 and 04. Convert to standard military drawing format and change drawing CAGE code. Add figure 4, test circuit and switching waveforms. Inactivate device types 01 and 02 for new design. Editorial changes throughout.	88-12-20	M. A. Frye
B	Update to reflect latest changes in format and requirements. Editorial changes throughout. --les	05-02-08	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE 67268

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS			REV	B	B	B	B	B	B	B	B	B	B	B	B	B				
OF SHEETS			SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13				

PMIC N/A

PREPARED BY

Greg A. Pitz

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY

Ray Monnin

APPROVED BY

Michael A. Frye

DRAWING APPROVAL DATE

85-05-08

REVISION LEVEL

B

MICROCIRCUITS, DIGITAL, TTL, OCTAL D-TYPE TRANSPARENT LATCH,

MONOLITHIC SILICON

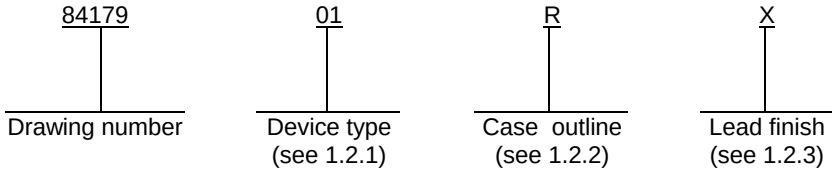
SIZE	CAGE CODE	
A	**14933**	**84179**

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01, 03	8282	Octal, D-type, transparent latch with 3-state outputs
02, 04	8283	Octal, D-type, transparent latch with inverted 3-state outputs

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	dual-in-line
3	CQCC1-N28	28	leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-1.0 V dc at -18 mA to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	1 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage :	
Device types 01 and 02	4.5 V dc minimum to 5.5 V dc maximum
Device types 03 and 04	4.75 V dc minimum to 5.25 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Input to STB setup time $t_{(setup)}$	0 ns minimum
Input to STB hold time $t_{(hold)}$	25 ns minimum
input pulse width (t_P) (Strobe)	15 ns minimum

1/ Maximum power dissipation is defined as V_{CC} x I_{CC}, and must withstand the added P_D due to short-circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.2.5 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = minimum, I_{OH} = -5 mA	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	V_{CC} = minimum, I_{OL} = 20 mA	1, 2, 3	All		0.45	V
Input clamp voltage	V_{IC}	V_{CC} = minimum, I_{IN} = -5 mA, T_C = +25°C	1	All		-1	V
High level input voltage	V_{IH}	V_{CC} = 5 V, I_{OH} = -5 mA, C_L = 300 pF	1, 2, 3	All	2.0		V
Low level input voltage	V_{IL}	V_{CC} = 5 V, I_{OL} = 20 mA, C_L = 300 pF	1, 2, 3	All		0.8	V
High level input current	I_{IH}	V_{CC} = maximum, V_{IH} = 5.25 V	1, 2, 3	All		50	µA
Low level input current	I_{IL}	V_{CC} = maximum, V_{IL} = 0.45 V	1, 2, 3	All		-200	µA
Supply current	I_{CC}	V_{CC} = maximum	1, 2, 3	All		160	mA
Output current, high level, outputs OFF	I_{OZH}	V_{CC} = maximum, V_{OH} = 2.7 V	1, 2, 3	All		50	µA
Output current, low level, outputs OFF 2/	I_{OZL}	V_{CC} = maximum, V_{OH} = 0.45 V	1, 2, 3	All		-50	µA
Functional tests		See 4.3.1c	7	All			

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Transition time, low to high (from 0.8 V to 2.0 V) 2/	t_{TLH}	C_L = 300 pF ±10%, R_L = 78Ω, See figure 4	9, 10, 11	All		20	ns
Transition time, high to low (from 2.0 V to 0.8 V) 2/	t_{THL}		9, 10, 11	All		12	ns
Propagation delay time to high level (STB to output) 3/ 4/	t_{PLH1}	V_{CC} = 5.0 V, C_L = 300 pF ±10%, R_L = 78Ω, See figure 4	9, 10, 11	01, 03		55	ns
				02, 04		45	
Propagation delay time to low level (STB to output) 3/ 4/	t_{PHL1}		9, 10, 11	01, 03		55	ns
				02, 04		45	
Propagation delay time to high level (data to output) 4/	t_{PLH2}		9, 10, 11	01, 03		35	ns
				02, 04		25	
Propagation delay time to low level (data to output) 4/	t_{PHL2}		9, 10, 11	01, 03		35	ns
				02, 04		25	
Output control ON to high level output	t_{PZH}	C_L = 300 pF ±10%, R_L = 78Ω, See figure 4	9, 10, 11	All	10 2/	50	ns
Output control ON to low level output	t_{PZL}		9, 10, 11	All	10 2/	50	ns
High level output to output control OFF	t_{PHZ}		9, 10, 11	All		25	ns
Low level output to output control OFF	t_{PLZ}		9, 10, 11	All		25	ns

1/ V_{CC} = 4.5 V minimum to 5.5 V maximum for device types 01 and 02, unless otherwise specified.
V_{CC} = 4.75 V minimum to 5.25 V maximum for device types 03 and 04, unless otherwise specified.
2/ Tested only initially and after any design change.
3/ For device types 02 and 04 only, output may be momentarily invalid following the high going STB transition.
4/ Device types 02 and 04 limits shown are guaranteed by design but tested to the applicable device types 01 and 03 limits.

Device type	01 and 03		02 and 04	
Case outlines	R	3	R	3
Terminal number	Terminal symbol		Terminal symbol	
1	1D	NC	1D	NC
2	2D	1D	2D	1D
3	3D	2D	3D	2D
4	4D	3D	4D	3D
5	5D	NC	5D	NC
6	6D	4D	6D	4D
7	7D	5D	7D	5D
8	8D	NC	8D	NC
9	$\overline{OE}$	6D	$\overline{OE}$	6D
10	GND	7D	GND	7D
11	STB	NC	STB	NC
12	8Q	8D	$\overline{8Q}$	8D
13	7Q	$\overline{OE}$	$\overline{7Q}$	$\overline{OE}$
14	6Q	GND	$\overline{6Q}$	GND
15	5Q	NC	$\overline{5Q}$	NC
16	4Q	STB	$\overline{4Q}$	STB
17	3Q	8Q	$\overline{3Q}$	$\overline{8Q}$
18	2Q	7Q	$\overline{2Q}$	$\overline{7Q}$
19	1Q	NC	$\overline{1Q}$	NC
20	V_{CC}	6Q	V_{CC}	$\overline{6Q}$
21	- - -	5Q	- - -	$\overline{5Q}$
22	- - -	NC	- - -	NC
23	- - -	4Q	- - -	$\overline{4Q}$
24	- - -	3Q	- - -	$\overline{3Q}$
25	- - -	NC	- - -	NC
26	- - -	2Q	- - -	$\overline{2Q}$
27	- - -	1Q	- - -	$\overline{1Q}$
28	- - -	V_{CC}	- - -	V_{CC}

FIGURE 1. Terminal connections.

Device types 01 and 03

OUTPUT ENABLE	STROBE	DATA	OUTPUT
$\overline{OE}$	STB	D	Q
H	X	X	Z
L	L	X	Q_0
L	H	L	L
L	H	H	H

Device types 02 and 04

OUTPUT ENABLE	STROBE	DATA	OUTPUT
$\overline{OE}$	STB	D	$\overline{Q}$
H	X	X	Z
L	L	X	$\overline{Q}_0$
L	H	L	L
L	H	H	H

H = High level (steady state)
L = Low level (steady state)
Z = High impedance state
X = Irrelevant
Q_0 = The level of Q or $\overline{Q}$ before the indicated input conditions were established

FIGURE 2. Truth tables.

DEVICE TYPES 01 AND 03

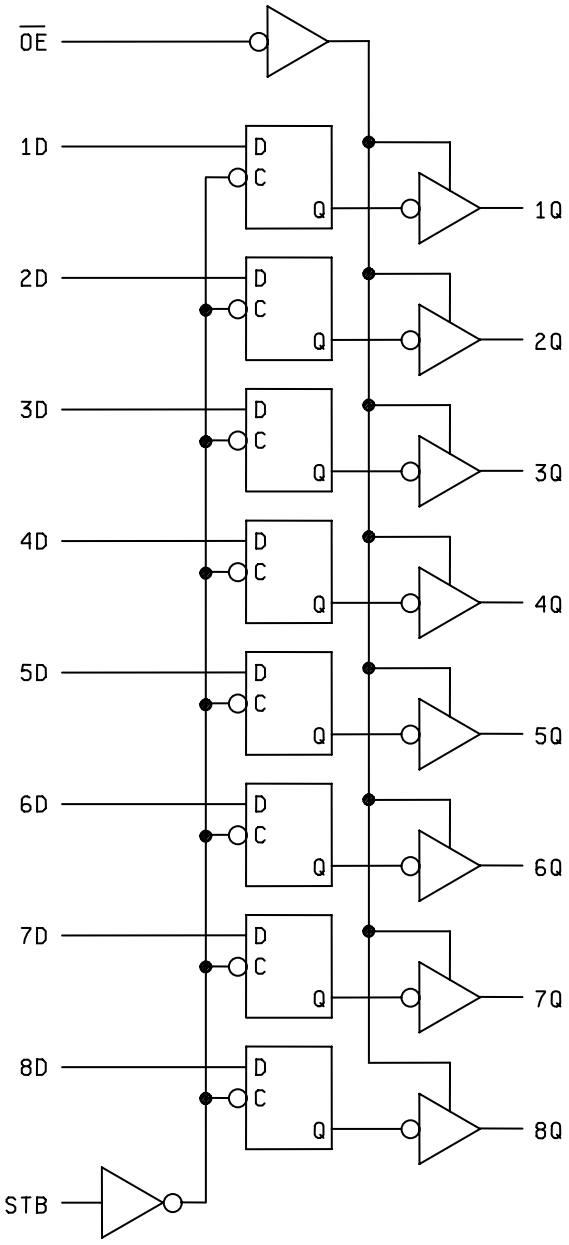


FIGURE 3. Logic diagram.

DEVICE TYPES 02 AND 04

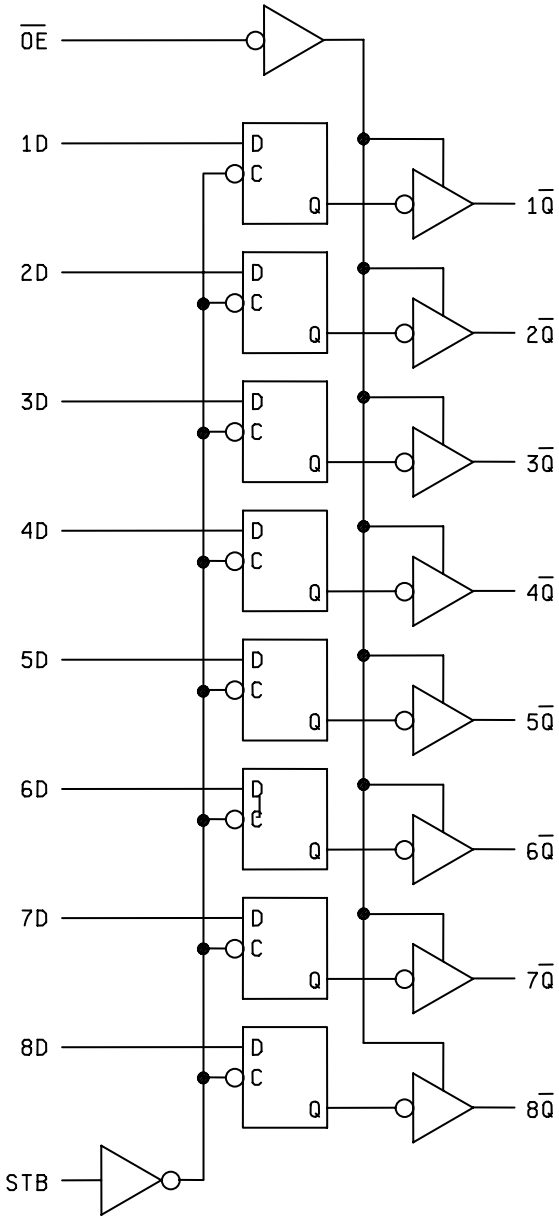
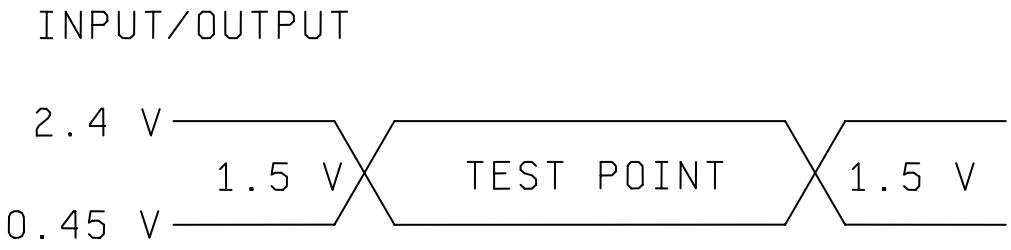


FIGURE 3. Logic diagram - Continued.



AC testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 1.5 V for both a logic "1" and "0". Input rise and fall times are measured from 0.8 V to 2.0 V and are driven at 5 ns ±2 ns.

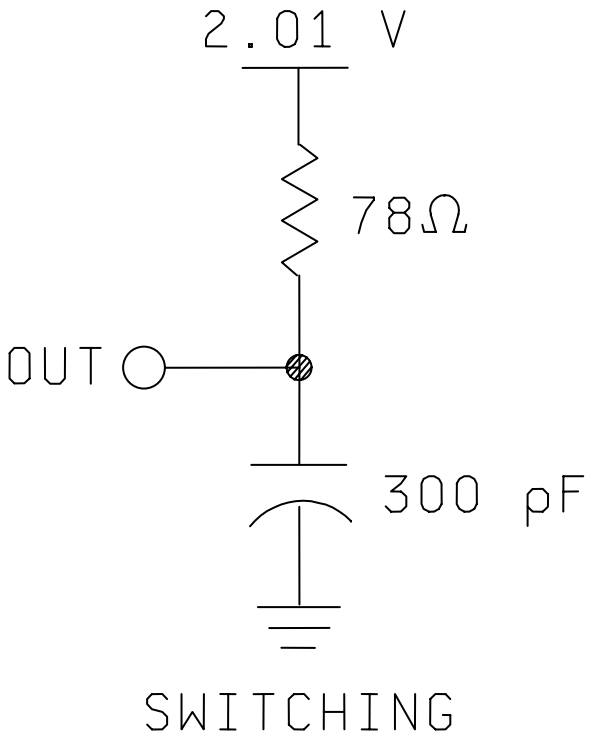


FIGURE 4. Test circuit and switching waveforms.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8A, 10

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-02-08

Approved sources of supply for SMD 84179 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
8417901RA	3/	MD8282
84179013A	3/	MR8282
8417902RA	3/ 58625	MD8283 IL8283/BRA
84179023A	3/ 58625	MR8283 IL8283/B3A
84179023C	58625	IL8283/B3C
8417903RA	3/ 58625	MD8282/B IL8282/BRA
84179033A	3/ 58625	MR8282/B IL8282/B3A
84179033C	58625	IL8282/B3C
8417904RA	3/ 58625	MD8283/B IL8283/BRA
84179043A	3/	MR8283/B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
58625	Lansdale Semiconductor Inc. 2929 South 48th St. Tempe, AZ 85282