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DATA SHEET

by

SYNTEK®

=========STK6006=========

8051 Embedded LCD Monitor Micro-Controller

Version 1.0

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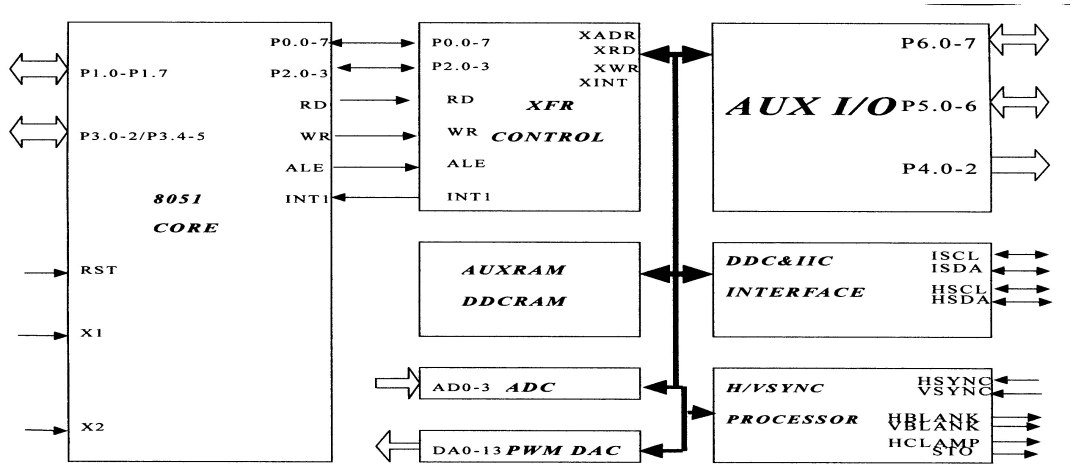
1. GENERAL DESCRIPTION

The STK6006, an LCD monitor controller, is an embedded device with 8051 CPU core, which is in particularly designed for application to an LCD Monitor. It consists of an 8051 CPU core, a 1024-byte SRAM, 14 built PWM DACs, a VESA DDC interface, a 4-channel A/D converter, and a 64k-byte internal program Flash ROM. STK6006 works with both 5V/3.3V power supply and I/O, and 3.3V core operating voltage.

2. FEATURES

- **14 channels of PWM DAC (max.)**
- **31 I/O pins (max.)**
- **8051 core, available for operating frequency at 12MHz with double CPU clock F/W optional**
- **1024 bytes of RAM; 64K bytes of program Flash ROM support In-System Programming function (ISP)**
- **5V/3.3V power supply and I/O; 3.3V core operating voltage**
- **Built-in self-test pattern generator with programmable free-running timing (15 –150KHz)**
- **Built-in lower power reset circuit**
- **SYNC processor for composite separation/insertion, H/V polarity/frequency check, and polarity adjustment**
- **Single master I^2C interface for internal device to communicate**
- **Two slave I^2C addresses; H/W auto-transfer DDC1/DDC2x data**
- **Feature corresponding to VESA DDC1/2B/2Bi/2B+**
- **4 channels of 6-bit ADC (max.)**
- **A selection to protection from the Flash ROM program code**
- **Watchdog timer featuring programmable interval**
- **Package designed with 40-pin DIP, 42-pin SDIP, or 44-pin PLCC**

3. BLOCK DIAGRAM



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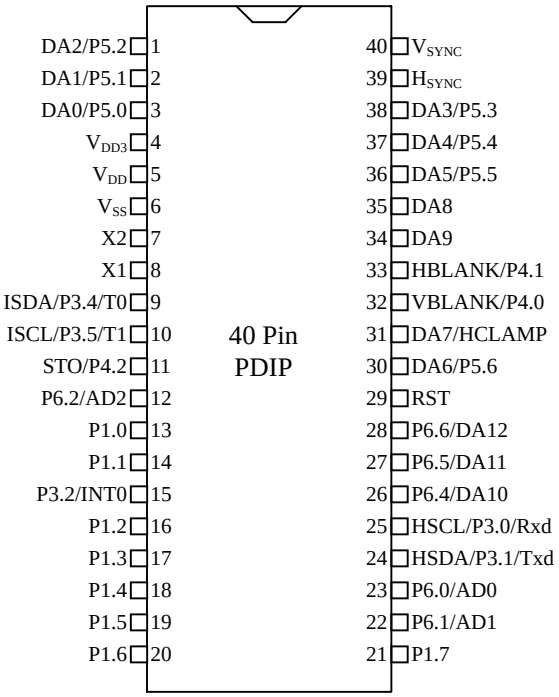
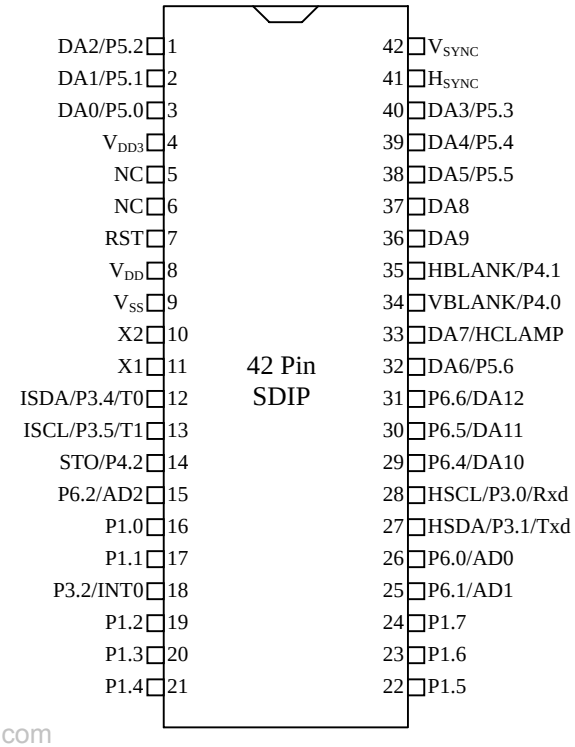
4. PIN CONNECTION





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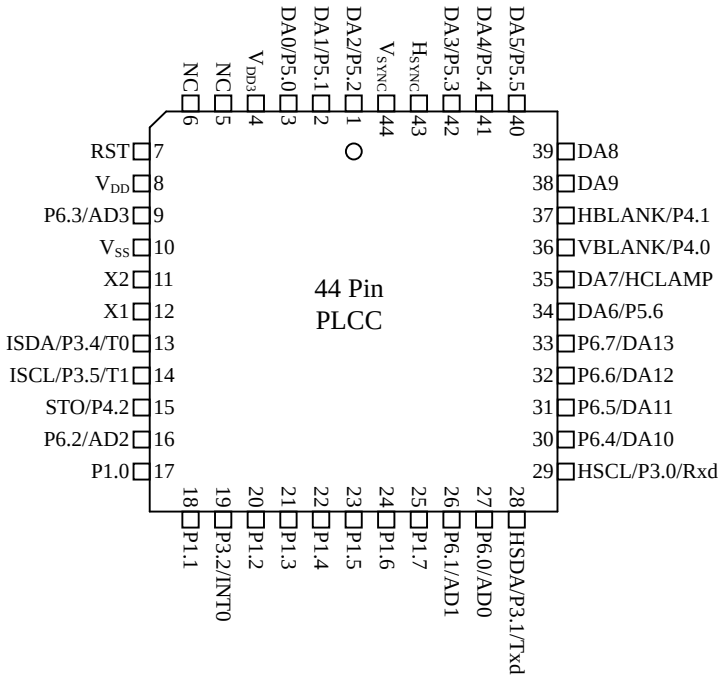

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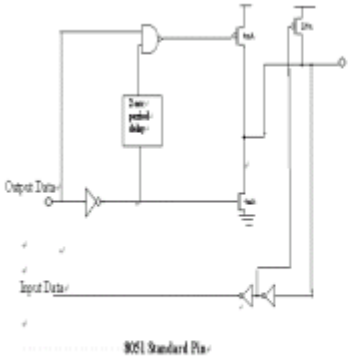
5. PINS CONFIGURATION

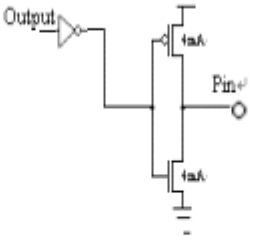
"Open drain pin" means the pin may sink at least 4mA current but drive only 10~20uA to V_{DD}. It may be used as input or output function and needs an external pull-up resistor.

"CMOS output" means the pin may sink at least 4mA and drive. It is not preferred to use such pin as input function.

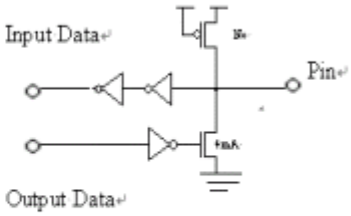
"8051 standard pin" is a pseudo-open drain pin. It may sink at least 4mA current when output stays at a low level, and drives at least 4mA current for 2 X'tal period when output changes from a low level to a high level, and then drives at 120μA for a high level. It can be used as input or output function and needs an external pull-up resistor when driving a device with heavy load.



8051 Standard Pin



CMOS Output Pin



Open Drain Pin

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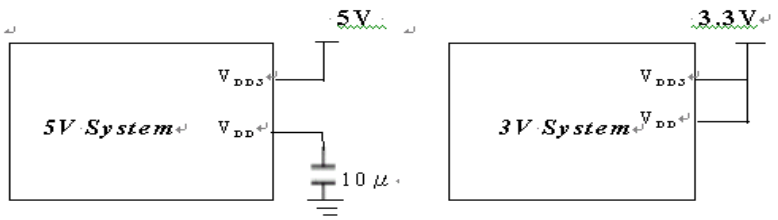
6. POWER CONFIGURATION

The STK6006 works in a system with a 5V or 3.3V power supply. In a 5V-power system, the V_{DD} pin is connected to a 5V power supply and the V_{DD3} is connected to external capacitor; all output pins changes from 0 to 5V, and input pins can accept a voltage ranging from 0 to 5V. The voltage range of ADC conversion is 5V. However, the X1 and X2 pins operating below 3.3V.

In a 3.3V power system, V_{DD} and V_{DD3} are connected to 3.3V power, all output pins change from 0 to 3.3V, H_{SYNC}, V_{SYNC} and open drain pin may allow input ranging from 0 to 5V, and other input pins only allow input ranging from 0 to 3.3V. The voltage range of ADC conversion is 3.3V.



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7. PINS DESCRIPTION

Name	Pin No.			I/O Type	Description
	40 pins	42 pins	44 pins		
DA0/P5.0	3	3	3	I/O	PWM DAC output / General purpose I/O (CMOS)
DA1/P5.1	2	2	2	I/O	PWM DAC output / General purpose I/O (CMOS)
DA2/P5.2	1	1	1	I/O	PWM DAC output / General purpose I/O (CMOS)
DA3/P5.3	38	40	42	I/O	PWM DAC output / General purpose I/O (CMOS)
DA4/P5.4	37	39	41	I/O	PWM DAC output / General purpose I/O (CMOS)
DA5/P5.5	36	38	40	I/O	PWM DAC output / General purpose I/O (CMOS)
DA6/P5.6	30	32	34	I/O	PWM DAC output / General purpose I/O (CMOS)
DA7/HCLAMP	31	33	35	O	PWM DAC output / Hsync clamp pulse output (CMOS)
DA8	35	37	39	O	PWM DAC output (open drain)
DA9	34	36	38	O	PWM DAC output (open drain)
P1.0	13	16	17	I/O	General purpose I/O (CMOS output or 8051 standard)
P1.1	14	17	18	I/O	General purpose I/O (CMOS output or 8051 standard)
P1.2	16	19	20	I/O	General purpose I/O (CMOS output or 8051 standard)
P1.3	17	20	21	I/O	General purpose I/O (CMOS output or 8051 standard)
P1.4	18	21	22	I/O	General purpose I/O (CMOS output or 8051 standard)
P1.5	19	22	23	I/O	General purpose I/O (CMOS output or 8051 standard)
P1.6	20	23	24	I/O	General purpose I/O (CMOS output or 8051 standard)
P1.7	21	24	25	I/O	General purpose I/O (CMOS output or 8051 standard)
P6.0/AD0	23	26	27	I/O	General purpose I/O / ADC Input (CMOS)
P6.1/AD1	22	25	26	I/O	General purpose I/O / ADC Input (CMOS)
P6.2/AD2	12	15	16	I/O	General purpose I/O / ADC Input (CMOS)
P6.3/AD3	-	-	9	I/O	General purpose I/O / ADC Input (CMOS)
P6.4/DA10	26	29	30	I/O	General purpose I/O / PWM DAC output (CMOS)
P6.5/DA11	27	30	31	I/O	General purpose I/O / PWM DAC output (CMOS)
P6.6/DA12	28	31	32	I/O	General purpose I/O / PWM DAC output (CMOS)
P6.7/DA13	-	-	33	I/O	General purpose I/O / PWM DAC output (CMOS)
V_{DD3}	4	4	4	O	3.3V core power
V_{DD}	5	8	8	-	5V or 3.3V Positive Power Supply
V_{SS}	6	9	10	-	Ground
VBLANK/P4.0	32	34	36	O	Vertical blank / General purpose Output (CMOS)
HBLANK/P4.1	33	35	37	O	Horizontal blank / General purpose Output (CMOS)
X2	7	10	11	O	Oscillator output
X1	8	11	12	I	Oscillator input
RST	29	7	7	I	Active-high reset
ISDA/P3.4/T0	9	12	13	I/O	Master I^2C data / General purpose I/O / T0 (open drain)
ISCL/P3.5/T1	10	13	14	I/O	Master I^2C clock / General purpose I/O / T1 (open drain)
HSCL/P3.0/Rxd	25	28	29	I/O	Slave I^2C clock / General purpose I/O / Rxd (open drain)
HSDA/P3.1/Txd	24	27	28	I/O	Slave I^2C data / General purpose I/O / Txd (open drain)
P3.2/INT0	15	18	19	I/O	General purpose I/O / INT0 (8051 standard)
H_{SYNC}	39	41	43	I	Horizontal SYNC or Composite SYNC Input
V_{SYNC}	40	42	44	I	Vertical SYNC input
STO/P4.2	11	14	15	O	Self-test video output / General purpose Output (CMOS)

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8. FUNCTIONAL DESCRIPTIONS

8.1 8051 CPU Core

The CPU core of STK6006 is compatible to 8051 industry standard, it consists of 256 bytes of RAM, special function registers (SFR), two timers, five interrupt sources, and a serial interface. The CPU core catches its program code from a 64K-byte Flash in STK6006. In addition, it uses the port0 and port2 to access an external special function register (XFR) and an external auxiliary RAM (AUXRAM).

When CPUclk is set, the CPU core can work at double rate. And then the CPU operates as if a 24-MHz crystal is applied to STK6006, but I^2C, DDC, and the H/V processor still work at the original frequency.

Note: Listed in this data sheet, all registers are collected in the external RAM area of 8051. You may refer to the 8051 specifications for an internal RAM memory map in detail.

8.2 Allocation of Memory

8.2.1 Internal Special Function Registers (SFR)

The SFR are the same as the 8051 standard.

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8.2.2 Internal RAM

The 256 bytes of internal RAM kept in STK6006 are the same as the 8052 standard.

8.2.3 Auxiliary RAM (AUXRAM)

Total 512 bytes of auxiliary RAM is configured in the 8051 external RAM area 800h - 9FFh. Programs can use the "MOVX" instruction to access the AUXRAM.

8.2.4 Dual Port RAM (DDCRAM)

256 bytes of a Dual Port RAM is configured in the 8051 external RAM area E00h - EFFh. Programs can use the "MOVX" instruction to access the RAM. The external DDC1/2 Host can access the RAM as if a 24LC02 EEPROM is connected to the interface.

8.2.5 External Special Function Registers (XFR)

The XFR is a group of registers configured in the 8051 external RAM area F00h - FFFh for the special functions. Programs can use the "MOVX" instruction to access these registers.

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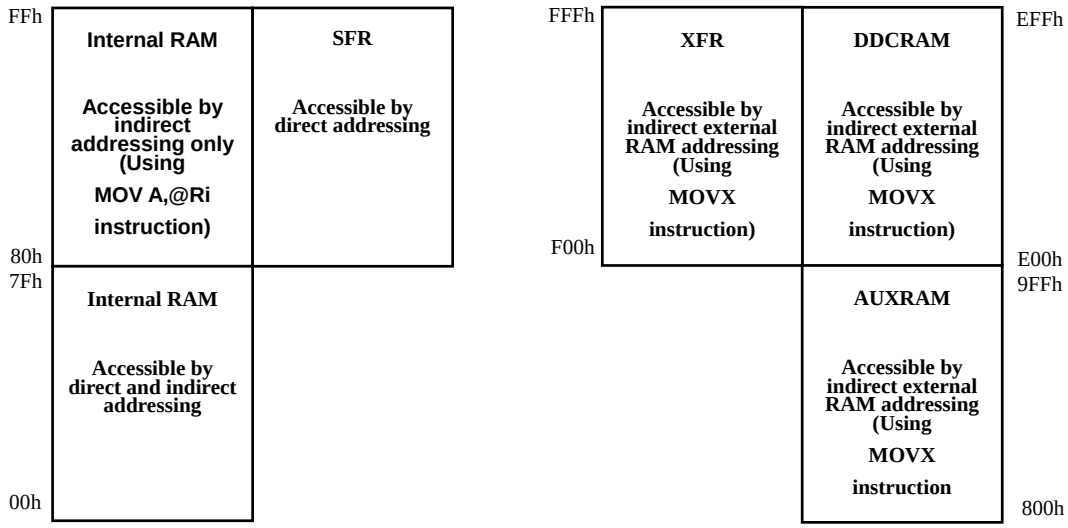

8.3 Chip Configuration

The Chip Configuration registers explain the chip configuration and the pin function.

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Reg. Name	Addr.	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
PADOPT	F50h(w)	DA13E	DA12E	DA11E	DA10E	AD3E	AD2E	AD1E	AD0E
PADOPT	F51h(w)		P56E	P55E	P54E	P53E	P52E	P51E	P50E
PADOPT	F52h(w)	HI2CE	II2CE			HCLPE	P42E	P41E	P40E
PADOPT	F53h(w)		P56oe	P55oe	P54oe	P53oe	P52oe	P51oe	P50oe
PADOPT	F54h(w)	P67oe	P66oe	P65oe	P64oe	P63oe	P62oe	P61oe	P60oe
PADOPT	F55h(w)	P17co	P16co	P15co	P14co	P13co	P12co	P11co	P10co
OPT	F56h(w)	PWMf	PWMd	CPUclk		HSCLlo	MI2CS	MI2CF1	MI2CF0

PADOPT (w): control registers in a pad mode, all standing for "0" in Chip Reset

DA13E = 1 → Pin “P6.7/DA13” for DA13
= 0 → Pin “P6.7/DA13” for P6.7
DA12E = 1 → Pin “P6.6/DA12” for DA12
= 0 → Pin “P6.6/DA12” for P6.6
DA11E = 1 → Pin “P6.5/DA11” for DA11
= 0 → Pin “P6.5/DA11” for P6.5
DA10E = 1 → Pin “P6.4/DA10” for DA10
= 0 → Pin “P6.4/DA10” for P6.4
AD3E = 1 → Pin “P6.3/AD3” for AD3
= 0 → Pin “P6.3/AD3” for P6.3

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AD2E = 1 → Pin "P6.2/AD2" for AD2

= 0 → Pin "P6.2/AD2" for P6.2

AD1E = 1 → Pin "P6.1/AD1" for AD1

= 0 → Pin "P6.1/AD1" for P6.1

AD0E = 1 → Pin "P6.0/AD0" for AD0

= 0 → Pin "P6.0/AD0" for P6.0

P56E = 1 → Pin "DA6/P5.6" for P5.6

= 0 → Pin "DA6/P5.6" for DA6

P55E = 1 → Pin "DA5/P5.5" for P5.5

= 0 → Pin "DA5/P5.5" for DA5

P54E = 1 → Pin "DA4/P5.4" for P5.4

= 0 → Pin "DA4/P5.4" for DA4

P53E = 1 → Pin "DA3/P5.3" for P5.3

= 0 → Pin "DA3/P5.3" for DA3

P52E = 1 → Pin "DA2/P5.2" for P5.2

= 0 → Pin "DA2/P5.2" for DA2

P51E = 1 → Pin "DA1/P5.1" for P5.1

= 0 → Pin "DA1/P5.1" for DA1

P50E = 1 → Pin "DA0/P5.0" for P5.0

= 0 → Pin "DA0/P5.0" for DA0

HI2CE = 1 → Pin "HSCL/P3.0/Rxd" for HSCL; pin "HSDA/P3.1/Txd" for HSDA

= 0 → Pin "HSCL/P3.0/Rxd" for P3.0/Rxd; pin "HSDA/P3.1/Txd" for P3.1/Txd

II2CE = 1 → Pin "FORDA/P3.4/T0" for FORDA; pin "FORCL/P3.5/T1" for FORCL

= 0 → Pin "FORDA/P3.4/T0" for P3.4/T0; pin "FORCL/P3.5/T1" for P3.5/T1

HCLPE = 1 → Pin "DA7/HCLAMP" for H_{SYNC} clamp pulse output

= 0 → Pin "DA7/HCLAMP" for DA7

P42E = 1 → Pin "STO/P4.2" for P4.2

= 0 → Pin "STO/P4.2" for STO

P41E = 1 → Pin "HBLANK/P4.1" for P4.1

= 0 → Pin "HBLANK/P4.1" for HBLANK.

P40E = 1 → Pin "VBLANK/P4.0" for P4.0.

= 0 → Pin "VBLANK/P4.0" for VBLANK.

P56oe = 1 → P5.6 used as output pin.

= 0 → P5.6 used as input pin.

P55oe = 1 → P5.5 used as output pin.

= 0 → P5.5 used as input pin.

P54oe = 1 → P5.4 used as output pin.

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= 0 → P5.4 used as input pin.

P53oe = 1 → P5.3 used as output pin.

= 0 → P5.3 used as input pin.

P52oe = 1 → P5.2 used as output pin.

= 0 → P5.2 used as input pin.

P51oe = 1 → P5.1 used as output pin.

= 0 → P5.1 used as input pin.

P50oe = 1 → P5.0 used as output pin.

= 0 → P5.0 used as input pin.

P67oe = 1 → P6.7 used as output pin.

= 0 → P6.7 used as input pin.

P66oe = 1 → P6.6 used as output pin.

= 0 → P6.6 used as input pin.

P65oe = 1 → P6.5 used as output pin.

= 0 → P6.5 used as input pin.

P64oe = 1 → P6.4 used as output pin.

= 0 → P6.4 used as input pin.

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P63oe = 1 → P6.3 used as output pin.

= 0 → P6.3 used as input pin.

P62oe = 1 → P6.2 used as output pin.

= 0 → P6.2 used as input pin.

P61oe = 1 → P6.1 used as output pin.

= 0 → P6.1 used as input pin.

P60oe = 1 → P6.0 used as output pin.

= 0 → P6.0 used as input pin.

P17co = 1 → Pin “P1.7” used as CMOS Output.

= 0 → Pin “P1.7” used as 8051 standard I/O.

P16co = 1 → Pin “P1.6” used as CMOS Output.

= 0 → Pin “P1.6” used as 8051 standard I/O.

P15co = 1 → Pin “P1.5” used as CMOS Output.

= 0 → Pin “P1.5” used as 8051 standard I/O.

P14co = 1 → Pin “P1.4” used as CMOS Output.

= 0 → Pin “P1.4” used as 8051 standard I/O.

P13co = 1 → Pin “P1.3” used as CMOS Output.

= 0 → Pin “P1.3” used as 8051 standard I/O.

P12co = 1 → Pin “P1.2” used as CMOS Output.

= 0 → Pin “P1.2” used as 8051 standard I/O.

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P11co = 1 → Pin "P1.1" used as CMOS Output.
= 0 → Pin "P1.1" used as 8051 standard I/O.
P10co = 1 → Pin "P1.0" used as CMOS Output.
= 0 → Pin "P1.0" used as 8051 standard I/O.

OPT (w):Configuration of chip optional, all standing for "0" in Chip Reset
PWMf = 1 → Selection of 94KHz PWM frequency
= 0 → Selection of 47KHz PWM frequency
PWMd = 1 → PWM pulse width for 253-step resolution
= 0 → PWM pulse width for 256-step resolution
CPUclk = 1 → CPU working at double rate
= 0 → CPU working at normal rate
HSCLlo = 1 → Enable slave I^2C block to keep HSCL pin low in case of STK6006 being unable to catch up with the external master's speed
MI2CS = 1 → Master I^2C block connected to HSCL/HSDA pins
= 0 → Master I^2C block connected to ISCL/ISDA pins
MI2CF1,MI2CF0 = 1,1 → 400KHz Master I^2C frequency is selected
= 1,0 → 200KHz Master I^2C frequency is selected
= 0,1 → 50KHz Master I^2C frequency is selected
= 0,0 → 100KHz Master I^2C frequency is selected

8.4 I/O Port

8.4.1 Port 1

Port 1, a group of pseudo-open drain pins or CMOS output pins selected by corresponding P1(n)co, can be used as general purpose I/O. The performance of port 1 is the same as 8051 standard if corresponding P1(n)co bit is cleared.

8.4.2 P3.0-2, P3.4-5

If these pins are not set as I^2C pins, Port 3 can be applied as general purpose I/O, interrupt, UART and Timer pins. The performance of Port 3 is the same as 8051 standard.

8.4.3 Port 4, Port 5 and, Port 6

Port 5 and Port 6 are used as general purpose I/O, other than port 4 for real output. S/W is needed to set the corresponding P5(n)oe and P6(n)oe to explain whether all these pins are input or output.

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Reg. Name	Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PORT4	F58h(w)								P40
PORT4	F59h(w)								P41
PORT4	F5Ah(w)								P42
PORT5	F30h(r/w)								P50
PORT5	F31h(r/w)								P51
PORT5	F32h(r/w)								P52
PORT5	F33h(r/w)								P53
PORT5	F34h(r/w)								P54
PORT5	F35h(r/w)								P55
PORT5	F36h(r/w)								P56
PORT6	F38h(r/w)								P60
PORT6	F39h(r/w)								P61
PORT6	F3Ah(r/w)								P62
PORT6	F3Bh(r/w)								P63
PORT6	F3Ch(r/w)								P64
PORT6	F3Dh(r/w)								P65
PORT6	F3Eh(r/w)								P66
PORT6	F3Fh(r/w)								P67

PORT4 (w): data output value of port 4

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PORT5 (r/w): data input/output value of port 5

PORT6 (r/w): data input/output value of port 6.

8.5 PWM DAC

Each 8 bits of PWMDA register in XFR control each output pulse width of PWM DAC converter. PWMf selects the frequency of PWM clock as 47KHz or 94KHz, and PWMd selects the total duty cycle step of these DAC outputs as 253 or 256. In case of PWMd=1, writing FDH/FEH/FFH to DAC register makes output stably high. Writing 00H to DAC register makes the output stably low.

Reg. Name	Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMDA	F20h(r/w)	Pulse width of PWM DAC 0							
PWMDA	F21h(r/w)	Pulse width of PWM DAC 1							
PWMDA	F22h(r/w)	Pulse width of PWM DAC 2							
PWMDA	F23h(r/w)	Pulse width of PWM DAC 3							
PWMDA	F24h(r/w)	Pulse width of PWM DAC 4							
PWMDA	F25h(r/w)	Pulse width of PWM DAC 5							
PWMDA	F26h(r/w)	Pulse width of PWM DAC 6							
PWMDA	F27h(r/w)	Pulse width of PWM DAC 7							
PWMDA	F28h(r/w)	Pulse width of PWM DAC 8							
PWMDA	F29h(r/w)	Pulse width of PWM DAC 9							
PWMDA	F2Ah(r/w)	Pulse width of PWM DAC 10							

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PWMDA	**F2Bh(r/w)**	**Pulse width of PWM DAC 11**
PWMDA	**F2Ch(r/w)**	**Pulse width of PWM DAC 12**
PWMDA	**F2Dh(r/w)**	**Pulse width of PWM DAC 13**

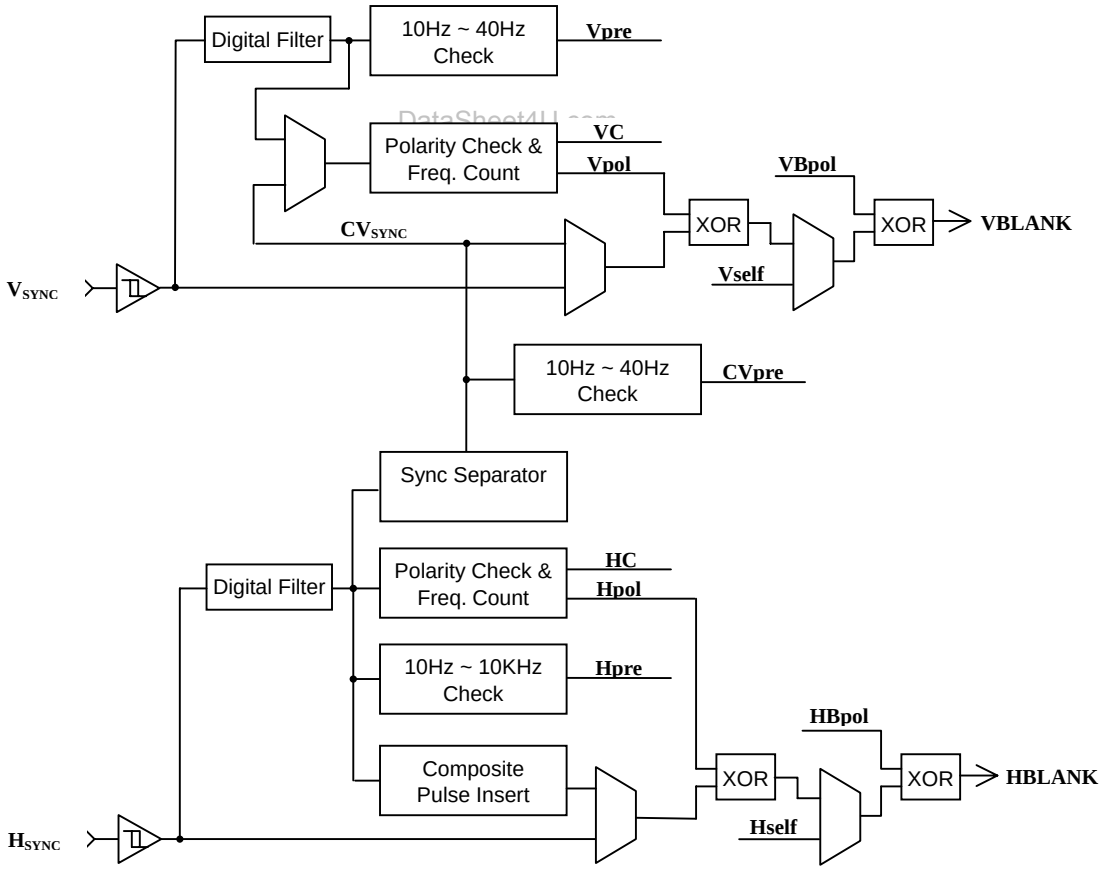
PWMDA (r/w):The mentioned-above output pulse width control is used for DA0-13.

* All of PWM DAC converters, after powered on, center on value 80h.

8.6 H_{SYNC} /V_{SYNC} Processing

H_{SYNC}/V_{SYNC} processing block functions as a composite signal separation/insertion, H/V sync inputs presence check, a frequency counting, a polarity detection and control, together with a protection of the VBLANK output while V_{SYNC} accelerates in a high clock rate of the DDC communication.

The H_{SYNC} present and frequency function block, depending on a digital filter, keep any pulse longer than the specified time period as pulse; the specified time period is under control of bits HDF1 and HDF0. However, the V_{SYNC} digital filter without control bit operates as (HDF1, HDF0) =(0,0) of H_{SYNC}.



H/V SYNC Processor Block Diagram

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8.6.1 H/V Frequency Counter

It is nice that the STK6006 can tell H_{SYNC} frequency and V_{SYNC} frequency and save the information in XFRs. We are sure that 14 bits of the Hcounter counts the time of 64*HSYNC period and then stores the result into an HCNT latch. When V_{SYNC}/CV_{SYNC} appears, the output value as [(128000000/H-Freq.)-1 is renewed per V_{SYNC}/CV_{SYNC} period, or else continuously renewed when V_{SYNC}/CV_{SYNC} disappear. 12 bits of the Vcounter counts the time between the two V_{SYNC} pulses and then stores the result into a VCNT latch. Furthermore, per V_{SYNC}/CV_{SYNC} period the output value as (62500/V-Freq.) is renewed. An additional overflow bit means that H/V counter overflows; the change or overflow of VCNT/HCNT value will set the IVC/IHC interrupt. For more information in detail, please see the HCNT/VCNT value under the operation at 12MHz in Table 8.6.2.1 and Table 8.6.2.2.

8.6.2 Composite SYNC Separation/Insertion

The input H_{SYNC} is continuously controlled by STK6006. Once the V_{SYNC} pulse is extracted from the H_{SYNC} input, a Cvpre flag will be set and users can select the extracted "CV_{SYNC}" for the sources of polarity check, frequency count, and VBLANK output. In comparison with the original signal, the CV_{SYNC} has an 8μs delay time. Also, the STK6006, during the active time of composite V_{SYNC}, can insert pulse to HBLANK output. The width of inserted pulse counts up 1/8 H_{SYNC} period and the inserted frequency can be corresponding to the original H_{SYNC}. When "HinsB" control bit is set, the inserted pulse of HBLANK will be disabled, if "HinsB" is set to "1", then HBLANK output will be equal to H_{SYNC} input. A polarity can surely be controlled by HBpol bit.

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8.6.2.1 Horizontal Frequency table

H-Freq(KHz)		14-bit Output Value
		12MHz-OSC (hex/dec)
1	31.5	0FDEh / 4062
2	37.5	0D54h / 3412
3	43.3	0B8Bh / 2955
4	46.9	0AA8h / 2728
5	53.7	094Fh / 2383
6	60.0	0854h / 2132
7	68.7	0746h / 1862
8	75.0	06AAh / 1706
9	80.0	063Fh / 1599
10	85.9	05D1h / 1489
11	93.8	0554h / 1364
12	106.3	04B3h / 1203

8.6.2.2 Vertical Frequency table

V-Freq (Hz)		12-bit Output Value
		12MHz-OSC (hex/dec)
1	56	45Ch / 1116

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2	**60**	**411h / 1041**
3	**70**	**37Ch / 892**
4	**72**	**364h / 868**
5	**75**	**341h / 833**
6	**85**	**2DFh / 735**

8.6.3 Output HBLANK/VBLANK Control and Polarity Adjustment

HBLANK is a mux output of the H_{SYNC}, composite Hsync and self-test horizontal pattern; VBLANK is a mux output of the V_{SYNC}, CV_{SYNC} and self-test vertical pattern. The mux selection and output polarity are S/W controllable. If the frequency of V_{SYNC} exceeds 250Hz, then the VBLANK output will be cut off. The HBLANK/VBLANK and P4.1/P4.0 share the output pin together.

8.6.4 Detection of H/V Polarity

The polarity functions can detect a high and low pulse duty cycle of the input H_{SYNC}/V_{SYNC}. If the time width of high pulse is longer than that of low pulse, a negative polarity will be asserted; if not, a positive polarity, asserted. The change of Hpol value will set the IHpol interrupt; the change of Vpol will set the IVpol interrupt.

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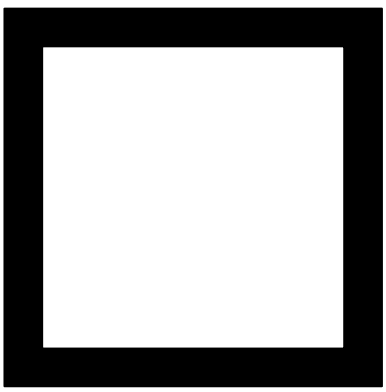
8.6.5 Self-Test Pattern Generator

STK6006 is able to generate various free-running timings with full white and full black patterns. User can properly set the content of the dot counters, DCNT, to get the free-running HBLANK frequency, and set the content of the line counters, LCNT, to get the free-running VBLANK frequency. The HBLANK/VBLANK pulse width, video front porch, and video back porch are controlled by PAT_HPUS, PAT_HBPO, PAT_HACT, PAT_VFPO, PAT_VPUS, and PAT_VBPO registers. The self-test pattern generator supports monitor manufacturer to do burn-in test, or offers end-user a reference to check the monitor. The output STO of the generator shares the output pin with P4.2.



Full white (with black frame)

Full black

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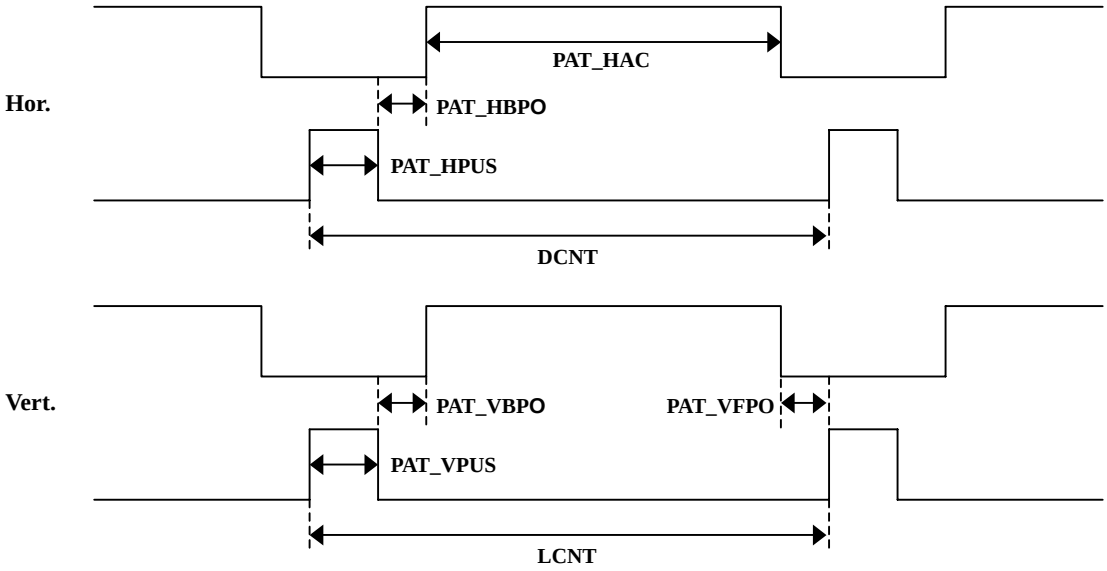

8.6.6 Real-Time Check on H/V

The Hpresent function checks the input H_{SYNC} pulse, while the H_{SYNC} rating above 10KHz will set the Hpre flag or if H_{SYNC} raiting below 10Hz will clear the flag. Similarly, the Vpresent function checks the input V_{SYNC} pulse, while the V_{SYNC} rating above 40Hz will set the Vpre flag or if V_{SYNC} rating below 10Hz will clear the flag. The change of Hpre value will set the IHpre interrupt; the change of Vpre/C Vpre will set the IVpre interrupt.

8.6.7 V_{SYNC} Interrupt

The STK6006 monitors the V_{SYNC} input pulse and generates an interrupt on its leading edge. The V_{SYNC} flag is set each time when STK6006 detects a V_{SYNC} pulse. The flag will be cleared if S/W writes a "0".

8.6.8 H_{SYNC} Clamp Pulse Output

Setting an "HCLPE" control bit enables the HCLAMP output. The leading-edge position, pulse width, and polarity of HCLAMP are regarded as S/W controllable.

8.6.9 H_{SYNC} /V_{SYNC} Processing Register

Reg. Name	Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HVSTUS	F40h(r)	CVpre		Hpol	Vpol	Hpre	Vpre	Hoff	Voff
HCNT	F41h(r)	HCovf		HC13	HC12	HC11	HC10	HC9	HC8
HCNT	F42h(r)	HC7	HC6	HC5	HC4	HC3	HC2	HC1	HC0
VCNT	F43h(r)	VCovf				VC11	VC10	VC9	VC8
VCNT	F44h(r)	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0

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HVCTR	**F40h(w)**	**C1**	**C0**	**HinsB**				**HBpol**	**VBpol**
HVSELF	**F42h(w)**			**ESelft**				**RT**	**INTL**
HCLAMP	**F43h(w)**		**CLPEG**	**CLPPO**	**CLPW2**	**CLPW1**	**CLPW0**		
HDF	**F44h(w)**							**HDF1**	**HDF0**
INTFLG	**F48h(r/w)**	**IHpre**	**IVpre**	**IHpol**	**IVpol**	**IHC**	**IVC**		**IVsync**
INTEN	**F49h(w)**	**EIHpre**	**EIVpre**	**EIHpol**	**EIVpol**	**EIHC**	**EIVC**		**EIVsync**
DCNT	**F60h(w)**							**DCNT9**	**DCNT8**
DCNT	**F61h(w)**	**DCNT7**	**DCNT6**	**DCNT5**	**DCNT4**	**DCNT3**	**DCNT2**	**DCNT1**	**DCNT0**
PAT_HACT	**F62h(w)**							**HACT9**	**HACT8**
PAT_HACT	**F63h(w)**	**HACT7**	**HACT6**	**HACT5**	**HACT4**	**HACT3**	**HACT2**	**HACT1**	**HACT0**
PAT_HPUS	**F64h(w)**	**HPUS7**	**HPUS6**	**HPUS5**	**HPUS4**	**HPUS3**	**HPUS2**	**HPUS1**	**HPUS0**
PAT_HBPO	**F65h(w)**	**HBPO7**	**HBPO6**	**HBPO5**	**HBPO4**	**HBPO3**	**HBPO2**	**HBPO1**	**HBPO0**
LCNT	**F66h(w)**						**LCNT10**	**LCNT9**	**LCNT8**
LCNT	**F67h(w)**	**LCNT7**	**LCNT6**	**LCNT5**	**LCNT4**	**LCNT3**	**LCNT2**	**LCNT1**	**LCNT0**
PAT_VFPO	**F68h(w)**	**VFPO7**	**VFPO6**	**VFPO5**	**VFPO4**	**VFPO3**	**VFPO2**	**VFPO1**	**VFPO0**
PAT_VPUS	**F69h(w)**	**VPUS7**	**VPUS6**	**VPUS5**	**VPUS4**	**VPUS3**	**VPUS2**	**VPUS1**	**VPUS0**
PAT_VBPO	**F6Ah(w)**	**VBPO7**	**VBPO6**	**VBPO5**	**VBPO4**	**VBPO3**	**VBPO2**	**VBPO1**	**VBPO0**

HVSTUS (r) : A status of the polarity, present, and static level in H_{SYNC} and V_{SYNC}.

Hpol = 1 → H_{SYNC} input in positive polarity

= 0 → H_{SYNC} input negative polarity

Vpol = 1 → V_{SYNC} (CV_{SYNC}) in positive polarity

= 0 → V_{SYNC} (CV_{SYNC}) in negative polarity

Hoff = 1 → Off-level of H_{SYNC} input keeping high in case of Hpre=0 or Vpre=0

= 0 → Off-level of H_{SYNC} input keeping low in case of Hpre=0 or Vpre=0

Voff = 1 → Off-level of V_{SYNC} input keeping high

= 0 → Off-level of V_{SYNC} input keeping low

Hpre = 1 → H_{SYNC} input present

= 0 → H_{SYNC} input not present

Vpre = 1 → V_{SYNC} input present

= 0 → V_{SYNC} input not present

CVpre = 1 → An extracted CV_{SYNC} present

= 0 → An extracted CV_{SYNC} not present

HCNT (r): H-Freq counter

HCovf = 1 → H-Freq counter is overflowed; this bit is cleared by H/W when this condition is removed.

HC13 - 0: 14 bits of H-Freq counter.

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VCNT (r): V-Freq counter

VCovf = 1 → V-Freq counter is overflowed; this bit is cleared by H/W when this condition is removed.

VC11 - 0: 12 high bits of V-Freq counter

HVCTR (w): H/V SYNC processor control register

C1, C0 = 1,1→ To select CV_{SYNC} as a polarity, freq, and VBLANK source.

= 1,0→ To select V_{SYNC} as a polarity, freq, and VBLANK source

= 0,0→ To disable a composite function

= 0,1→ H/W automatically switching to CV_{SYNC} in case of CVpre=1 and VSpre=0

HinsB = 1 → HBLANK without any insert pulse in composite mode

= 0 → HBLANK with an insert pulse in composite mode

HBpol = 1 → HBLANK output in negative polarity

= 0 → HBLANK output in positive polarity

VBpol = 1 → VBLANK output in negative polarity

= 0 → VBLANK output in positive polarity

HVSELF (w): Self-test pattern generator control register

Eselft = 1 → To enable the generator

= 0 → To disable the generator

RT = 1 → An output in a full white pattern

= 0 → An output in a full black pattern

INTL = 1 → Interlace mode

= 0 → Non-interlace mode

HCLAMP (w): H_{SYNC} clamp pulse control register

CLPEG = 1 → Clamp pulse corresponding to a leading edge of the H_{SYNC}

= 0 → Clamp pulse corresponding to a trailing edge of the H_{SYNC}

CLPPO = 1 → Clamp pulse output in a positive polarity

= 0 → Clamp pulse output in a negative polarity

CLPW2: CLPW0 : Pulse width of clamp pulse gained by [(CLPW2:CLPW0) + 1] x 0.167 μs for 12MHz X'tal selection

HDF (w): H_{SYNC} digital filter control register.

HDF1, HDF0 :

= 0,0 → To make any H_{SYNC} pulse shorter than one OSC period (83.33ns) as noise, between one and two OSC period (83.33ns to 166.67ns) as unknown region, and longer than two OSC period (166.67ns) as pulse

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= 0,1 → To treat any H_{SYNC} pulse shorter than half OSC period (41.66ns) as noise, between half and one OSC period (41.66ns to 83.33ns) as unknown region, and longer than one OSC period (83.33ns) as pulse

= 1,x → To Disable the digital filter for H_{SYNC}

INTFLG (w) : An Interrupt flag. An interrupt event will set its individual flag; a zero level will drive the INT1 source of 8051 core if the corresponding interrupt enable bit is set. Seriously, while serving the interrupt routine, software must clear this register.

IHpre = 1 → No operation.

= 0 → To clear the H_{SYNC} presence change flag.

IVpre = 1 → No operation.

= 0 → To clear the V_{SYNC} presence change flag.

IHpol = 1 → No operation.

= 0 → To clear the H_{SYNC} polarity change flag.

IVpol = 1 → No operation.

= 0 → To clear the V_{SYNC} polarity change flag.

IHC = 1 → No operation.

= 0 → To clear the H_{SYNC} frequency change flag.

IVC = 1 → No operation.

= 0 → To clear the V_{SYNC} frequency change flag.

IVsync = 1 → No operation.

= 0 → To clear the V_{SYNC} interrupt flag.

INTFLG (r): Interrupt flag.

IHpre = 1 → To indicate an H_{SYNC} presence change.

IVpre = 1 → To indicate a V_{SYNC} presence change.

IHpol = 1 → To indicate an H_{SYNC} polarity change.

IVpol = 1 → To indicate a V_{SYNC} polarity change.

IHC = 1 → To indicate an H_{SYNC} frequency change or counter overflow.

IVC = 1→ To indicate a V_{SYNC} frequency change or counter overflow.

IVsync = 1 → To indicate a V_{SYNC} interrupt.

INTEN (w): Interrupt enable.

EIHpre = 1 → To enable the H_{SYNC} presence change interrupt.

EIVpre = 1 → To enable the V_{SYNC} presence change interrupt.

EIHpol = 1 → To enable the H_{SYNC} polarity change interrupt.

EIVpol = 1 → To enable the V_{SYNC} polarity change interrupt.

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EIHC = 1 → To enable the H_{SYNC} frequency change / counter overflow interrupt.
EIVC = 1 → To enable the V_{SYNC} frequency change / counter overflow interrupt.
EIVsync = 1 → To enable the V_{SYNC} interrupt.

DCNT (w): Dot divider in self-test pattern to get HBLANK output frequency.
DCNT9 - 0: HBLANK freq. = X'tal freq. / (DCNT9 – 0). The valid range is 15KHz to 150KHz. For example, if 12MHz X'tal is used and 100KHz free-running HBLANK frequency is wanted, then the following dot divider content will be set
DCNT = 12MHz / 100KHz = 120(dec) = 78(hex)

PAT_HACT (w): Horizontal active region dot number of self-test pattern output. Dot frequency = X'tal freq.

PAT_HPUS (w): HBLANK pulse width dot number of self-test pattern output. Dot frequency = X'tal freq.

PAT_HBPO (w): Horizontal back porch dot number of self-test pattern output. Dot frequency = X'tal freq.

LCNT (w): Line divider in self-test pattern to get VBLANK output frequency.
LCNT10 – 0: VBLANK freq. = HBLANK freq. / (LCNT10 – 0). For example, if 100Hz free-running VBLANK frequency is wanted at HBLANK frequency = 100KHz, then the following line divider content will be set
LCNT = 100KHz / 100Hz = 1000(dec) = 3E8(hex)

PAT_VFPO (w): Vertical front porch line number of self-test pattern output.

PAT_VPUS (w): VBLANK pulse width line number of self-test pattern output.

PAT_VBPO (w): Vertical back porch line number of self-test pattern output.

8.7 DDC & I^2C Interface

8.7.1 SlaveB Block

Connected to HSDA and HSCL pins, the SlaveB I^2C block can access the data using the I^2C protocols. S/W may write the SLVBADR register to define the slave address.

The SlaveB block in a receiving mode first detects an I^2C slave address matching the condition and then issues an ISlvBM interrupt. When a data byte is received, the data received from HSDA is transited into the shift register and then written to the RCBBUF register; the first data written in RCBBUF is a word address, and the slave address is dropped. Once the RCBBUF is written in every time, this block generates an IRCB

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interrupt (RCBBUF full interrupt). However, if software cannot in time read out the RCBBUF, the next byte in shift register is naturally not loaded into the RCBBUF and the SlaveB block sends NACK back to the master. The WadrB flag can determine for software whether the data in RCBBUF is a word address or not.

Similarly, the block in a transmitting mode first detects an I^2C slave address matching the condition, and then issues an ISlvBM interrupt, while the data loaded in the TXBBUF is written to the shift register every time, which results in an empty TXBBUF and generates a ITXB interrupt (TXBBUF empty interrupt). Before an empty shift register is formed, S/W should write a new byte to the TXBBUF for the next transfer.

Writing "0" to a corresponding bit in the INTFLG register clears the ISlvBM; reading RCBBUF out clears the IRCB; writing TXBBUF clears the ITXB.

If you want to learn more about " Slave I^2C Block Timing", please refer to the attachment.

8.7.2 DDC1/DDC2x Mode, DDCRAM, and SlaveA Block

After reset, the STK6006 exists in the DDC1 mode, and then V_{SYNC} is used as a data clock. The HSCL pin should keep at a high level. the data output to the HSDA is accessed from a shift register in the STK6006; the shift register automatically fetches an EDID data from the lower 128-byte Dual Port RAM (DDCRAM), and sends it in 9 bits of a pocket format together with a null bit (=1) as a pocket separator. By way of setting/clearing the EDDC1 control bit, software may enable/disable DDC1 function.

Detecting a high-to-low transition on the HSCL pin, the STK6006 switches to a DDC2x mode. In this mode, the SlaveA I^2C block automatically transmits/receives the data to /from the I^2C Master. The accessed data is taken from the DDCRAM and/or saved to the DDCRAM; namely, the STK6006 can operate as 24LC02 EEPROM. S/W writes only the EDID data to DDCRAM, so S/W can select the slave address of SlaveA block as 5-bit, 6-bit, or 7-bit one. Let's take it for example that if S/W selects a 5-bit slave address as 10100b, then the SlaveA I^2C block answers to slave address 10100xxb. Setting/clearing the ESlvA bit can enable/disable the SlaveA. By means of setting/clearing the EW128/EW256 bit, the I^2C Master may freely write the lower/upper DDCRAM. In addition, if the only only128 control bits are set, the SlaveA accesses only the lower 128-byte DDCRAM.

If HSCL is kept high for 128 V_{SYNC} periods, then the STK6006 goes back to the DDC1 mode. Having been detected on an HSCL/HSDA bus, a valid I^2C address (1010xxxb) locks in a DDC2B mode; therefore, the DDC2 flag reflecting the present DDC status, S/W may clear it by writing a "0" to it.

8.7.3 I^2C Function Block in Master Mode

The selection of a MI2CS control bit may have the I^2C block in the master mode connected to the ISDA/ISCL pins, in which, its speed ranging from 50KHz to 400KHz when software sets up the MI2CF1/MI2CF0 control bit. Through this interface the S/W program can access the external I2C device.

The master I^2C access process is summarized as follows:

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8.7.3.1. To read the I²C Device

1. Write the Slave Address to MBUF.
2. Set S bit to Start.
3. The STK6006 transmitting this byte, an IMbuf interrupt is triggered.
4. Set or reset the MAckO flag with respect to the I²C protocol.
5. Read the useless byte out of MBUF to continue the data transfer.
6. The STK6006 receiving a new byte, the IMbuf interrupt is once more triggered.
7. Read MBUF will trigger the next receiving operation, but set P bit before read will stop I²C operation.

8.7.3.2. To write the I²C Device

1. Write the Slave Address to MBUF.
2. Set S bit to Start.
3. The STK6006 transmitting this byte, an IMbuf interrupt is triggered.
4. Programs can write MBUF to transfer a next byte or to set P bit to stop.

Reg. Name	Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2CCTR	F00h (r/w)	DDC2					MAckO	P	S
I2CSTUS	F01h (r)	WadrB		SlvRWB	SAckIn	SLVS			MackIn
INTFLG	F03h (r)	ITXB	IRCB	ISlvBM	ISTOP	IReSta	IWSlvA		IMbuf
INTFLG	F03h (w)			ISlvBM	ISTOP	IReSta	IWSlvA		IMbuf
INTEN	F04h (w)	EITXB	EIRCB	EISlvBM	EISTOP	EIReSta	EIWSlvA		EIMbuf
MBUF	F05h (r/w)	Master I²C receive/transmit data buffer							
DDCCTR	F06h (w)	EDDC1	EW128	EW256	Only128			SlvAs1	SlvAs0
SLVAADR	F07h (w)	ESlvA	I²C Slave A address						
RCBBUF	F08h (r)	I²C Slave B receiving buffer							
TXBBUF	F08h (w)	I²C Slave B transmitting buffer							
SLVBADR	F09h (w)	ESlvB	I²C Slave B address						

IICCTR (w): I²C interface control register.

DDC2 = 0 → Force STK6006 back to the DDC1 mode from the DDC2 mode

MackO = 1 → NACK will be returned by STK6006 in the master receiving mode

= 0 → ACK will be returned by STK6006 in the master receiving mode

S, P = ↑, 0 → Start condition in case of Master I²C being not during transfer

= X, ↑ → Stop condition in case of Master I²C being not during transfer

= 1, X → Resume transfer after a read/write MBUF operation

IICCTR (r): I²C interface status register.

DDC2 = 1 → DDC2 active

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= 0 → STK6006 in the DDC1 mode

IICSTUS (r) : I^2C interface status register.

WadrB = 1 → The data in RCBBUF used as word address

SlvRWB = 1 → Current transfer used as slave transmit

= 0 → Current transfer used as slave receive

SAckIn = 1 → The external I^2C host responding NACK

= 0 → The external I^2C host responding ACK

SLVS = 1 → The slave block having detected a START, but cleared it when STOP detected

MAckIn = 1 → NACK received from the slave I^2C device in Master I^2C

= 0 → ACK received from the slave I^2C device in Master I^2C

INTFLG (w): Interrupt flag. An interrupt event will set its individual flag, and, if the corresponding interrupt enable bit is set, a zero level will drive the 8051 INT1 source. Software is necessary to clear this register while serving the interrupt routine.

ISlvBM= 1→ No operation.

= 0→ To clear the ISlvBM flag.

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ISTOP= 1→ No operation.

= 0→ To clear the ISTOP flag.

IReSta = 1→ No operation.

= 0→ To clear the IReSta flag.

IWSlvA = 1→ No operation.

= 0→ To clear the IWSlvA flag.

IMbuf= 1→ No operation.

= 0→ To clear the Master I^2C bus interrupt flag (IMbuf).

INTFLG (r): Interrupt flag.

ITXB = 1 → To indicate the TXBBUF needs a new data byte, cleared by writing TXBBUF.

IRCB = 1 → To indicate the RCBBUF has received a new data byte, cleared by reading RCBBUF.

ISlvBM = 1 → To indicate the slave I^2C address B match condition.

ISTOP = 1 → To indicate the slave I^2C has detected a STOP condition.

IReSta = 1 → To indicate the slave I^2C has detected a repeated START condition.

IWSlvA = 1 → To indicate the slave A I^2C has detected a STOP condition in write mode.

IMbuf = 1 → To indicate a byte is sent to and/or received from the master I^2C bus.

INTEN (w): Interrupt enable.

EITXB= 1→ To enable the TXBBUF interrupt.

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EIRCB= 1→ To enable the RCBBUF interrupt.

EISlvBM = 1→ To enable the slave address B match interrupt.

EISTOP = 1→ To enable the I^2C bus STOP interrupt.

EIReSta = 1→ To enable the I^2C bus repeated START interrupt.

EIWSlvA = 1→ To enable the slave A I^2C bus STOP of interrupt in write mode

EIMbuf= 1→ To enable the Master I^2C bus interrupt.

Mbuf (w) : Master I^2C data shift register; after START and before STOP condition, writing this register resumes STK6006's transmission to the I^2C bus.

Mbuf (r) : Master I^2C data shift register; after START and before STOP condition, reading this register resumes STK6006's reception from the I^2C bus

DDCCTR (w): DDC interface control register.

EDDC1 = 1 → To enable the DDC1 data transfer in DDC1 mode.

= 0 → To disable the DDC1 data transfer in DDC1 mode.

EW128 = 1 → To indicate that I2C master can write the lower 128-byte(00-7F) DDCRAM

= 0 → To indicate that I2C master can not write the lower 128-byte(00-7F) DDCRAM

EW256 = 1 → To indicate that I2C master can write the higher 128-byte(80-FF) DDCRAM

= 0 → To indicate that I2C master can not write the higher 128-byte(80-FF) DDCRAM

Only128 = 1 → To indicate that the SlaveA always accesses EDID data from the lower 128-byte of DDCRAM

= 0 → To indicate that the SlaveA accesses EDID data from the complete 256-byte of DDCRAM

SlvAs1,SlvAs0 : Slave I^2C block A's slave address length.

= 1,0→ 5 bits of the slave address.

= 0,1→ 6 bits of the slave address.

= 0,0→ 7 bits of the slave address.

SLVAADR (w): Slave I^2C block A's enable and address.

ESlvA = 1 → To enable slave I^2C block A.

= 0 → To disable slave I^2C block A.

bit6-0: Slave I^2C address A where the slave block should respond

RCBBUF (r): Slave I^2C block B receiving the data buffer

TXBBUF (w): Slave I^2C block B transmitting the data buffer

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SLVBADR (w): Slave I^2C block B's enable and address.

ESlvB = 1 → To enable slave I^2C block B.

= 0 → To disable slave I^2C block B.

bit6-0 : Slave I^2C address B where the slave block should respond

8.8 A/D converter

Installed with four 6-bit A/D converters in V_{DD} ranges is the STK6006. Software can choose a current converting channel by setting the SAD3/SAD2/SAD1/SAD0 bits. The refresh rate of the ADC may be gained by OSC freq./1536 (128μs for 12MHz crystal).

The voltage on the input pin is compared with the voltage on the internal V_{DD} x N / 64, where N=0-63, by the ADC. The ADC output value is N when pin voltage is higher than V_{DD} x N / 64 and lower than V_{DD} x (N+1) / 64.

Reg. Name	Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADC	F10h (r)			ADC converting result					
ADC	F10h (w)	EADC				SAD3	SAD2	SAD1	SAD0

ADC (w): ADC control.

ENADC= 1→ To enable the ADC.

SADC0= 1→ To select the ADC0 pin input.

SADC1= 1→ To select the ADC1 pin input.

SADC2= 1→ To select the ADC2 pin input.

SADC3= 1→ To select the ADC3 pin input.

ADC (r): ADC converting result

8.9 Low Power Reset (LVR) & Watchdog Timer

The Low Power Reset rise a chip reset signal when the voltage level of power supply goes below 3.8V / 2.5V in 5V / 3.3V system in a specific period of time. After the voltage level of power supply rise above 3.8V / 2.5V in 5V/3.3V system, LVR stays at a reset state for 414 crystal cycles to make sure the chip exits from reset condition with a stable crystal oscillation.

When Watchdog Timer is overflowed, it automatically ensures a device reset. The overflow interval is gained by 0.25 sec x N, in which N is a number ranging from 1 to 8, and it can be programmed by way of register WDT2-0. Since the timer function is disabled after power-on reset, users may enable this function by setting EWDT and clear the timer by setting WDTclr.

Reg. Name	Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

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WDT	F18h (w)	EWDT	WDTclr				WDT2	WDT1	WDT0

WDT (w): Watchdog Timer control register.

EWDT = 1 → To enable the Watchdog Timer

WDTclr = 1 → To clear the Watchdog Timer

WDT2: WDT0 = 0 → Overflow interval = 8 x 0.25 sec.

= 1 → Overflow interval = 1 x 0.25 sec.

= 2 → Overflow interval = 2 x 0.25 sec.

= 3 → Overflow interval = 3 x 0.25 sec.

= 4 → Overflow interval = 4 x 0.25 sec.

= 5 → Overflow interval = 5 x 0.25 sec.

= 6 → Overflow interval = 6 x 0.25 sec.

= 7 → Overflow interval = 7 x 0.25 sec.

8.10 In-System Programming Function (ISP)

The features of ISP are outlined as below:

1. Block Erase: 128 Byte, 10mS
2. Whole Flash erase: 100mS
3. Byte programming Cycle time: 40uS per byte
4. Whole 64K-byte Flash programming within 6 Sec.
5. CRC check.

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After Power On/Reset, The STK6006 runs the original Program Code. Once the S/W detects an ISP request, S/W can accept the request following the steps below:

1. Clear watchdog and disable all interrupt.
2. Write ISP control block slave address to ISPSLV.
3. Write 93h to ISP enable register (ISPEN) to enable ISP.
4. Enter 8051 idle mode immediately.

When ISP is enabled, the STK6006 enter into ISP mode in 15-22.5uS. In the mode, PWM DACs and I/O pins keep running at their former status.

Reg. Name	Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISPSLV	F0Bh(w)	ISP Control Block Slave Address							
ISPEN	F0Ch(w)	Write 93h to enable the ISP mode							

8.10.1 ISP Control Block

STK6006 built in a ISP control block, that is a I^2C slave device. By this block, user can treats the 64K-byte Flash as 32 EEPROM (like as 24C16, called “EEPROM_like” in this data sheet). There are two type of I^2C bus transfer in this block:

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Write: S-ttttttt0k-000000wwk-ddddddddk-P

Read: S-ttttttt1k-CCCCCCCCK-cccccccK-P

Where

S = start P = stop

ttttttt = ISP Control Block Slave Address ww = word address

k = ack by slave K = ack by host (0 or 1)

ddddddddd = data

CCCCCCCC = crc_register[15:8] cccccccc = crc_register[7:0]

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h(w)	SDP	SDUP	ERASE	BLANK			CRCclr	CPUclr
01h(w)				BANK4	BANK3	BANK2	BANK1	BANK0
02h(w)	EPSadr							

00h(w):

SDP = 1 → To enable the S/W data protection of Flash. User needs to set this bit in the end of ISP mode.

SDUP = 1 → To disable the S/W data protection of Flash. User needs to set this bit in the start of ISP mode.

ERASE = 1 → To erase one page (128-byte) of Flash.

BLANK = 1 → To erase whole Flash.

CRCclr = 1 → To clear CRC register.

CPUclr = 1 → To reset STK6006.

Above 6 bits will be clear by I^2C STOP condition. And only one bit can be set to 1 at the same time.

01h(w):

BANK4 - 0 : EEPROM_like bank selection. Choice any one of EEPROM_like to access.

02h(w):

EPSladr : EEPROM_like slave address.

8.10.2 Start to ISP Data Write/Read

In STK6006, the ISP function works following the step below:

1. Define EEPROM_like slave address.
2. Set SDUP bit to disable Flash soft-ware data protection.
3. Set CRCclr bit to reset CRC_register.
4. Define the bank of EEPROM_like.
5. Set ERASE/BLANK bit to block-erase/chip-erase Flash.
6. Access EEPROM_like as standard EEPROM.
7. Check CRC_register.
8. Set SDP bit to enable Flash soft-ware data protection.
9. Set CPUclr bit to reset STK6006.

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The step between 4 and 6 are re-cycled until all data are written into Flash.

There are four type of I^2C bus transfer in EEPROM_like:

Byte Write: S-ttttAAA0-k-wwwwwwww-k-dddddddd-k-P

Page Write: S-ttttAAA0-k-wwwwwwww-k-dddddddd-k-dddddddd-k- … -P

Random Read: S-ttttAAA0-k-wwwwwwww-k(-P)-S-ttttAAA1-k-dddddddd-K-P

Sequential Read: S-ttttAAA0-k-wwwwwwww-k(-P)-S-ttttAAA1-k-dddddddd-K-dddddddd-K- … -P

Where

S = start or re-start
P = stop

tttt = EEPROM_like Slave Address

AAA = page block address
wwwwwwww = word address

k = ack by slave
K = ack by host (0 or 1)

dddddddd = data

The word address automatically increases every time when data byte is transferred. The page size is 256-byte.

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In STK6006 Flash memory, the program cycle time is 40us. If the ISP slave is not able to complete the program cycle in time, it returns non-ack to the following data byte. In the meantime, the word address does not increase and the CRC does not count the non-acked data byte.

8.10.3 Cyclic Redundancy Check (CRC)

The ISP Host is able to read the ISP Control Block directly to get the CRC value, instead of reading each byte in Flash. The CRC register counts each data byte acknowledged by the ISP slave during data program period. All bits “1” will be loaded into 16 bits of the CRC register by setting CRCclr bit. Msb is the data byte first shifted into the CRC register.

CRCin = CRC[15]^DATAin;

CRC[15:0] = {CRC[14]^CRCin, CRC[13:2], CRC[1]^CRCin, CRC[0], CRCin};

Where^ = XOR

example:

data_byte	CRC_register_remainder
	FFFFH
F6H	FF36H
28H	34F2H
C3H	7031H

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9. MEMORY MAP of XFR

Reg. Name	Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IICCTR	F00h (r/w)	DDC2					MAckO	P	S
IICSTUS	F01h (r)	WadrB		SlvRWB	SAckIn	SLVS			MackIn
INTFLG	F03h (r)	ITXB	IRCB	ISlvBM	ISTOP	IReSta	IWSlvA		IMbuf
INTFLG	F03h (w)			ISlvBM	ISTOP	IReSta	IWSlvA		IMbuf
INTEN	F04h (w)	EITXB	EIRCB	EISlvBM	EISTOP	EIReSta	EIWSlvA		EmbufI
MBUF	F05h (r/w)	Master IIC receives/transmits data buffer							
DDCCTR	F06h (w)	EDDC1	EW128	EW256	Only128			SlvAs1	SlvAs0
SLVAADR	F07h (w)	ESlvA	Slave A I^2C Address						
RCBBUF	F08h (r)	Slave B I^2C receives buffer							
TXBBUF	F08h (w)	Slave B I^2C transmits buffer							
SLVBADR	F09h (w)	ESlvB	Slave B I^2C Address						
ISPSLV	F0Bh(w)	ISP Control Block Slave Address							
ISPEN	F0Ch(w)	Write 93h to enable the ISP mode							
ADC	F10h (w)	ENADC				SADC3	SADC2	SADC1	SADC0
ADC	F10h (r)			ADC Converting Result					
WDT	F18h (w)	EWDT	WDTclr				WDT2	WDT1	WDT0
PWMDA	F20h(r/w)	Pulse width of PWM DAC 0							
PWMDA	F21h(r/w)	Pulse width of PWM DAC 1							
PWMDA	F22h(r/w)	Pulse width of PWM DAC 2							
PWMDA	F23h(r/w)	Pulse width of PWM DAC 3							
PWMDA	F24h(r/w)	Pulse width of PWM DAC 4							
PWMDA	F25h(r/w)	Pulse width of PWM DAC 5							
PWMDA	F26h(r/w)	Pulse width of PWM DAC 6							
PWMDA	F27h(r/w)	Pulse width of PWM DAC 7							
PWMDA	F28h(r/w)	Pulse width of PWM DAC 8							
PWMDA	F29h(r/w)	Pulse width of PWM DAC 9							
PWMDA	F2Ah(r/w)	Pulse width of PWM DAC 10							
PWMDA	F2Bh(r/w)	Pulse width of PWM DAC 11							
PWMDA	F2Ch(r/w)	Pulse width of PWM DAC 12							
PWMDA	F2Dh(r/w)	Pulse width of PWM DAC 13							
PORT5	F30h(r/w)								P50
PORT5	F31h(r/w)								P51
PORT5	F32h(r/w)								P52
PORT5	F33h(r/w)								P53
PORT5	F34h(r/w)								P54
PORT5	F35h(r/w)								P55
PORT5	F36h(r/w)								P56
PORT6	F38h(r/w)								P60
PORT6	F39h(r/w)								P61
PORT6	F3Ah(r/w)								P62
PORT6	F3Bh(r/w)								P63
PORT6	F3Ch(r/w)								P64
PORT6	F3Dh(r/w)								P65
PORT6	F3Eh(r/w)								P66

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PORT6	F3Fh(r/w)								P67
HVSTUS	F40h(r)	CVpre		Hpol	Vpol	Hpre	Vpre	Hoff	Voff
HCNT	F41h(r)	Hovf		HF13	HF12	HF11	HF10	HF9	HF8
HCNT	F42h(r)	HF7	HF6	HF5	HF4	HF3	HF2	HF1	HF0
VCNT	F43h(r)	Vovf				VF11	VF10	VF9	VF8
VCNT	F44h(r)	VF7	VF6	VF5	VF4	VF3	VF2	VF1	VF0
HVCTR	F40h(w)	C1	C0	HinsB				HBpol	VBpol
HVSELF	F42h(w)			ESelft				RT	INTL
HCLAMP	F43h(w)		CLPEG	CLPPO	CLPW2	CLPW1	CLPW0		
HDF	F44h(w)							HDF1	HDF0
INTFLG	F48h(r/w)	IHpre	IVpre	IHpol	IVpol	IHC	IVC		Vsync
INTEN	F49h(w)	EIHpre	EIVpre	EIHpol	EIVpol	EHF	EVF		EVsync
PADOPT	F50h(w)	DA13E	DA12E	DA11E	DA10E	AD3E	AD2E	AD1E	AD0E
PADOPT	F51h(w)		P56E	P55E	P54E	P53E	P52E	P51E	P50E
PADOPT	F52h(w)	HI2CE	II2CE			HCLPE	P42E	P41E	P40E
PADOPT	F53h(w)		P56oe	P55oe	P54oe	P53oe	P52oe	P51oe	P50oe
PADOPT	F54h(w)	P67oe	P66oe	P65oe	P64oe	P63oe	P62oe	P61oe	P60oe
PADOPT	F55h(w)	P17co	P16co	P15co	P14co	P13co	P12co	P11co	P10co
OPT	F56h(w)	PWMf	PWMd	CPUclk		HSCLlo	MI2CS	MI2CF1	MI2CF0
PORT4	F58h(w)								P40
PORT4	F59h(w)								P41
PORT4	F5Ah(w)								P42
DCNT	F60h(w)							DCNT9	DCNT8
DCNT	F61h(w)	DCNT7	DCNT6	DCNT5	DCNT4	DCNT3	DCNT2	DCNT1	DCNT0
PAT_HACT	F62h(w)							HACT9	HACT8
PAT_HACT	F63h(w)	HACT7	HACT6	HACT5	HACT4	HACT3	HACT2	HACT1	HACT0
PAT_HPUS	F64h(w)	HPUS7	HPUS6	HPUS5	HPUS4	HPUS3	HPUS2	HPUS1	HPUS0
PAT_HBPO	F65h(w)	HBPO7	HBPO6	HBPO5	HBPO4	HBPO3	HBPO2	HBPO1	HBPO0
LCNT	F66h(w)						LCNT10	LCNT9	LCNT8
LCNT	F67h(w)	LCNT7	LCNT6	LCNT5	LCNT4	LCNT3	LCNT2	LCNT1	LCNT0
PAT_VFPO	F68h(w)	VFPO7	VFPO6	VFPO5	VFPO4	VFPO3	VFPO2	VFPO1	VFPO0
PAT_VPUS	F69h(w)	VPUS7	VPUS6	VPUS5	VPUS4	VPUS3	VPUS2	VPUS1	VPUS0
PAT_VBPO	F6Ah(w)	VBPO7	VBPO6	VBPO5	VBPO4	VBPO3	VBPO2	VBPO1	VBPO0

10. ELECTRICAL PARAMETERS

10.1 DC Characteristics

Conditions at: Ta=0 ~ 70 ^{O}C, V_{DD}=5.0V/3.3V, V_{SS}=0V

Name	Symbol	Conditions	Min.	Max.	Unit
Output "L" Voltage	Vol	Iol=5mA		0.45	V
Output "H" Voltage on 8051 I/O port pin	Voh1	V_{DD}=5V, Ioh=-50µA	4		V

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	Voh2	V_{DD}=3.3V, Ioh=-50µA	2.65		V
Output "H" Voltage on CMOS output	Voh3	V_{DD}=5V, Ioh=-4mA	4		V
	Voh4	V_{DD}=3.3V, Ioh=-4mA	2.65		V
Input "L" Voltage	Vil1	V_{DD}=5V	-0.3	0.2 x V_{DD}	V
	Vil2	V_{DD}=3.3V	-0.3	0.3 x V_{DD}	V
Input "H" Voltage	Vih1	V_{DD}=5V	0.4 x V_{DD}	V_{DD} +0.3	V
	Vih2	V_{DD}=3.3V	0.6 x V_{DD}	V_{DD} +0.3	V
RST Pull Down Resistor	Rrst	V_{DD}=5V	150	250	Kohm
Pin Capacitance	Cio			15	pF

10.2 AC Characteristics

Conditions at: Ta=0 ~ 70 ^{o}C, V_{DD}=5.0V/3.3V, V_{SS}=0V

Name	Symbol	Conditions	Min.	Typ.	Max.	Unit
Crystal Frequency	fXtal			12		MHz
PWM DAC Frequency	fDA	fXtal=12MHz	46.875		94.86	KHz
H_{SYNC} input pulse Width	tHIPW	fXtal=12MHz	0.3		7.5	µs
V_{SYNC} input pulse Width	tVIPW	fXtal=12MHz	3			µs
H_{SYNC} to HBLANK output jitter	tHHBJ				5	ns
H+V to VBLANK output delay	tVVBD	fXtal=12MHz		8		µs
CV_{SYNC} pulse width in H+V signal	tVCPW	FXtal=12MHz	20			µs

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10.3 Absolute Maximum Ratings

Conditions at: Ta= 0 ~ 70 ^{o}C, V_{SS}=0V

Name	Symbol	Range	Unit
Operating Temperature	Topg	0 ~ +70	^{o}C
Storage Temperature	Tstg	-25 ~ +125	^{o}C
Output Voltage	Vout	-0.3 ~ V_{DD}+0.3	V
Input Voltage (other pins)	Vin2	-0.3 ~ V_{DD}+0.3	V
Supply Voltage	V_{DD}	-0.3 ~ +6.0	V
Input Voltage (H_{SYNC}, V_{SYNC} & open-drain pins)	Vin1	-0.3 ~ 5V+0.3	V

10.4 Operating Conditions Allowable

Conditions at: Ta= 0 ~ 70 ^{o}C, V_{SS}=0V

Name	Symbol	Conditions	Min.	Max.	Unit
Supply Voltage	V_{DD}	5V system	4.5	5.5	V
		3.3V system	3.0	3.6	V
Operating Freq.	Fopg		-	15	MHz

11. PACKAGE DIMENSION

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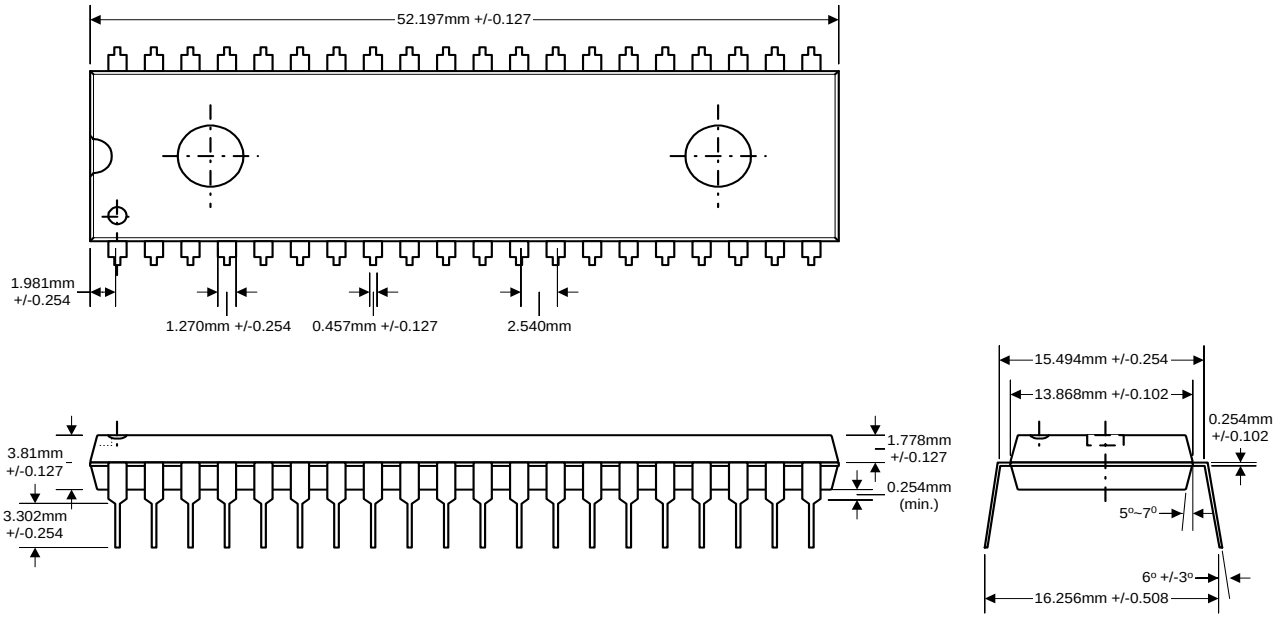
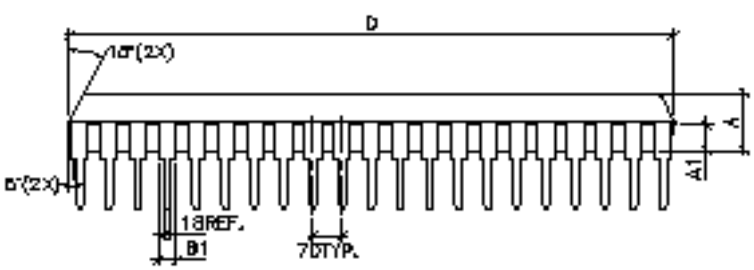
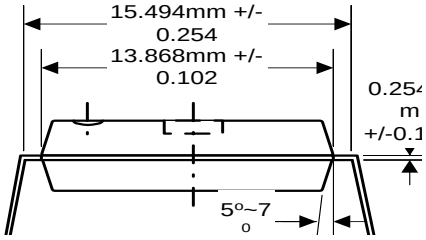
11.1 40-Pin PDIP 600 Mil



11.2 42-Pin SDIP Unit: mm

Symbol	Dimension in mm		
	Min	Nom	Max
A	3.937	4.064	4.2
A1	1.78	1.842	1.88
B1	0.914	1.270	1.118
D	36.78	36.83	36.88
E1	13.945	13.970	13.995
F	15.19	15.240	15.29
eB	15.24	16.510	17.78
θ	0 °	7.5 °	15 °





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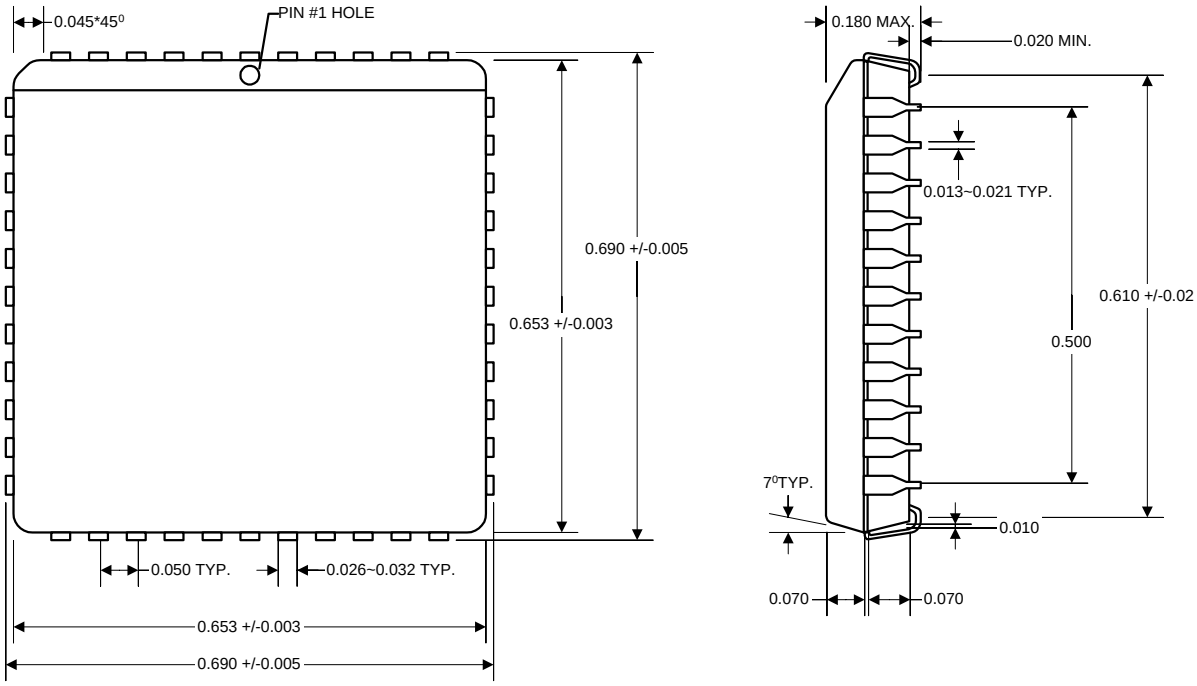
11.3 44-Pin PLCC Unit:



12. Information

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12.1 Order Information:

Part No.	Pin Count	Package	Marking
STK6006-F1	**40**	**P-DIP**	**Syntek Logo STK6006-F1** **Manu. No**
STK6006-F2	**42**	**S-DIP**	**Syntek Logo STK6006-F2** **Manu. No**
STK6006-F3	**44**	**PLCC**	**Syntek Logo STK6006-F3** **Manu. No**

12.2 Contact Information :

If you need more details information or samples requested, PLS contact the next window then we will response you as soon as we can.

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