

# **STFV4N150**

## N-channel 1500V - 5Ω - 4A - TO-220FH Very high voltage PowerMESH™ Power MOSFET

### **General features**

Туре	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	Pw
STFV4N150	1500V	<7Ω	4A	40W

- Avalanche ruggedness
- Gate charge minimized
- Very low intrinsic capacitances
- High speed switching
- Fully plastic TO-220 package
- Creepage distance path is > 4mm

### Description

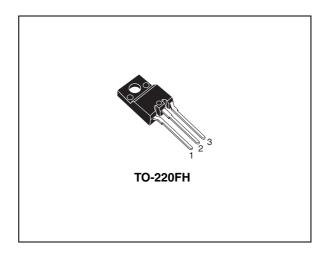
Using the well consolidated high voltage MESH OVERLAY<sup>™</sup> process, STMicroelectronics has designed an advanced family of Power MOSFETs with outstanding performances. The strengthened layout coupled with the Company's proprietary edge termination structure, gives the lowest RDS(on) per area, unrivalled gate charge and switching characteristics. The creepage path is what makes this package unique from TO-220FP. The creepage distance path between each lead and between the leads and the heatsink has been increased to >4.0mm, making this package met all stringent safety norms in high voltage applications.

### Applications

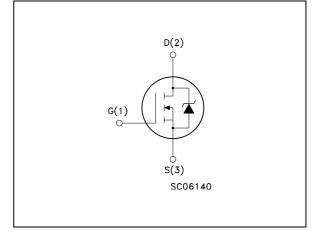
Switching application

### **Order codes**

Part number	Marking	Package	Packaging
STFV4N150	FV4N150	TO-220FH	Tube



### Internal schematic diagram



## Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuit	9
4	Package mechanical data 1	0
5	Revision history1	2



# 1 Electrical ratings

Table 1.	Absolute	maximum	ratings
	Absolute	maximum	ruungo

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	1500	V
V <sub>DGR</sub>	Drain-gate voltage (R <sub>GS</sub> = 20 kΩ)	1500	V
V <sub>GS</sub>	Gate- source voltage	± 30	V
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> = 25°C	4	Α
Ι <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100°C	2.5	Α
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	12	A
P <sub>TOT</sub>	Total dissipation at $T_{C} = 25^{\circ}C$	40	W
	Derating factor	0.32	W/°C
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s; $T_C=25^{\circ}C$ )	2500	v
T <sub>j</sub> T <sub>stg</sub>	Operating junction temperature Storage temperature	-55 to 150	°C

1. Limited only by maximum temperature allowed

2. Pulse width limited by safe operating area

#### Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case Max	3.12	°C/W
Rthj-amb	Thermal resistance junction-ambient Max	62.5	°C/W

#### Table 3. Avalanche data

Symbol	Parameter	Value	Unit
I <sub>AR</sub>	Avalanche current, repetitive or not-repetitive (pulse width limited by T <sub>j</sub> max)	4	A
E <sub>AS</sub>	Single pulse avalanche energy (starting $T_j = 25^{\circ}C$ , $I_D = I_{AR}$ , $V_{DD} = 50V$ )	350	mJ

## 2 Electrical characteristics

(T<sub>CASE</sub>=25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1mA, V <sub>GS</sub> = 0	1500			V
I <sub>DSS</sub>	Zero gate voltage Drain current (V <sub>GS</sub> = 0)	$V_{DS} = Max rating$ $V_{DS} = Max rating, T_C = 125^{\circ}C$			10 500	μΑ μΑ
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	$V_{GS} = \pm 30V$			± 100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	3	4	5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	$V_{GS}$ = 10V, $I_D$ = 2A		5	7	Ω

#### Table 4. On/off states

#### Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
g <sub>fs</sub> <sup>(1)</sup>	Forward transconductance			3.5	indixi	S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	V <sub>DS</sub> = 25V, f = 1MHz, V <sub>GS</sub> = 0		1300 120 12		pF pF pF
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 600V, I_D = 4A,$ $V_{GS} = 10V$ (see Figure 15)		30 10 9	50	nC nC nC

1. Pulsed: Pulse duration =  $300 \ \mu$ s, duty cycle 1.5%.



	ownoning times					
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub> t <sub>r</sub> t <sub>d(off)</sub> t <sub>f</sub>	Turn-on delay time Rise time Turn-off-delay time Fall time	$V_{DD} = 750V, I_D = 2A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 14)		35 30 45 45		ns ns ns ns

Table 6. Switching times

#### Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Тур.	Max	Unit
I <sub>SD</sub> I <sub>SDM</sub> <sup>(1)</sup>	Source-drain current Source-drain current (pulsed)				4 12	A A
V <sub>SD</sub> <sup>(2)</sup>	Forward on voltage	$I_{SD} = 4A, V_{GS} = 0$			2	V
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse recovery time Reverse recovery charge Reverse recovery current	I <sub>SD</sub> = 4A, di/dt = 100A/μs V <sub>DD</sub> = 45V <i>(see Figure 19)</i>		510 3 12		ns μC Α
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse recovery time Reverse recovery charge Reverse recovery current	I <sub>SD</sub> = 4A, di/dt = 100A/μs V <sub>DD</sub> = 45V, T <sub>j</sub> = 150°C ( <i>see Figure 19)</i>		650 4 12.6		ns μC Α

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300  $\mu$ s, duty cycle 1.5%.



#### **Electrical characteristics (curves)** 2.1

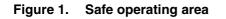


Figure 2. **Thermal impedance** 

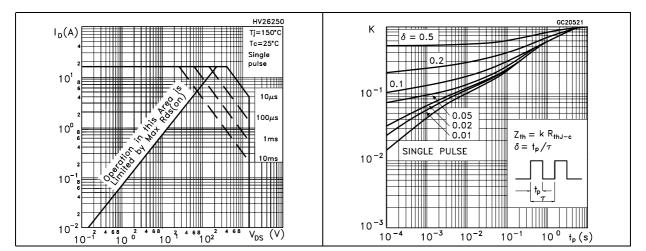


Figure 3. **Output characterisics** 

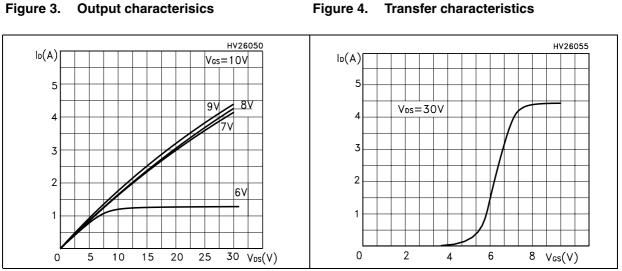
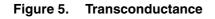
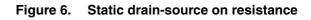
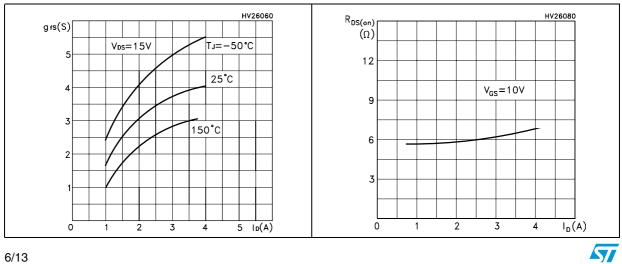
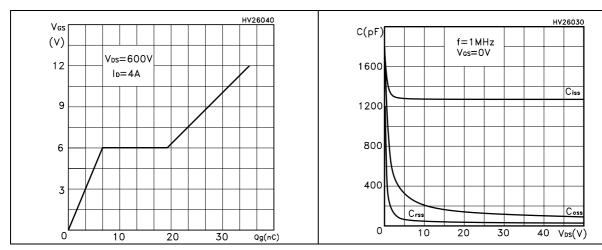


Figure 4.









#### Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

Figure 9. Normalized gate threshold voltage vs temperature

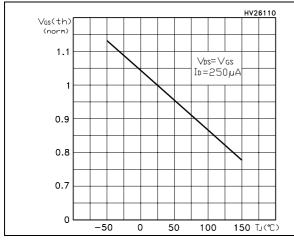


Figure 11. Source-drain diode forward characteristics

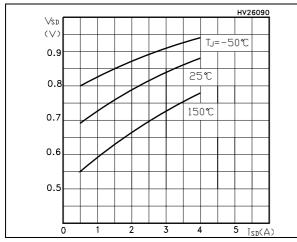


Figure 10. Normalized on resistance vs temperature

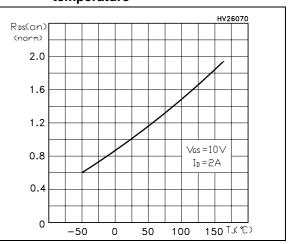
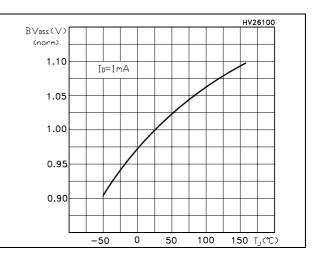
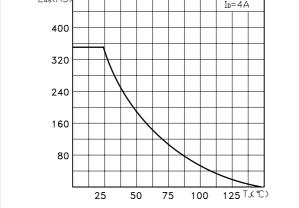


Figure 12. Normalized B<sub>VDSS</sub> vs temperature



57



## 3 Test circuit

Figure 14. Switching times test circuit for resistive load

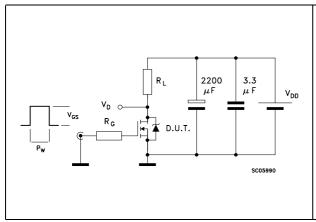
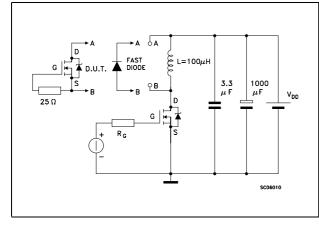


Figure 16. Test circuit for inductive load switching and diode recovery times





57

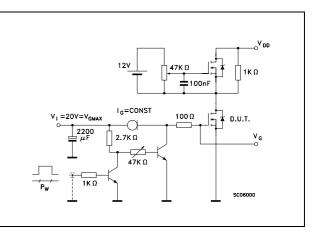


Figure 17. Unclamped inductive load test circuit

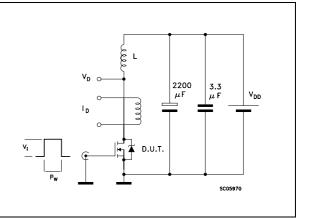


Figure 19. Switching time waveform

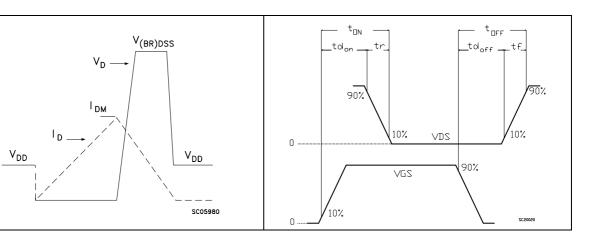


Figure 15. Gate charge test circuit

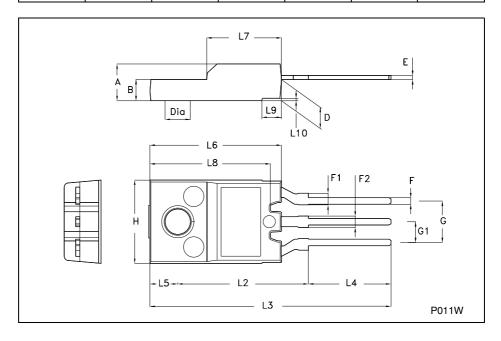
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com



		mm			inch	
DIM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
А	4.4		4.6	0.173		0.181
В	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
Е	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.3		1.8	0.051		0.070
F2	1.3		1.8	0.051		0.070
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
Н	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L5		3.4			0.134	
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
L8	14.5		15	0.570		0.590
L9		2.4			0.094	

## TO-220FH (Fully plastic High voltage) MECHANICAL DATA





# 5 Revision history

Date	Revision	Changes
07-Jul-2005	1	First Release
06-Jun-2006	2	New template, inerted new value on Absolute maximum ratings
28-Jun-2006	3	The document has been reformatted
06-Mar-2007	4	Typo mistake on page 1



#### Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZE REPRESENTATIVE OF ST, ST PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS, WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2007 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

