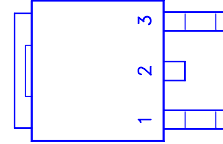
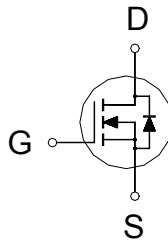


**NIKO-SEM****N-Channel Logic Level Enhancement  
Mode Field Effect Transistor****P75N02LD  
TO-252 (D<sup>2</sup>PAK)****PRODUCT SUMMARY**

$V_{(BR)DSS}$	$R_{DS(ON)}$	$I_D$
25	5m $\Omega$	75A



1. GATE
2. DRAIN
3. SOURCE

**ABSOLUTE MAXIMUM RATINGS (T<sub>c</sub> = 25 °C Unless Otherwise Noted)**

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		$V_{GS}$	±20	V
Continuous Drain Current	T <sub>c</sub> = 25 °C	$I_D$	75	A
	T <sub>c</sub> = 100 °C		50	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	170	
Avalanche Current		$I_{AR}$	60	
Avalanche Energy	L = 0.1mH	$E_{AS}$	140	mJ
Repetitive Avalanche Energy <sup>2</sup>	L = 0.05mH	$E_{AR}$	5.6	
Power Dissipation	T <sub>c</sub> = 25 °C	$P_D$	65	W
	T <sub>c</sub> = 100 °C		38	
Operating Junction & Storage Temperature Range		T <sub>j</sub> , T <sub>stg</sub>	-55 to 150	°C
Lead Temperature ( <sup>1</sup> / <sub>16</sub> " from case for 10 sec.)		T <sub>L</sub>	275	

**THERMAL RESISTANCE RATINGS**

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		2.3	°C / W
Junction-to-Ambient	$R_{\theta JA}$		62.5	
Case-to-Heatsink	$R_{\theta CS}$	0.6		

<sup>1</sup>Pulse width limited by maximum junction temperature.<sup>2</sup>Duty cycle ≤ 1%**ELECTRICAL CHARACTERISTICS (T<sub>c</sub> = 25 °C, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	25			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.5	3	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$			±250	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20V, V_{GS} = 0V$			25	$\mu A$
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125\text{ °C}$			250	

On-State Drain Current <sup>1</sup>	$I_{D(ON)}$	$V_{DS} = 10V, V_{GS} = 10V$	70			A
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 30A$		5	7	mΩ
		$V_{GS} = 7V, I_D = 24A$		6	8	
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = 15V, I_D = 30A$		16		S
<b>DYNAMIC</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$		5000		pF
Output Capacitance	$C_{oss}$			1800		
Reverse Transfer Capacitance	$C_{rss}$			800		
Total Gate Charge <sup>2</sup>	$Q_g$	$V_{DS} = 0.5V_{(BR)DSS}, V_{GS} = 10V,$ $I_D = 35A$		140		nC
Gate-Source Charge <sup>2</sup>	$Q_{gs}$			40		
Gate-Drain Charge <sup>2</sup>	$Q_{gd}$			75		
Turn-On Delay Time <sup>2</sup>	$t_{d(on)}$	$V_{DS} = 15V, R_L = 1\Omega$ $I_D \cong 30A, V_{GS} = 10V, R_{GS} = 2.5\Omega$		7		nS
Rise Time <sup>2</sup>	$t_r$			7		
Turn-Off Delay Time <sup>2</sup>	$t_{d(off)}$			24		
Fall Time <sup>2</sup>	$t_f$			6		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T<sub>C</sub> = 25 °C)</b>						
Continuous Current	$I_S$				75	A
Pulsed Current <sup>3</sup>	$I_{SM}$				170	
Forward Voltage <sup>1</sup>	$V_{SD}$	$I_F = I_S, V_{GS} = 0V$			1.3	V
Reverse Recovery Time	$t_{rr}$	$I_F = I_S, di_F/dt = 100A / \mu S$		37		nS
Peak Reverse Recovery Current	$I_{RM(REC)}$			200		A
Reverse Recovery Charge	$Q_{rr}$			0.043		μC

<sup>1</sup>Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

<sup>2</sup>Independent of operating temperature.

<sup>3</sup>Pulse width limited by maximum junction temperature.

**REMARK: THE PRODUCT MARKED WITH "P75N02LD", DATE CODE or LOT #**

**TO-252 (DPAK) MECHANICAL DATA**

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	9.35		10.1	H		0.8	
B	2.2		2.4	I	6.4		6.6
C	0.48		0.6	J	5.2		5.4
D	0.89		1.5	K	0.6		1
E	0.45		0.6	L	0.64		0.9
F	0.03		0.23	M	4.4		4.6
G	6		6.2	N			

